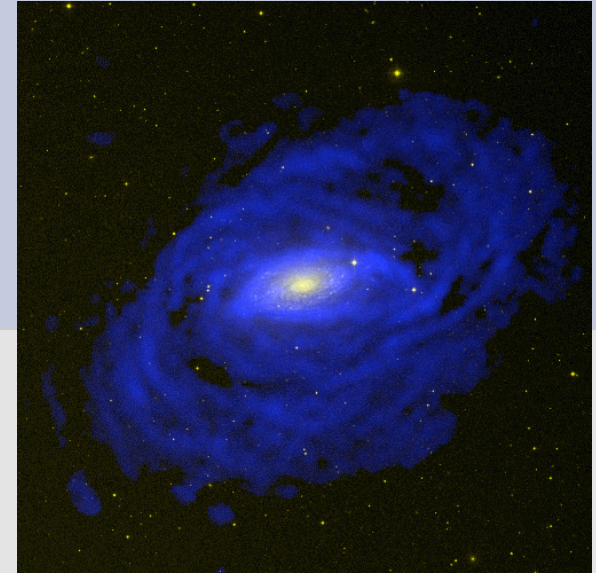




BAO project in radio

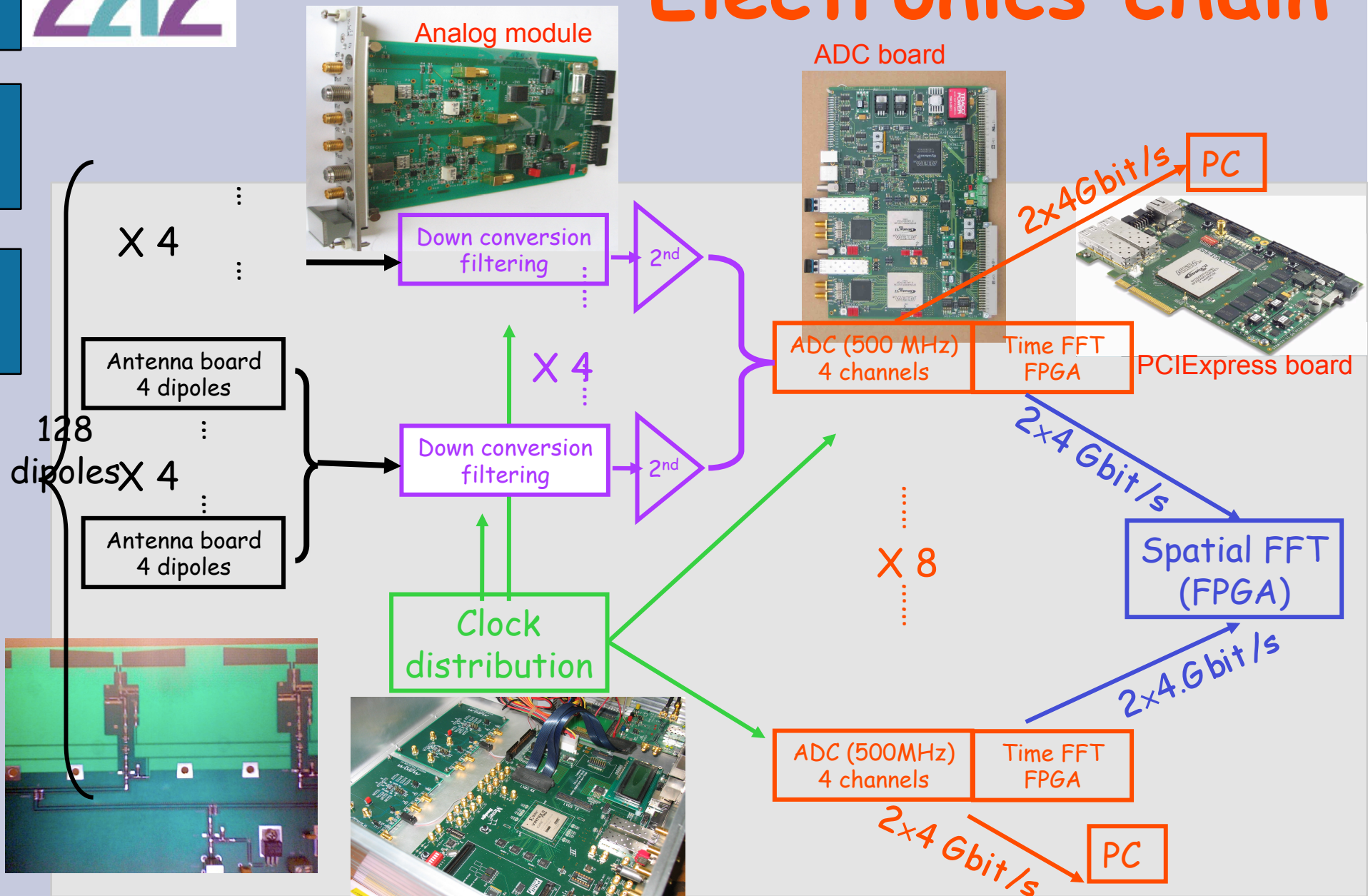


Fast acquisition system
for 3D mapping of cosmological
matter distribution in radio

CEA/Irfu IN2P3/LAL CMU Fermilab collaboration



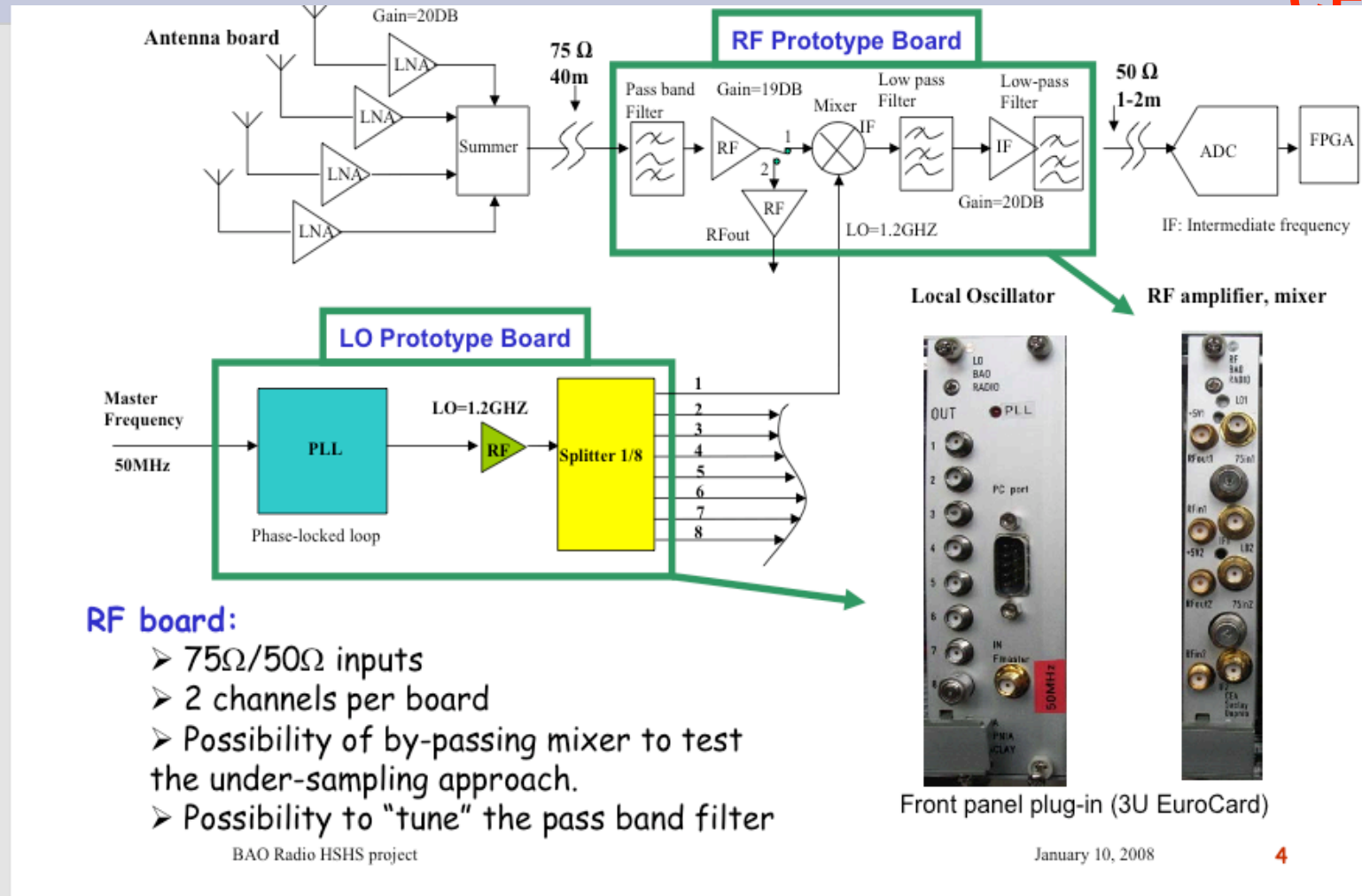
Electronics chain





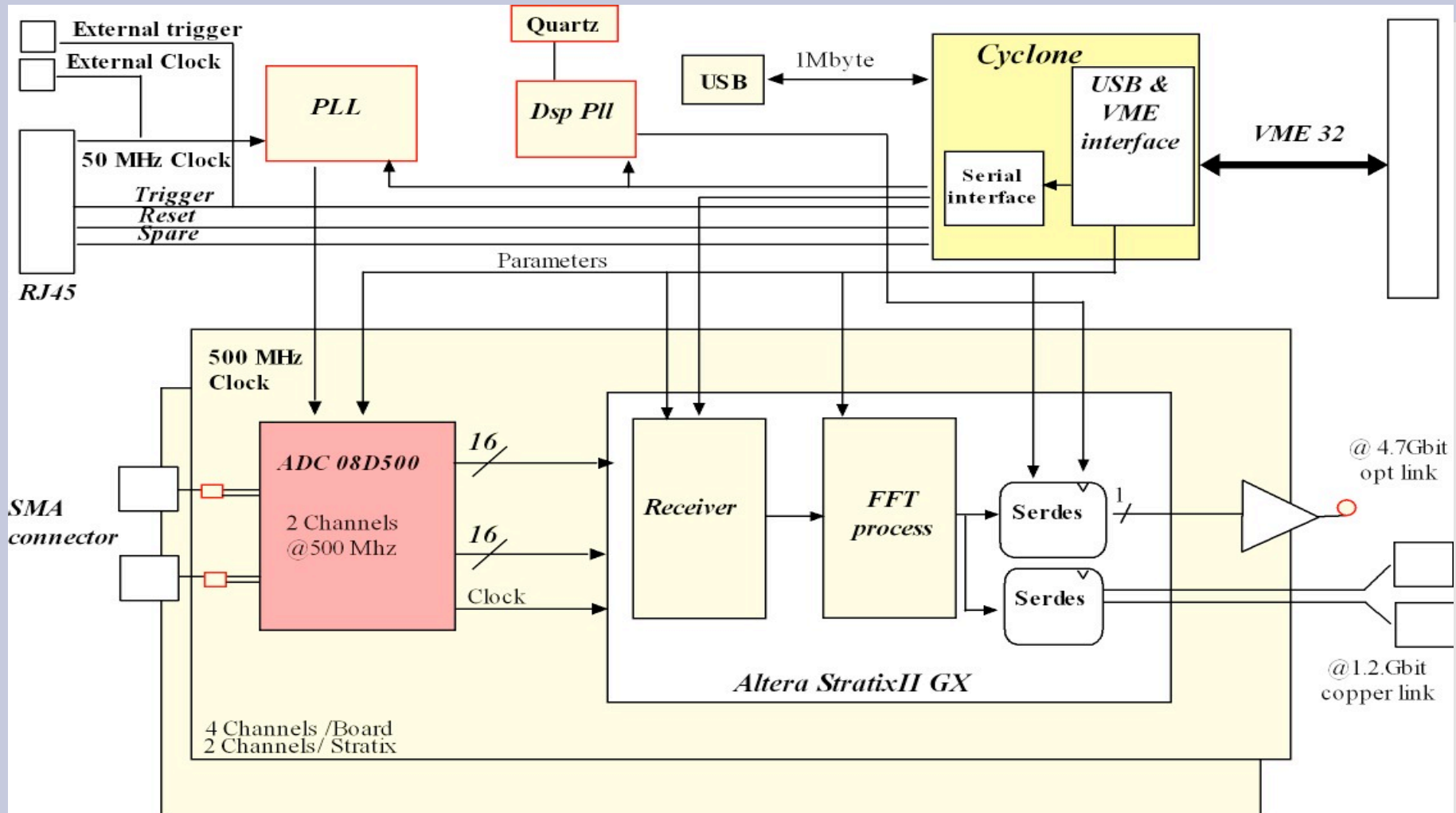
Analog chain for RF prototype board

CEA irfu



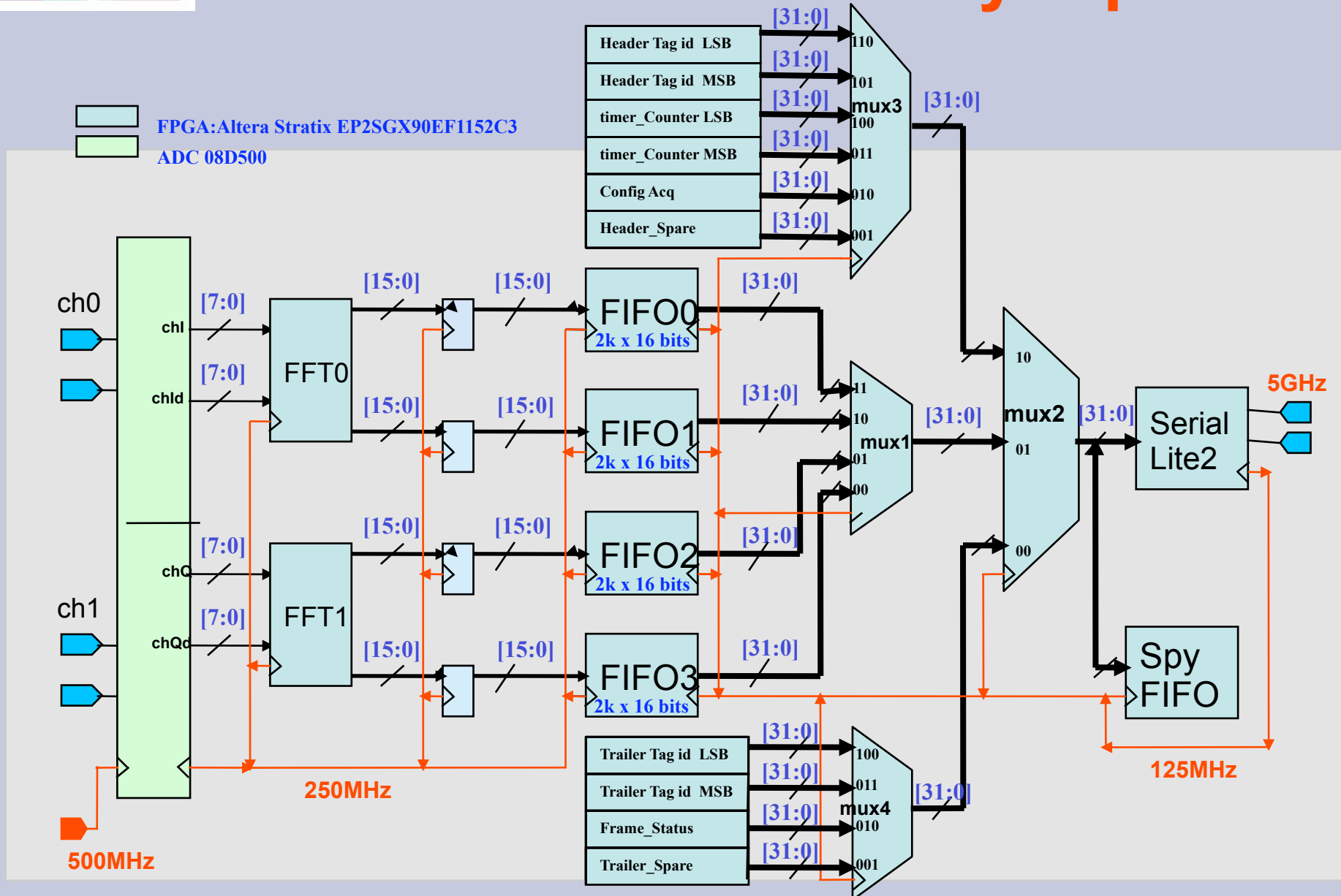


LAL ADC board Synoptic





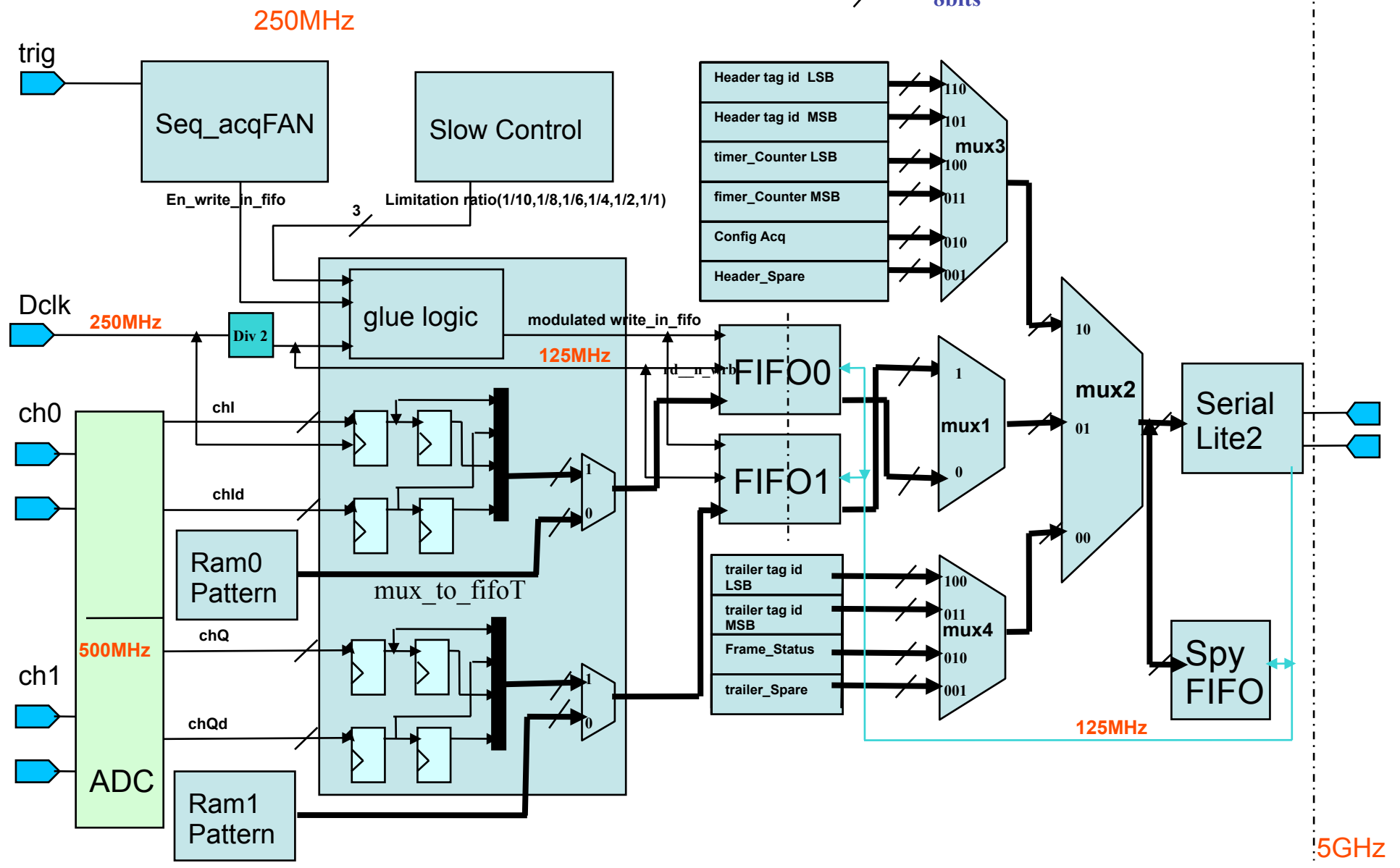
ADC board FPGA Synoptic



path and size of RawDatas transmitted on 2 channels in Bandwidth limitation mode.

Altera Stratix EP2SGX90EF1152C3

- PGA:
- ADC 08D500
- 32bits
- 8bits



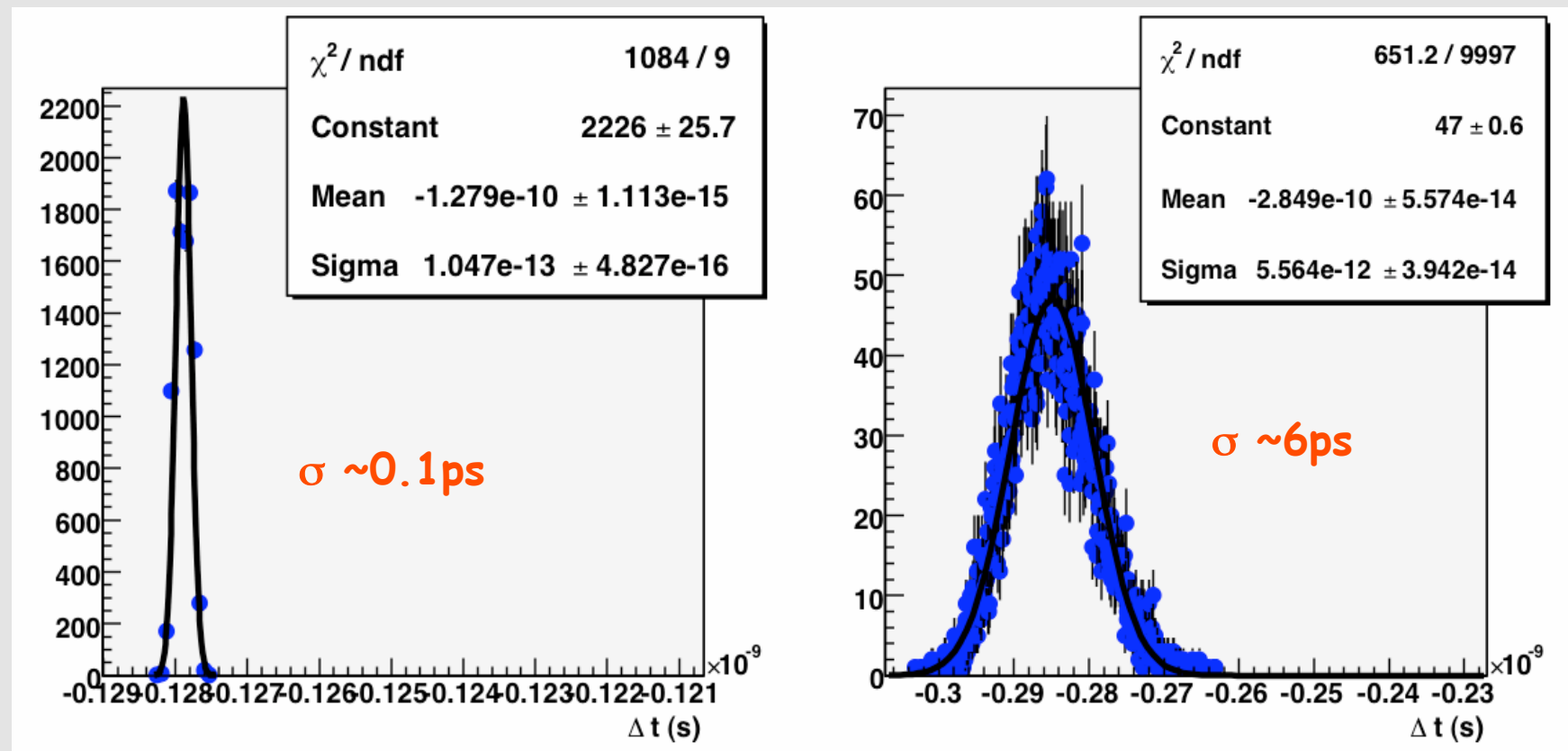


Post ADC processing: Temporal FFT

Evolutions réalisées

- Saturation datas sortie
- Correction bug exposant saturé
- Modif passage 8bits->12 bits interne
 - Résultats préliminaires encourageants (SNR)
 - À confirmer

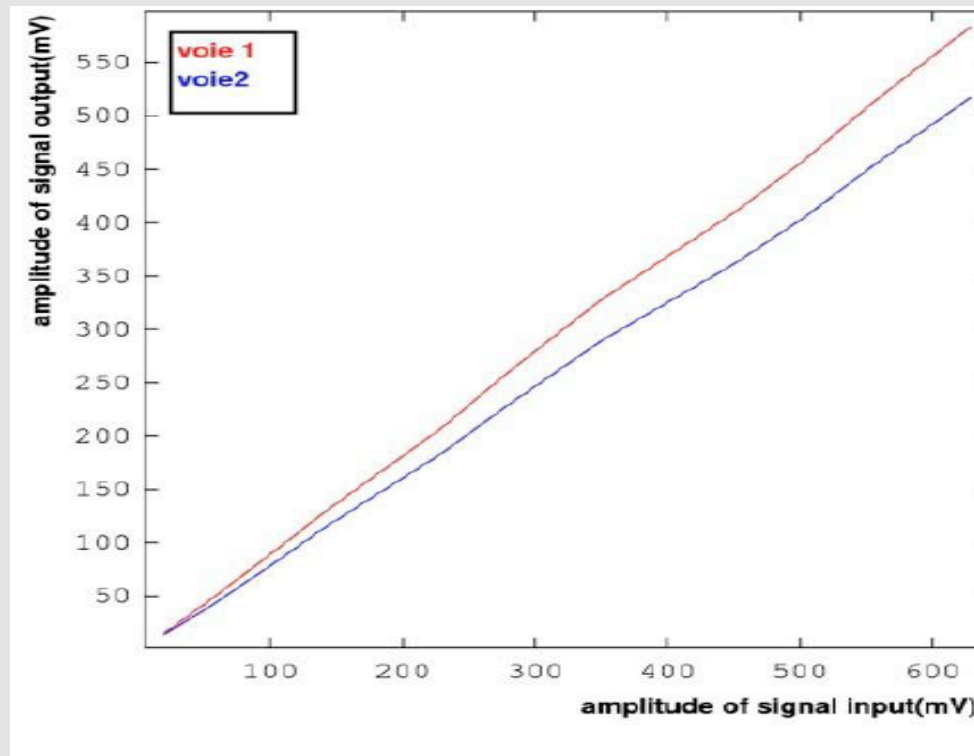
Analog characteristic: 1 Time resolution



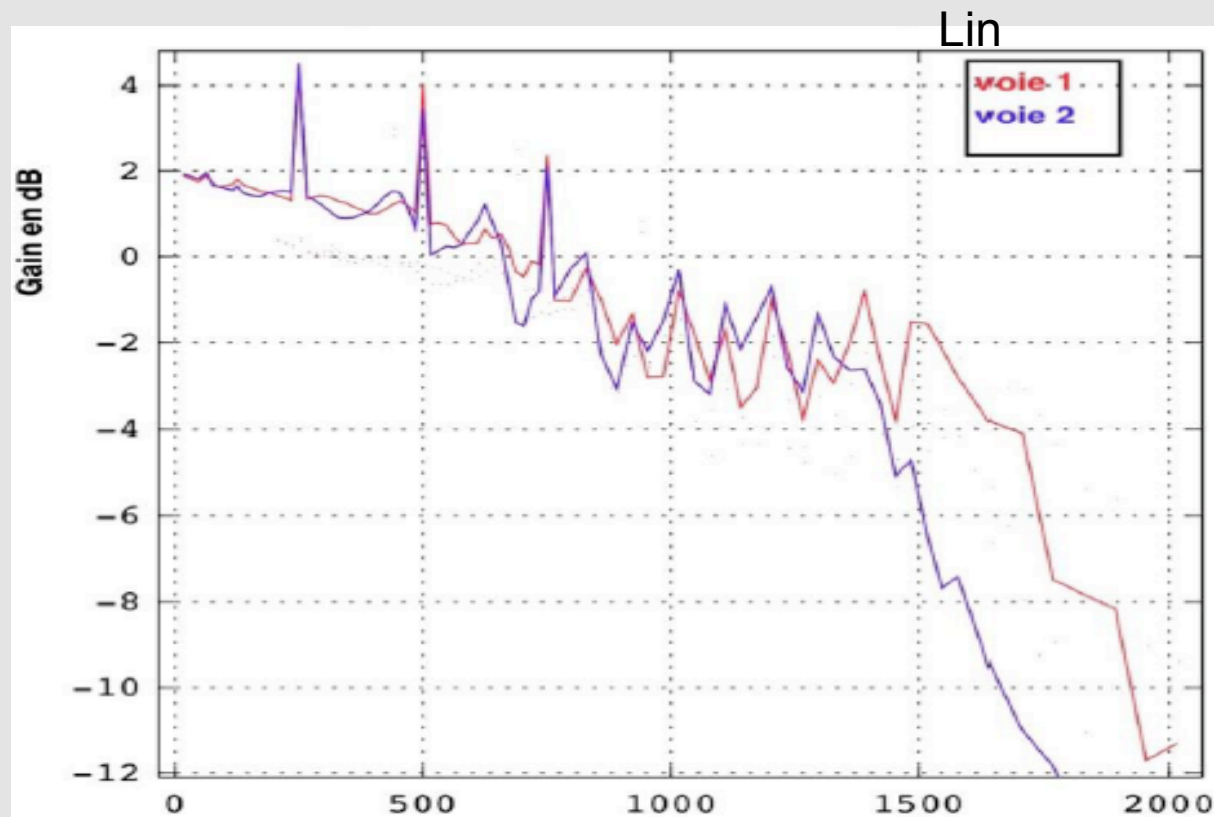
Analog characteristic :2

Linearity

Linearity at 1.4GHz
Lin

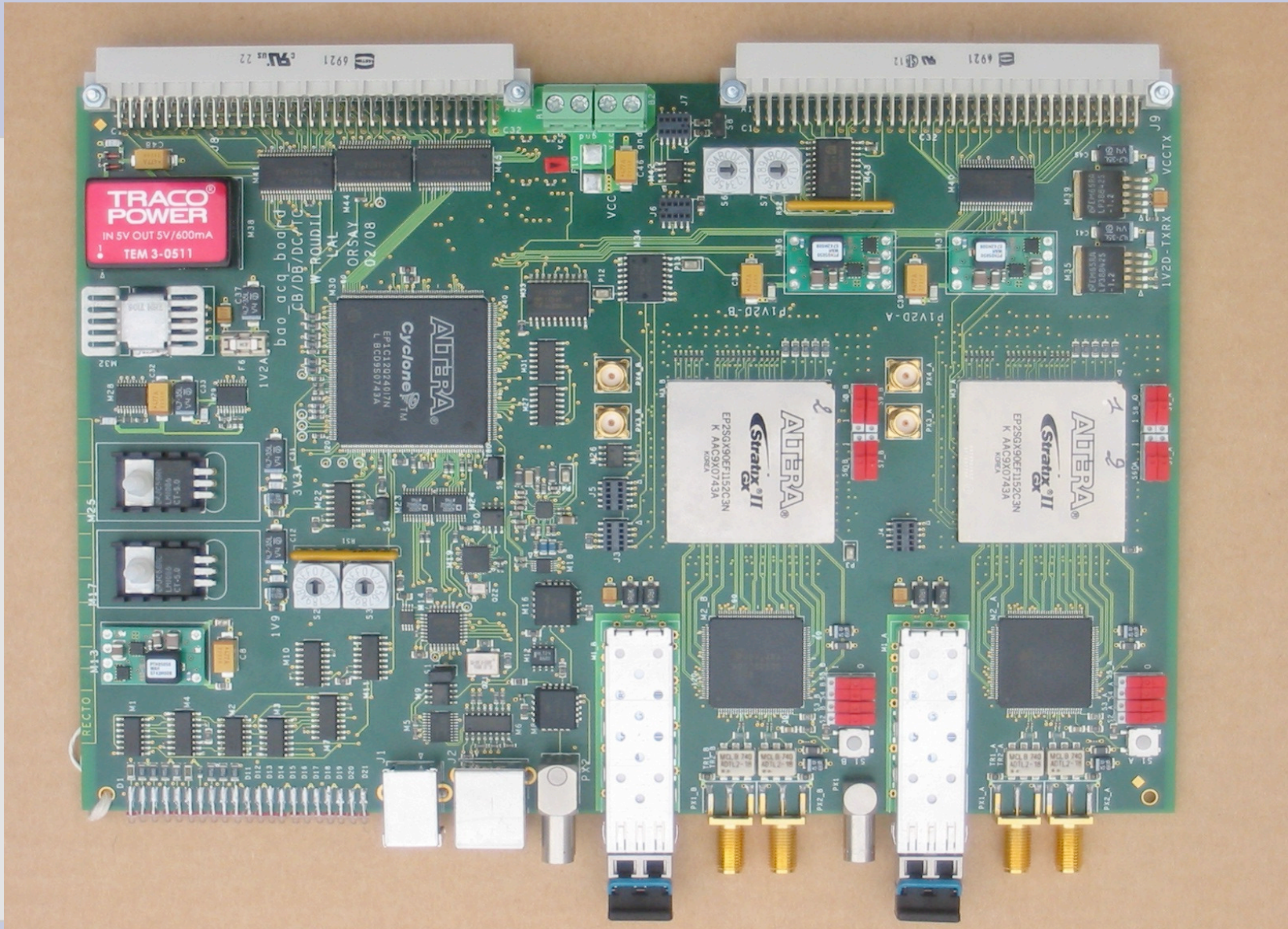


Analog characteristic : 3 Bode diagram



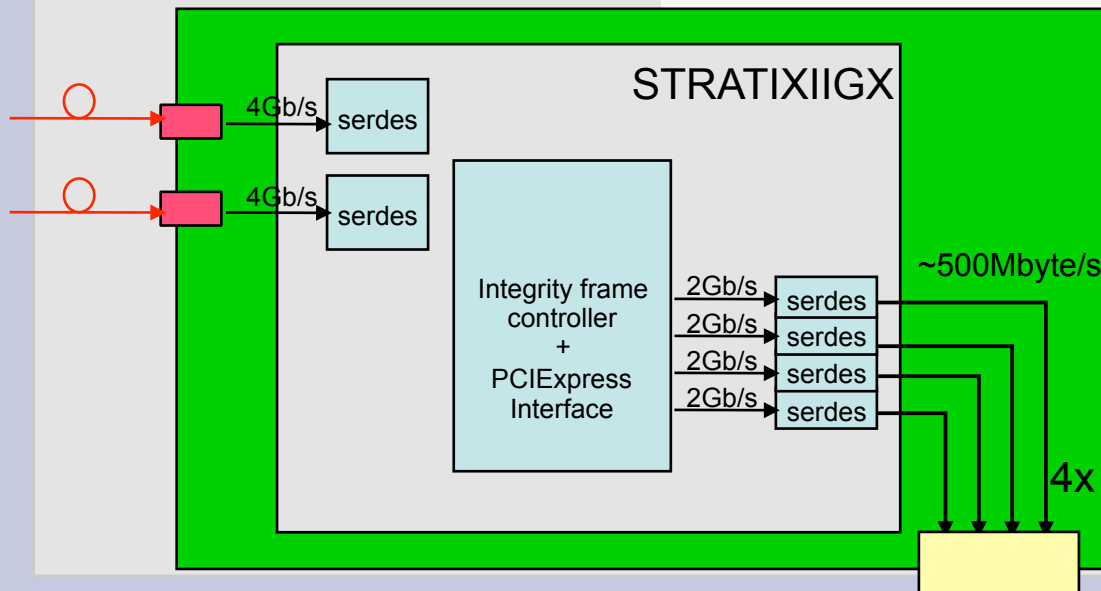
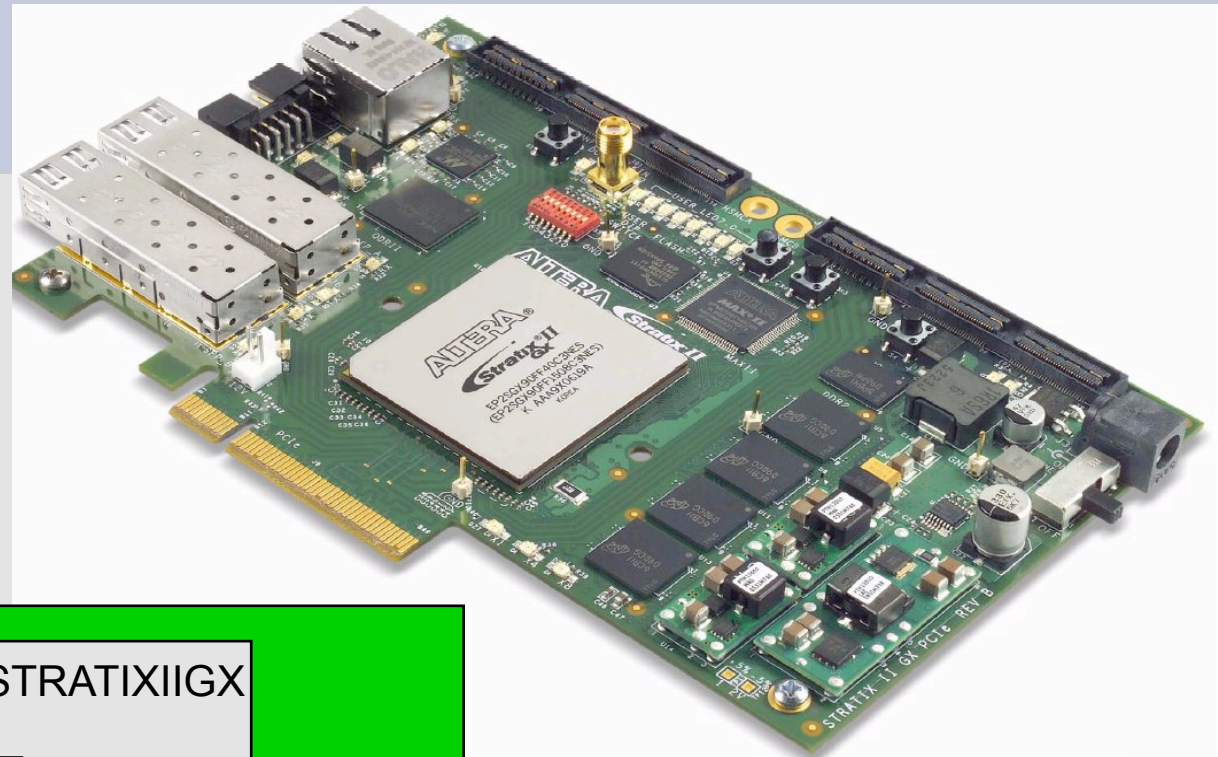


LAL ADC board





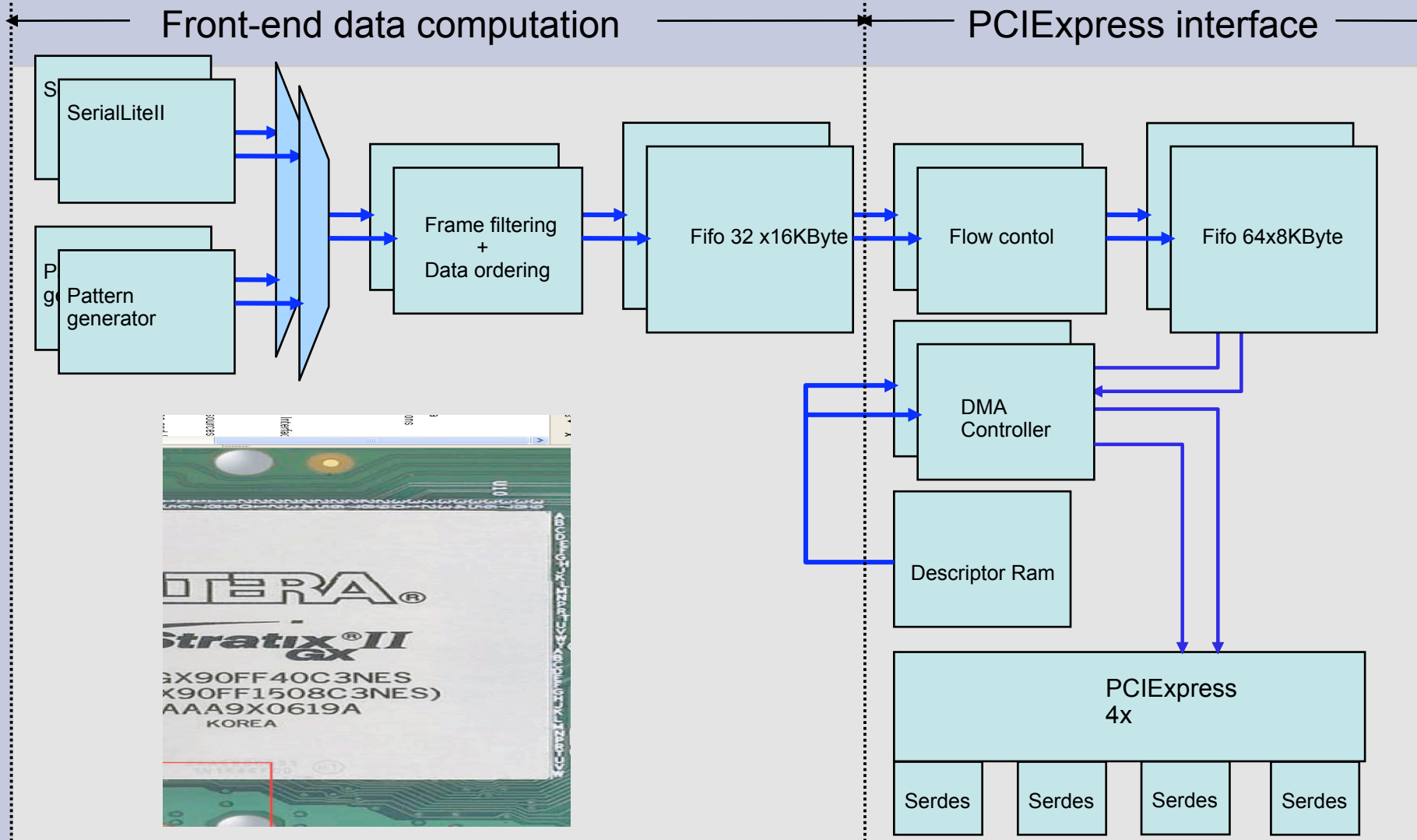
PCIExpress evaluation board





Synoptic FPGA PCIeExpress

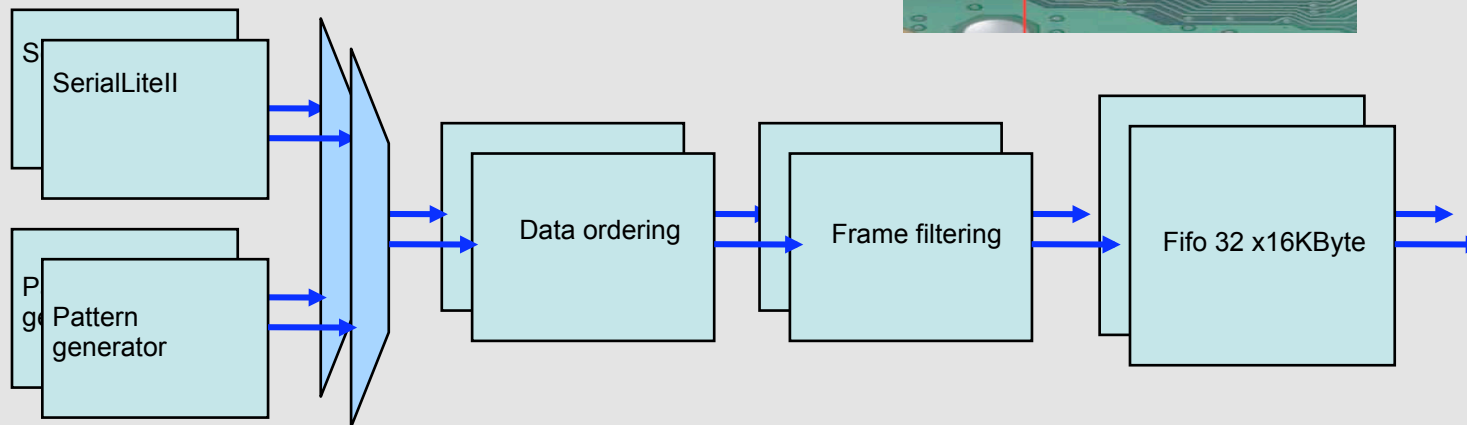
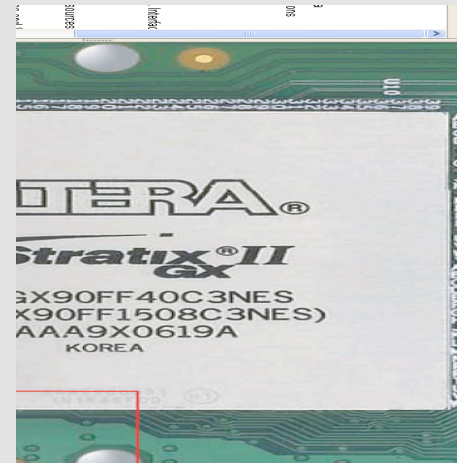
Evaluation board





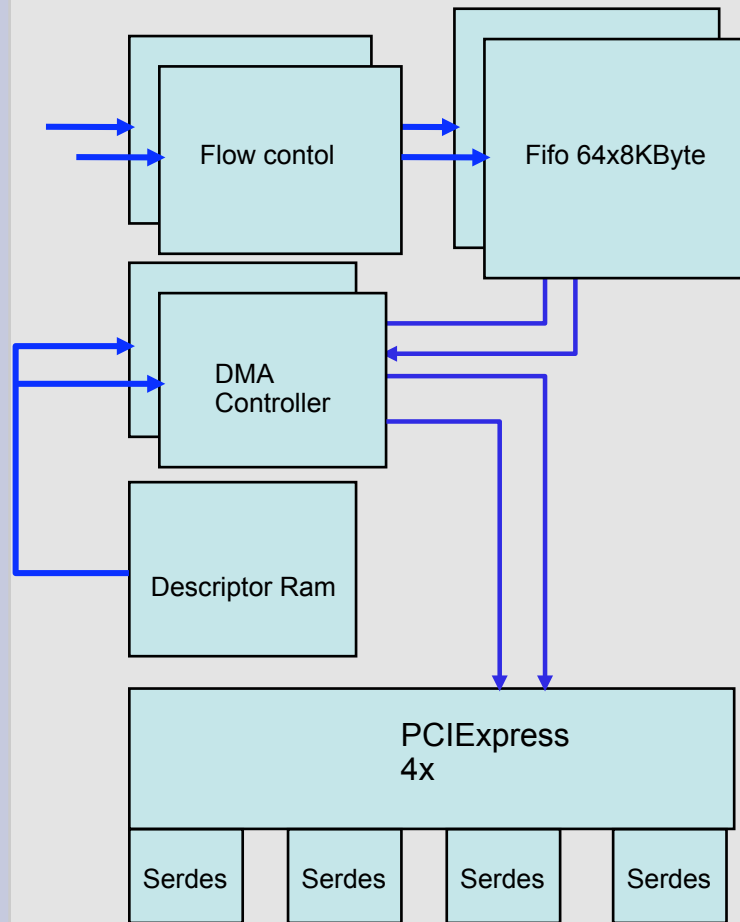
FPGA synoptic: Front-end data computation

- Link interface: SerialLiteII.
- Pattern generator.
- Data ordering.
- Frame filtering.
- Buffering: FIFO 64KByt





FPGA synoptic: PCIExpress interface



- FIFO buffering
- Scatter-gather DMA
- PCIExpress:
 - End point
 - 4X

System On Programmable Chip module

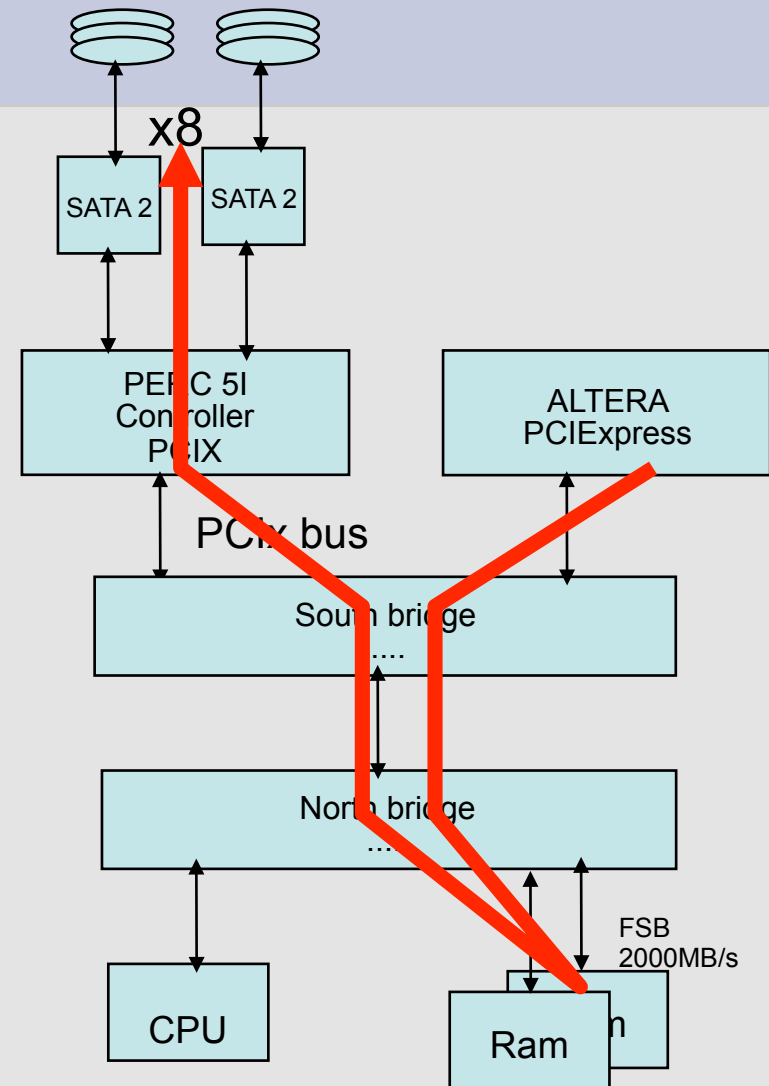
The screenshot shows the Altera SDC Builder interface with a table of connections. The table has columns for Use, Connections, Module Name, Description, Clock, Base, End, and IRG. The connections listed include:

Use	Connections	Module Name	Description	Clock	Base	End	IRG
<input checked="" type="checkbox"/>		pciexpress_compiler	PCIExpress compiler				
<input checked="" type="checkbox"/>		bar1_0_Prefetchable	Avion Memory Mapped Master	clk	0x00000000	0x00003fff	I3Q 0
<input checked="" type="checkbox"/>		bar2_0_Prefetchable	Avion Memory Mapped Master	clk	0x00004000	0x00007fff	I3Q 1
<input checked="" type="checkbox"/>		Control_Prognter_Acc	Avion Memory Mapped Slave	clk	0x00008000	0x0000bfff	
<input checked="" type="checkbox"/>		Tr_Interface	Avion Memory Mapped Slave	clk	0x0000c000	0x0000ffff	
<input checked="" type="checkbox"/>		onchip_mem	On-Chip Memory (SRAM or ROM)	clk	0x00004000	0x00004fff	
<input checked="" type="checkbox"/>		st	Avion Memory Mapped Slave	clk	0x00005000	0x00005fff	
<input checked="" type="checkbox"/>		scgma	Scatter-Gather DMA Controller	clk	0x00006000	0x00006fff	
<input checked="" type="checkbox"/>		onchip_mem_1	On-Chip Memory (SRAM or ROM)	clk	0x00007000	0x00007fff	
<input checked="" type="checkbox"/>		st_1	Avion Memory Mapped Slave	clk	0x00008000	0x00008fff	
<input checked="" type="checkbox"/>		descriptor_read	Avion Memory Mapped Master	clk	0x00009000	0x00009fff	
<input checked="" type="checkbox"/>		descriptor_write	Avion Memory Mapped Master	clk	0x0000a000	0x0000afff	
<input checked="" type="checkbox"/>		m_write	Avion Memory Mapped Master	clk	0x0000b000	0x0000bfff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x0000c000	0x0000cfff	
<input checked="" type="checkbox"/>		fifo	Avion-ST Single Clock FIFO	clk	0x0000d000	0x0000dfff	
<input checked="" type="checkbox"/>		csr	Avion Memory Mapped Slave	clk	0x0000e000	0x0000efff	
<input checked="" type="checkbox"/>		in_1	Avion Streaming Sink	clk	0x0000f000	0x0000ffff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x00010000	0x00010fff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x00011000	0x00011fff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x00012000	0x00012fff	
<input checked="" type="checkbox"/>		timing_adapter	Avion-ST Timing Adapter	clk	0x00013000	0x00013fff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x00014000	0x00014fff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x00015000	0x00015fff	
<input checked="" type="checkbox"/>		interface	streaming_0_interface	clk	0x00016000	0x00016fff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x00017000	0x00017fff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x00018000	0x00018fff	
<input checked="" type="checkbox"/>		timing_adapter_1	Avion-ST Timing Adapter	clk	0x00019000	0x00019fff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x0001a000	0x0001afff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x0001b000	0x0001bfff	
<input checked="" type="checkbox"/>		interface_1	streaming_1_interface	clk	0x0001c000	0x0001cfff	
<input checked="" type="checkbox"/>		in	Avion Streaming Sink	clk	0x0001d000	0x0001dfff	
<input checked="" type="checkbox"/>		out	Avion Streaming Source	clk	0x0001e000	0x0001efff	



Aquisition test

- Poweredge 2900
 - 2 hardware configuration:
 - 1 double core cpu, 2GB ram, 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
 - 1 quadruple core cpu, 4GB ram 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
 - Software configuration
 - Multi thread acquisition:
 - Data reading in DMA mode PCIExpress board and
 - Reading the shared memory and writing on disk

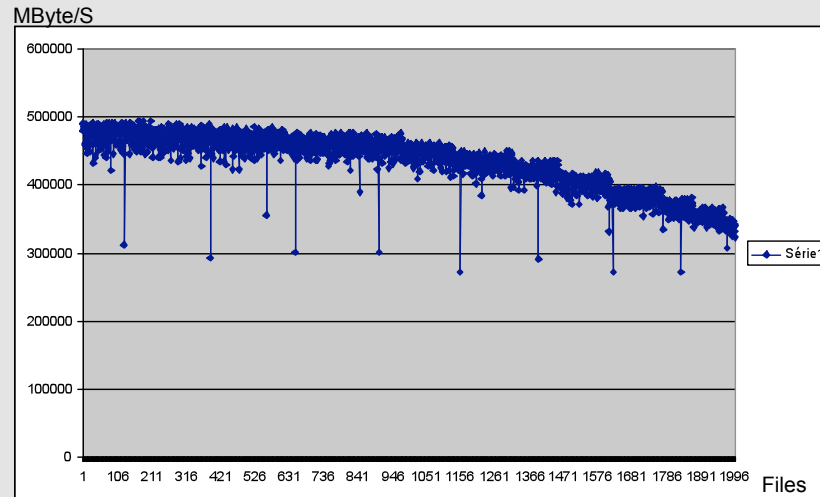




PC Data flow

PCIExpress DMA transfert :

Average throughput 430MB/s



Multi-thread acquisition software:
PCIExpress DMA
Disk write

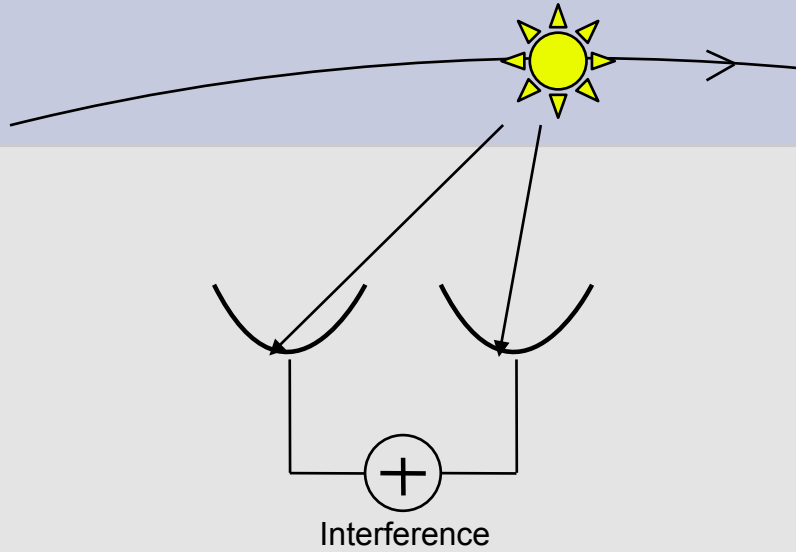
300MB/s substained data rate from
digitilizer to PC-disk

PC Data flow

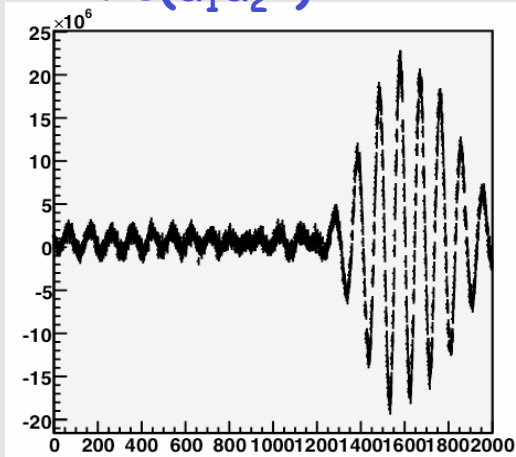
	pc-bao1	pc-sitr2	nb-planck7	pc-bao2	pc-bao3
	Workstation 390 monoproc. 2cores	PowerEdge2900 monoproc. 2cores	PowerEdge2900 monoproc. 4cores	PowerEdge T100 monoproc. 4cores	PowerEdge R710 2proc. 8cores
transfert DMA	496 Mo/s	496 Mo/s	252 Mo/s	295 Mo/s	349 Mo/s
Perte	1 pqt sur 4600	1 pqt sur 5170	1 pqt sur 2	1 pqt sur 2,4	1 pqt sur 3,3
Acquisition sans écriture sur disque	382 Mo/s	374 Mo/s	231 Mo/s	262 Mo/s	318 Mo/s
Acquisition avec écriture sur disque	46 Mo/s (pas de RAID)	290 Mo/s	230 Mo/s	127 Mo/s	296 Mo/s



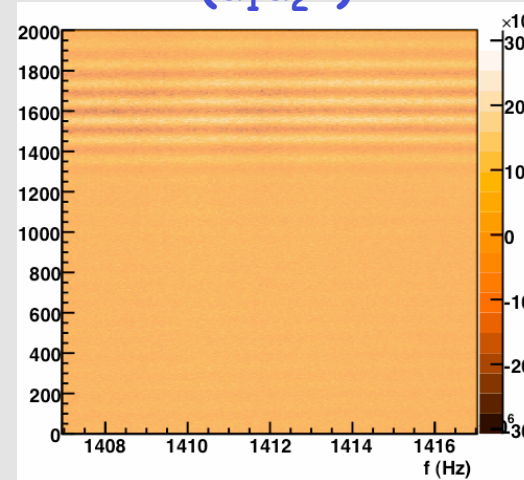
Test in Pittsburgh



$\text{Re}(a_1 a_2^*)$



$\text{Re}(a_1 a_2^*)$

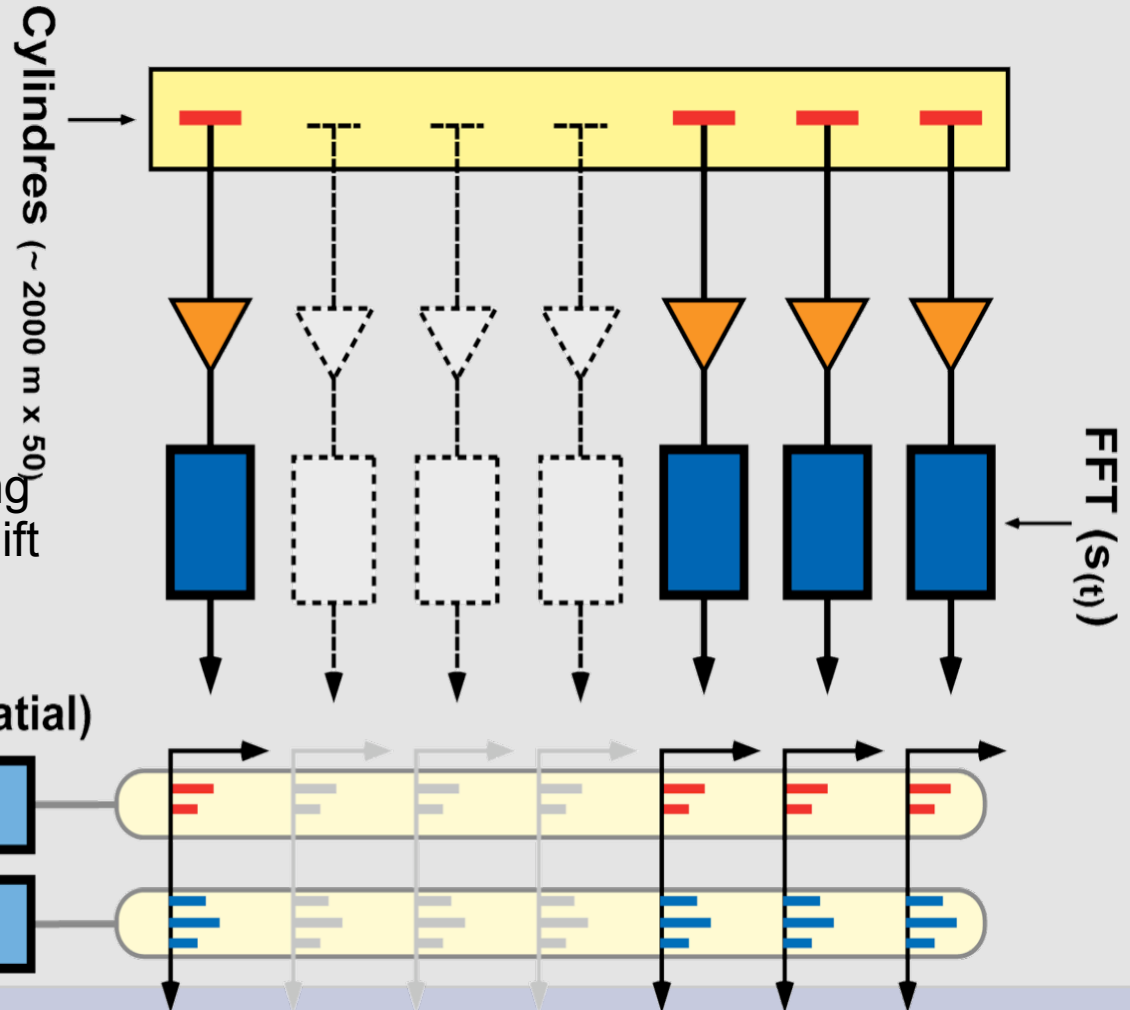
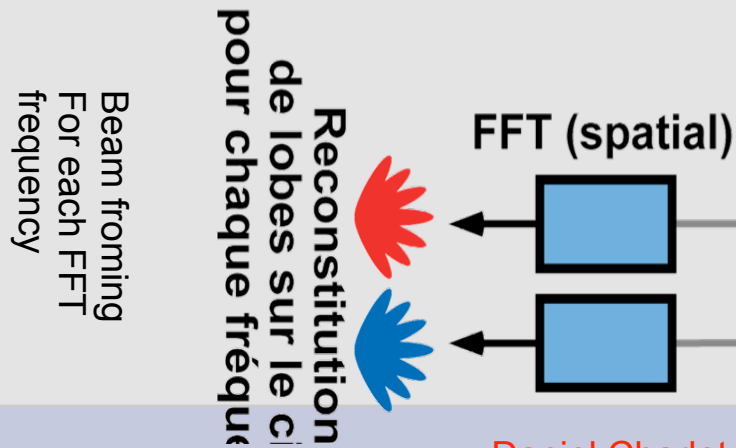




Numerical correlator

- Each channel:
 - Fast Fourier Transform
- ALL channel:
 - Combination of the
 - Same frequency

3 dimensions:
 2 angles : FFT beam forming
 Distance : frequency red-shift





In conclusion