# EICROC Project: update (March 5th, 2024)

- **Scrutinizing TDC data shifting External Trigger for all 16 channels: didn't have the time to work further on it…**
- **Working on a *complete* proposal (Step 2 of the French National Agency, 20 pages) to be submitted March 28th to try to obtain a budget to contribute to EICROC2 production + 3 years post-doctoral position at IJCLab.**
- **EICROC0 chips**
  - Feb. 20th, 2024: **24 EICROC0** ASICs were delivered to BNL in view of hybridation (EICROC0+AC-LGAD)
- ~~20~~ **10** pieces **Updated EICROC0 PCBs (test boards) and Related topics**
  - Cabling is being performed at IJCLab: **will be finalized tomorrow**
    [omitting crossing components to allow for the wire-bonding]
  - **3 PCBs** will be sent **shortly** to IPHC (Strasbourg, France) to wire-bond an EICROC0
    We propose to first test this configuration (board operational)
    * before wire-bonding EICROC0 & AC-LGAD
    * ordering 10 more PCBs
  - 3 PCBs will be sent **shortly** to BNL with associated crossing components
  - **Some AC-LGAD sensors** (from BNL) will be transferred to CERN **next week** to be given to IJCLab

[*2 PCBs are intended to be sent later on to IPHC (Strasbourg, France) to wire-bond an EICROC0 + AC-LGAD*]
*(AC-LGAD sensors provided by BNL)*
[*2 PCBs will wait for hybrids from BNL. They will be sent to IPHC (Strasbourg, France) for wire-bonding*]