Introduction and status

Tiina Suomijärvi
for the Trigger and UUB commissioning task

AugerPrime SDEU F2F meeting
3 - 5 June 2024

PIERRE AUGER OBSERVATORY

Goals of the meeting

SDEU Commissioning in progress since the end of 2020

- Meetings every 2 weeks
- Minutes of the meetings on Wiki:

https://www.auger.unam.mx/AugerWiki/SDEU_Front_Page

Trigger and UUB commissioning work packages, please, sign in!

Goals of the meeting

- Identify open issues
- Define actions and work packages

Meeting organisation

Monday 3 June

14:00 – 15:30 Introduction and noise
16:00 – 17:30 Towards high-level analysis

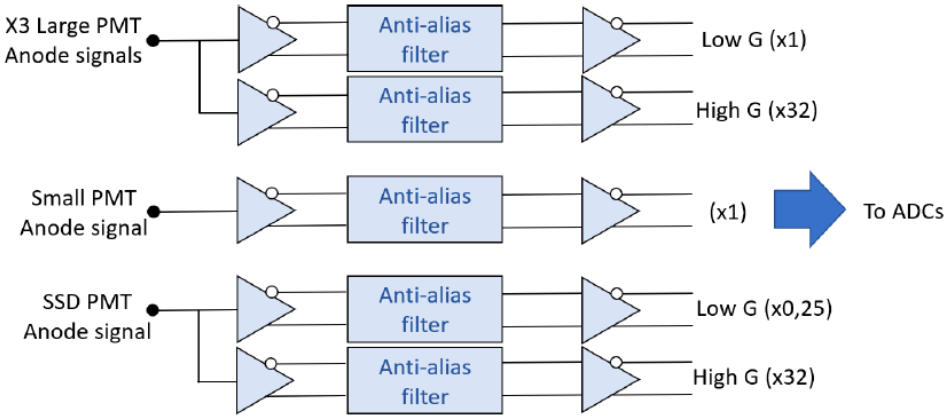
Tuesday 4 June

9:00 – 10:30 Quality control
11:00 – 12:30 Timing and calibration
13:30 – 15:30 Triggers
16:00 – 17:30 DAQ and CDAS

Wednesday 5 June

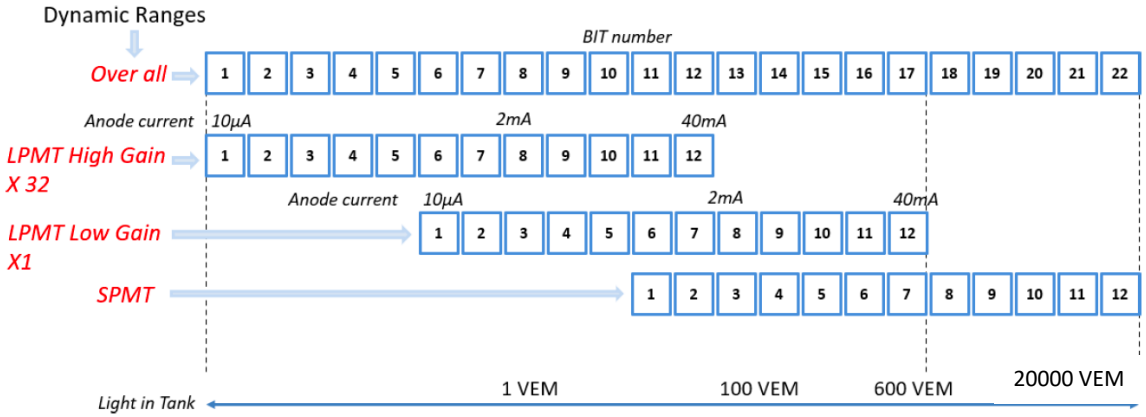
9:00 – 10:30 Hands-On Session
11:00 – 12:30 New triggers
13:30 – 15:00 Meeting outcome

Front-end



Increased WCD dynamic range by adding 1'' PMT (SPMT, Hamamatsu R8619) to the three 9" PMTs (Photonis XP1805) of the WCD.

- 10 ADC analog inputs to handle the two gains for each of the three existing PMTs, the added PMT of the SSD, and the SPMT (plus a spare channel).
- Commercial 12-bit 120 MHz dual-channel FADCs (Analog Devices AD9628)



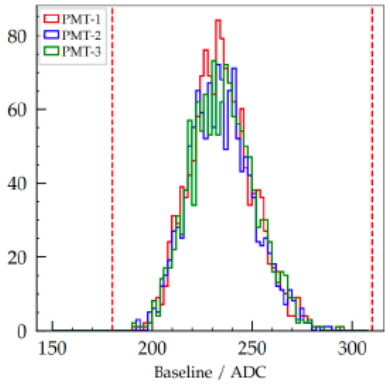
Front-end

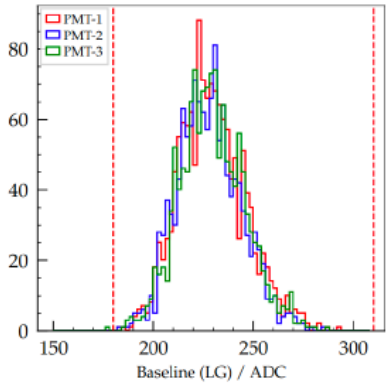
The intrinsic electronic noise measured in laboratory on the high-gain channels is about 2 LSB and 1/2 LSB on the low-gain channels.

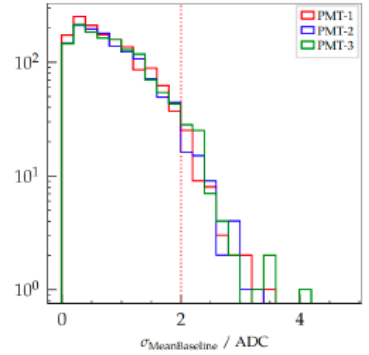
Cross-calibration measured in laboratory is 32.2 ± 0.3 for the WCD channels and 126.7 ± 1.3 for the SSD channels.

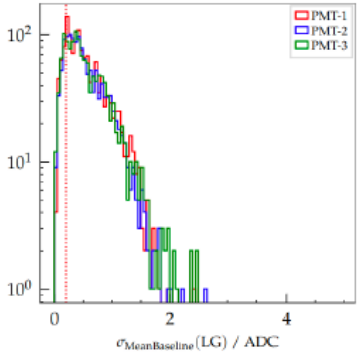
Action: Confirmation of HG/LG ratio in laboratory (Prague)

Baseline values and their variations are in the expected range.





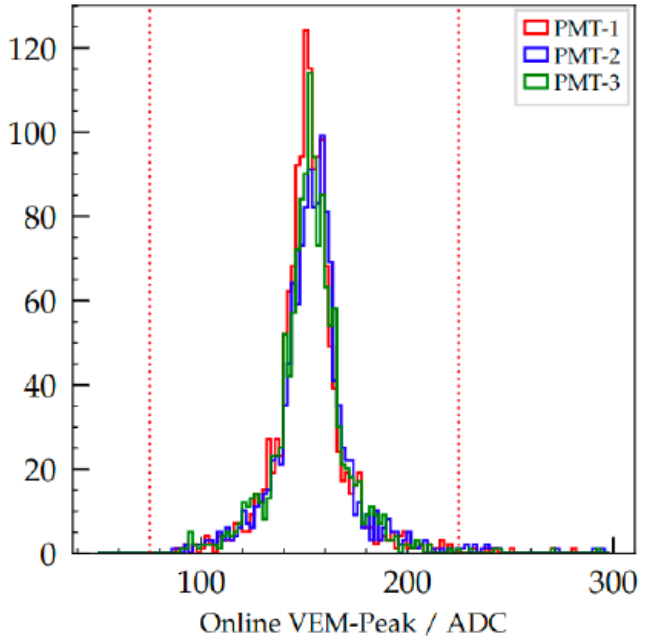




See Martin's presentation on the noise issues.

Calibration

- UUB records calibration histograms for LPMTs and SSD PMTs for offline calibration.
- UUB provides an online calibration of the VEM-peak for the compatibility traces.
- Mean value 150 ADC with sigma ~20 ADC
  Instabilities from unstable PMTs
  (otherwise, variation < 1 ADC per day)



Actions

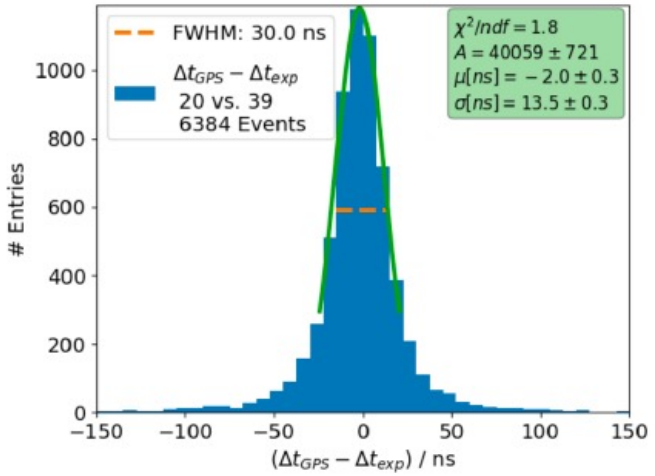
- Use SSD for better accuracy in WCD calibration
- Provide SSD online calibration of the MIP peak
- Online/offline charge values?

For SPMT calibration see the presentation by Gialex.
See also the presentation by Paul for SSD calibration.

Timing

- Synchronization by tracking variations of the local 120 MHz clock with respect to the 1 PPS signal of the Global Positioning System (GPS)
- Synergy SSR-6TF timing GPS receivers, functionally compatible with the Motorola Oncore UT+ GPS used with previous electronics

The relative timing accuracy (variance on the timing of common signal between two SSR-6TF receivers) was measured in laboratory to be around 2ns and in the field between two detector stations (with fiber) around 5ns.



Measured timing resolution on showers using 2 nearby stations. Single station resolution is 13.5/√2 = 9.5 ns.

Actions

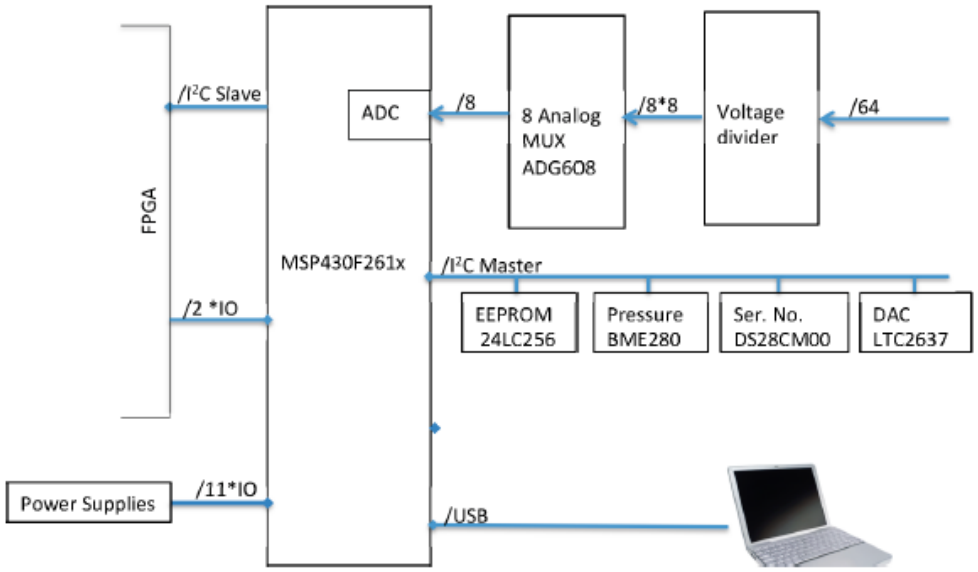
- Confirm relative offsets measured in laboratory (CWRU): about 5 ns, negligible?
- Confirm the time difference between SSD and WCD muons: about 50 ns, implement in muon buffers?
  See the presentation by Ioana.

WCD and FD time difference confirmed to be about 68 ns (Fabio and Francesco, 260324), problem with Co.

Action: Study impact on FD reconstruction

Control and monitoring

- 16-bit RISC CPU ultra-low-power micro-controller (MSP430)
- Controls and monitors the PMT high voltages and various supply voltages
- Provides watchdog and reset functionality
- Controls 16 logic I/O lines, steers a 12-bit DAC with eight analog outputs, and senses through multiplexers up to 64 analog signals with its internal 12-bit ADC



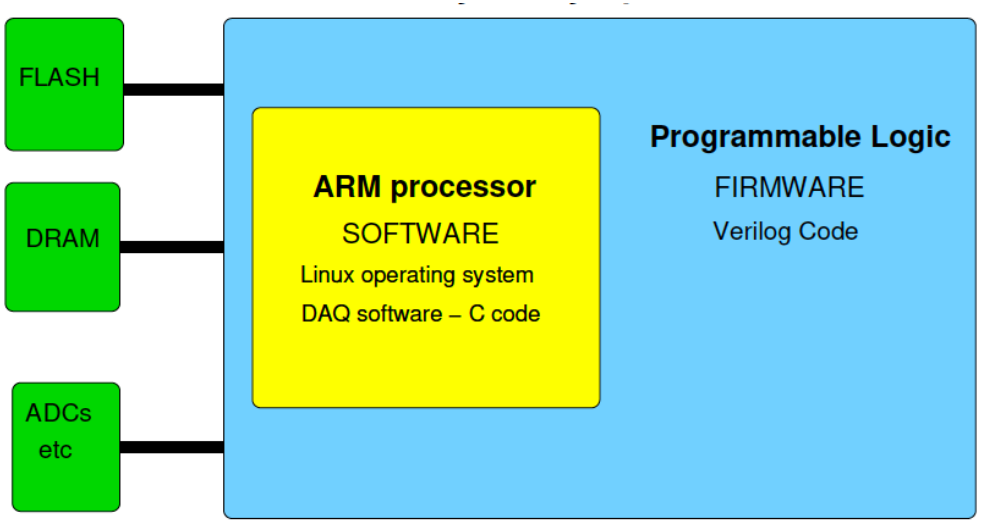
Action: Need to update quality cuts and alarms

See the presentation by Julian on the status of monitoring.
See the presentation by Piera on the PMT quality selections.

Firmware/Software

- The UUB architecture designed with a Xilinx Zynq FPGA containing two embedded ARM Cortex A9 333 MHz microprocessors
- The FPGA connected to a 4-Gbit LP-DDR2 memory and a 2-Gbit Flash memory
- The FPGA implements all basic digital functions such as the read-out of the ADCs, the generation of triggers, the interface to LED flasher, GPS receiver, clock generator, and memories
- High-level functions like data handling and communications with the radio transceiver are implemented under Linux.

Xilinx Zynq FPGA



See the presentations by Ricardo (DAQ) and David (CDAS).

Trigger

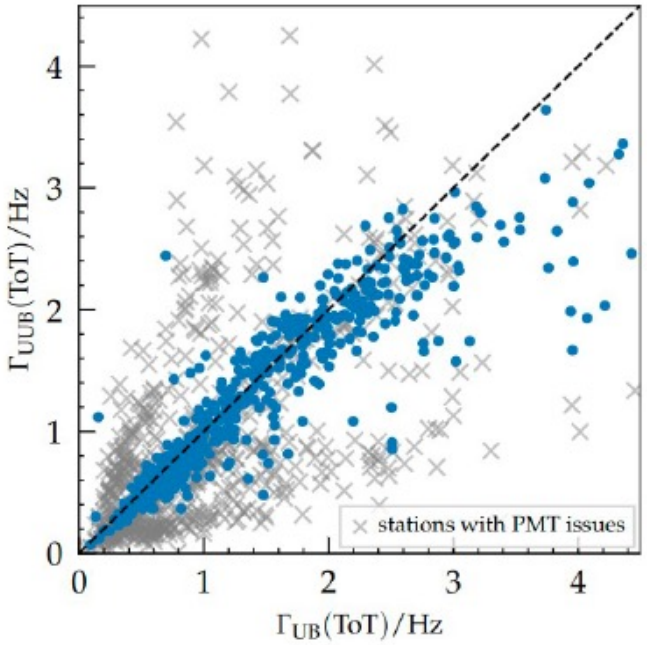
Multi-level triggering scheme

- T1 is formed by the programmable logic and causes the traces to be transferred to the ARM processor. The local T2 trigger is formed by software.
- The previous local triggers, threshold, and time-over-threshold (ToT) triggers are transferred to new electronics: compatibility triggers (40 MHz).
- WCD trigger is used for the readout of SSD and RD.
- New triggers (RD) are under development.

Rates for standard triggers in compatibility mode are similar to those of UB.
See the presentation by Martin.

MoPS and ToTd are still in commissioning due to transient noise problems.

See the presentation by Dave.
For new triggers: Dave and Jannis.



Action
Get MoPS and ToTd working.

Interfaces

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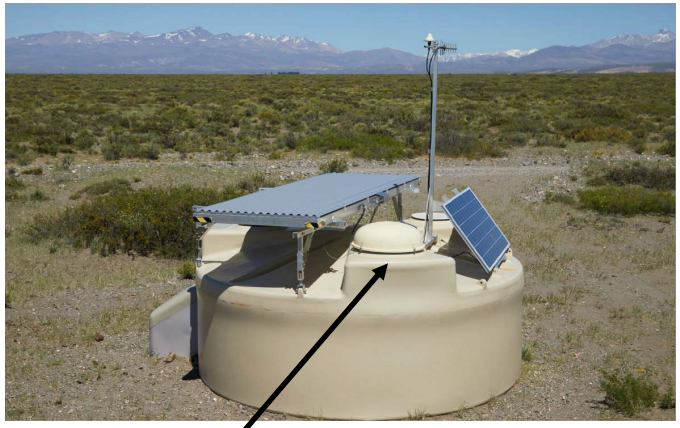
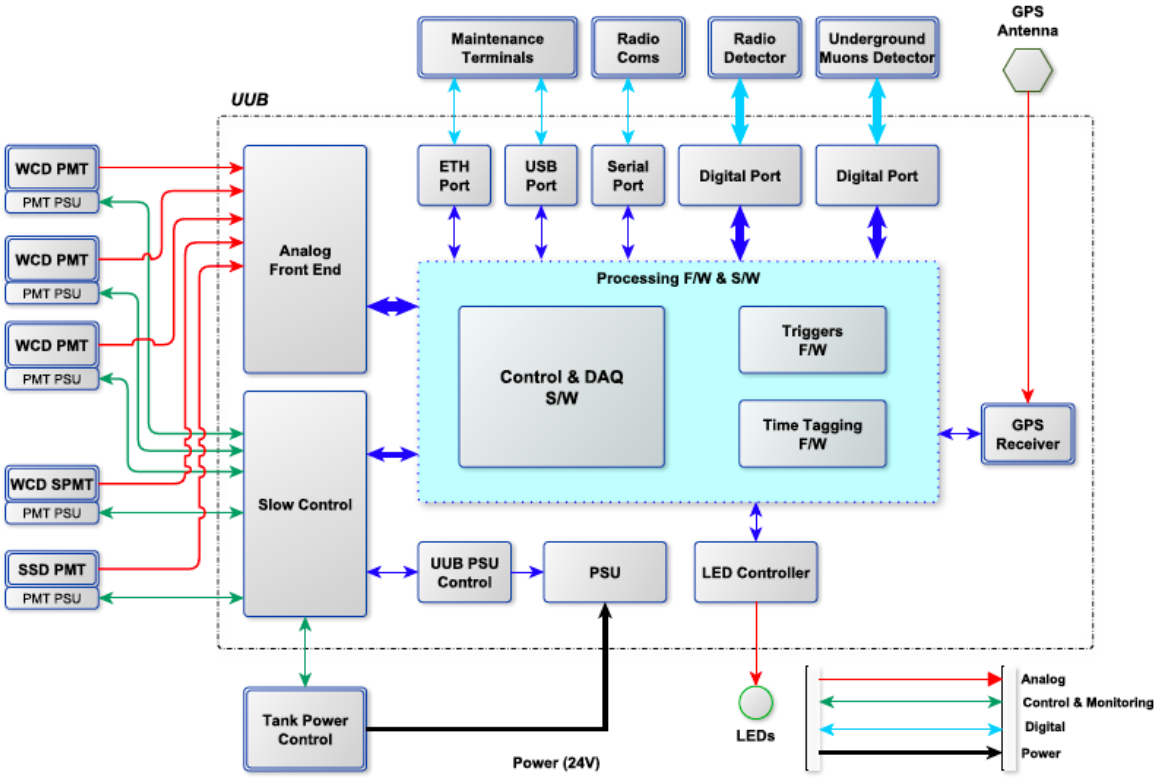
UUB



Electronics under a weather enclosure

Electrical interfaces of UUB

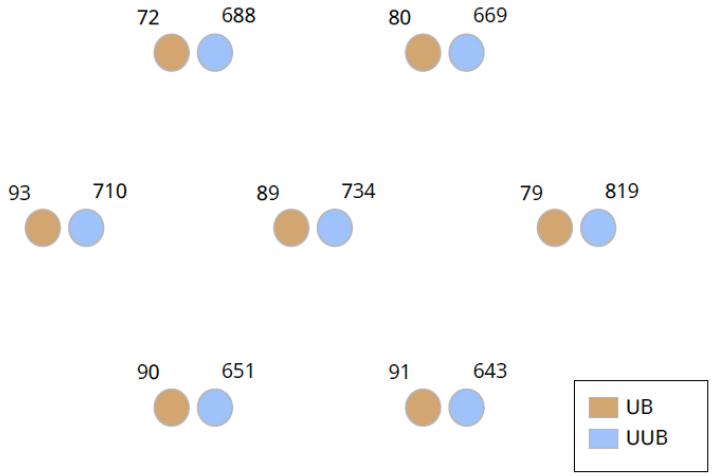


- Two 8-bit digital ports provided for additional detectors
- UUB interfaced with the actual communication system providing 1200 bps data transmission rate, and with the power system providing 24 V from the batteries

Interfaces have been tested and work.

UB – UUB comparison

The UB-UUB compatibility has been verified by using the UUB-UB hexagon array (Allan Peyras, GAP 2023-033).



UUB-UB hexagon array

TB: Hexagon triplet with UB-UUB-UUB

Actions

- Perform the studies of Allan with better statistics?
- Define missing studies
- Plan for paper: Phase 2 – Phase 1 performance comparison?

Field issues

Some noise issues were observed in the field possibly related to bad cabling, bad grounding, lightning, TPCB, and open connectors. Some of them have already been mitigated: TPCB modification, 50 Ohm caps, and better cabling.

See the presentation by Martin on the noise issues.

Actions

- Confirm the field mitigations.
- Estimate the effect of noise issues on data.

See also the presentation by Corinne on Hexagon monitoring.

Towards high-level analysis: requirements by David.

Agenda

Monday 3 June

14:00 – 15:30 Introduction and noise issues
14:00 – 14:30 Introduction and status, T. Suomijärvi
14:30 – 15:00 Noise overview, M. Schimassek
15:00 – 15:30 Discussion
15:30 – 16:00 Coffee, Conviviality room

16:00 – 17:30 Towards high-level analysis
16:00 – 16:30 Requirements for high-level analysis, D. Schmidt
16:30 – 17:00 Online – Offline comparison
17:00 – 17:30 Discussion

Wednesday 5 June

9:00 – 10:30 **Hands-On Session**, Organized by M. Schimassek
10:30 – 11:00 Coffee, Conviviality room

11:00 – 12:30 New triggers
11:00 – 11:30 RD trigger, J. Pawlowsky
11:30 – 12:00 Other new triggers, D. Nitz
12:00 – 12:30 Discussion
12:30 – 13:30 Lunch buffet, Conviviality room

13:30 – 15:00 Meeting outcome
13:30 – 14:00 Timeline for firmware changes, D. Nitz
14:00 – 14:30 Action items, T. Suomijärvi
14:30 – 15:00 Discussion

Tuesday 4 June

9:00 – 10:30 Quality control
9:00 – 9:30 SD-Performance: Quality Selections, P. Ghia
9:30 – 10:00 What is missing in monitoring and alarms? J. Rautenberg
10:30 – 11:00 Discussion
10:30 – 11:00 Coffee, Conviviality room

11:00 – 12:30 Timing and calibration
11:00 – 11:20 Timing between SSD and WCD, I. Maris
11:20 – 11:40 SSD calibration, P. Filip
11:40 – 12:00 Status of SPMT calibration, G. Anastasi
12:00 – 12:30 Discussion
12:30 – 13:30 Lunch buffet, Conviviality room

13:30 – 15:30 Triggers
13:30 – 13:50 Hexagon exposure, C. Berat
13:50 – 14:10 Comparison of UB and UUB triggers, M. Schimassek
14:10 – 15:00 MOPS and ToTD, D. Nitz
15:00 – 15:30 Discussion
15-30 – 16:00 Coffee, Conviviality room

16:00 – 17:30 DAQ and CDAS
16:00 – 16:30 DAQ open items, R. Sato
16:30 – 17:00 CDAS open items, D. Schmidt
17:00 – 17:30 Discussion

Practical information

The dinner on Tuesday will be at **Le Petit Cervantes 36, rue des Cinq Diamants, 75013 Paris (Butte aux Cailles).**

Take **RERB to Denfert Rochereau**, change to **Metro 6 direction Nation**, Get out in **Corvisart** station, exit left, then go up the stairs through the building, after you will cross Rue Cinq Diamants.

I wish you all a nice meeting!