FPGA Characterization

EICROC0 Meeting

IJCLab

July 19, 2024

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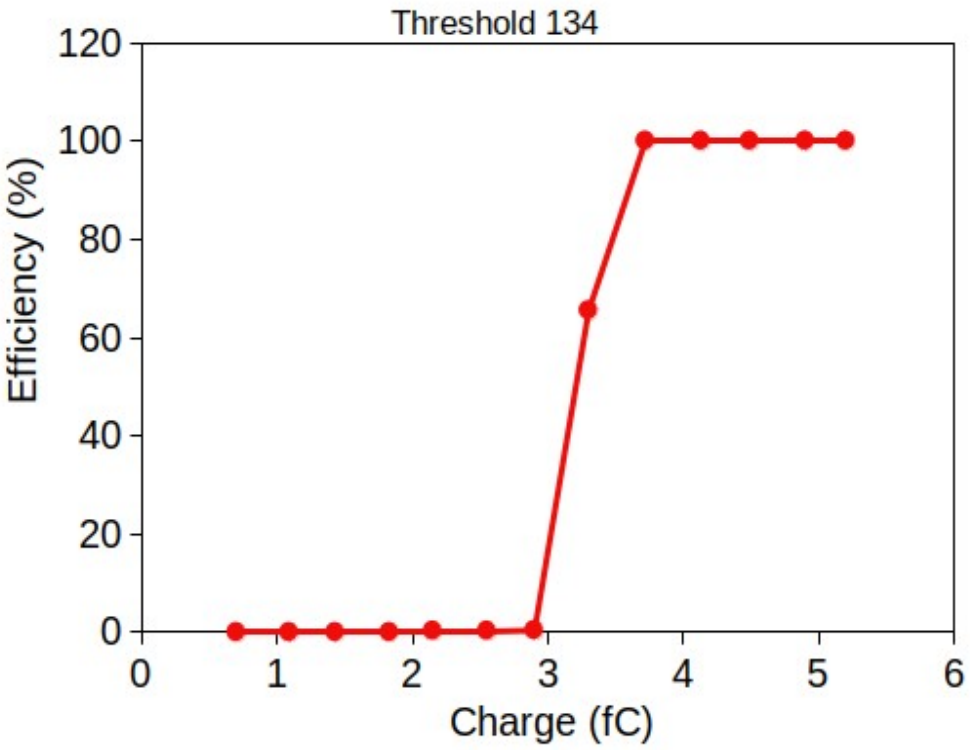
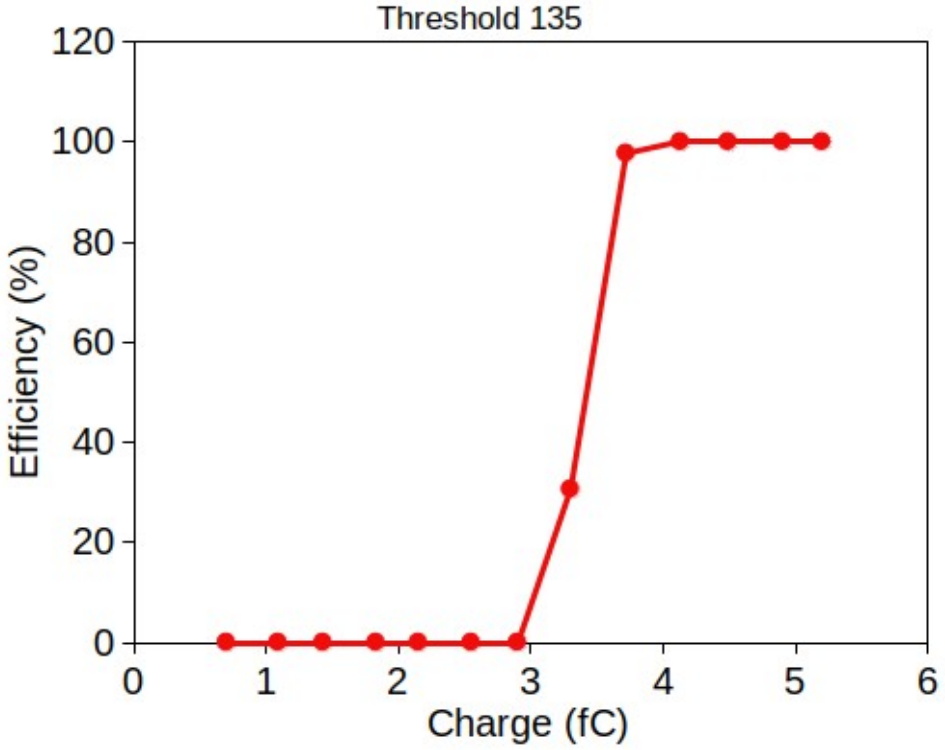
Efficiency vs Charge

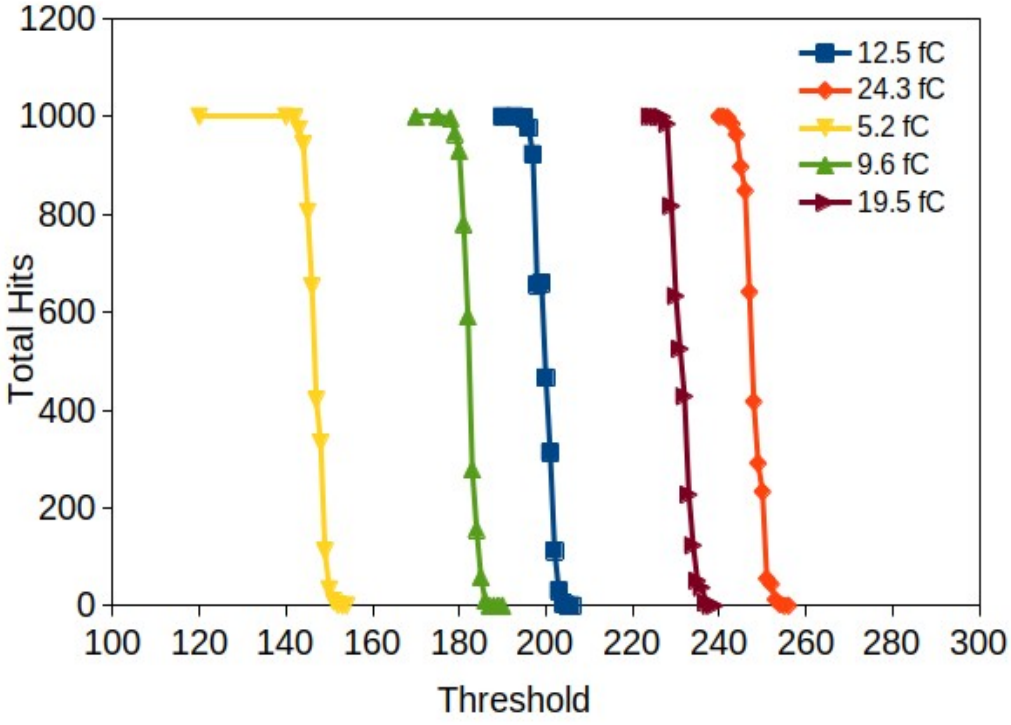
Measurements for channel1 / pixel (0,1) for board with no sensor

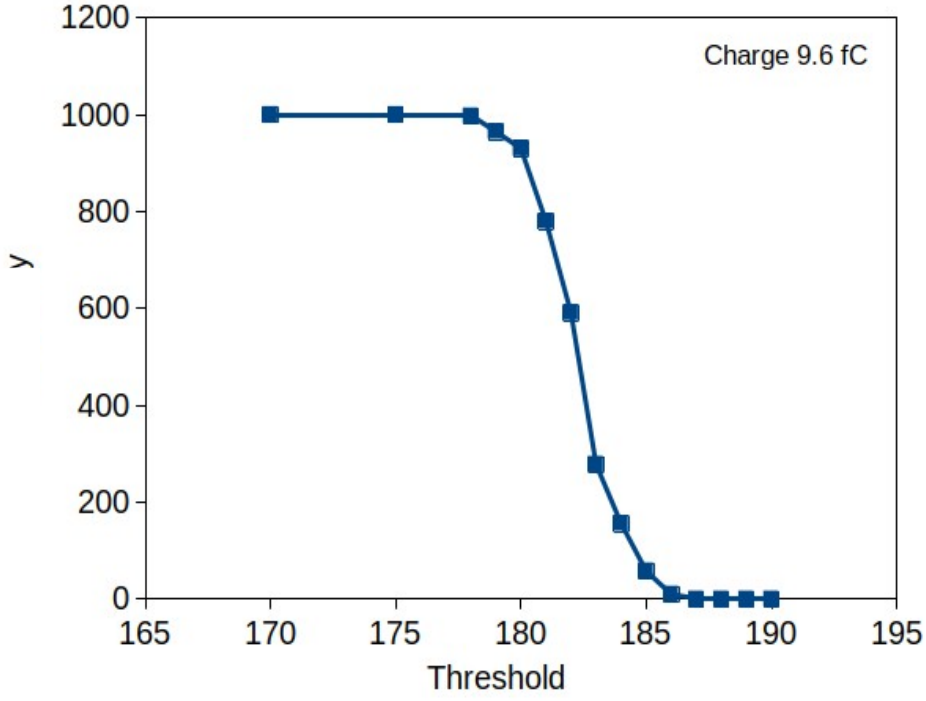




- Threshold below 134, gives events at DACu 0 (at 133, 2% eff)
- At 134, 100% eff at 3.7 fC
- At 135, 98% eff at 3.7 fC

Efficiency as a function of Threshold

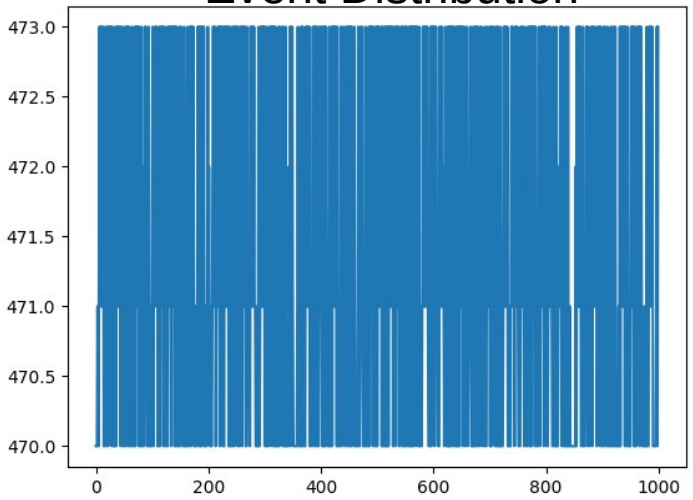




Require internal charge – threshold calibration

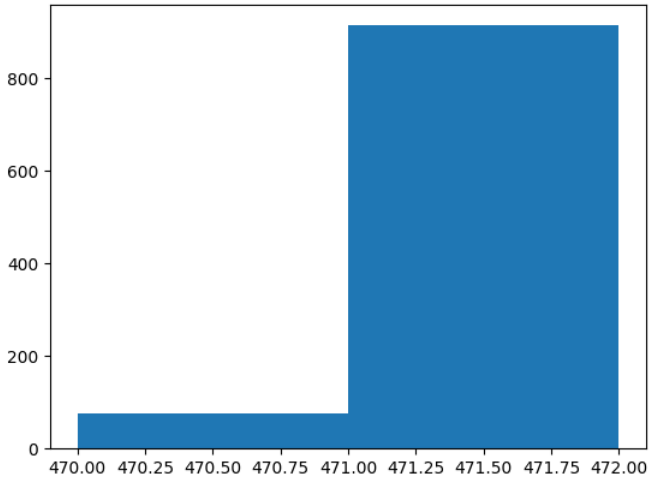
TDC distribution

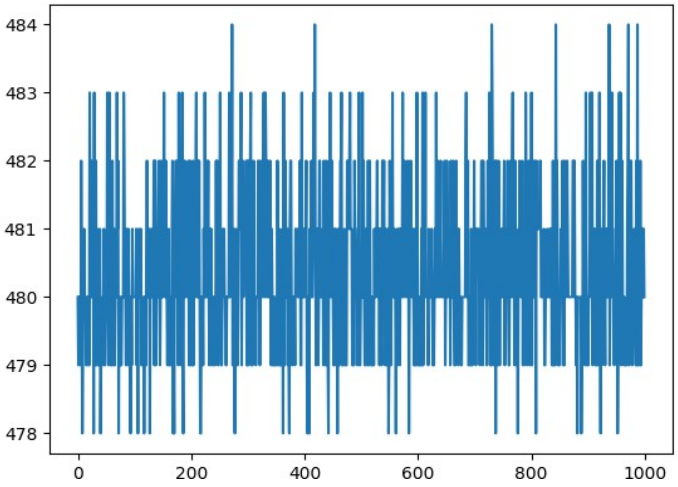
Event Distribution



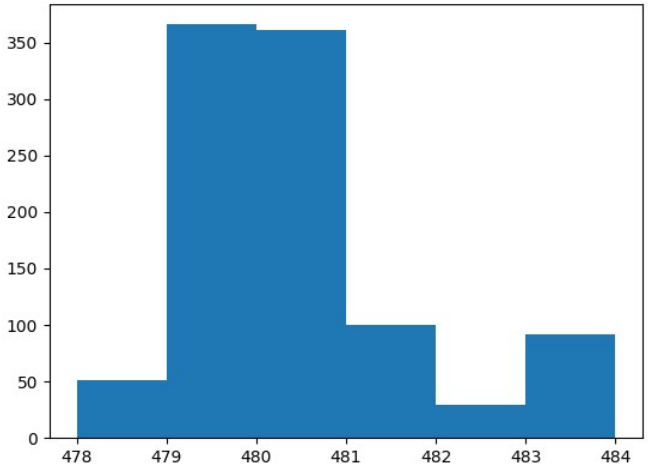
DAC55

Time Distribution





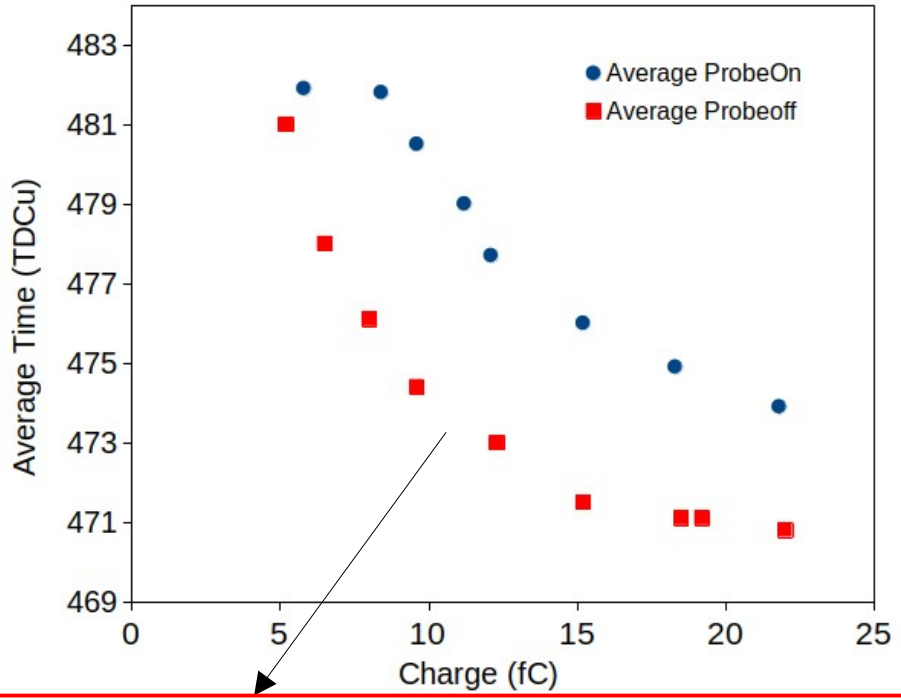
DAC16

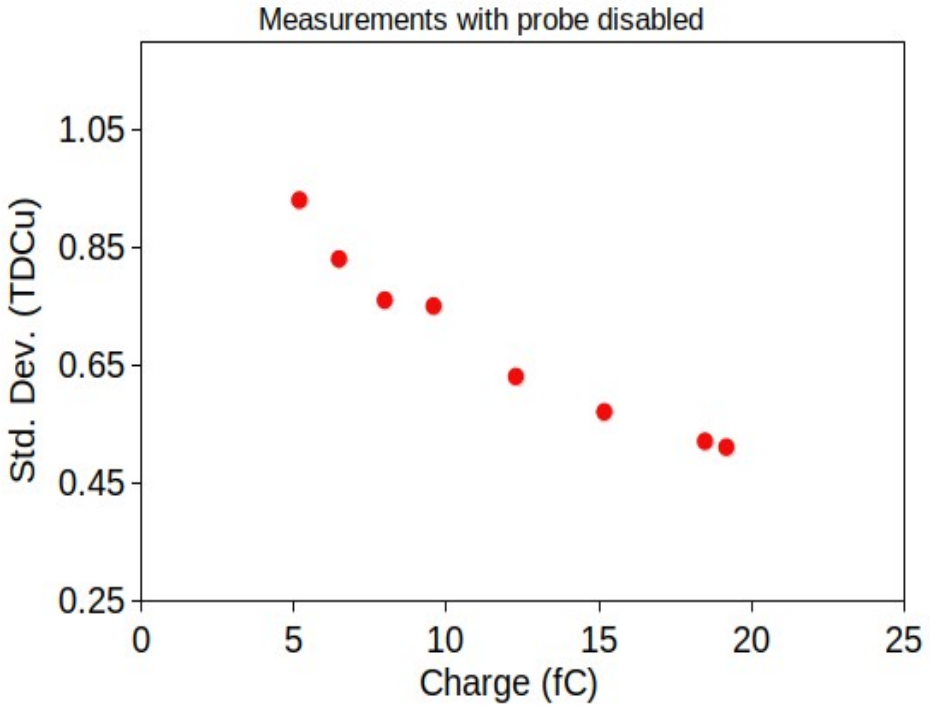


TDC Measurements

- Average time and standard deviation measured as a function of charge.
- Threshold at 135 (100% trigger efficiency for Q > 4fC).

At 20 fC,
σ = 12.5 ps
1 TDCu = 25 ps



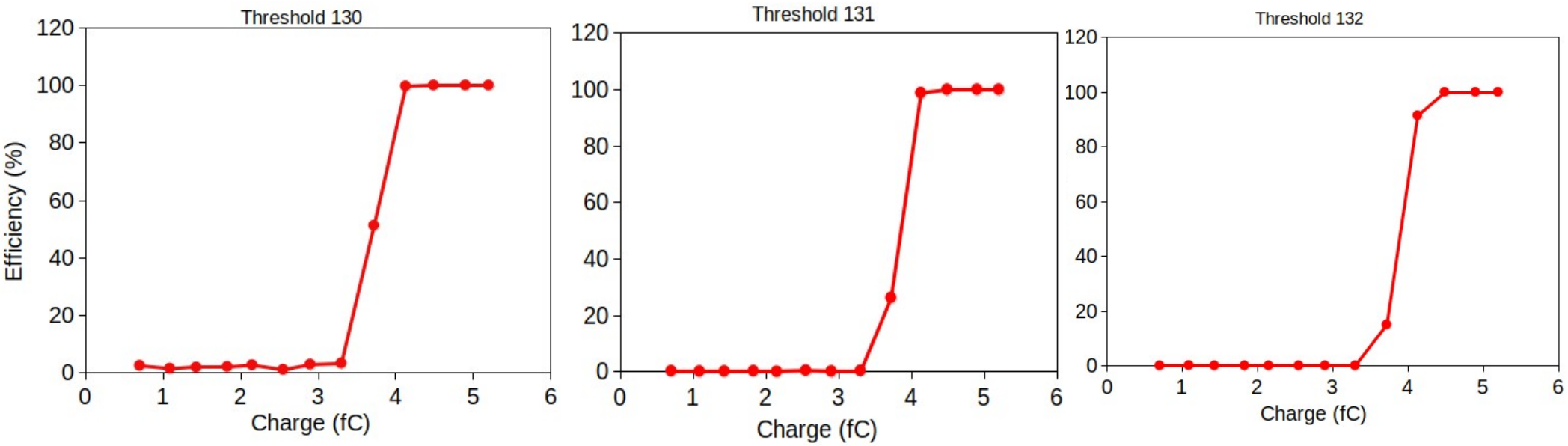


Different Amplitude Implies time walk

Conclusion

- Tests performed for board without sensor and with one of the channels
- Characterization tests performed for understanding different charge and threshold values.
- So far, with channel1, 100% efficiency obtained with charge ~ 3.7 fC at threshold 134.
- Sigma obtained ~12.5 ps at 20 fC charge.

Efficiency vs Charge



100% efficiency observed for charge > 4 fC.
At 130 threshold, minimum charge (DAC0) has hit efficiency of 2.5%.
At 130 threshold, more than 50% efficiency.