IDROGEN : An high data rate acquisition system synchronize by a enhance WhiteRabbit node

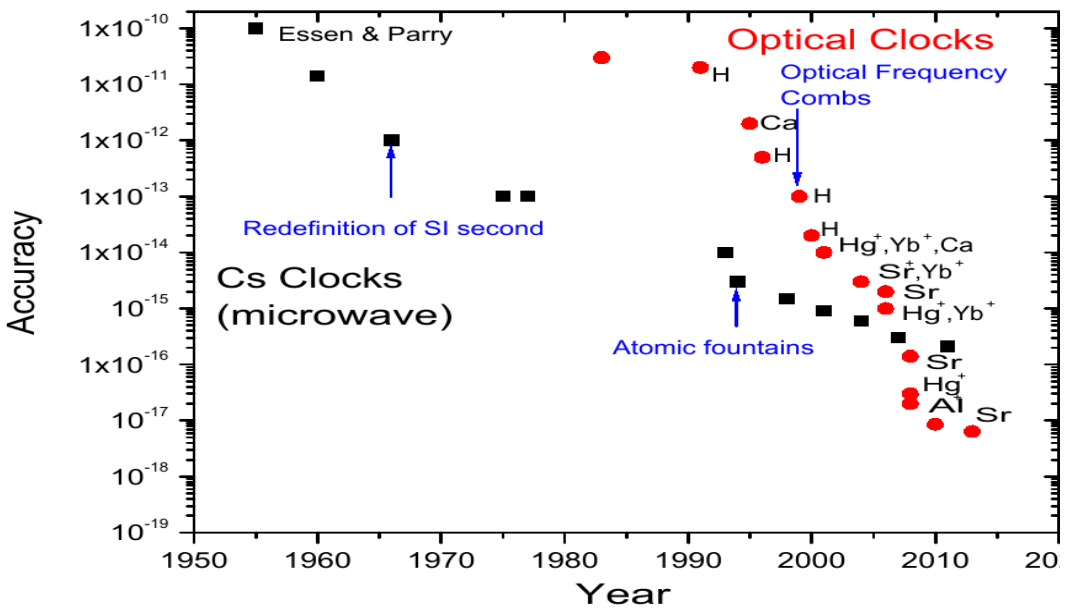
The collaboration

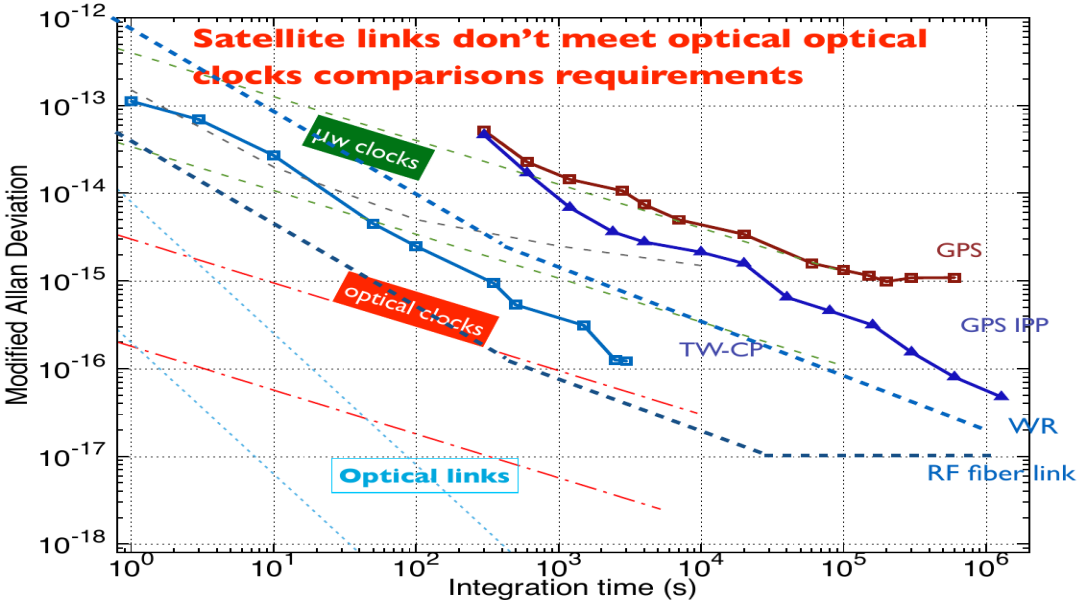
- **IJCLab** : Scientific themes : Astroparticles, Astrophysics &Cosmology, Nuclear physics, High Energy Physics, Accelerator Physics, Theory, Heath, Energy
  - Hardware : Daniel Charlet
  - Firmware : Eric Plaige, Antoine Back, Cédric Esnault, D.Charlet
  - Software : Monique Taurigna, Chafik Cheikali, A.Back, Christelle Soulet
  - Test : Cédric Esnault, Daniel Charlet
- **Paris Observatory :** Scientific themes : Time and frequency metrology, time and frequency transfer, inertial sensors, space-time reference frames, theory, epistemology
- **SYRTE**
  - Clock expertise and qualification : Paul-Eric Pottie
  - Hardware : Michel lours
- **Obs Nancay**
  - Firmware : Cédric Viou

l'Observatoire de Paris | SYRTE
Systèmes de Référence Temps-Espace
Station de Radioastronomie de Nançay

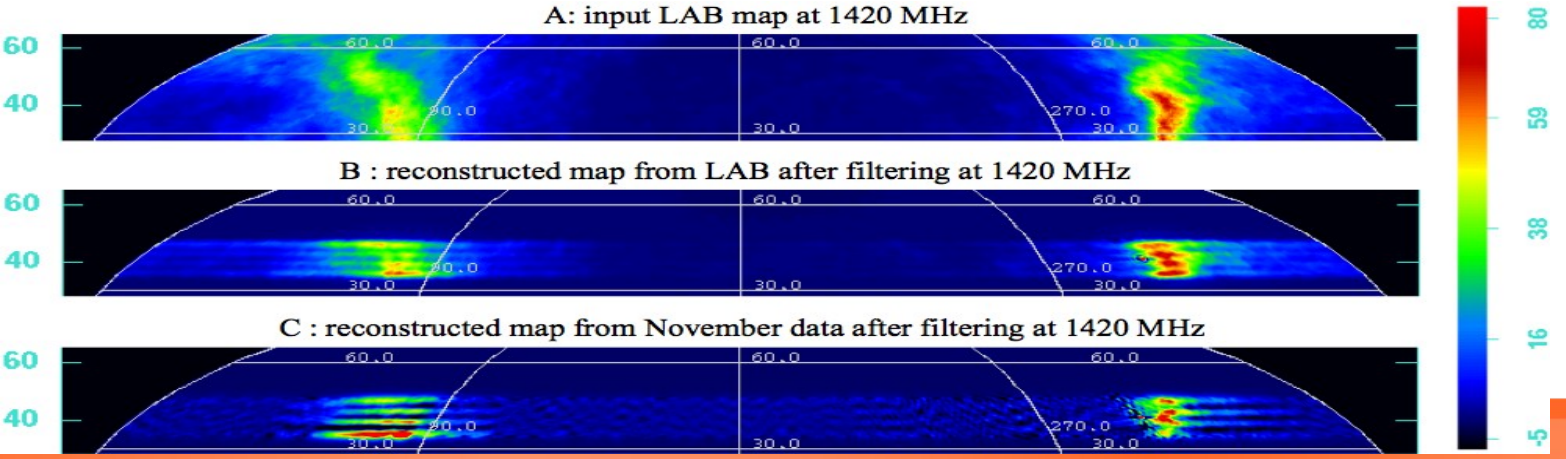
Clock and time distribution performance

- Drastic improvement in clock performance

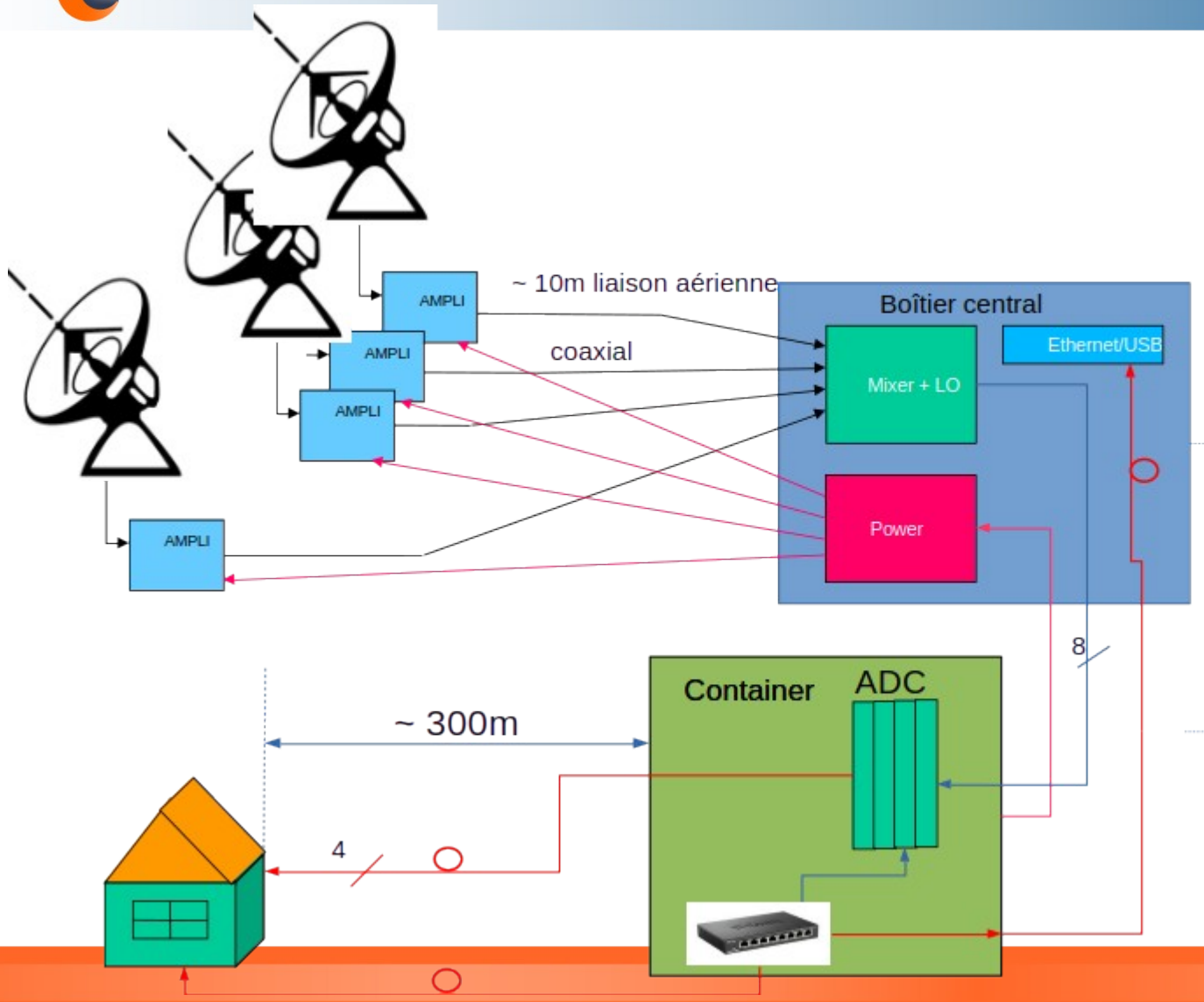




- PAON IV Radio interferometer
- 3D mapping of cosmological matter distribution in the univer.
- Use the 21 cm line of the atomic Hydrogen (1.4GHz)
- Locate at Nancay observatory
- 4 dishs of 5 meter



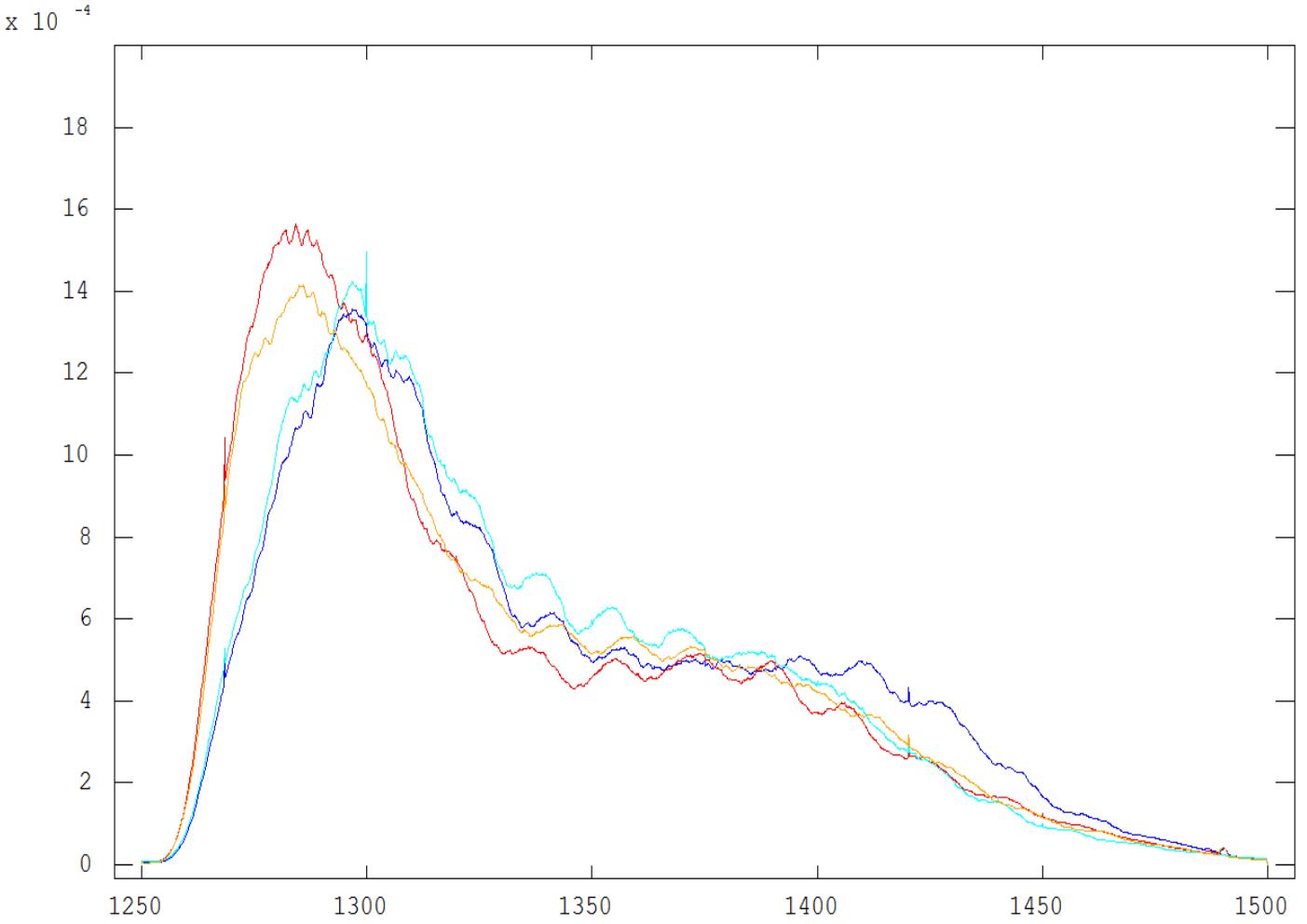
PAON4 : Historical configuration



- Centralize acquisition system
  - Benefits
    - System synchronization
    - System configuration
    - Global packaging
    - Maintenance
  - Disavantages
    - Surface limited extension
    - Limited coaxial length

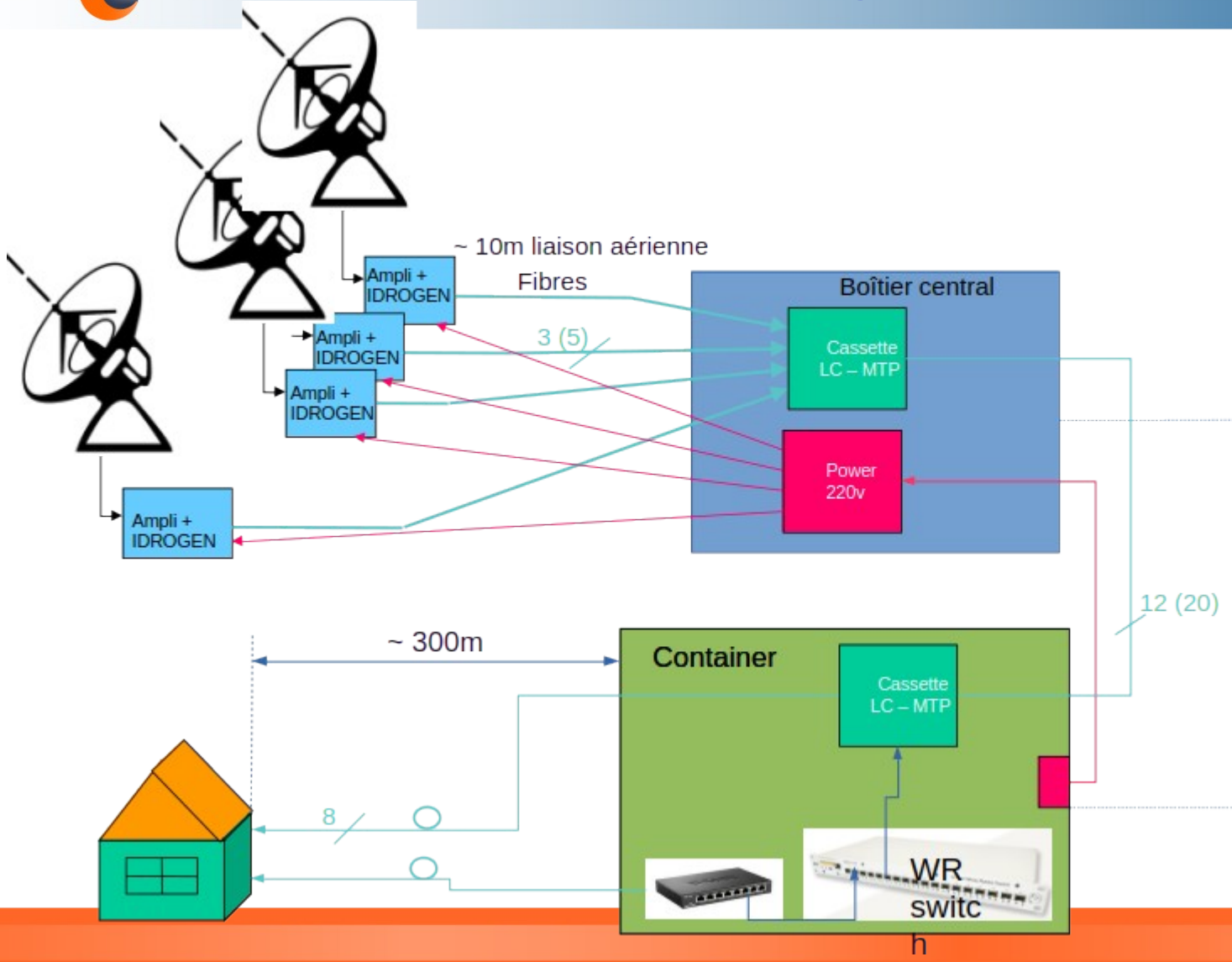
      (attenuation, bandwith, prices, thermal effect, ...

Analog limitations



- SWR problem
  - long RF cables,
  - adaptation mismatch,
  - wide band acquisition
  - frequency shifting
  - technical constraints for packaging
- Calibration
  - Thermal effects due to atmospheric condition

PAON4 : Future configuration

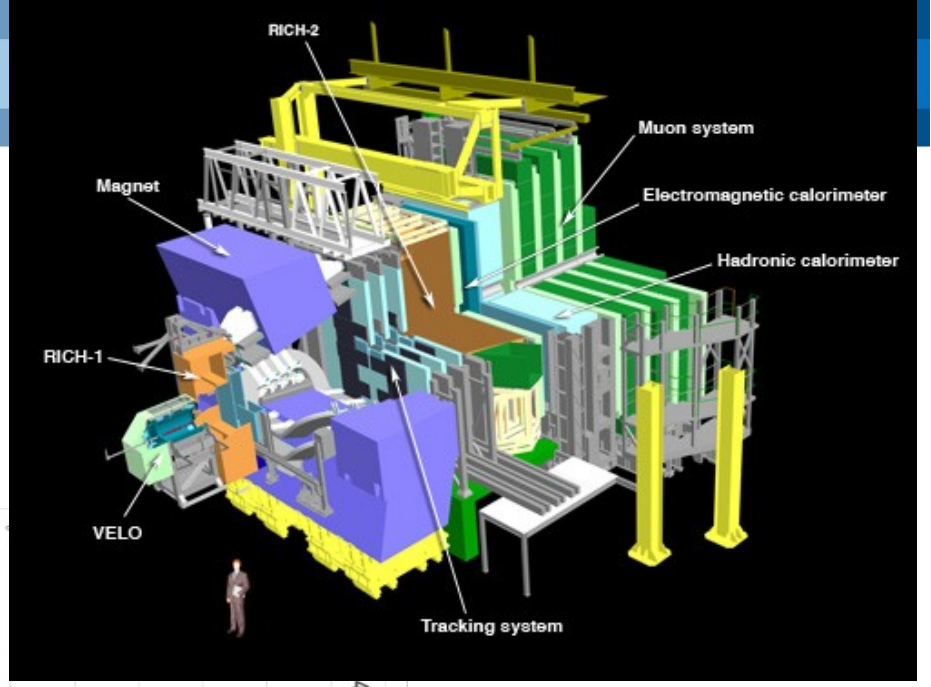


- Distributed acquisition system
  - Benefits
    - No limited extension
    - Short RF extension
  - Disavantages
    - Long distance synchronization
    - Individual packaging
    - Distributed maintenance

Accelerator : Master oscillator distribution

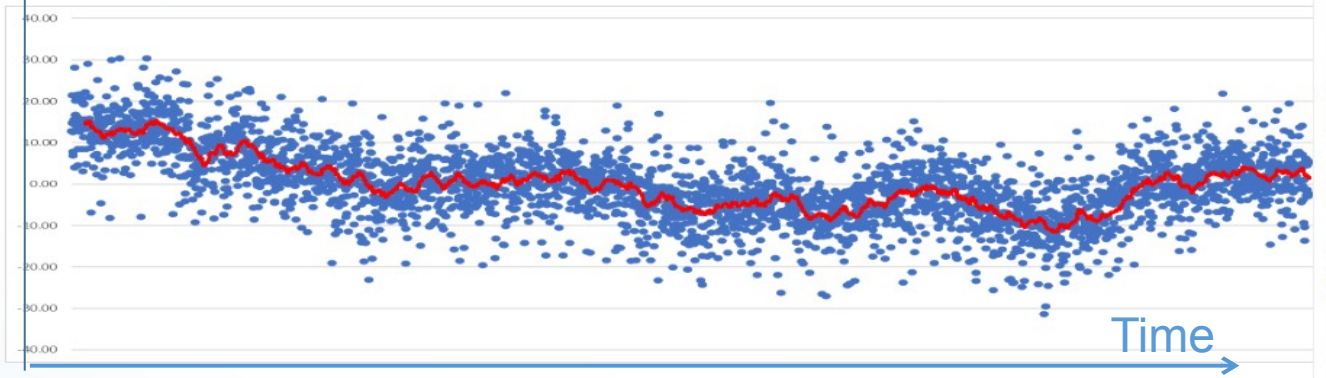
- Real-timed communication system : tight time constraints
- Long distances between nodes : long transmission delays
- Numbers of nodes : several hundred
- Dynamic changes to the numbers of nodes : not easy

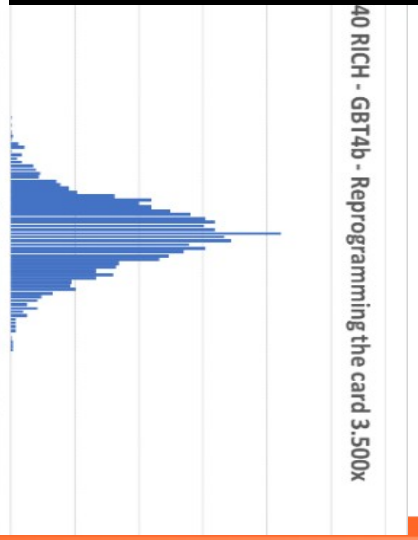
Ritch detector : clock drift example



Over 5 days

SOL40 RICH – GBT4b – Reprogramming SOL40 3500x
Over 5 days of test
Center of recovered clock distribution drifted over ~25ps
Most likely due to temperature





The resolution of the SOL40 PLL shift is ~100ps

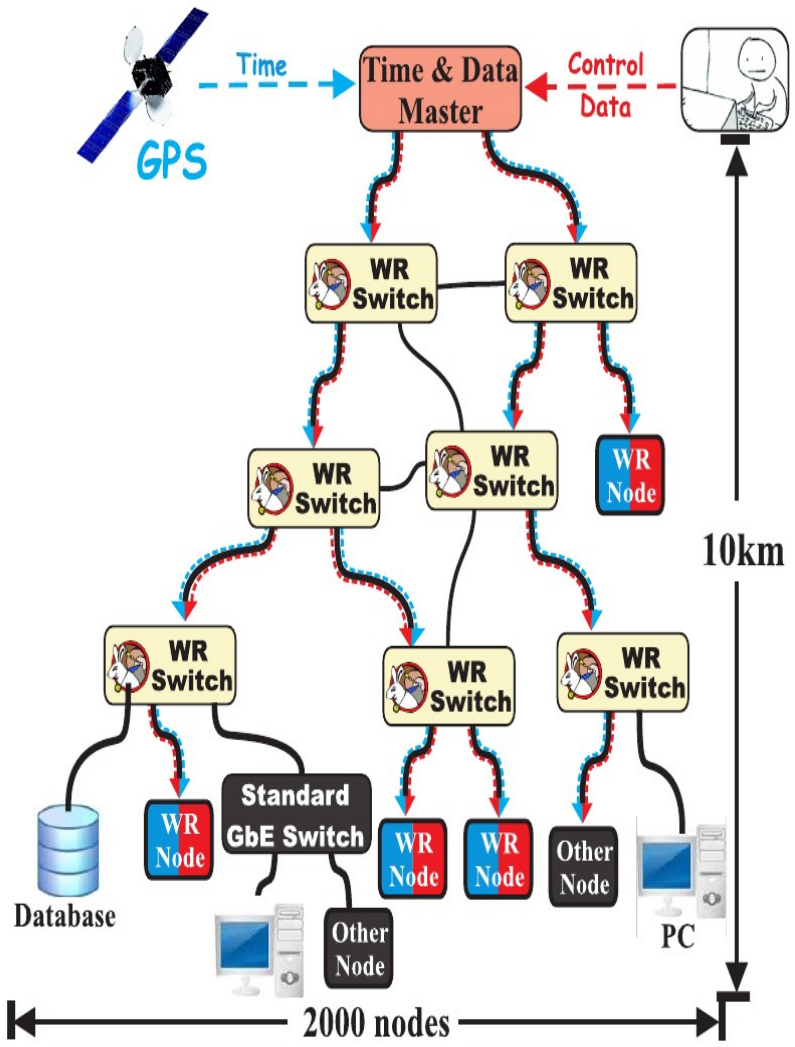
WhiteRabbit : working principles

- SynchE
- PTP
- DDMTD

WhiteRabbit for long distance < 10Km

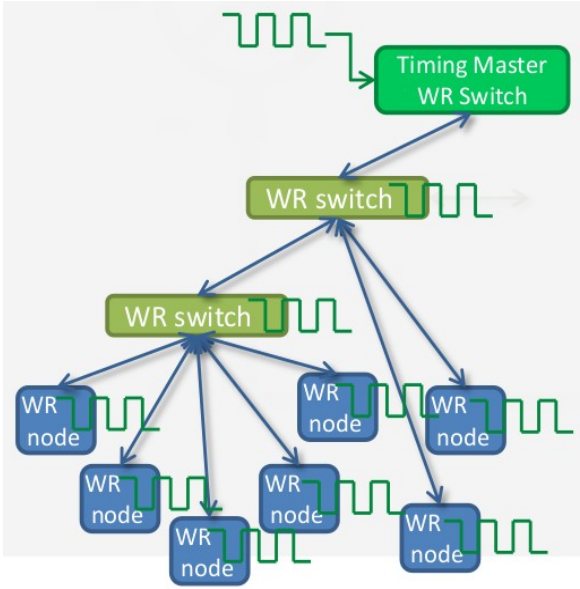
- T+REFIMEVE reaserch facility

White Rabbit principle : Enhanced Ethernet



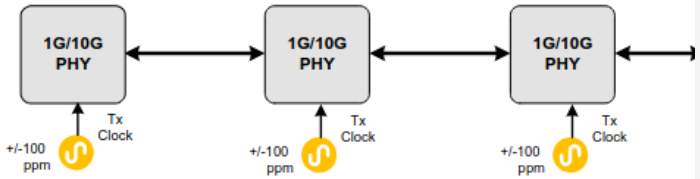
- An extension of Ethernet which provides :
  - Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
  - Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.
- Technology overview
  - Precision Time Protocole (IEEE1588)
  - Synchronous Ethernet
  - DDMTD Phase tracking (Digital Dual Mixer Domain) …

TECHNOLOGY OVERVIEW : Synchronous Ethernet (Sync-E)

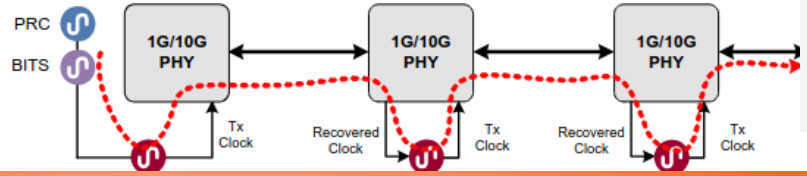


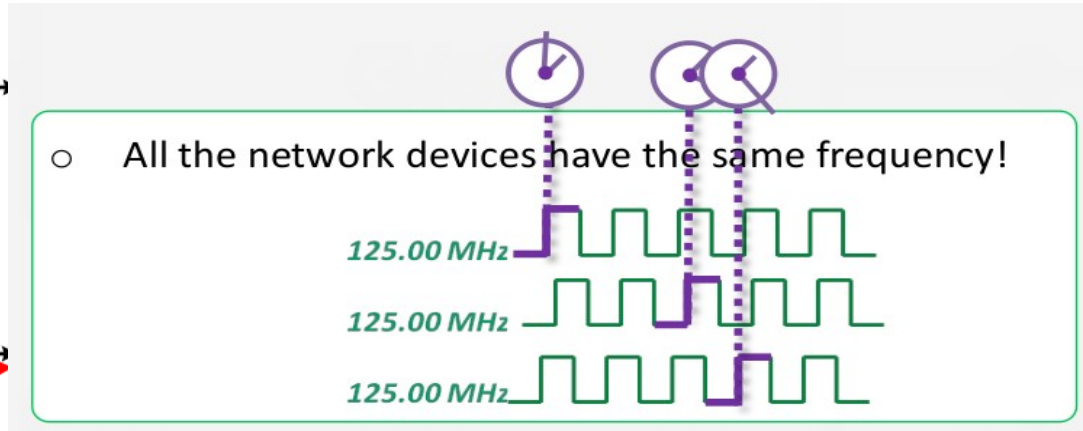
- All network nodes use the same physical layer clock
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip (PHY)
- A master and unique clock for the whole network
- High precision clock definition, 20 times better than standard Ethernet
  - ~ 10ns of StdDev at 10MHz no SynchE
  - ~ 400ps of StdDev at 10MHz with SynchE

Packet Transmission using Asynchronous Timing

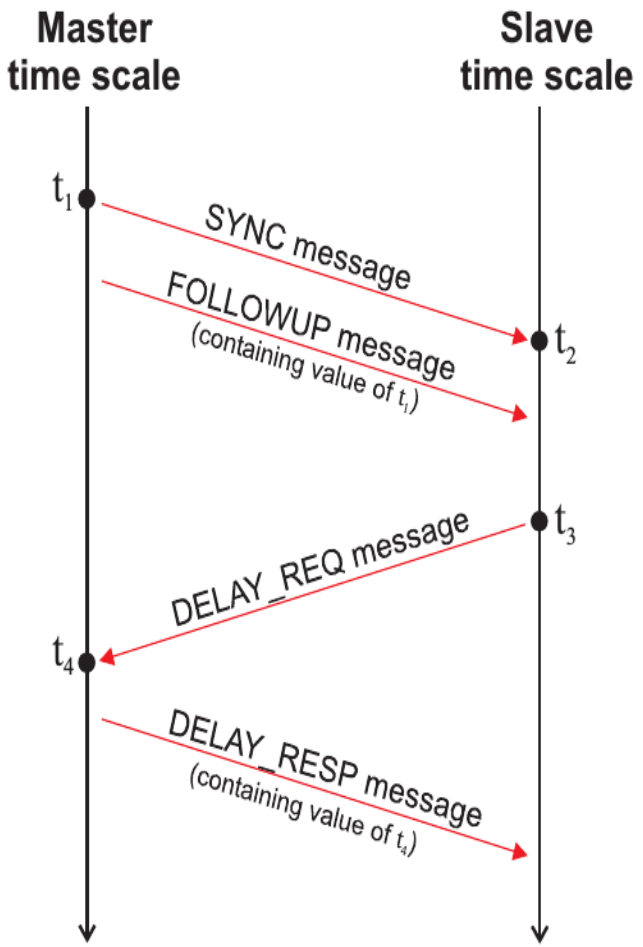


Packet Transmission with SyncE Physical Layer Timing Distribution





TECHNOLOGY OVERVIEW : Precision Time Protocol (PTP)



- Packet-based synchronization protocol
- Synchronizes the local clock with the master clock by measuring and compensating the delay introduced by the link
- Link delay evaluated by measuring and exchanging tx/rx timestamped packets
- PTP is used only for clock offset compensation

Having the values of t1 ... t4 , the slave can:

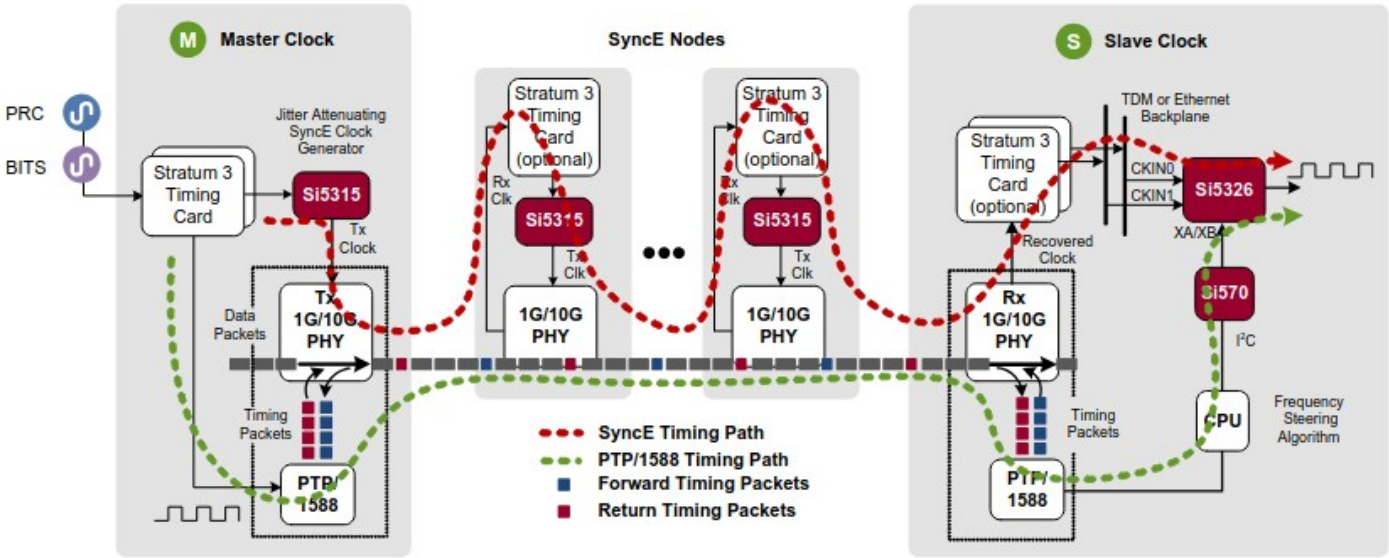
- calculate the one-way link delay:

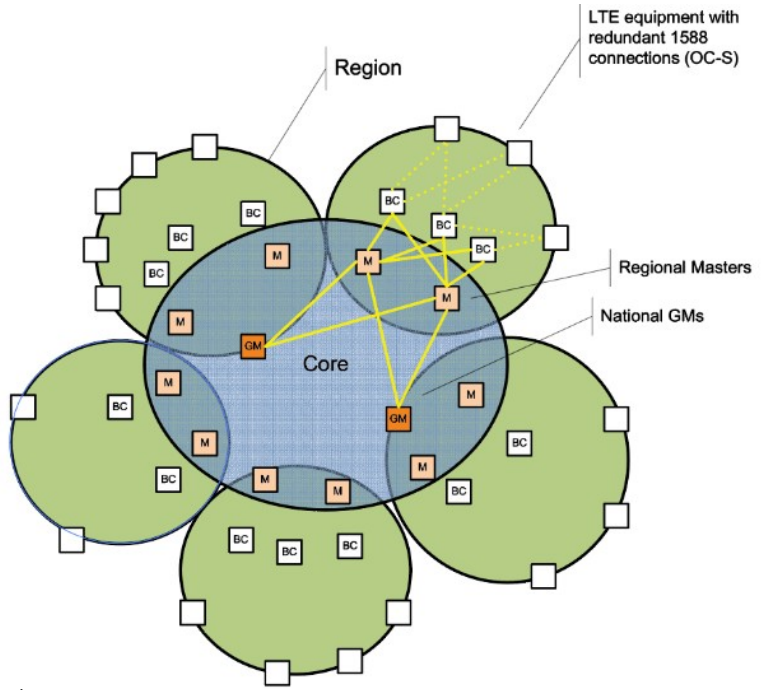
  $$\delta ms = ((t4 - t1) - (t3 - t2)) / 2$$

- syntonize its clock rate with the master by tracking the value of
  t2 - t1

- compute the clock offset:
  $$offset = t2 - t1 + \delta ms$$

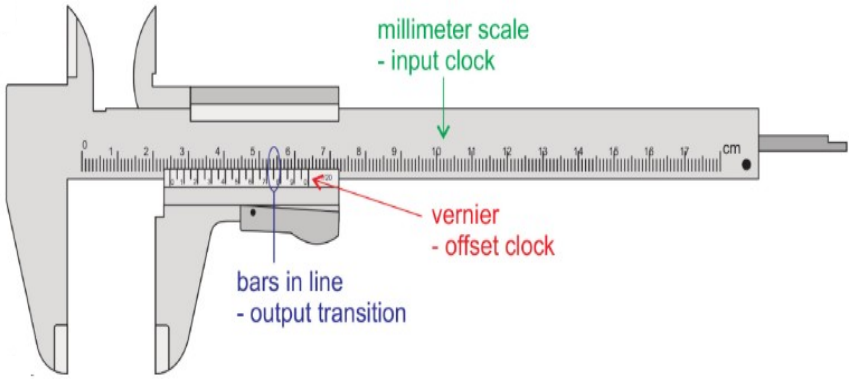
TECHNOLOGY OVERVIEW : PTP + (Sync-E)



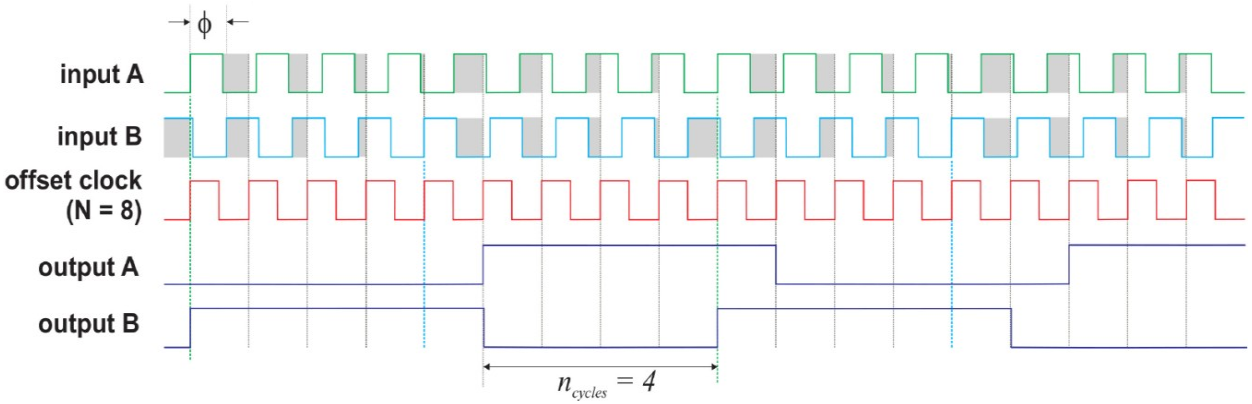


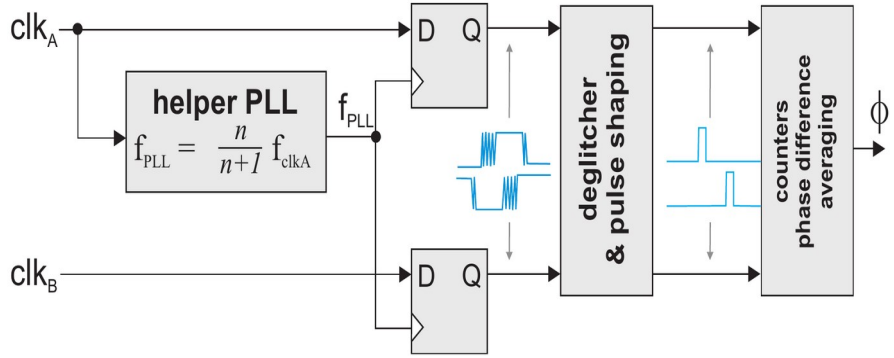
	EEC Option 1 (G.813 Option 1)	EEC Option 2 (G.812 Option IV)
Free-run Accuracy (ppm)	±4.6 ppm	±4.6 ppm
Holdover Stability (ppm/day)	±2 ppm	±0.37 ppm
Filtering Bandwidth	1 - 10 Hz	0.1 Hz
Jitter Generation (ps pk-pk) (@ Ethernet Output Interface)	GbE: 400 ps pp, 2.5 kHz to 10 MHz	
	10GbE: 50 ps pp, 20 kHz to 80 MHz	

TECHNOLOGY OVERVIEW : Digital Dual Mixer Time Domain (DDMTD) phase detector



- Measurement of the phase shift between transmit and receive clock on the master side, taking advantage of Synchronous Ethernet
- Continuous phase monitoring of bounced-back clock
- Phase-locked loop in the slave follows the phase changes measured by the master packet-based synchronization protocol





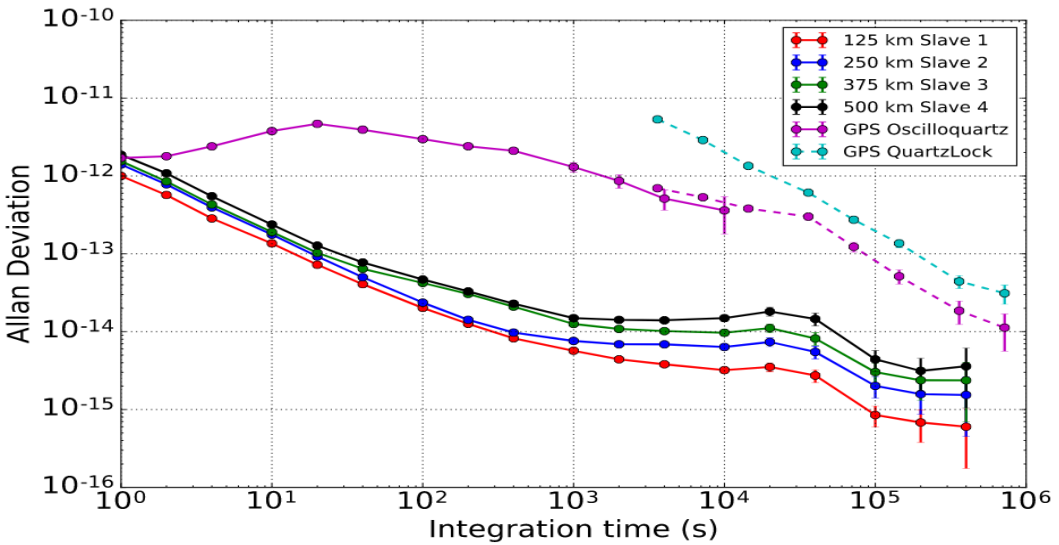
WHITE RABBIT PERFORMANCES POSITIONING

Wide user community

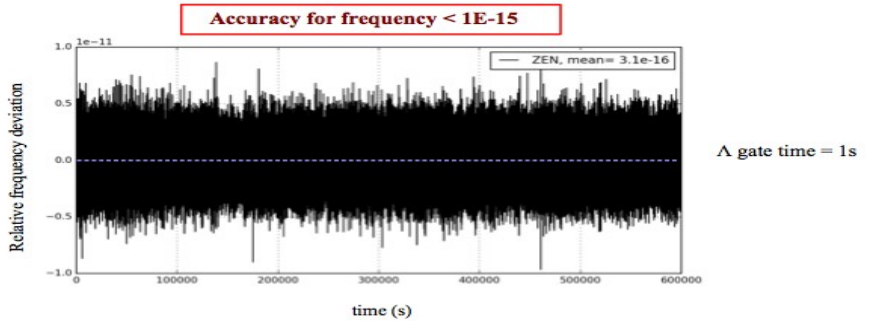
Best performance

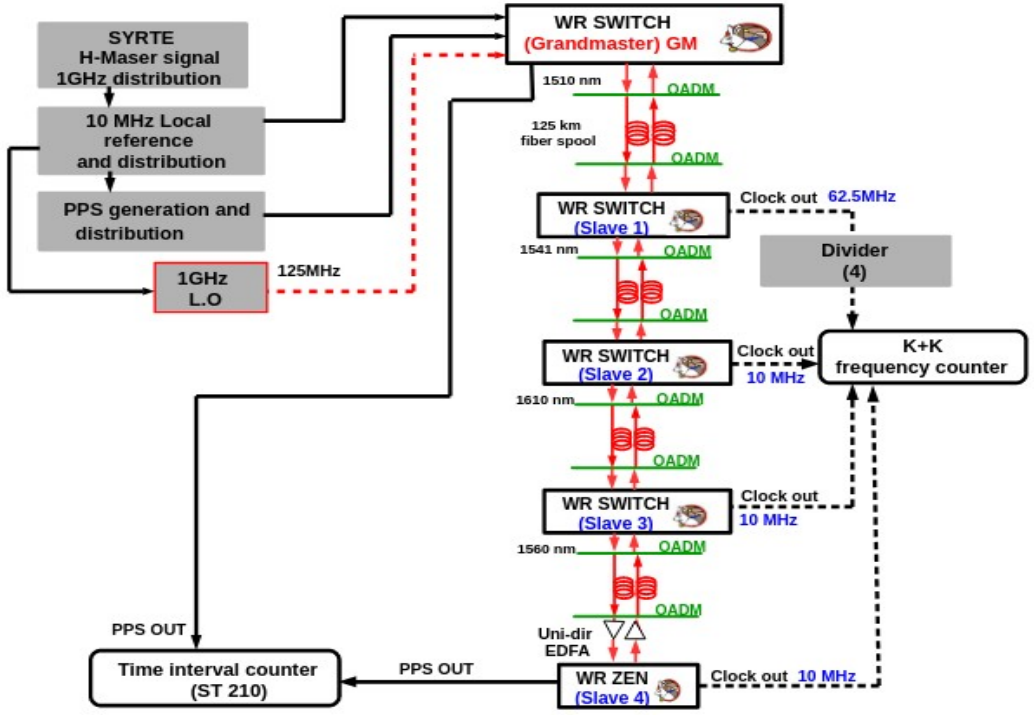
System	accuracy	Note
GPS	10ns -200ns	Propagation in non-stationary disruptive environment. Problem of the multi-way.
GPS-IPPP	2 – 3 ns	Resolution of phase ambiguities using RIMEX data. More complex implementation
On the shelf WR switch without calibration	500ps - 100ns	Tested with WR switch SAFRAN in master configuration
On the shelf WR switch with calibration	200ps – 2 ns	Tested with WR switch SAFRAN in master configuration
IDROGEN enhanced WR node	13 ps	Tested with WR switch SAFRAN in grand master configuration
IDROGEN enhanced WR node	1 ps	2 IDROGEN boards on the WR switch configured in Grand Master and synchronized by T+ REFIMEVE fiber from Paris Observatory (SYRTE)
In development : IDROGEN & external functions	< ps	Aim of T+REFIMEVE

WR performance on long distance test



- 4 span Cascaded
- Better than Oscilloquartz GPS receiver
  - 500Km (4 x 125Km) of fiber
  - Uni-dir fiber
  - 2 OADM (multi wavelength)
- Fiber noise become dominant with the length
  - System disparity, reciprocity of the link

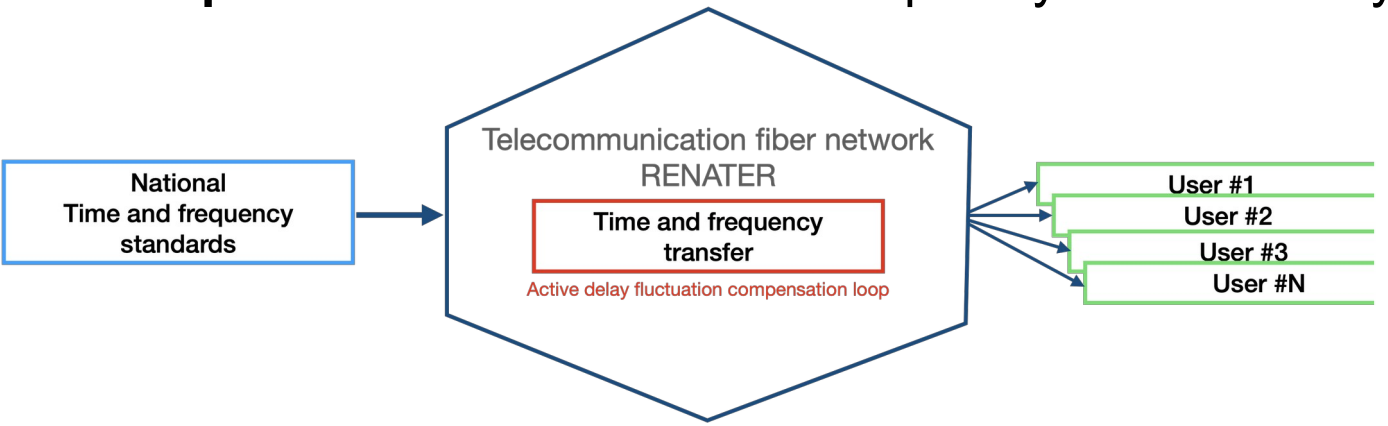




T+REFIMEVE

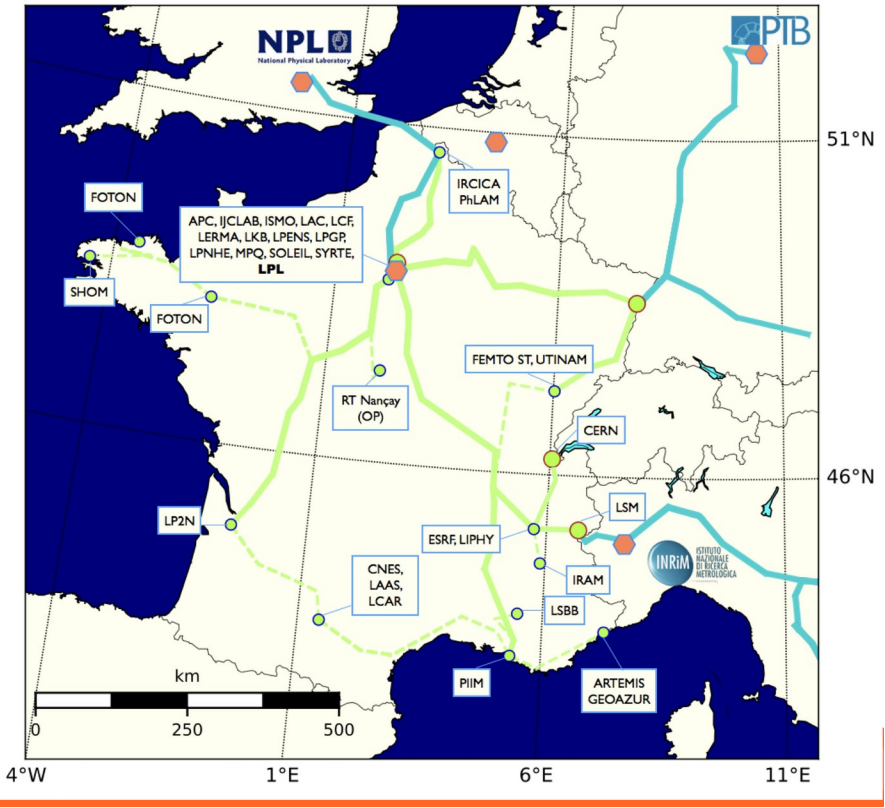
a new research infrastructure to disseminate time and frequency standards on active telecommunication network of RENATER (scientific data network)

Concept : Dissemination of time-frequency references by optical fiber



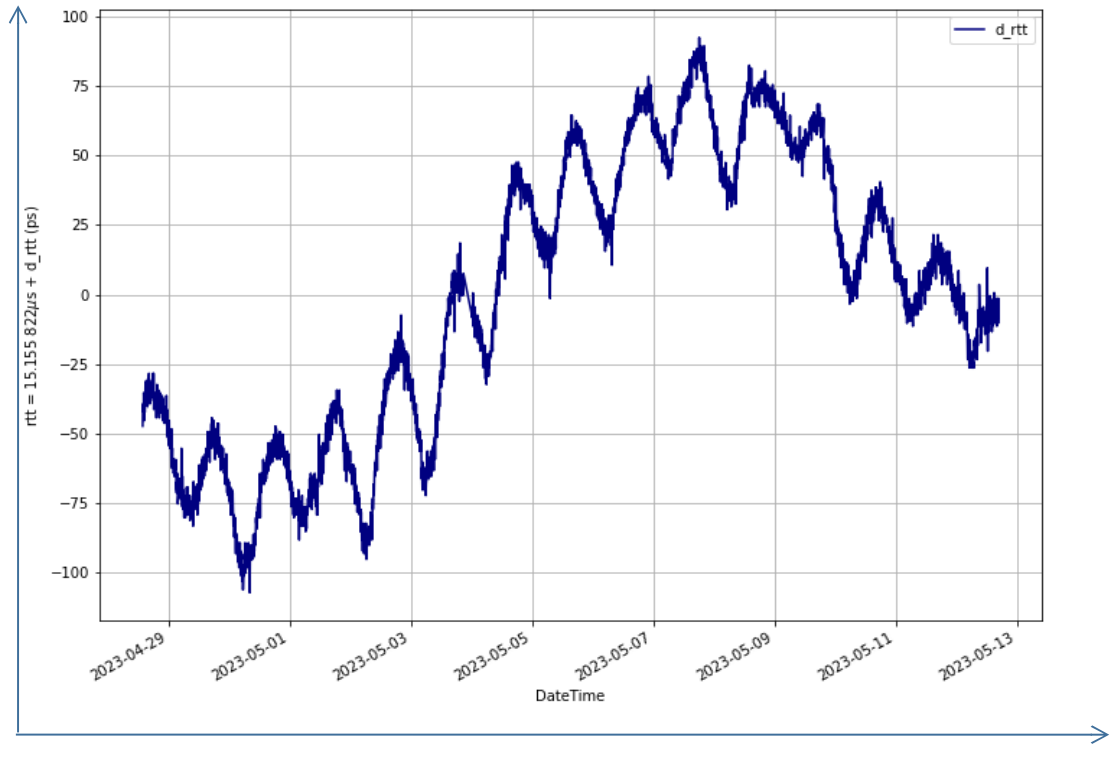
Signal to be provided by T-REFIMEVE

		Stability or relative stab. @1s	Stability or relative stab. @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1st pillar - 10 MHz (White Rabbit)*	1,00E-12	1,00E-15	1,00E-14	1,00E-15
	2nd pillar - 1 GHz	1,00E-13	3,00E-16	1,00E-14	2,00E-16
Time	1st pillar (White Rabbit)*	1 ns	1 ns	10 ns	10 ns
	2nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps§
Optical frequency (194,5 THz/1542 nm)	Today	1,00E-15	3,00E-16	1,00E-14	2,00E-17
	Expected progress in 5 years	1,00E-16	2,00E-17	1,00E-14	1,00E-18



WHITE RABBIT SUPERVISION EXAMPLE

Time propagation delay (ps)



Date

- WR supervision between SYRTE and LAC laboratory
- Monitoring at user equipment level
  - Fiber time propagation delays
  - 14 km of fiber
  - 5 levels of network stratum
  - 10 days of measurement
  - On the shelf equipment (Zen-TP)
  - **Time propagation delay dispersion ~ 200ps**

Current WR projects:

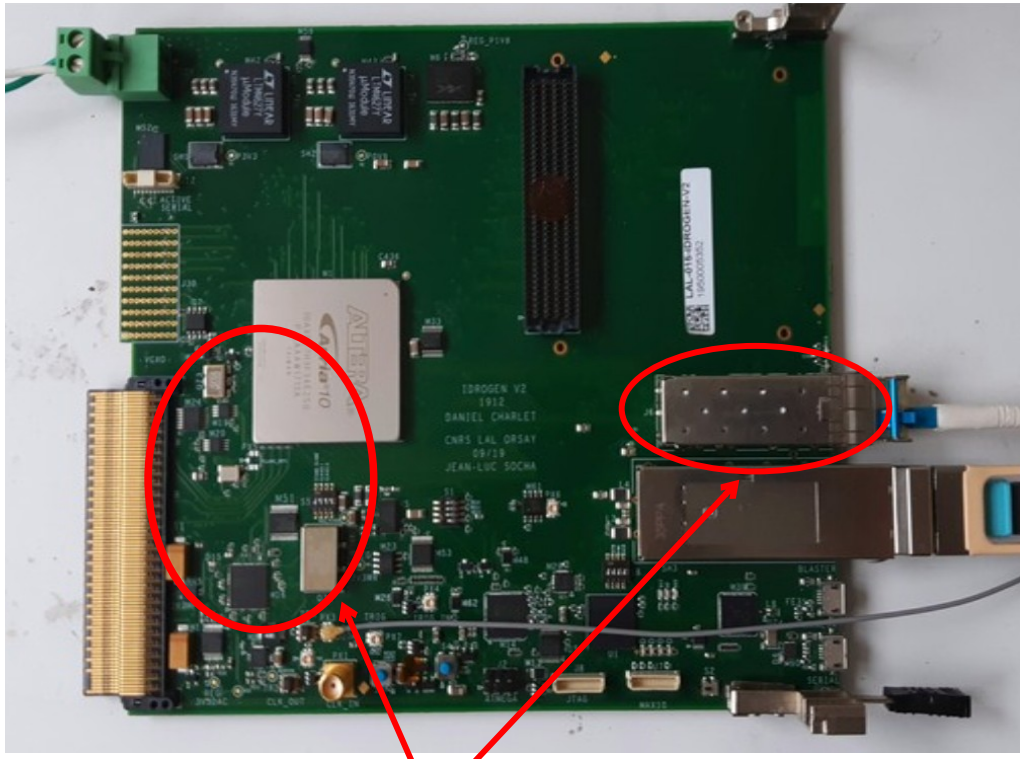
- R&T TIMED
- IDROGEN
  - Board
  - Performances
  - FMC-ADC
  - FMC-MasterOscillator
- ATF collaboration

WR RESEARCH & TECHNOLOGY IN2P3 : TIMED

- 5 Laboratories , 2 institutes (IN2P3 & INSU)
- Schedule : 4 years
- Budget : 80K€
- Goals : WR capability extensions :
  - xTCA crate implementation
  - WR implementation simplification
  - WR FPGA external functions integration
  - WR enhancements (High stability frequencies)
- Contributions :
  - LPC Caen : Performance evaluation of a commercial crate controller including a WR switch
  - LPSC : Custom development of a crate controller including a WR switch
  - LP2IB : WR external VCXO (controlled oscillator) integration
  - IJCLab : WR simplification & enhancements,
  - IJClab accelerator department & KEK accelerator: Master oscillator distribution
  - Observatoire de Paris : WR enhancements

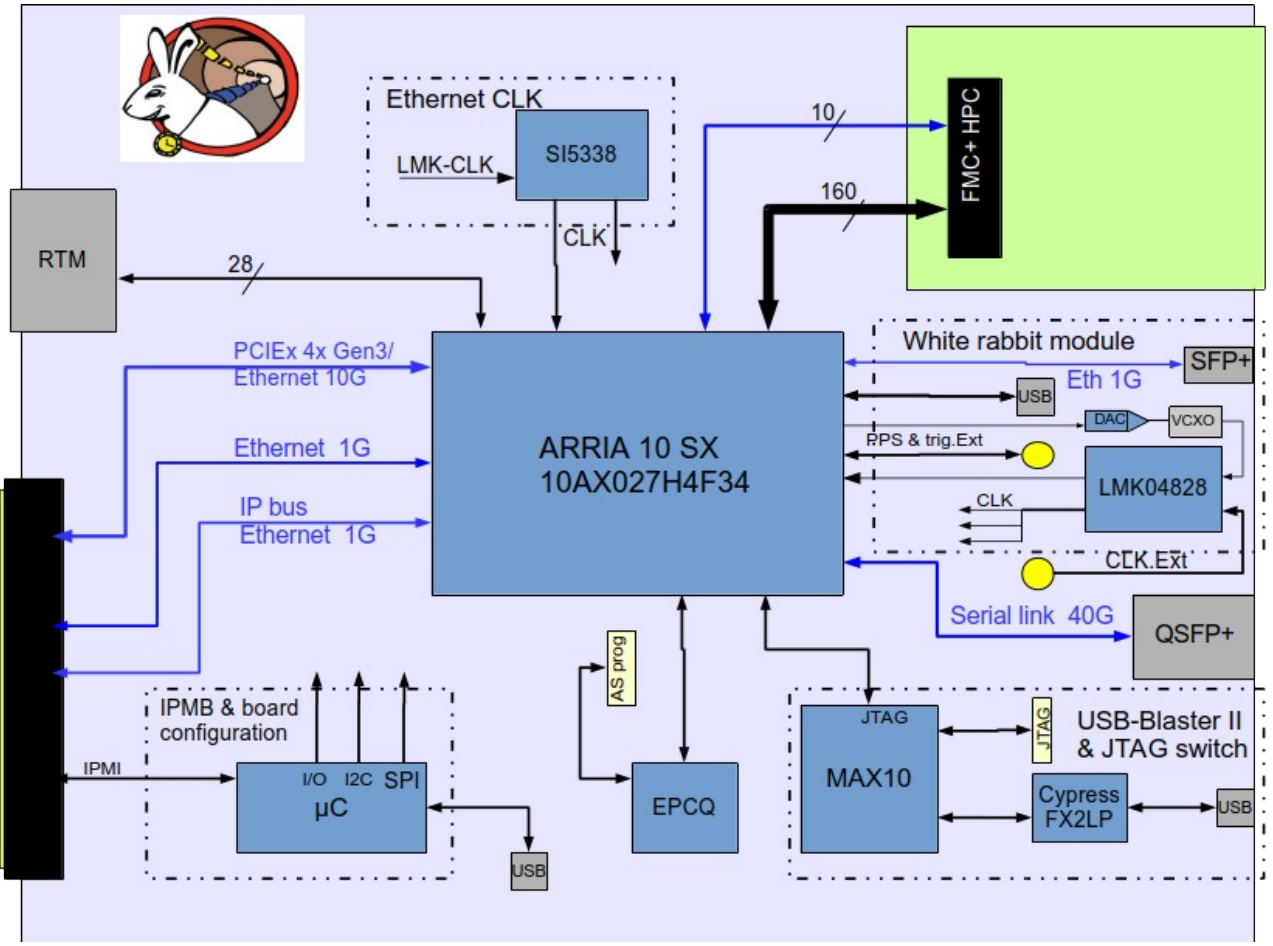
IDROGEN board

IDROGEN board : high speed data acquisition & Low phase noise WR node



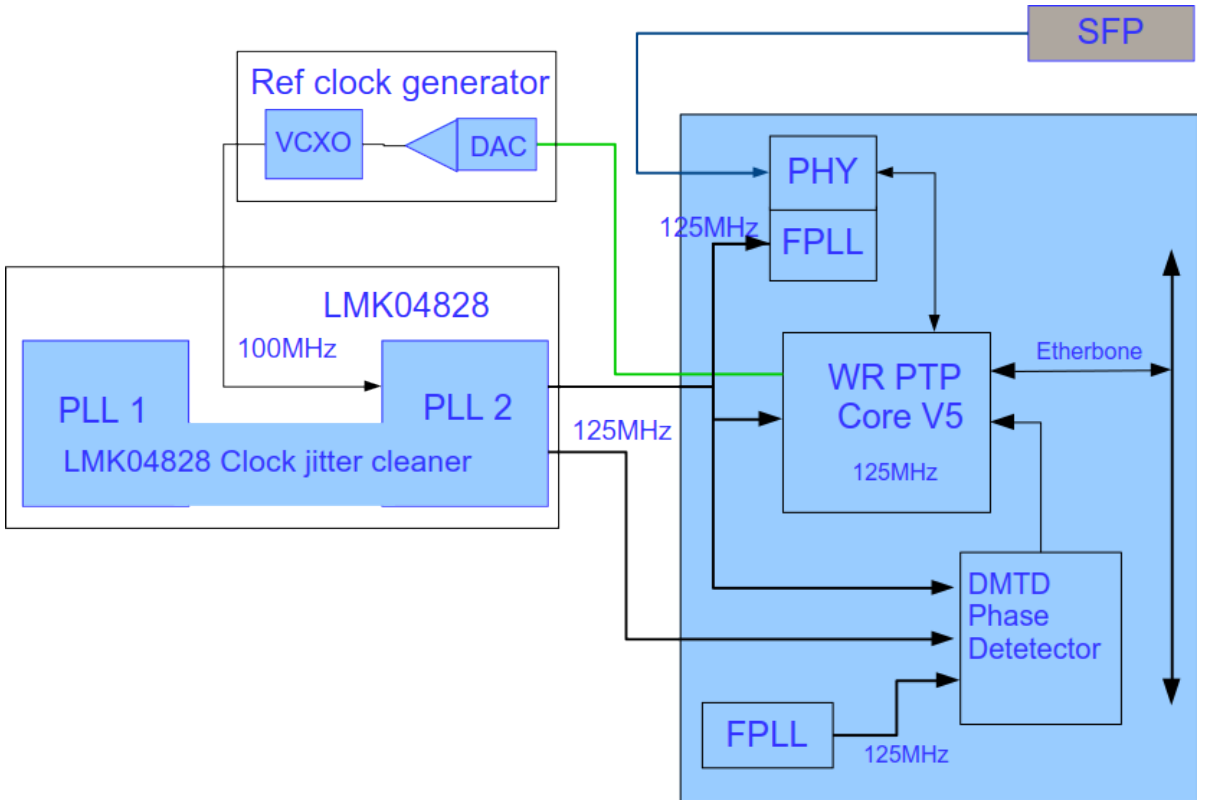
- Design & development done by IJCLab
- CERN schematic improved
  - Components upgrade : PLL, VCXO, FPGA
  - PCB design compliant with EMC rules
- High performance WR low jitter node :
  - Accuracy < 20ps, Jitter < 1ps
- High performance data acquisition system:
  - PCI express > 30Gbs, Ethernet > 20Gb
- Crate (µTCA) or stand alone use
- FMC+ carrier board for additional functions :
  - ADC, DAC, Clock synthesis, ...
- Firmware development done by Nancay Observatory and IJCLab
- Clock expertise and qualification by SYRTE (Observatoire de Paris)

IDROGEN board



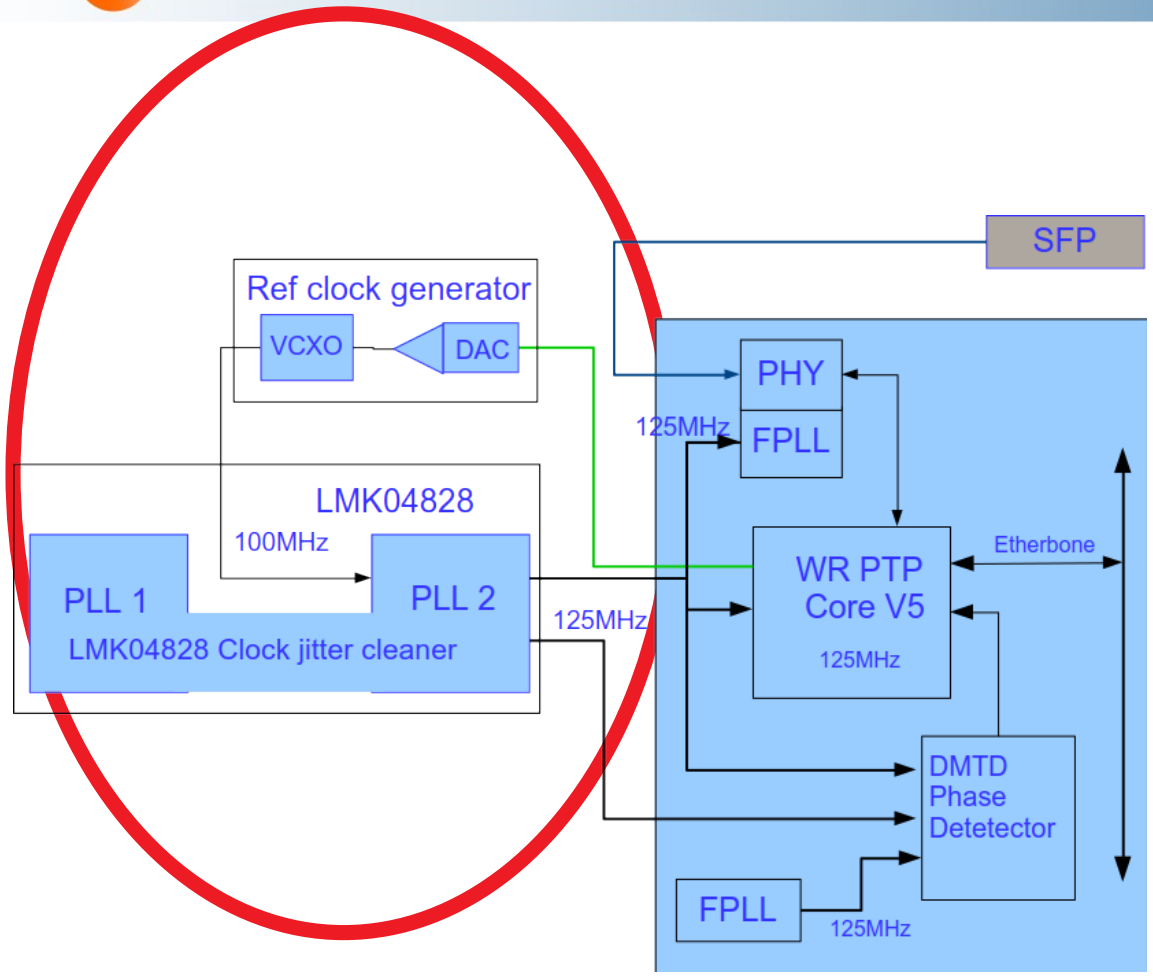
- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC+ slot)
- 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant
- Configurable output clock
- Front panel connectivity :
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity :
  - 1Gbe Ipbus, PCI 4x Gen3
  - IPMB, CLK & trigger lane
  - RTM connector : J30

IDROGEN board : WhiteRabbit implementation



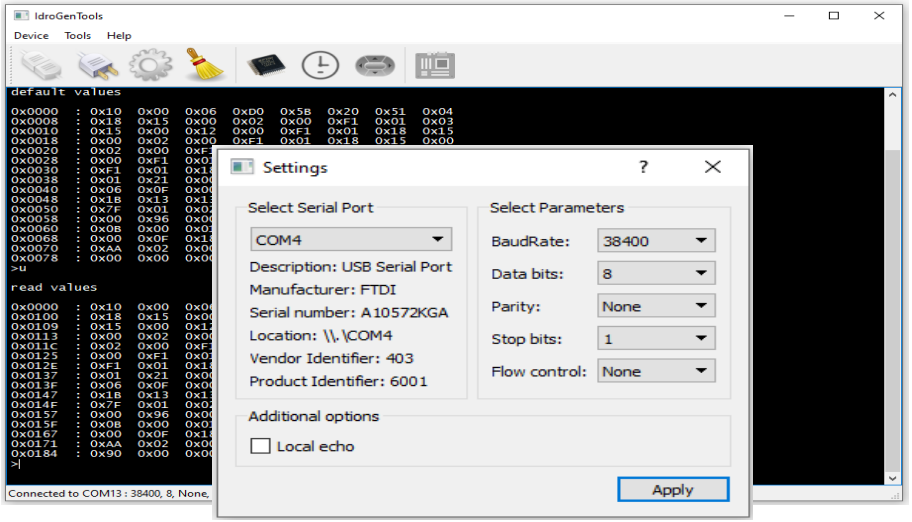
- Based on CERN open hardware with Enhancements
- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
  - Tx/Rx routing equalisation

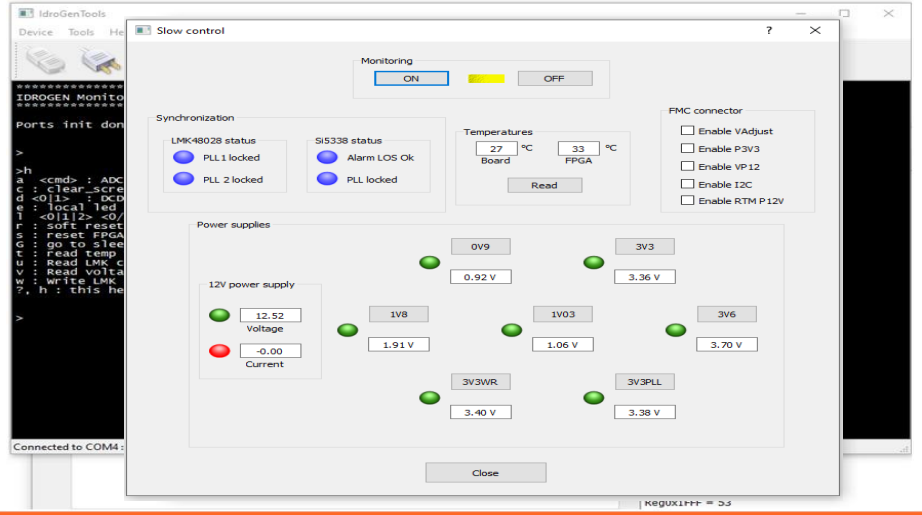
R & T TIMED : WR external function integration



- External PLL integration
  - Internal reconfiguration
- VCXO integration
  - Derived from video IP
- FPGA manufacturer & model dependent

IDROGEN : Slow control





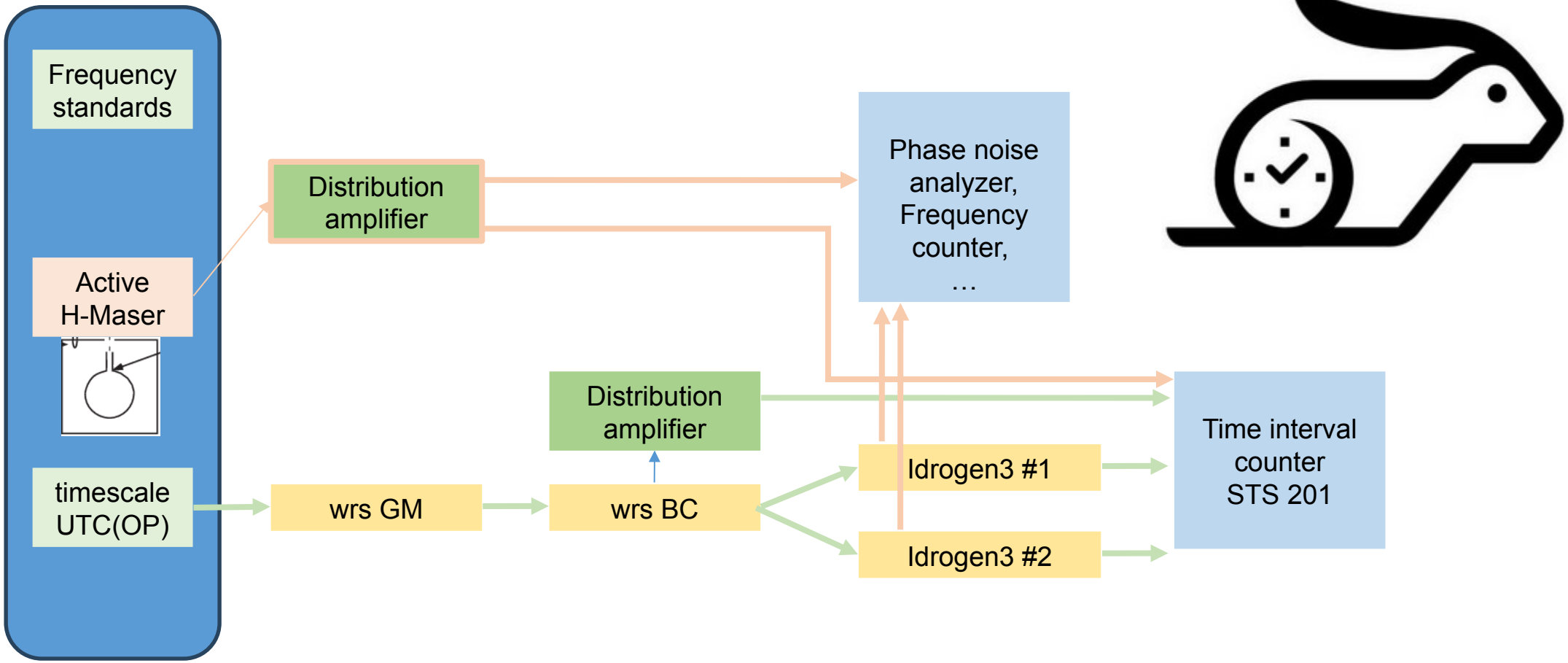
- IDROGEN MMC
  - Software for µC ATMEGA128
  - Base on MMC-DAQGEN package develop by LPSC laboratory
- IDROGEN Tools
  - USB interface
  - For configration and board debug
  - Develop in C++ with QT5 (LINUX and Windows)
- IDROGEN Config
  - For remote configuration & Status
  - Ipbus link
  - Develop in C++ with QT5 (LINUX and Windows)
- Board configuration and status :
  - Power, Pll configuration : LM04828 & SI5338,
  - µC : ATMEGA configuration,RTM & FMC configuration
- EPIX driver will be develop soon

IDROGEN : Firmwares

- WhiteRabbit core V4 & V5
  - Development of CERN & GSI
  - Adaptation for ARRIA 10
- PCIExpress v1
  - Based on INTEL-FPGA
- PCIexpress with enhance DMA
  - The DMA allows burst transfer near the maximum data transfer
  - Based on CERN LHCb development
  - Gen 3 4x End-point mode, 128-bit layer interface payload 256 bytes
  - High and continuous data rate acquisition
  - Software Driver C, DPDQ driver in development
  - Read or Write ~ 30Gb/s (Gen3 4x)
- GBT to PCIe
  - Based on CPPM LHCb for PCIE40 development
- IpBus 1G & 10G
  - Development by LPSC laboratory
  - Adaptation by IJCLAB for ARRIA 10
- Streamer 1G & 10G
  - Software C ,Multi Jumbo frame by event
  - 2 x 10Ge available, 40Gb future development
- JESD 204B for high speed ADC (1G/500M/250M)
  - Base on INTEL-FPGA IP
- Parallel 64 data acquisition
  - For 2 ADC 125MBPS 16bits
- IpBus on WR link (future development)
  - One optical link : timing, synchronisation, configuration, data readout

IDROGEN board WR performances

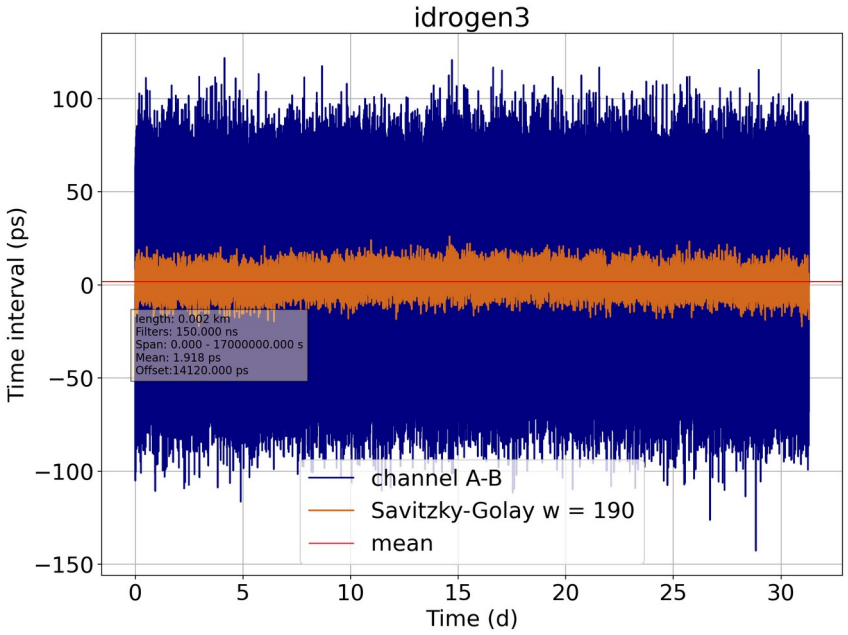
Syrte test setup

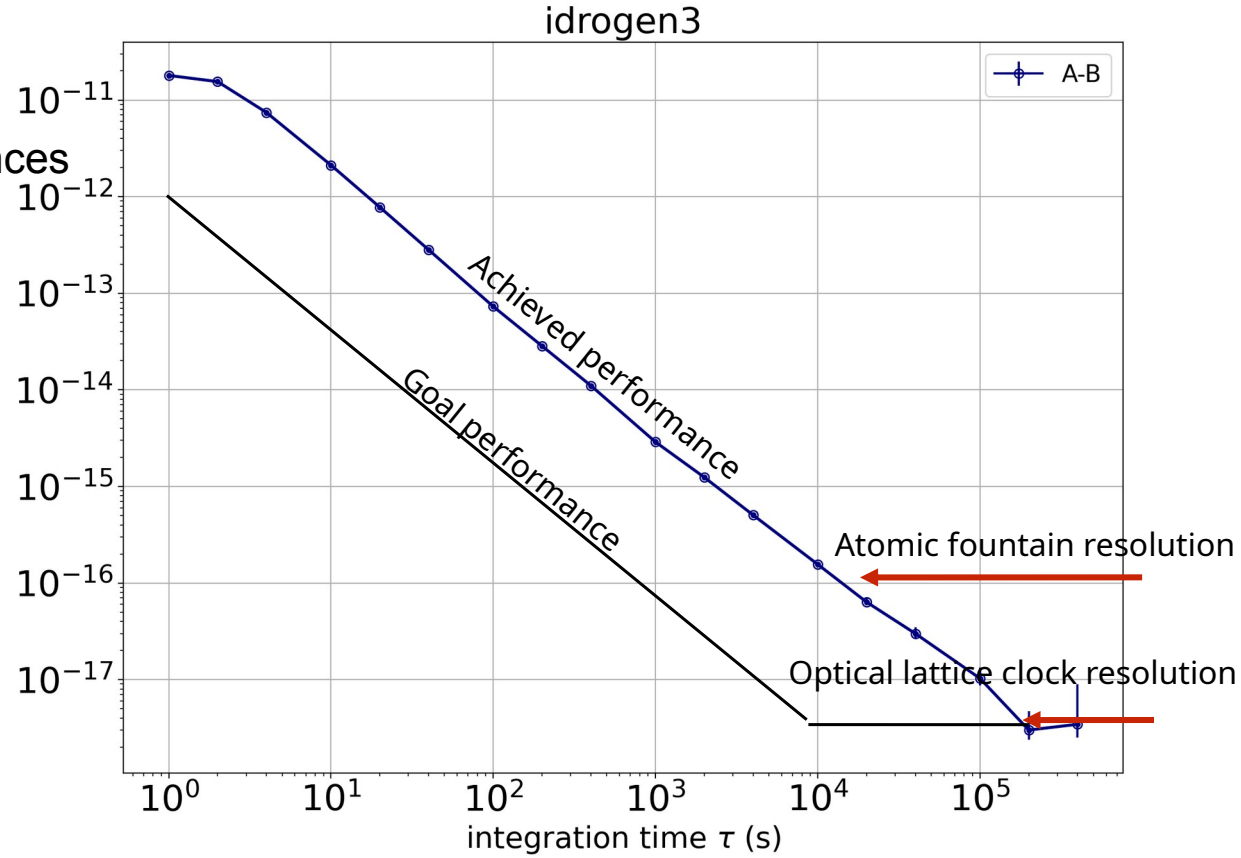


2 Idrogen boards, in the same chassis, connected by 2-m fiber to the same wrs. H-maser is in common view.

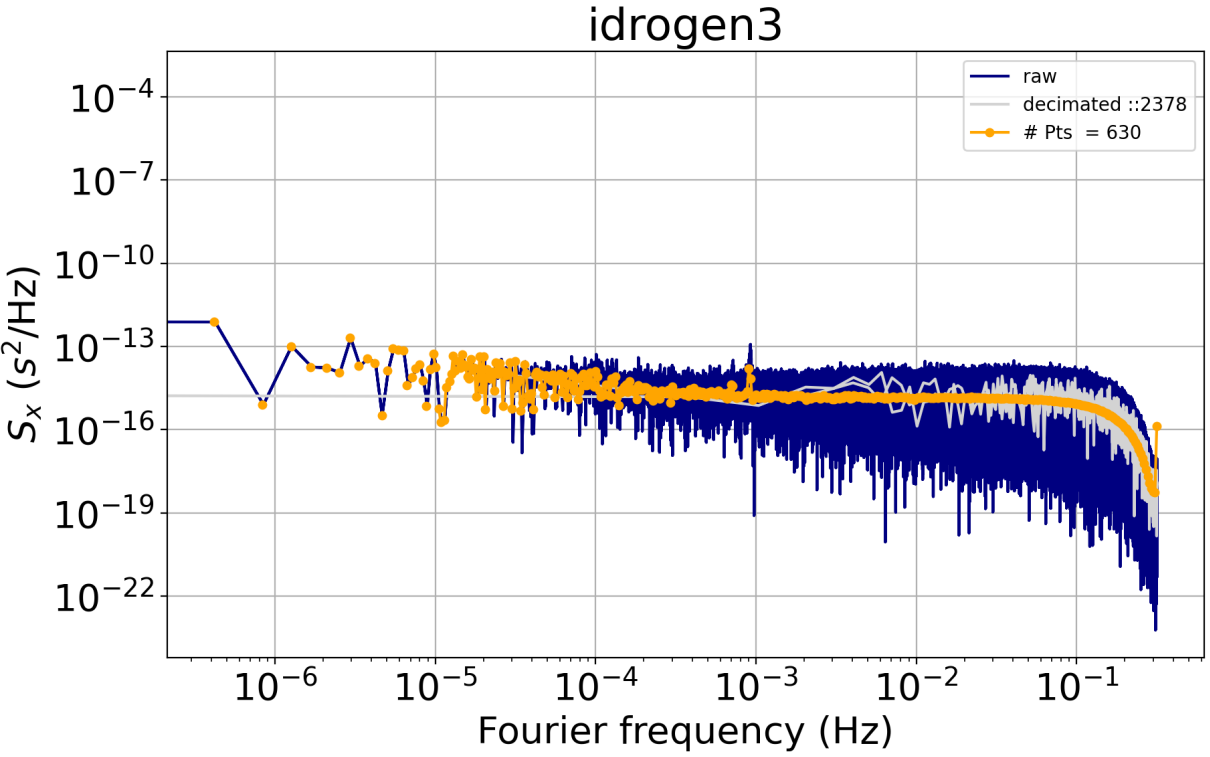
IDROGEN board performances

- PPS time difference between two independent IDROGEN3 boards
- Excellent long term stability : ~ 3E-18
- On-going work: improve short term performances

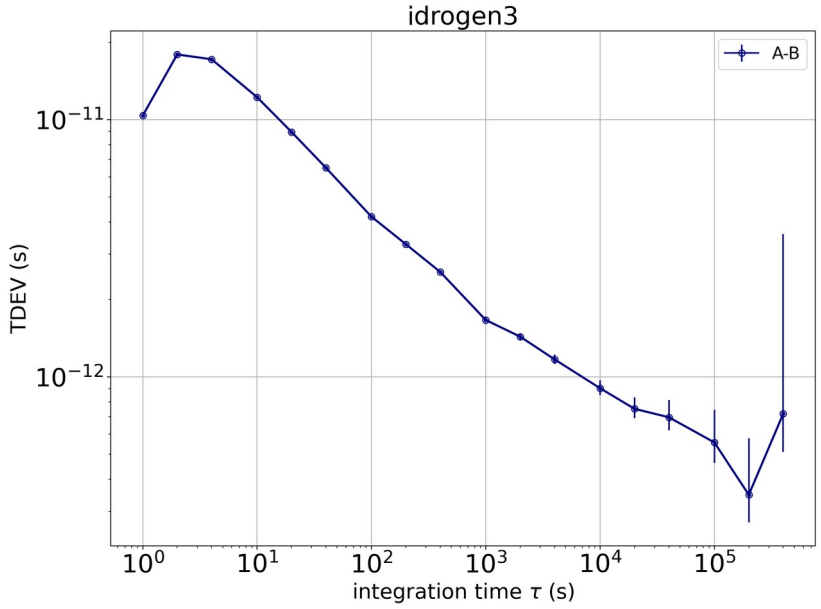




IDROGEN board performances

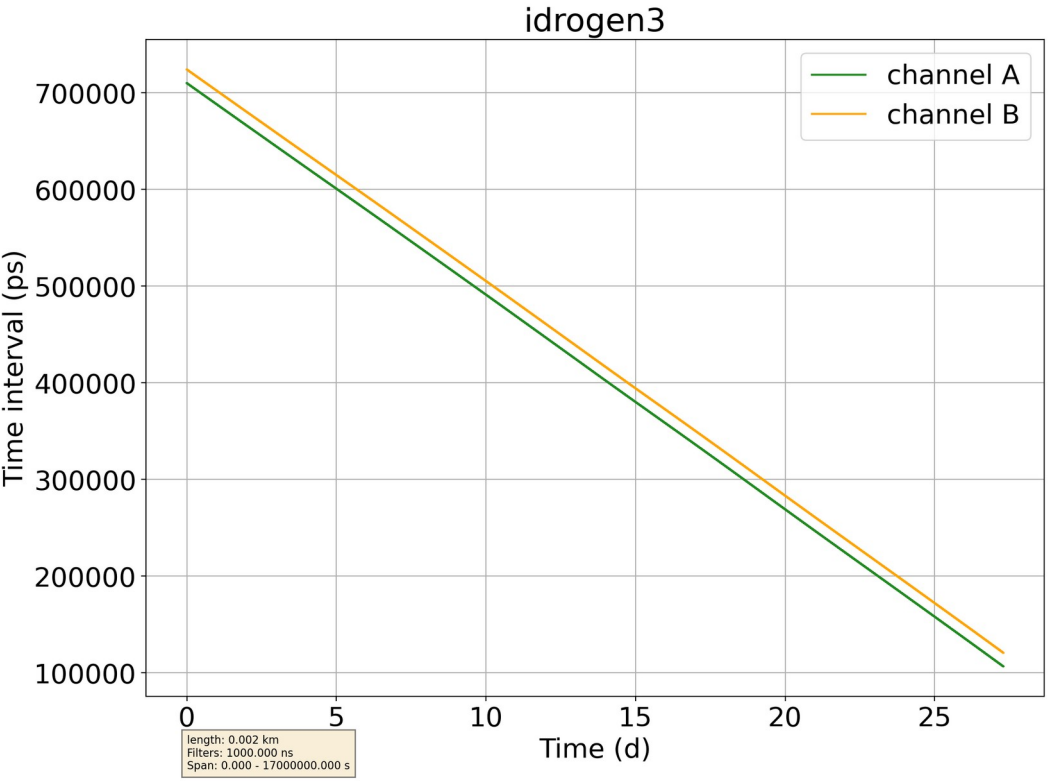


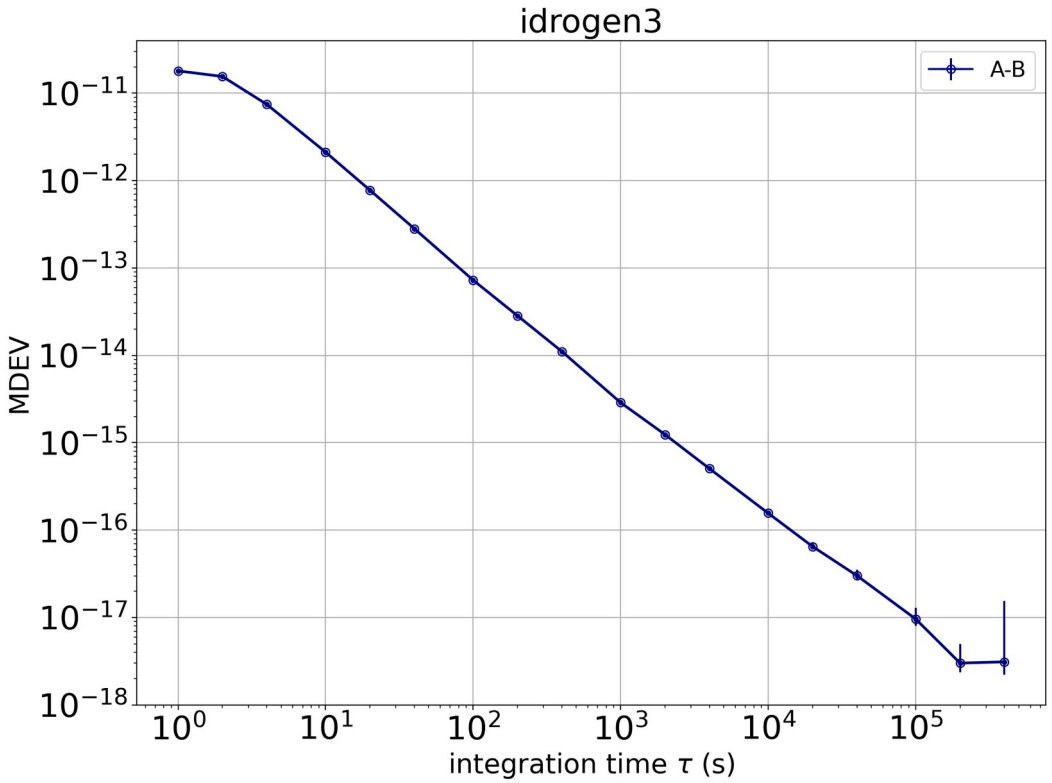
- the measurements were made by SYRTE (P.-E.Pottie)
- Measure the time interval between idrogen#1 and idrigen#2 PPS :
  - Rms jitter ~20 ps
  - TDEV: 10 ps @1s; <400 fs @ 2e5 s.
  - Flat FFT (ti) down to < 1e-6 Hz



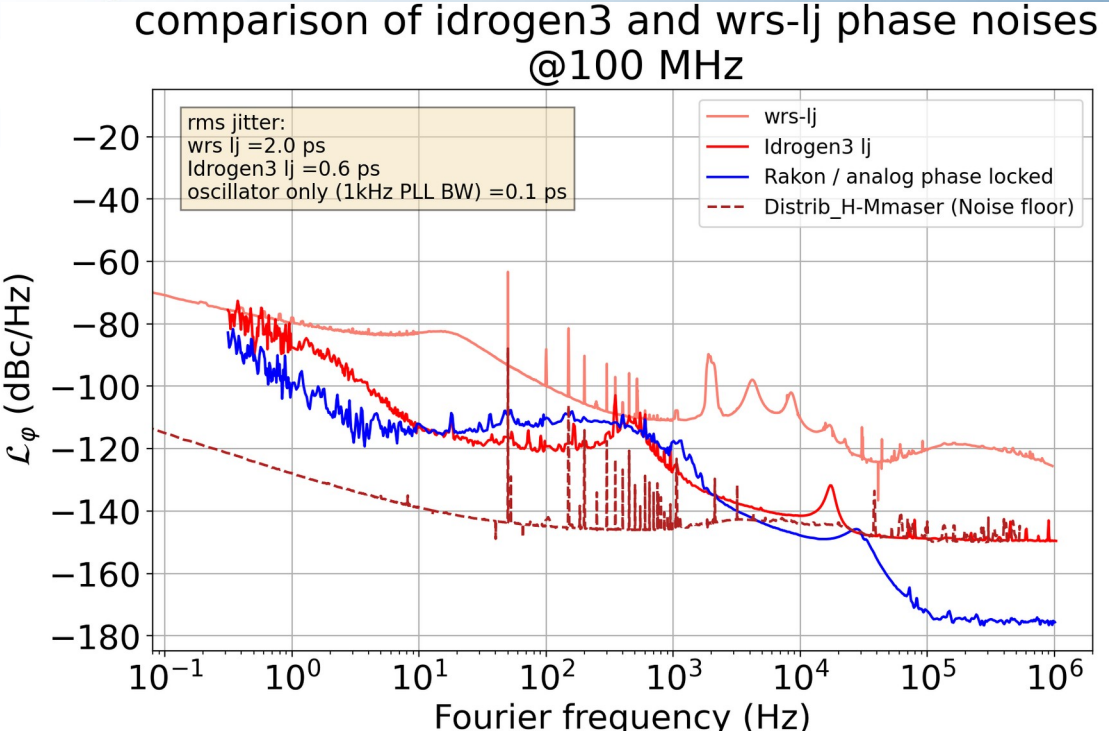
IDROGEN board performances

- the measurements were made by SYRTE (P.-E.Pottie)



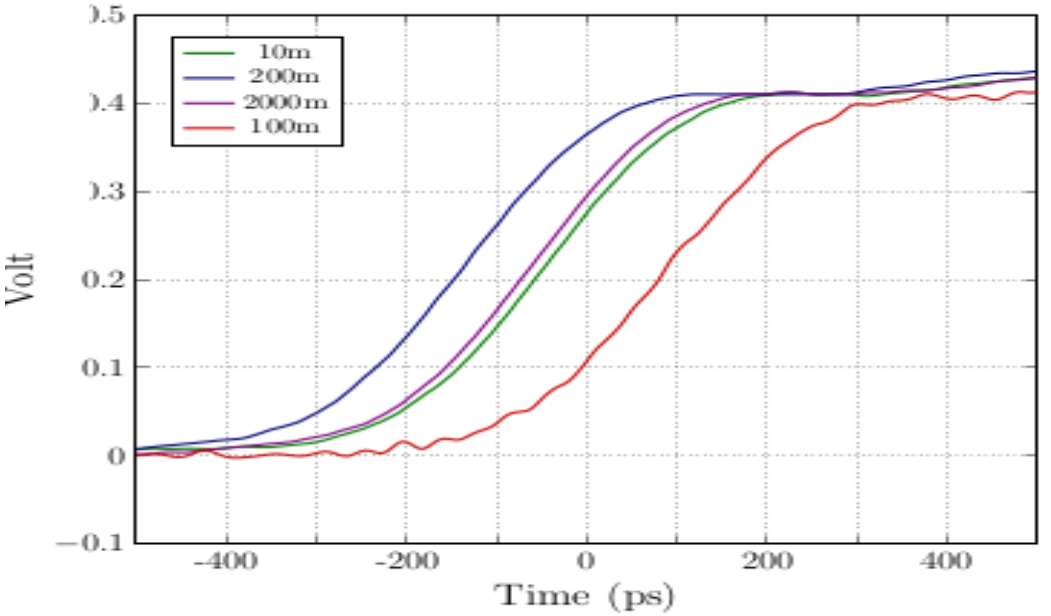


IDROGEN board performances

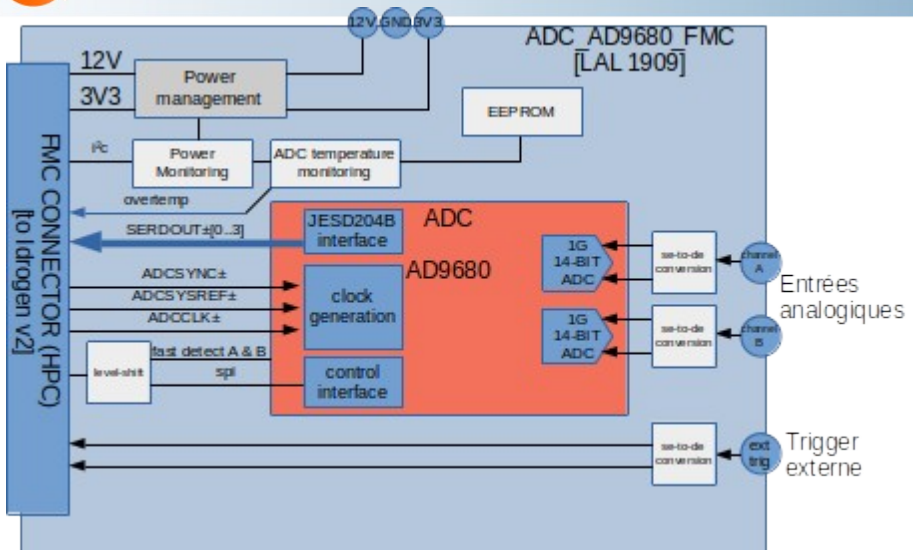


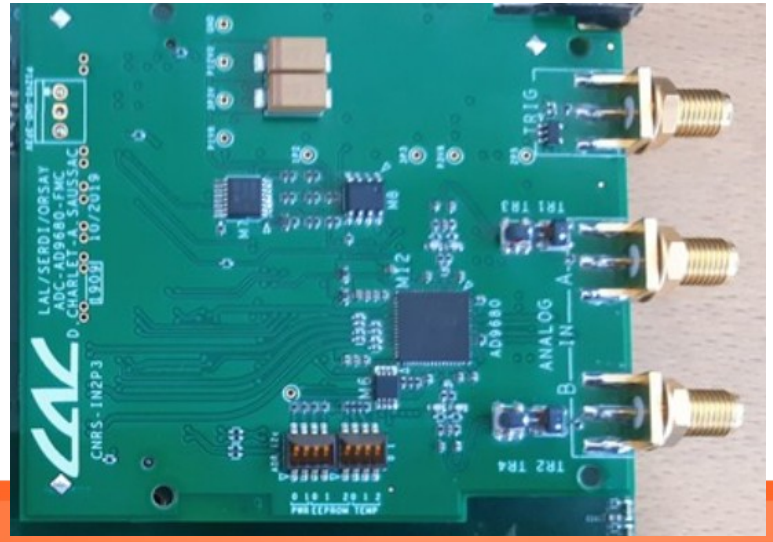
- PPS measurements for different fiber lengths
  - From 10 m to 2 km
- Time accuracy below 100 ps

- the measurements were made by SYRTE (P.-E.Pottie)
- transfer from one WR switch to two IDROGEN boards



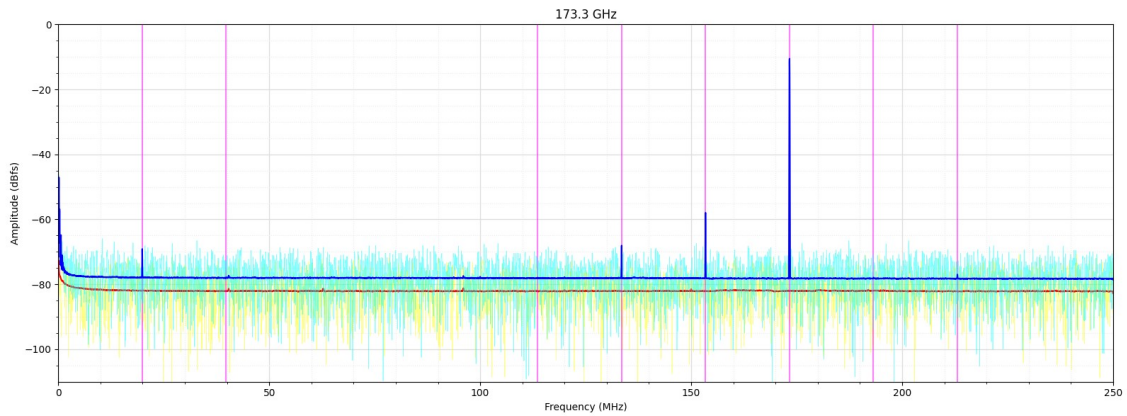
FMC_AD9680_500MSPS

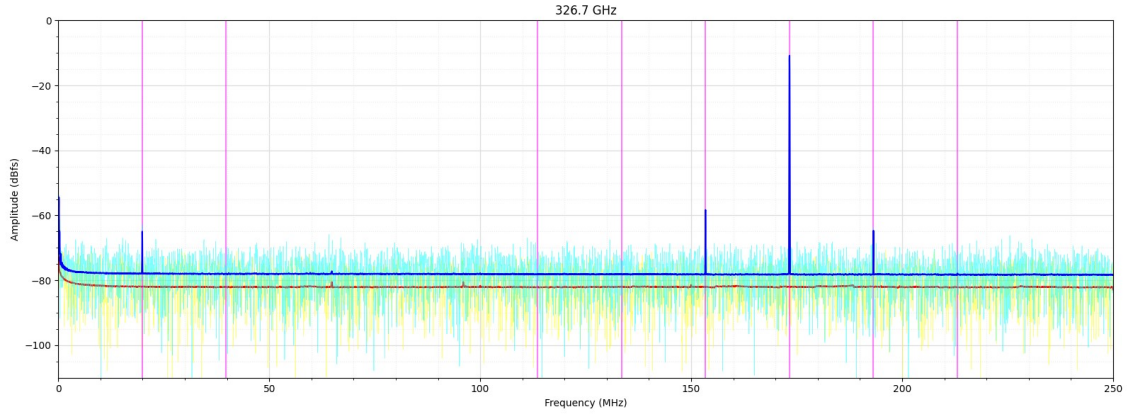


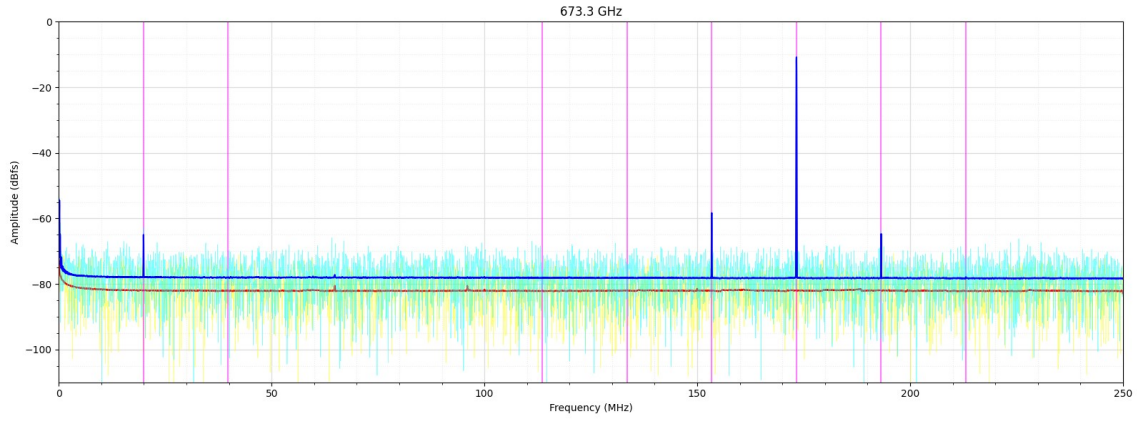


- The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :
  - includes : its own PLL.
  - ADC clock source : External clock
- Mezzanine main features :
  - VITA57.1 (FMC), ADC 9680, 2 channels, 14 bits
  - 500 MSPS, JESD204B, 2GHz analog bandwidth
  - External trigger in
- Bandwidth 500 MHz to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x 10G Ethernet
- Configuration by IPBus 10G

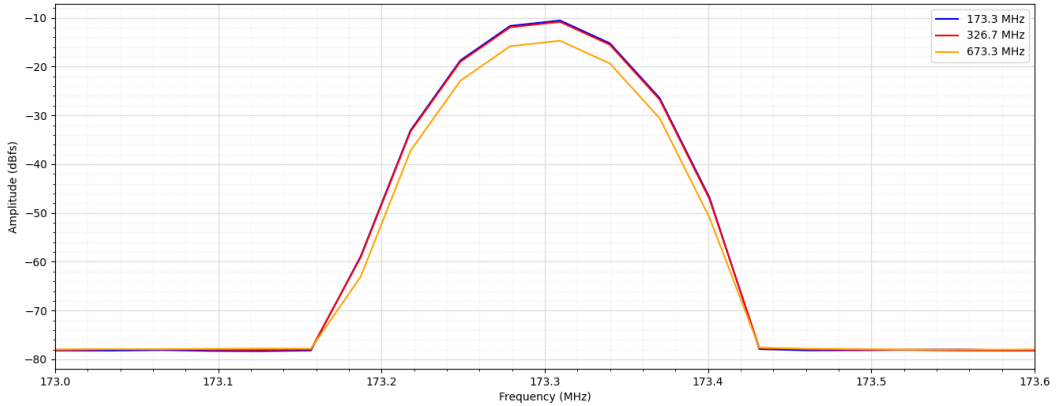
FMC_AD9680 results







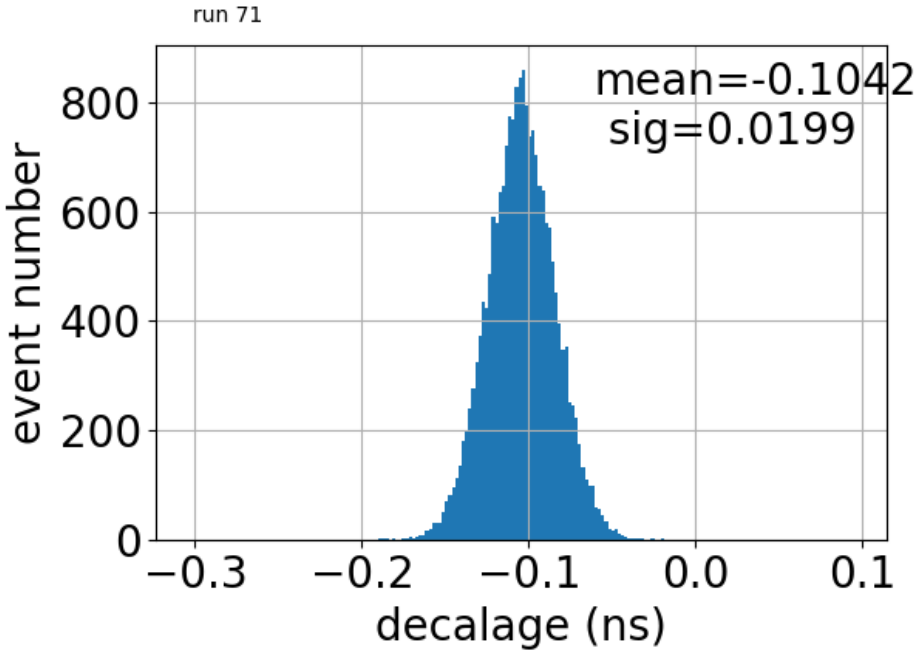
- Blue channel with signal
- FFT 16K, Average over 10000
- First : second , third Nyquist band



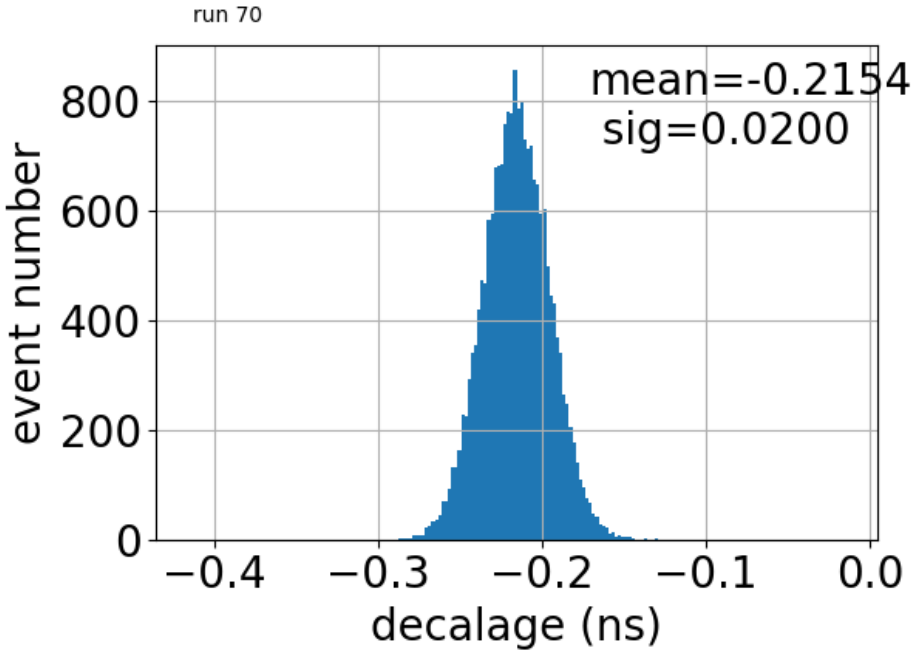
- Level of central frequency
- -0,4db on second Nyquist band
- -4db on Third Nyquist band
- Level calibration to be performed

FMC ADC preliminary results

- Phase difference effect
- Coax 1 length = Coax length 2
- 100ps

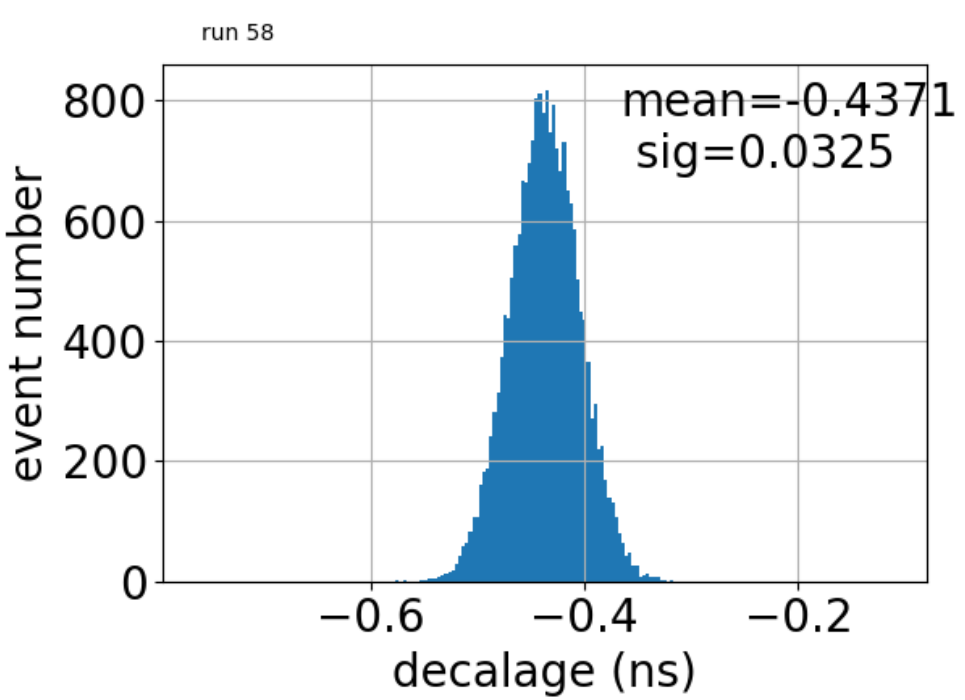


- Phase difference effect
- Coax 1 length = Coax length 2 + 20mm
- Δ ~ 110 ps → 20mm

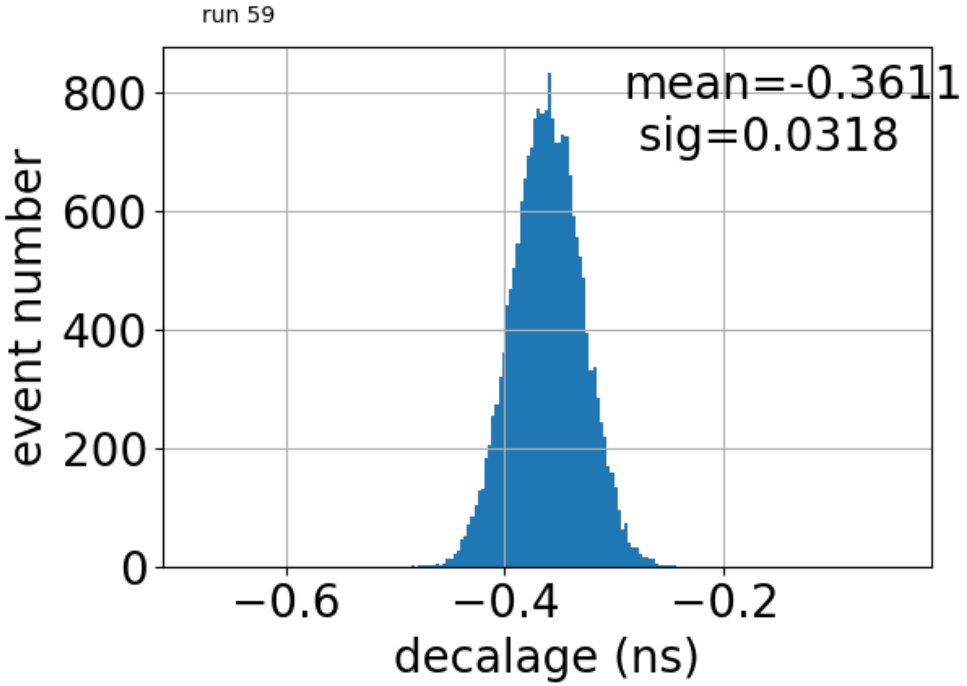


FMC ADC preliminary results

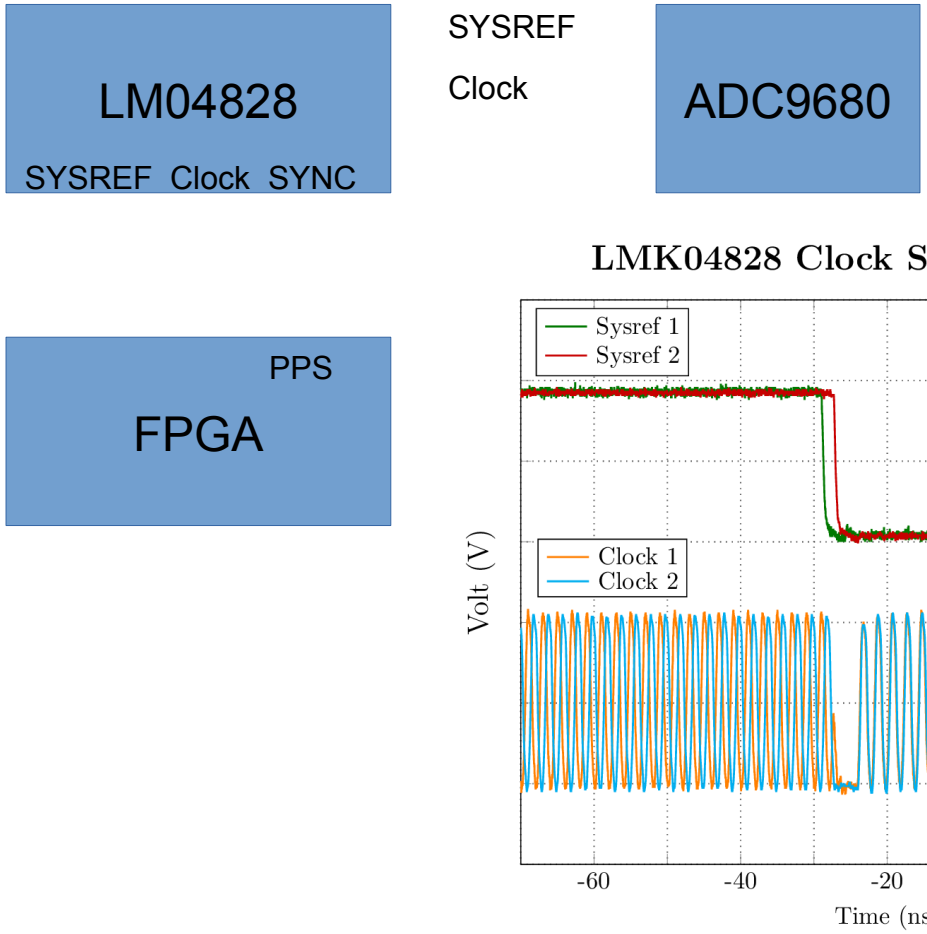
- Fiber length effect
- Fibers 1 = 2 (25m)
- 400ps ~ 8cm



- Fiber length effect
- Fibers 1 (25m); Fiber 2 (50m)
- Δ ~ 80ps

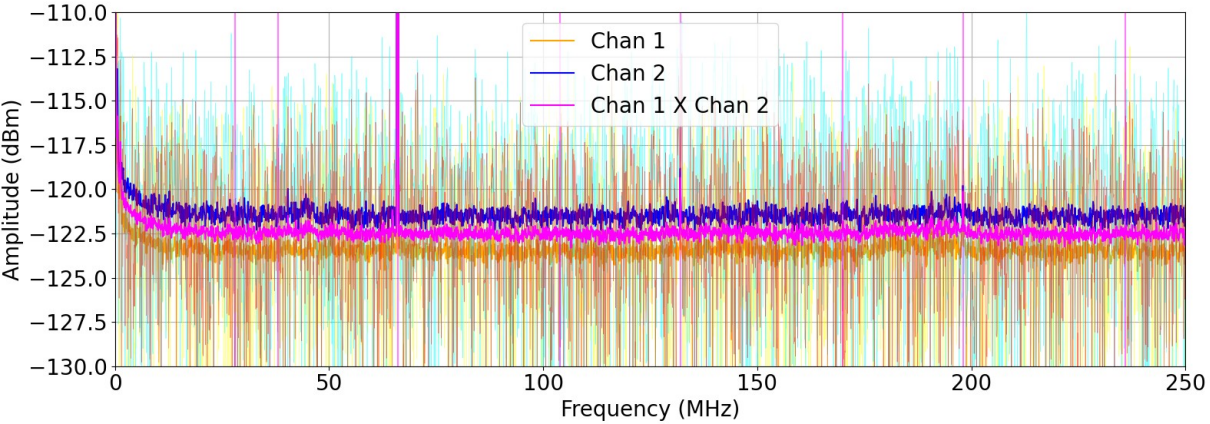


FMC ADC_9680 : Synchronisation

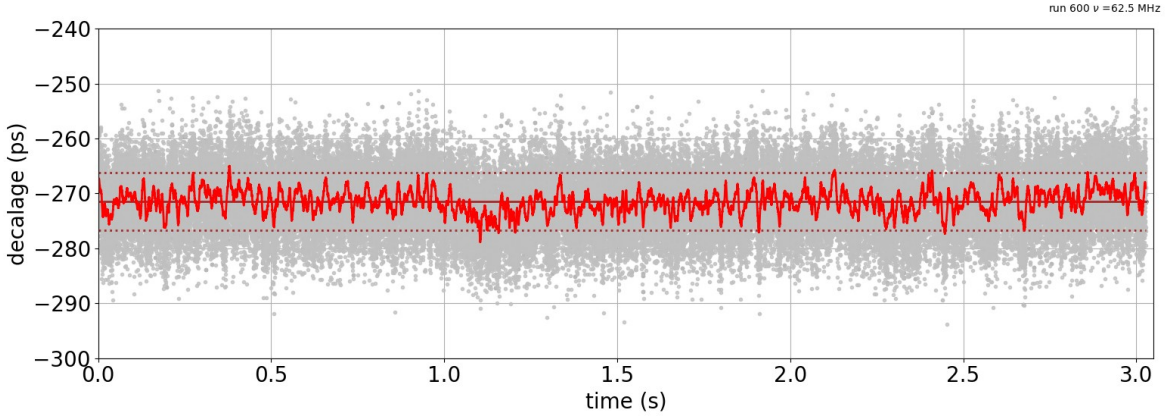


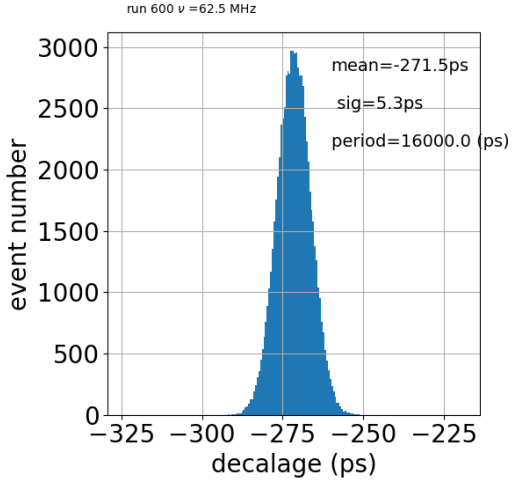
- 2 IDROGEN boards synchronize by WR
- PLL : LMK04828
- ADC data transfert : JESD204B class 1
- 500MHz Clock
- Phase alignment by PPS

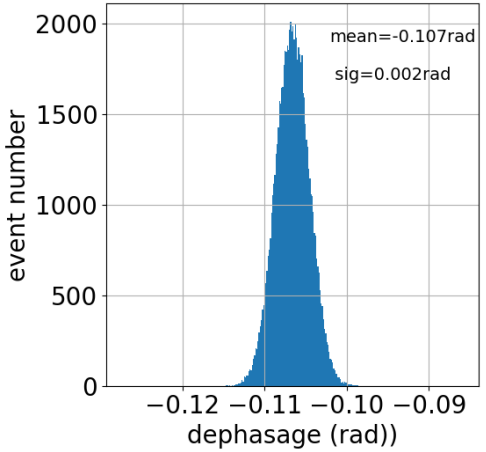
FMC ADC_9680 : Synchronisation



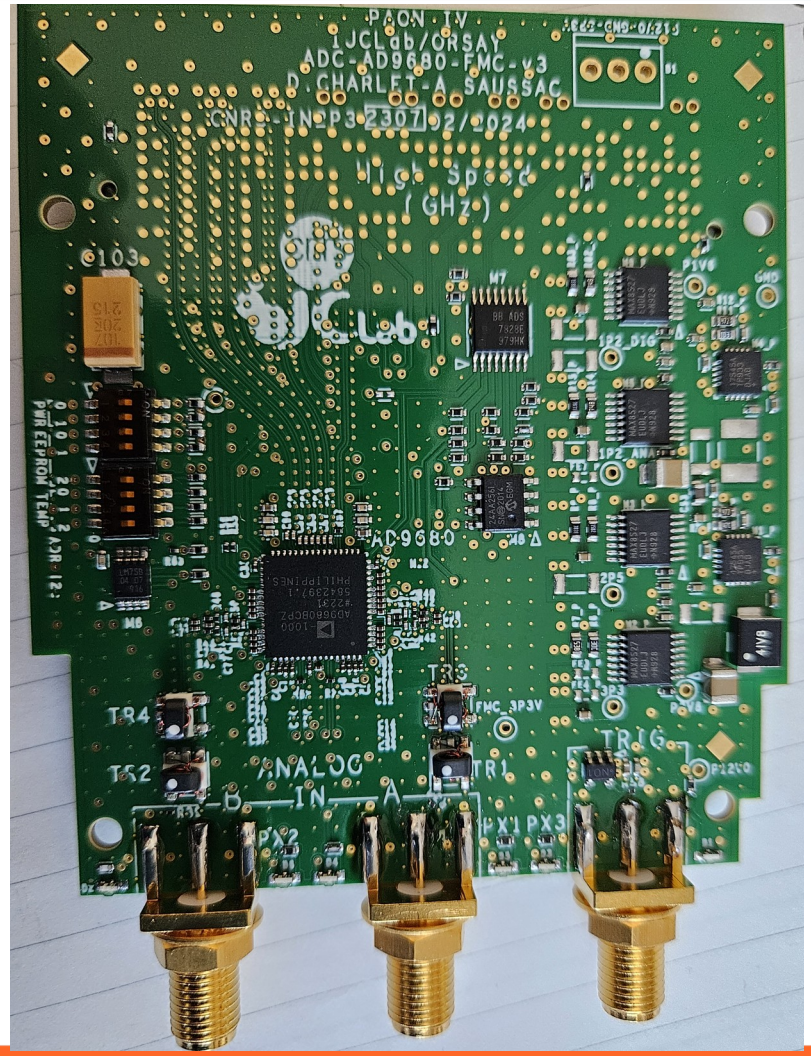
- 2 IDROGEN boards synchronize by WR
- Same RF signal (66MHz) split on boards
- FFT 16K point
- Cross correlation





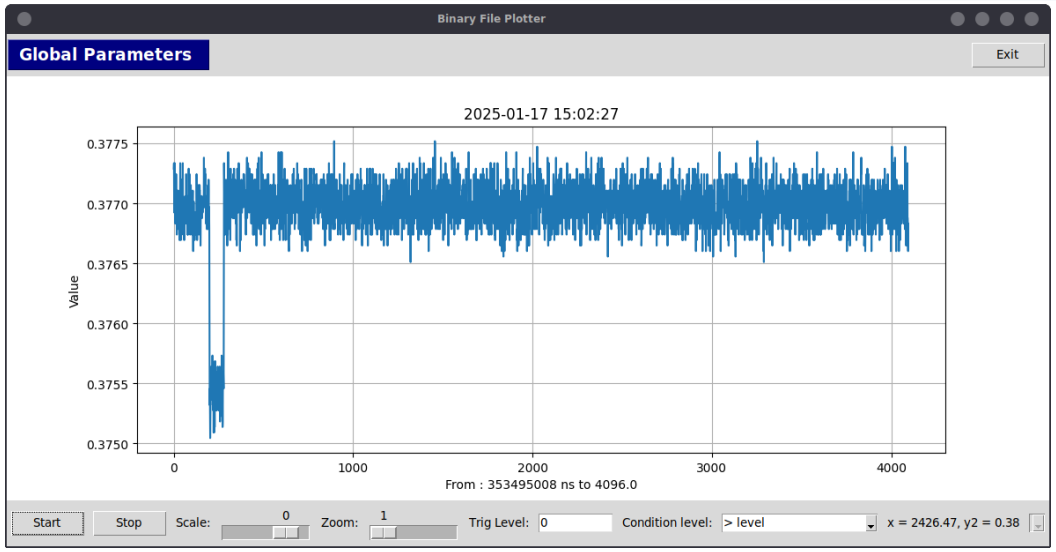


FMC_AD9680_1GSPS

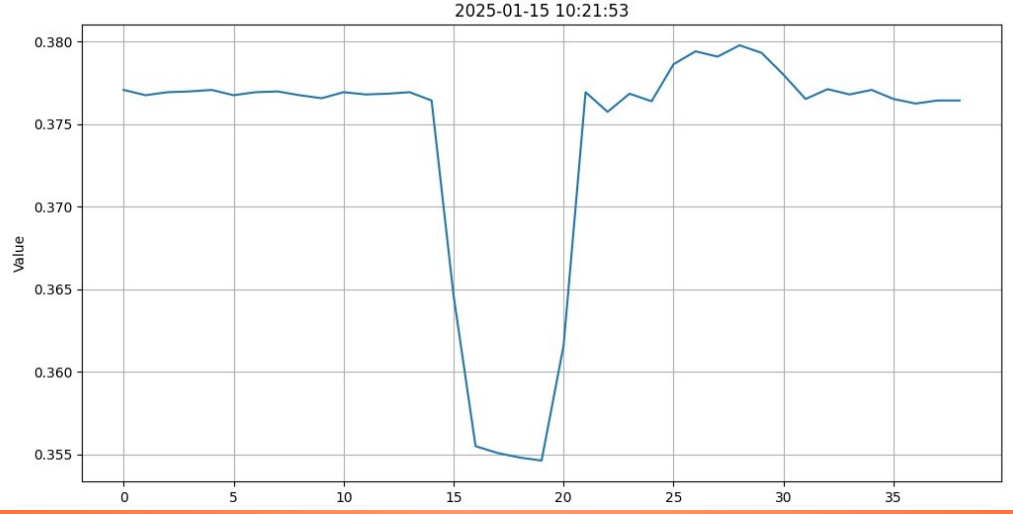


- Mezzanine main features :
  - VITA57.1 (FMC), ADC 9680, 2 channels, 14 bits
  - 1 GSPS, JESD204B, 2GHz analog bandwidth
  - External trigger in
- Bandwidth 500 MHz to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x 10G Ethernet
- Configuration by IPBus 10G

FMC_AD9680_1GSPS

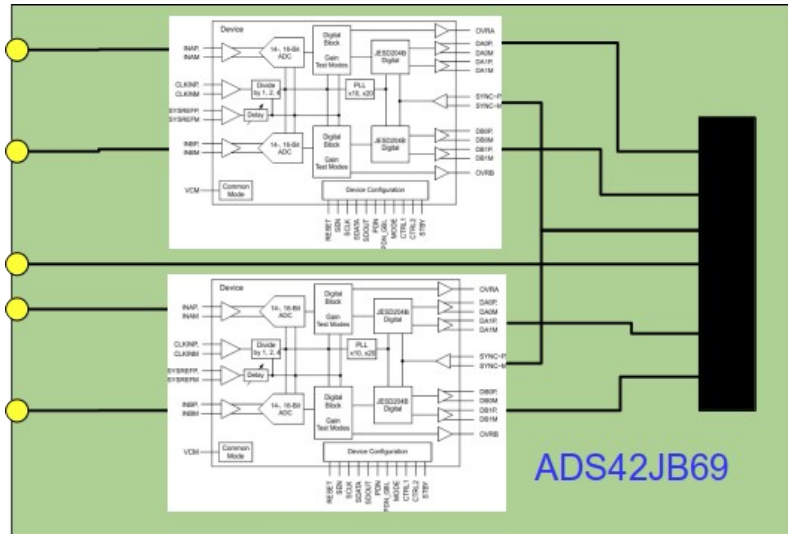


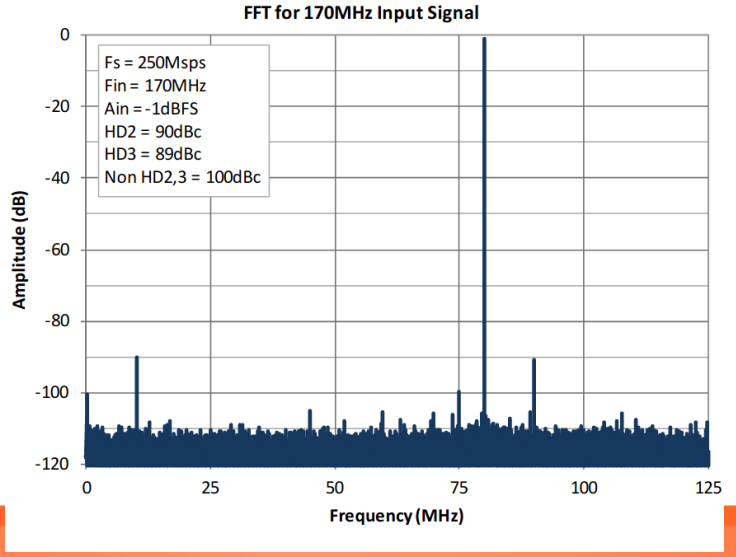
- Level trigger acquisition
- 5ns pulse
- 10mv of dynamic



- 5ns pulse
- 200mv of dynamic

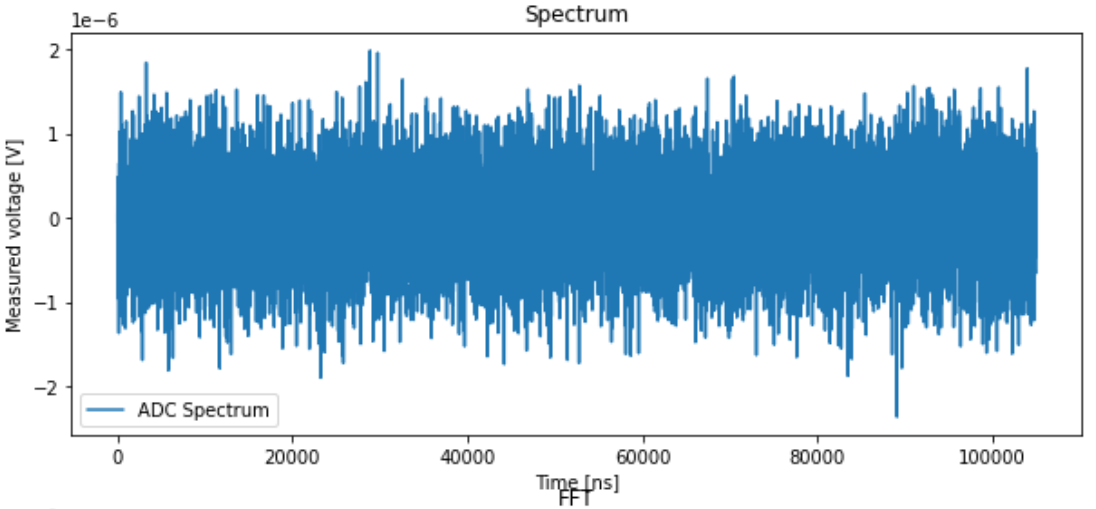
FMC_ADS42JB69 for IDROGEN

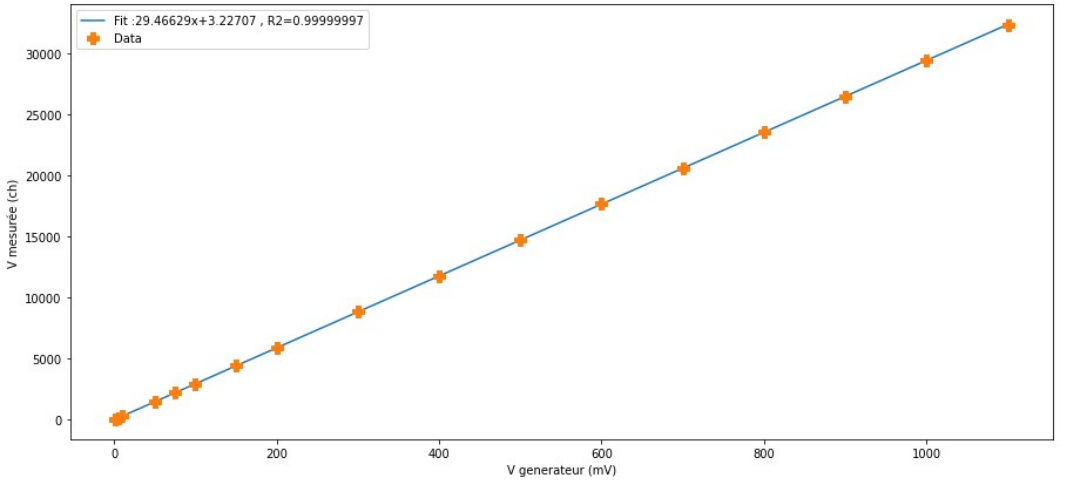


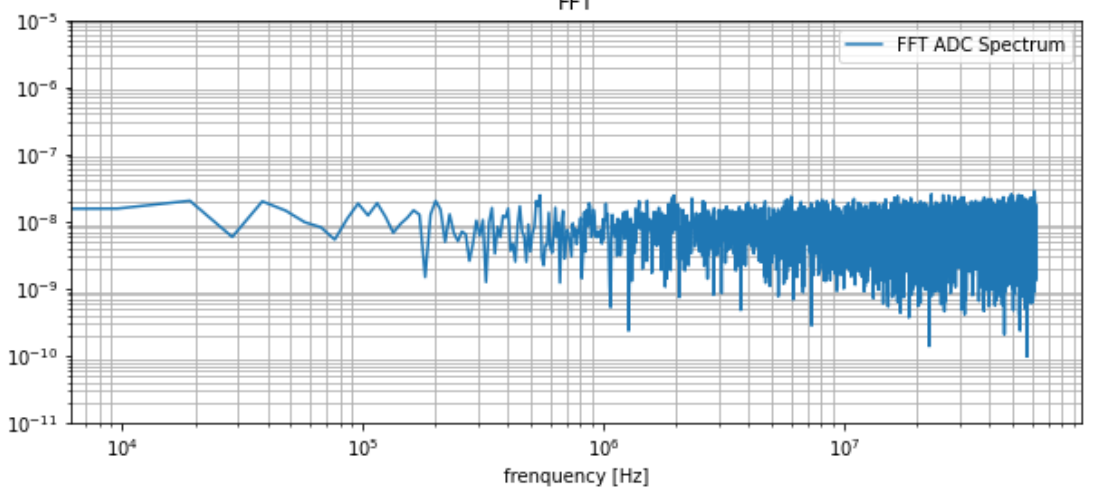


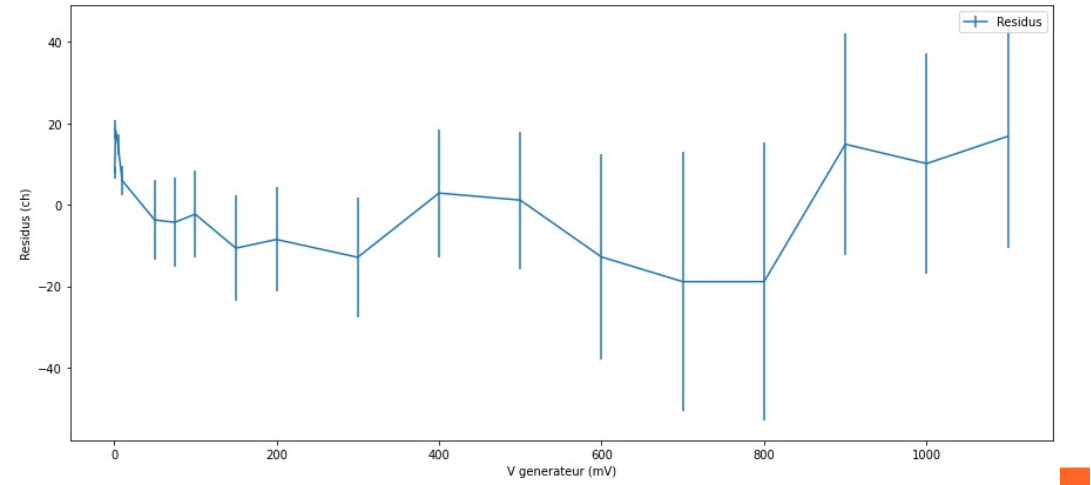
- The motivation to develop the FMC-ADS42JB69
  - **ADC Clock origine coming from IDROGEN**
- 4 channels 250MSPS 16bits
- One external trigger
  - Interface JESD204B
  - Analog input 900MHz
  - 2.5v input voltages

ADC & input filter validation





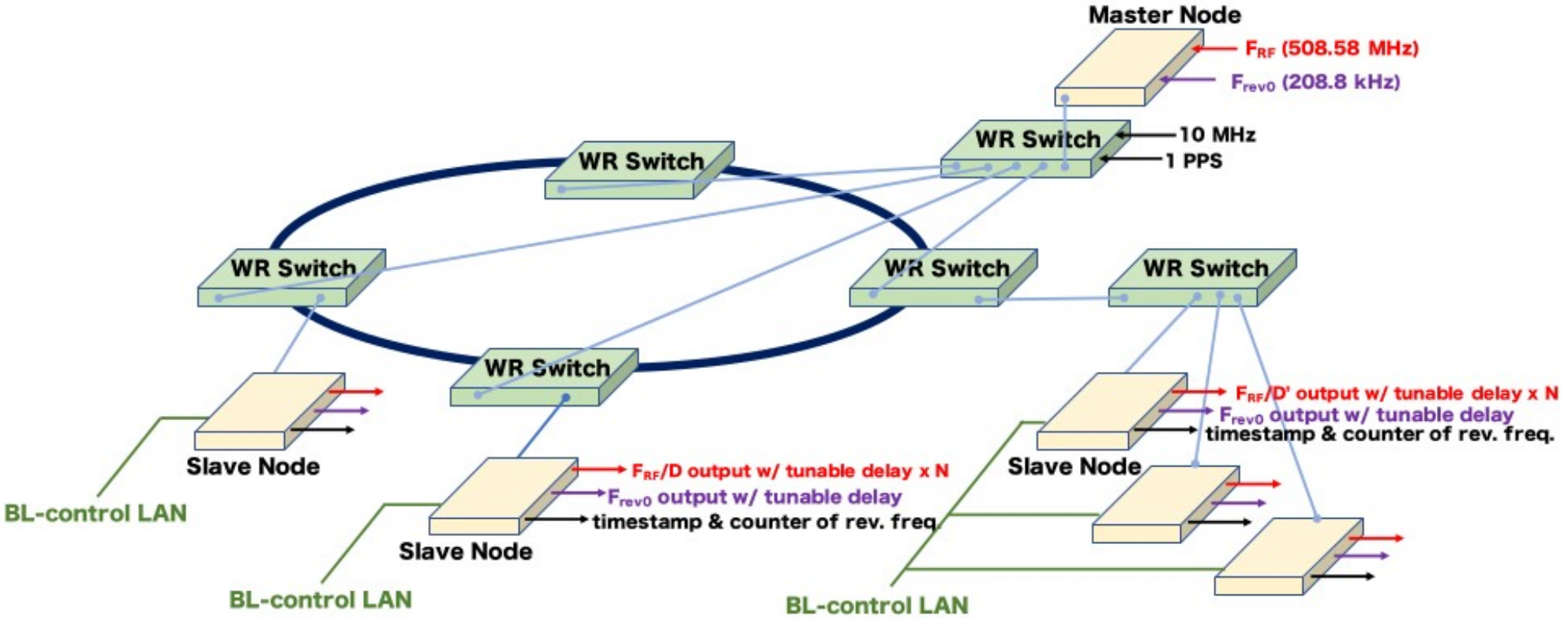




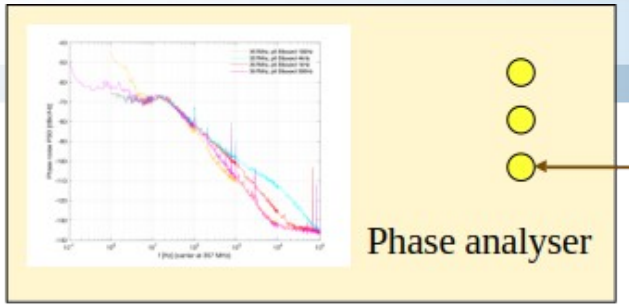
Master oscillator distribution

KEK accelerator : Master oscillator distribution

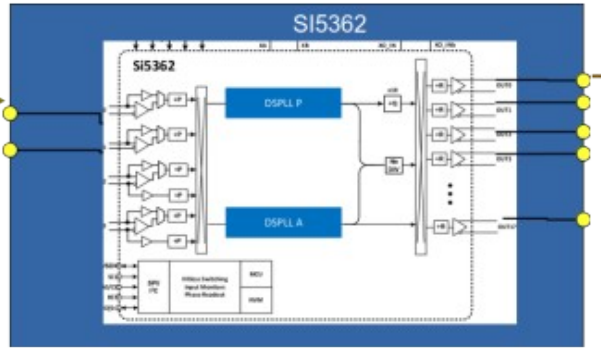
- Real-timed communication system : tight time constraints
- Long distances between nodes : long transmission delays
- Numbers of nodes : several hundred

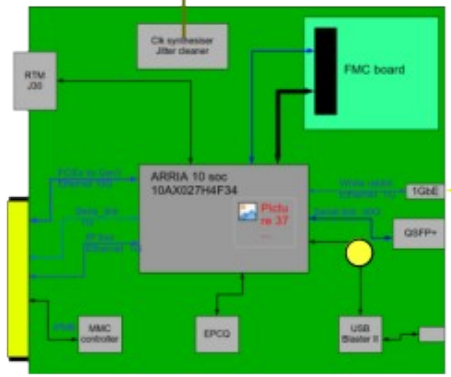


IJClab setup



Fractionnal PLL 80KHz < F < 3GHz





10MHz & PPS

IDROGEN Board 100MHz < F < 1.5GHz

FMC_SI536X Fractionnal PLL

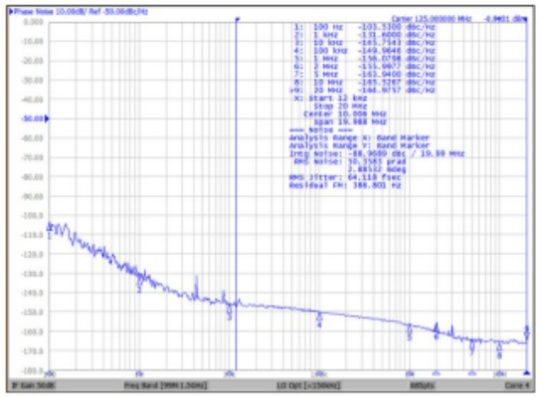
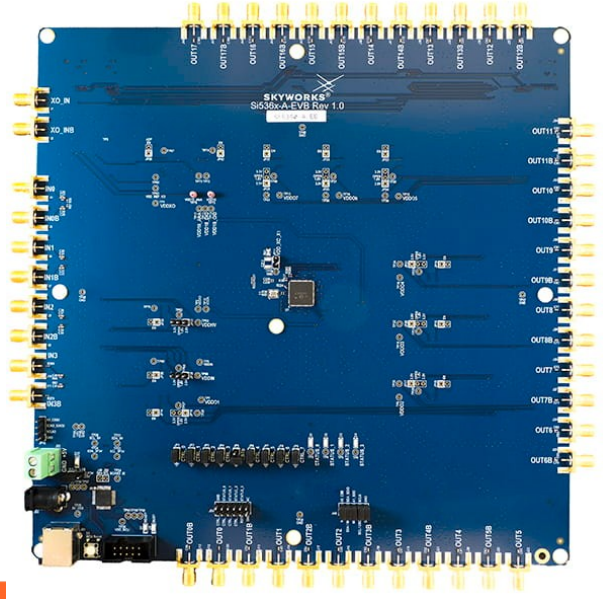
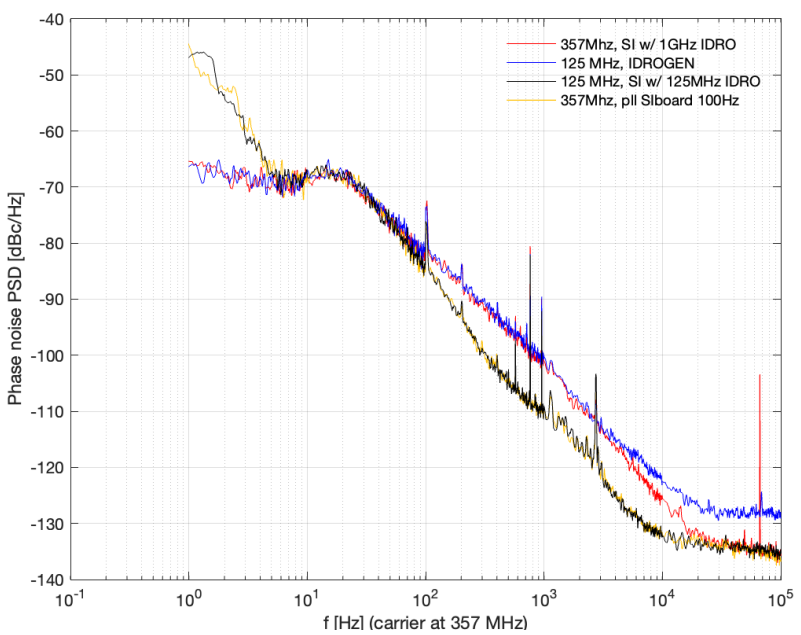


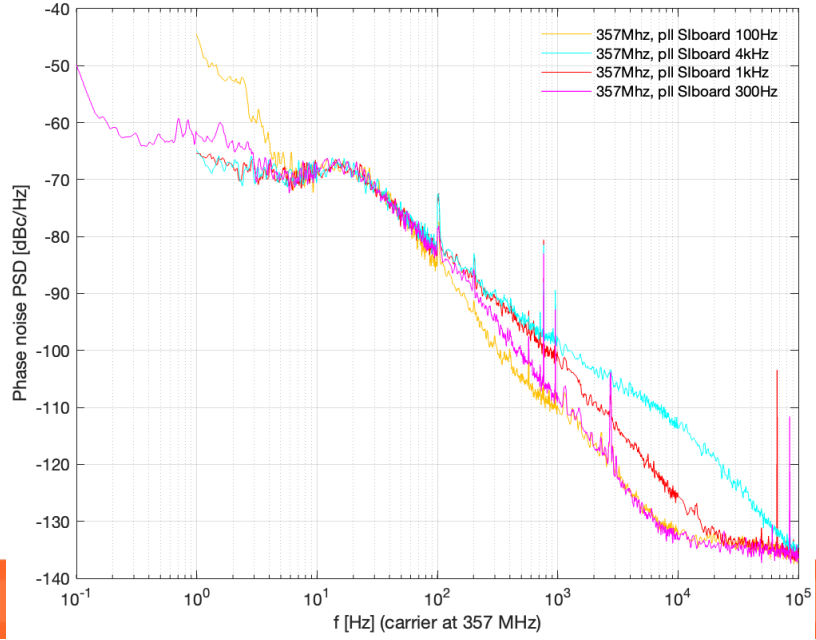
Figure 4.6. 64 fs Jitter for 125 MHz LVDS; Path=DSPLLP+Qdiv



- ANY input to ANY combination of output (not really...)
- frequencies up to 2.75 GHz (1.3GHZ for A version)
- • Ultra-low phase jitter (<55 fs typ)
- phase transients (35 ps typ)
- • Up to six differential/single-ended Inputs
- • Input frequency range
- - Differential: 8 kHz to 1000 MHz
- - LVCMOS: 8 kHz to 250 MHz
- • 18 Outputs
- • Output frequency range
- - Differential: 8 kHz to 2.75 GHz
- - LVCMOS: 8 kHz to 250 MHz
- • Fixed or user-adjustable output formats

FMC_SI536X and IDROGEN

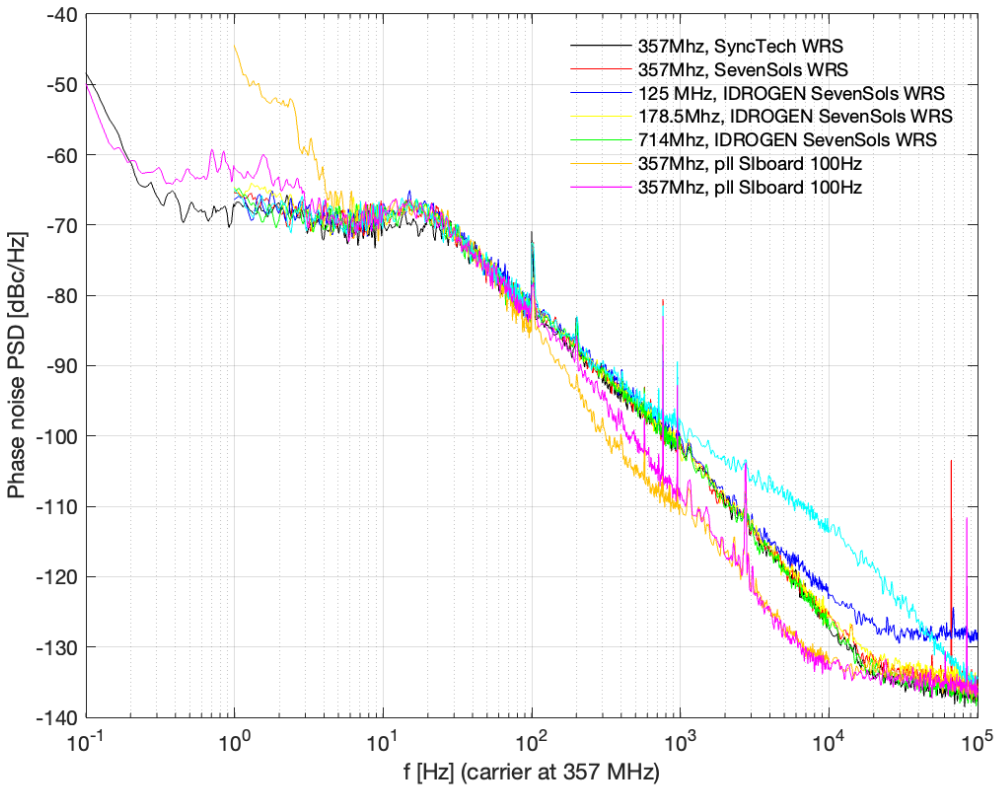




- Measurement of phase jitter
  - IDROGEN board alone
  - SI5362 synthonize IDROGEN at 100MHz & 1GHz

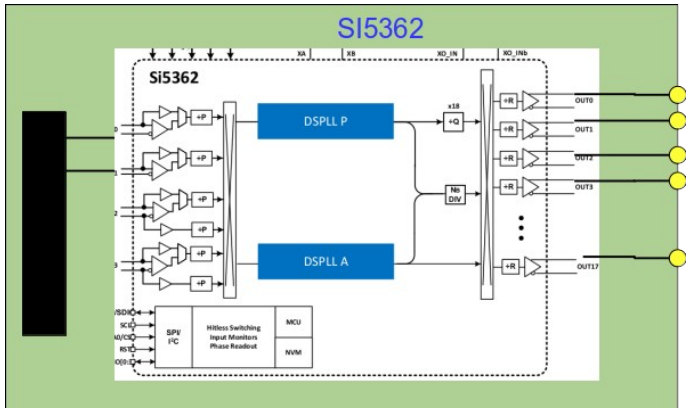
- Measurement of phase jitter for differents loop bandwidth

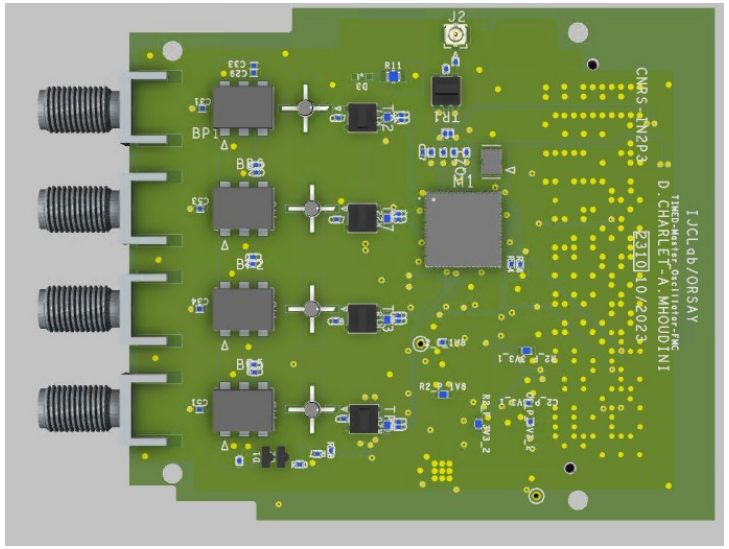
FMC_SI536X and IDROGEN



- Measurement of phase jitter
  - Differents output frequency
  - Different switchs : SEVENSOL & SyncTech

FMC_SI536X for IDROGEN





- The motivation to develop the PLL FMC
  - **Generate any frequency disciplined by WR clock**
  - ultra-high-performance jitter attenuator
  - Ultra-low phase jitter (<55 fs typ)
  - 18 outputs 10KHz to 2.75GHz
- FMC_SI536X
  - 4 single ended independent outputs clock
  - Configuration by PCIe or IPbus
  - Currently in cabling

KEK (Japan) ATF collaboration

“KEK ATF Low-Level RF system phase and amplitude feedback front-end electronics upgrade slides for IJClab seminar”

POPOV Konstantin

30th January
2025

KEK Accelerator Test Facility (ATF)

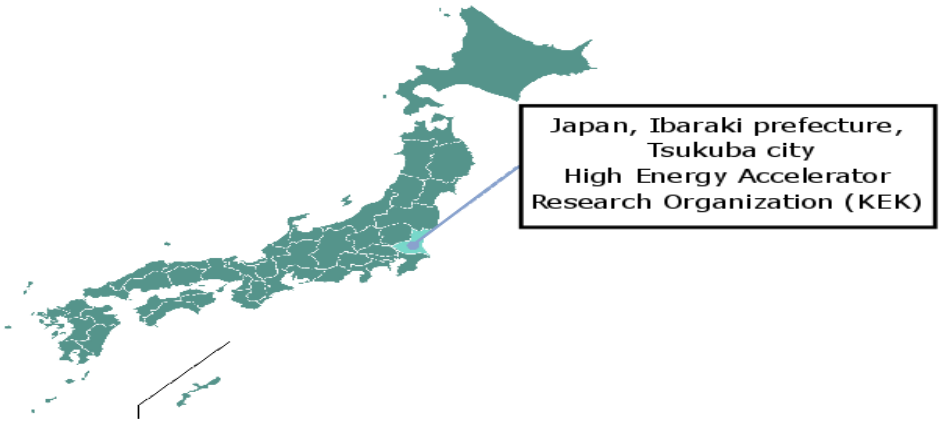


Figure 1: High Energy Accelerator Research Organization (KEK) location on the map of Japan

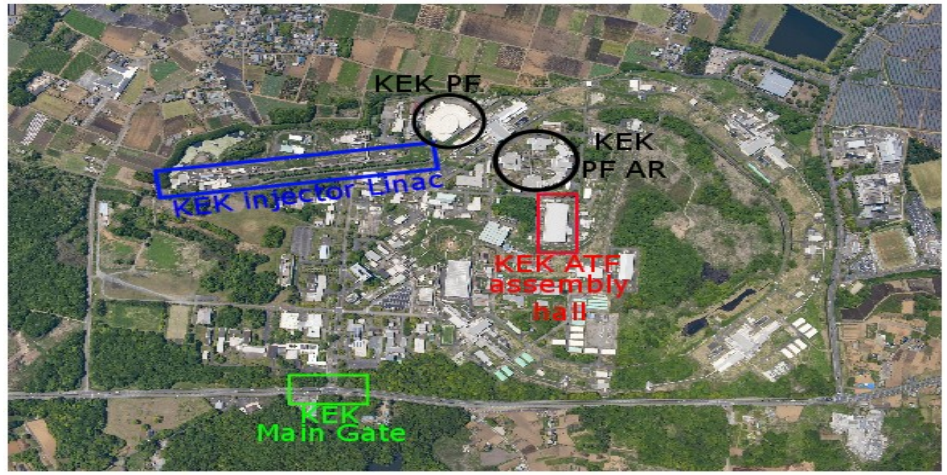


Figure 2: KEK ATF assembly hall location at the KEK Tsukuba campus

Figure 3: KEK ATF assembly hall building photo

KEK Accelerator Test Facility (ATF)

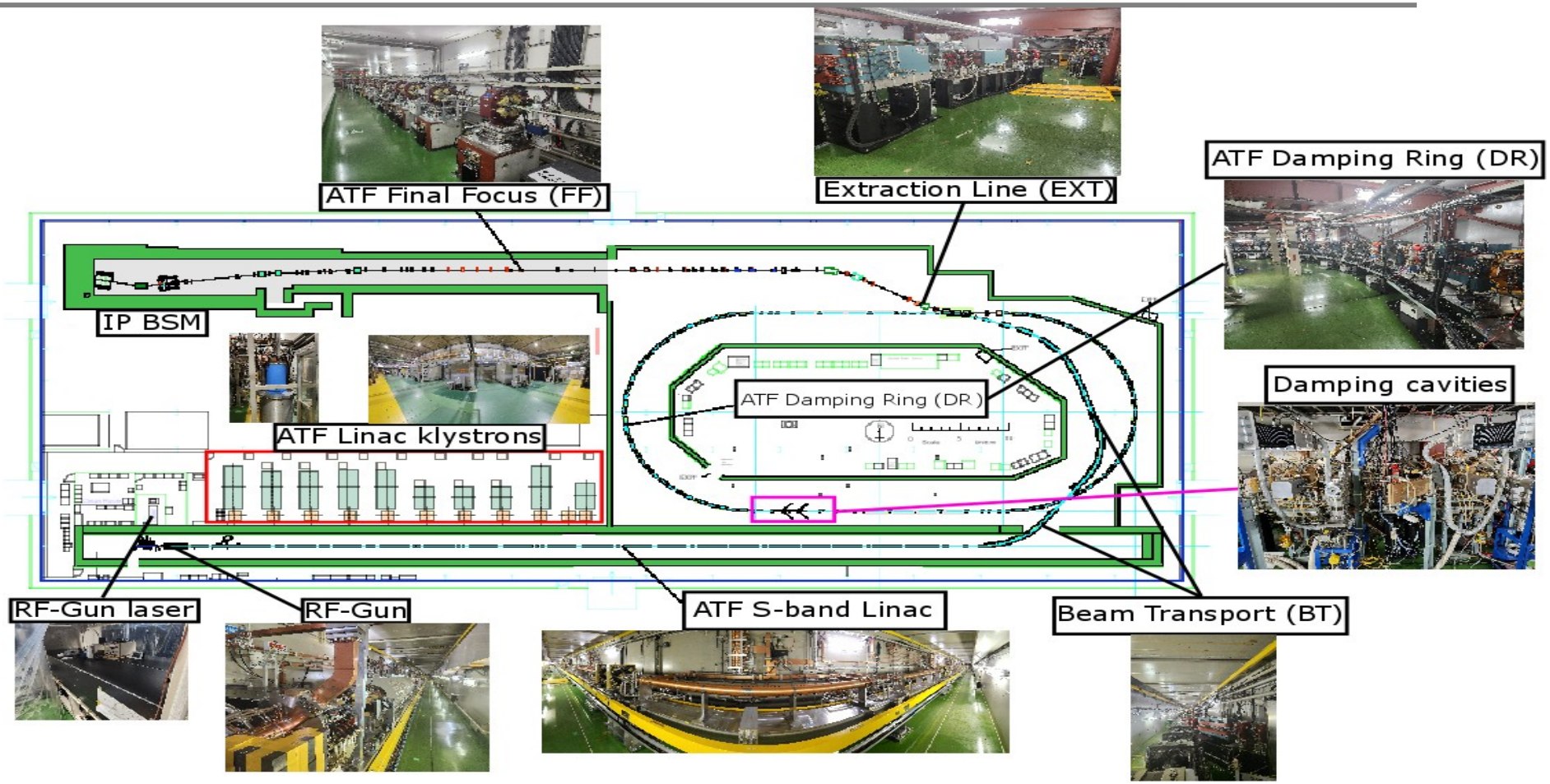


Figure 4: KEK ATF facility layout

KEK ATF is the Accelerator Test Facility devoted to develop beam instrumentation technologies for ILC project (International Linear Collider). It has laser-driven RF-Gun, 1.29 GeV S-band Linac, Damping Ring and Final Focus devoted for nanobeam study

ATF LINAC LLRF system simplified block-diagram

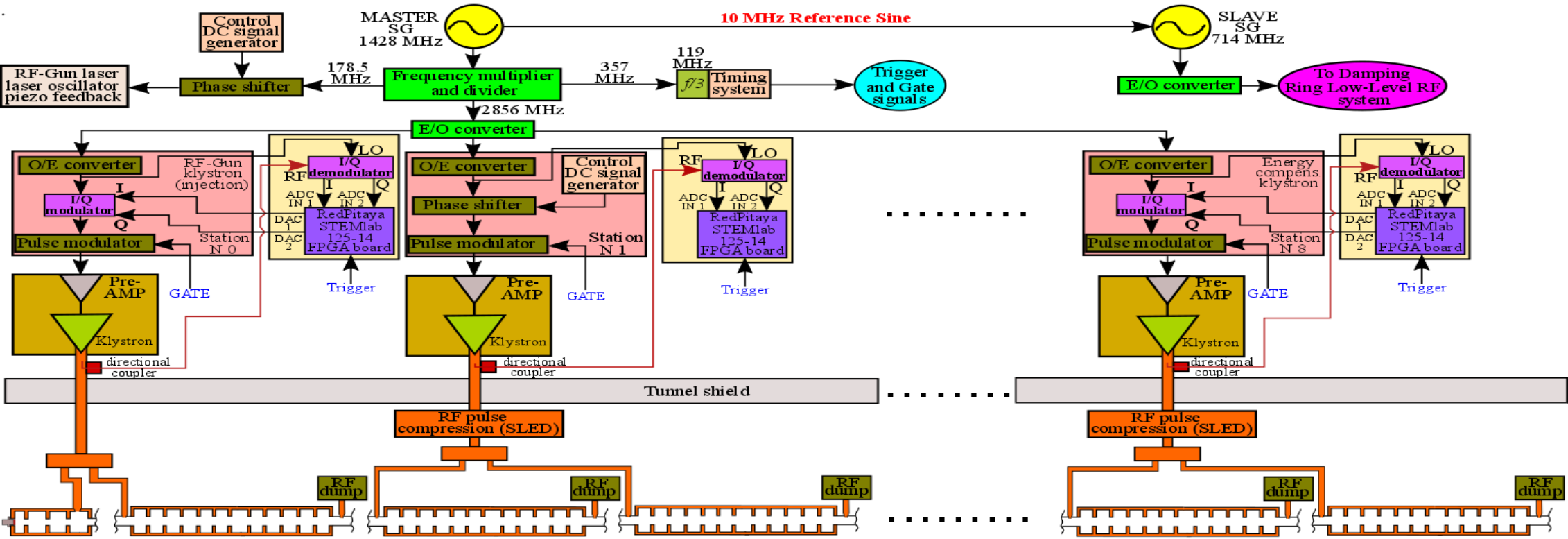


Figure 5: ATF LLRF system simplified block-diagram

Right now, KEK ATF Linac and Damping Ring LLRF system and its feedbacks are under upgrade. The analogue feedbacks are transferred to the FPGA board based processing systems. So, this upgrade requires highly stable, commercially available LO signal generator for every branch. The LO generator must be locked to the 10 MHz and be easily implemented into Event Generator and Event Receiver timing system

ATF DR LLRF system simplified block-diagram

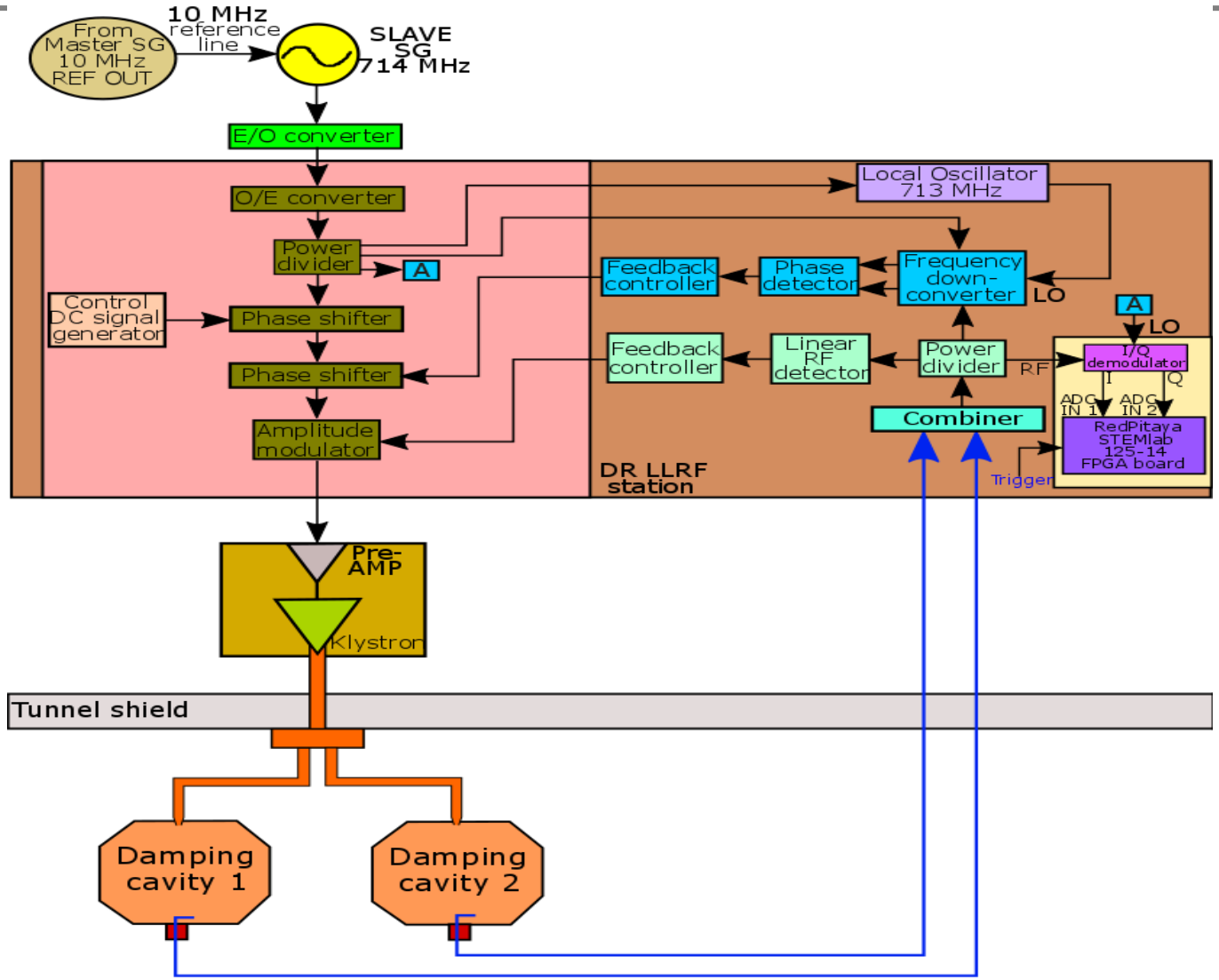


Figure 6: ATF DR LLRF system simplified block-diagram

The LO signals are devoted for the frequency down-conversion to be digitized by the 125 MSa/s ADC.
The LO signal phase noise (RMS) must be less than 0.2 degree for every frequency present in the KEK ATF LLRF system.
The phase noise distribution of the LO signals must be close to the present frequencies in the system

Figure 7: Agilent E5052B Signal Source Analyzer (SSA)

Phase noise maps measurement results

These spurs (spikes) mean the short-period phase fluctuations. The most noise signal is 714 MHz for ATF DR. The 10 MHz reference signal quality gives these spikes and problem at 1 kHz.

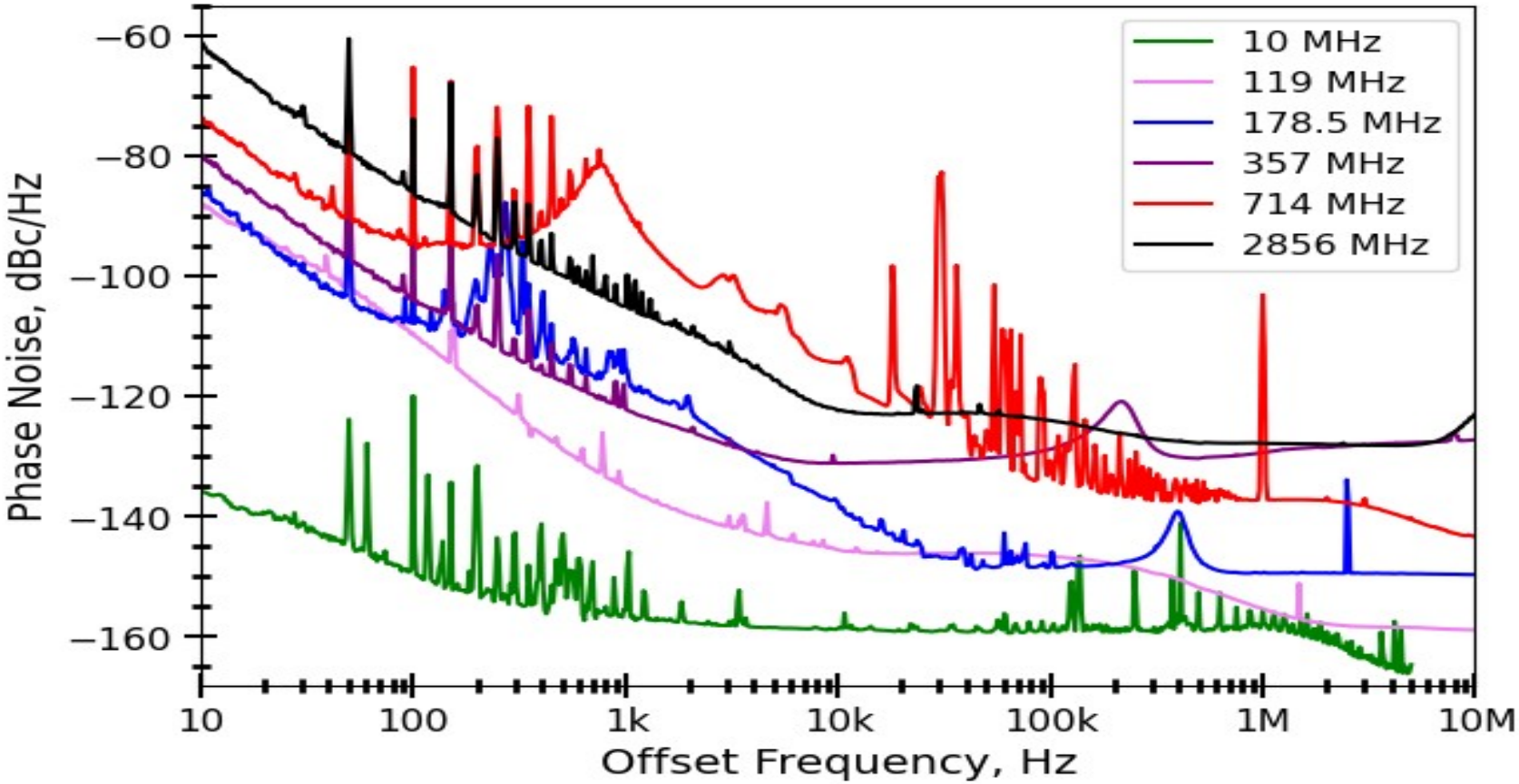
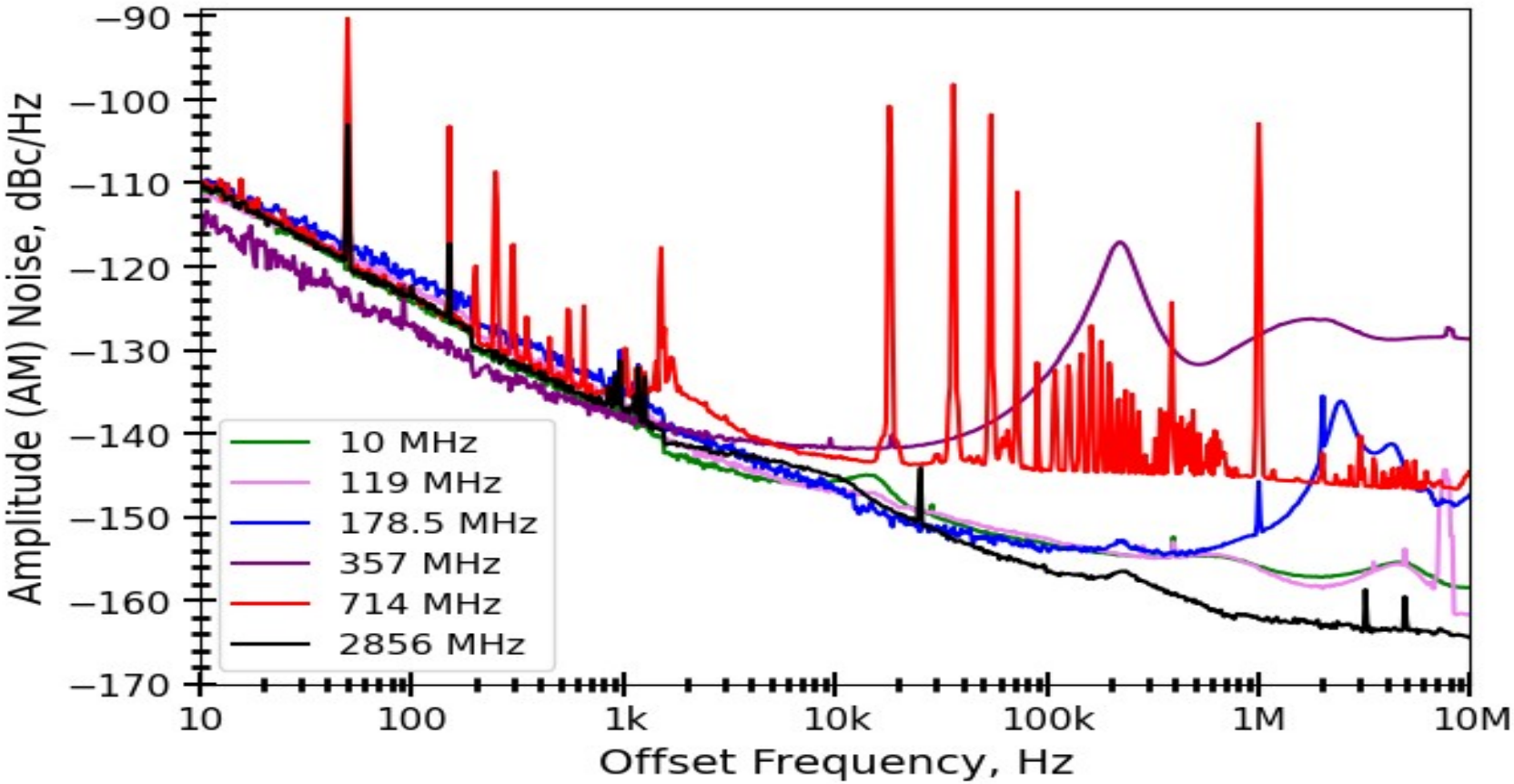


Figure 8: Phase noise map measured with SSA

Amplitude noise maps measurement results

These spurs (spikes) mean the short-period amplitude fluctuations. The most noise signal is 714 MHz for ATF DR. The 10 MHz reference signal quality gives these spikes and problem at 1 kHz.



According to the IDROGEN + SkyWorks clock generation board setup specifications, this hardware is the best choice for the KEK ATF LLRF system front-end electronics upgrade.

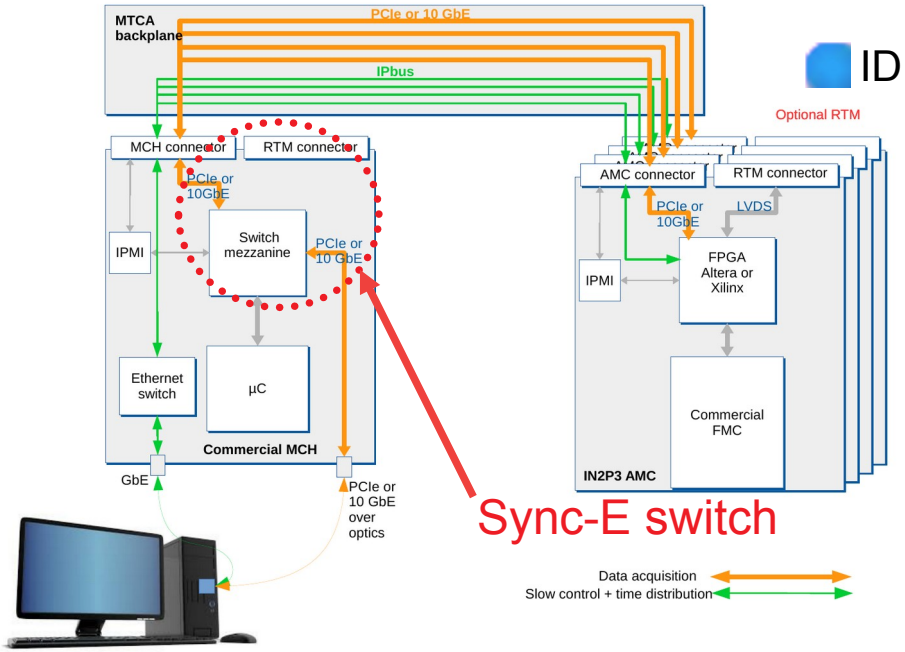
Conclusion

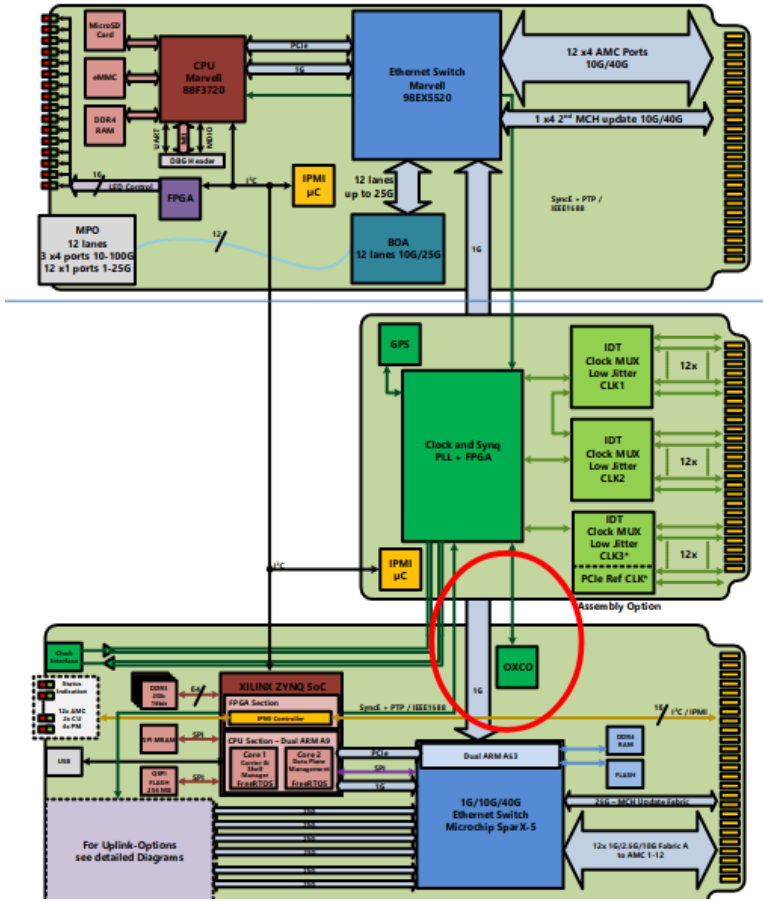
- Very promising results with IDROGEN board
- A new board version (V4) will be designed due to obsolescence of components
- New projects for IDROGEN system : CTAO-MST, NENUFAR (Nancay observatory), ATF LLREF , KEK accelerator, New Comet (Nuclear IJClab), ….

- Development efforts are to be focused on low frequencies phase noise (low frequency)
- A lot of improvements are possible on the WR → WhiteFox project (jitter < 100fs)

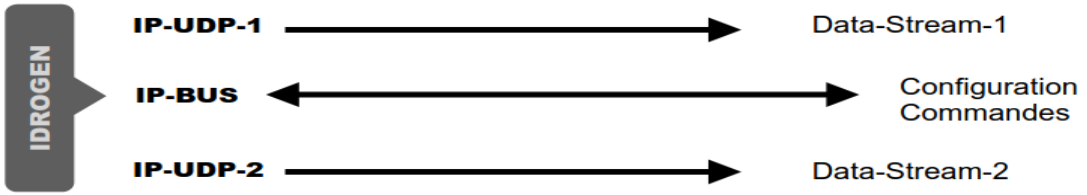
R & T TIMED : WR Crate integration

- WhiteRabbit on µTCA
  - Only switch functionality (no master)
  - WhiteRabbit on copper link
  - Sync-E function on MCH board
  - NAT-MCH-4
    - IEEE1588V2 compliant switch
  - IDROGEN board





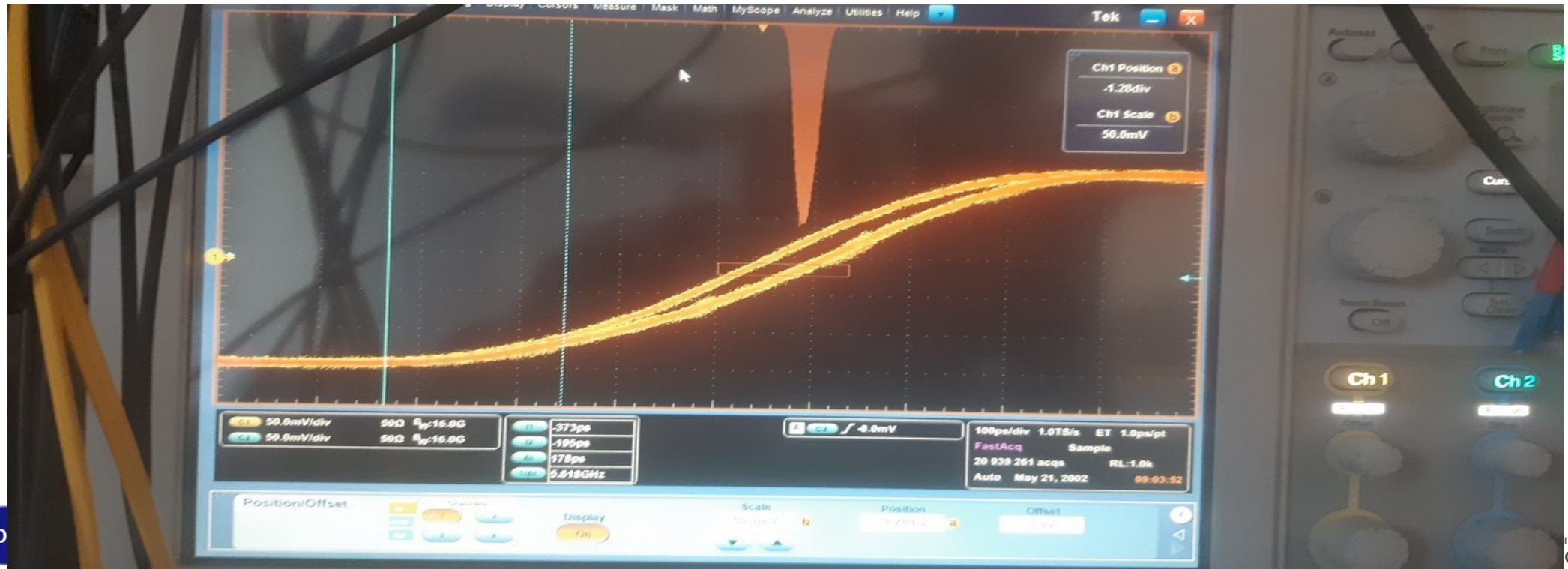
IDROGEN firmware : Ethernet readout

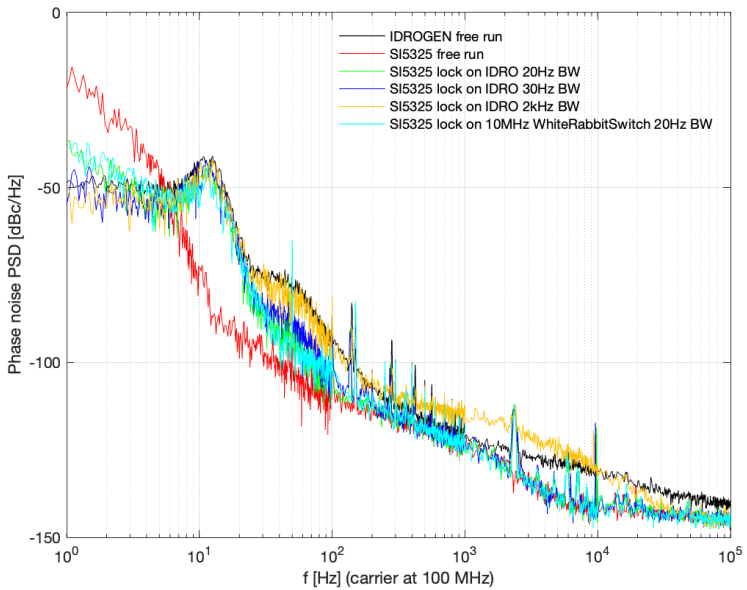


- 2 ETH 10G links
  - 1 Ipbus 10G link, share with UDP link
  - Multi Jumbo frame by event
- Header : 4 x 64b
  - Start mark : 4bytes
  - Paquet lenght : 2bytes
  - Paquet number : 2 bytes
  - Sernum paquet : 4 bytes
  - Board/Channel ID : 2 bytes
  - DataDescriptor : 2 bytes
  - TAI : 8 bytes

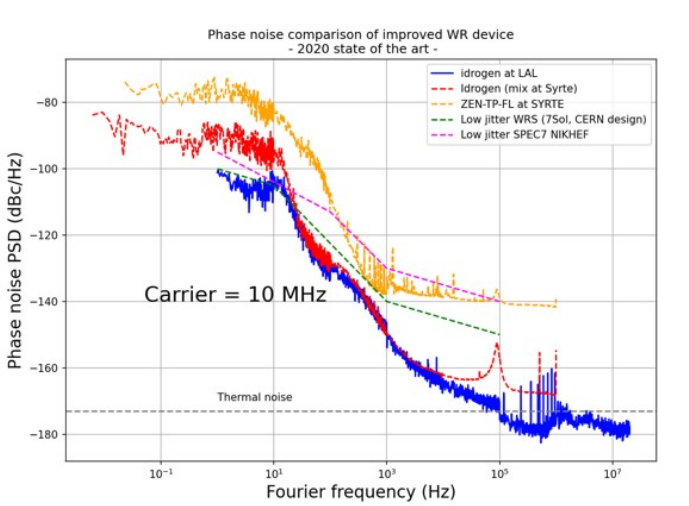
Pulse Per Second : IDROGEN

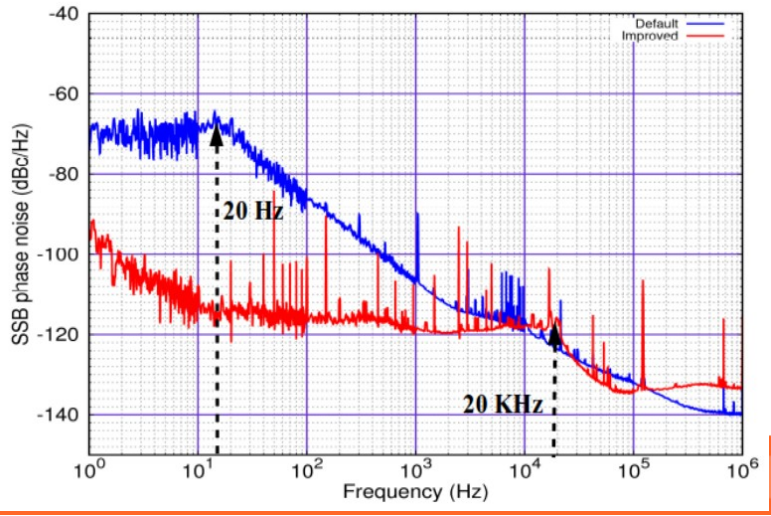
- PPS 2 IDROGEN board
- 25m & 125m of optic fiber
  - ~50ps of dispersion of the PPS with calibration




IDROGEN free run
SI5325 free run
SI5325 lock on IDRO 20Hz BW
SI5325 lock on IDRO 30Hz BW
SI5325 lock on IDRO 2kHz BW
SI5325 lock on 10MHz WhiteRabbitSwitch 20Hz BW
Phase noise PSD [dBc/Hz]
0
-50
-100
-150
10^0
10^1
10^2
10^3
10^4
10^5
f [Hz] (carrier at 100 MHz)

R & T TIMED : Increasing performances





- Collaboration with Paris Observatory Laboratory
  - Goal 1 : ~ 1ps
  - Goal 2 : < 100fs
- Soft PLL modification
  - Decreases the response time of software PLL : µP frequency upgrading
  - Gain integrator optimization : Kp, Ki dynamically connfigurable
- Increased PLL bandwidth of the GM Local oscillator
- Components upgrading
  - VCXO selection
  - Increased internal Frequency (PLL number reduction)
- Modification of WR principle
  - phase modulation and demodulation of an ultra-stable optical carrier
  - Replacement of message protocol by timecode
  - Phase measurement in optic
  - Link asymmetry mitigation
  - Time calibration at the pps level