Update Report

❖ Summer ‘24 activities at IJCLab/OMEGA:

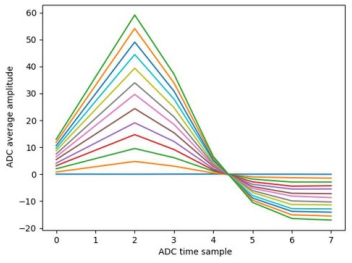
➢ Test boards (updated & 1st version PCB) with EICROC0 alone

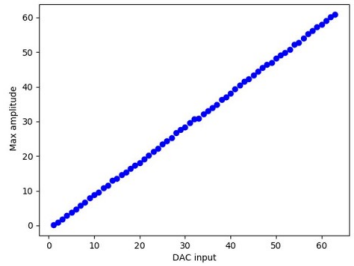
❑ TDC measurements:

- Individual channel discriminator adjustment (Vth_cor) based on Adrien’s code
- Jitter determination for all channels versus injected charges: σ = 10 ps at 24 fC
- Determination of minimal charge: ~4.5 fC
- Determination of the TDC quantization step (LSB) exploiting delay (CMD and external trigger): 25 ps, as expected by design)

❑ ADC measurements (still ongoing)

- Amplitude versus time for all channels
- Maximum amplitude versus injected charges

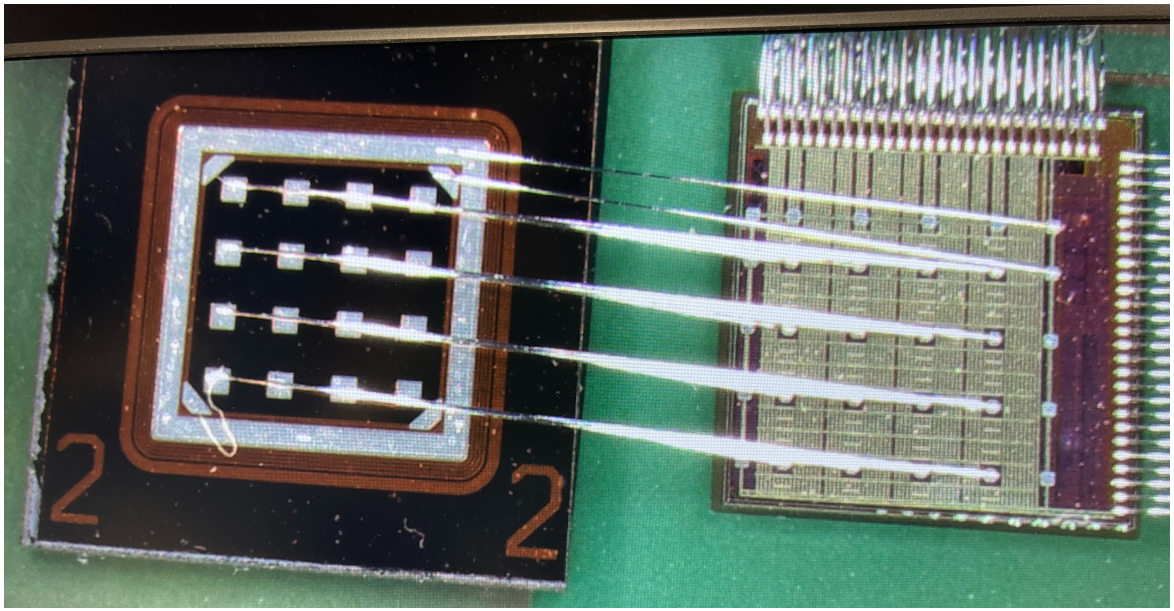




- **2 test boards (updated PCB) with <u>1 EICROC0 and 1 AC-LGAD:</u> 2.3 A & 2.3 B**
  (wire-bonding at IPHC Strasbourg late June; AC-LGAD sensors 6.19 & 8.13 – or 8.14)
  - Board **2.3 B**: measurements at OMEGA in June: sensor depleted at –100 V ⇔ 1 μA

  - August: **2.3 A** & **2.3 B** => unexpectedly show very high current: **-10 V** ⇔ ~ **10 μA !**

=> Had a look to the aspect of the wire-bonding with a microscope



No obvious defect…

=> Checked Analog probe (PA) DC level for all channels varying sensor HV applied

Analog probe (PA) DC level measurements for all channels varying sensor HV applied

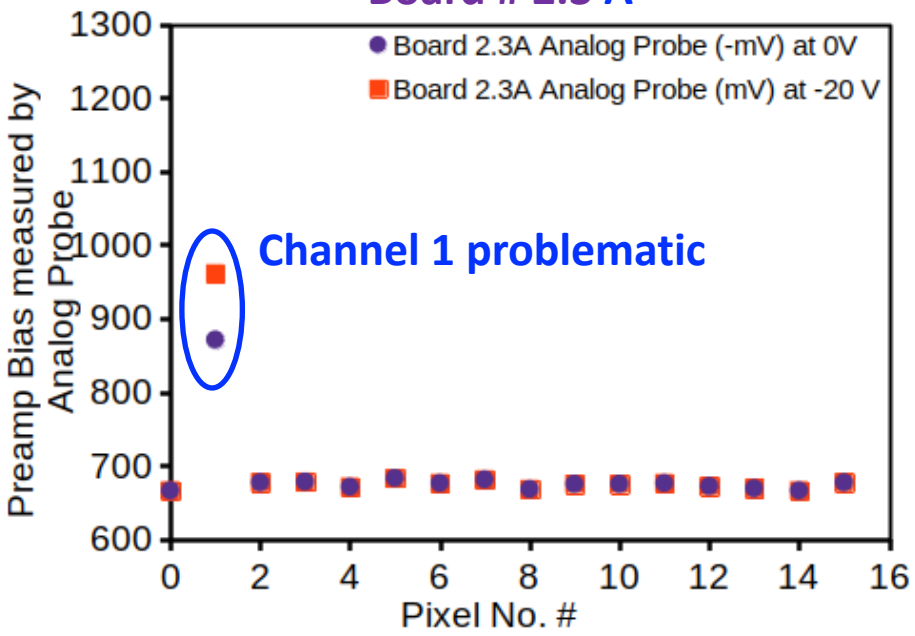
For each channel the measured PA DC level should not vary with the HV applied to the sensor

For both boards: $I_{measured}$ at **0 V** : **~ 0.3 µA**

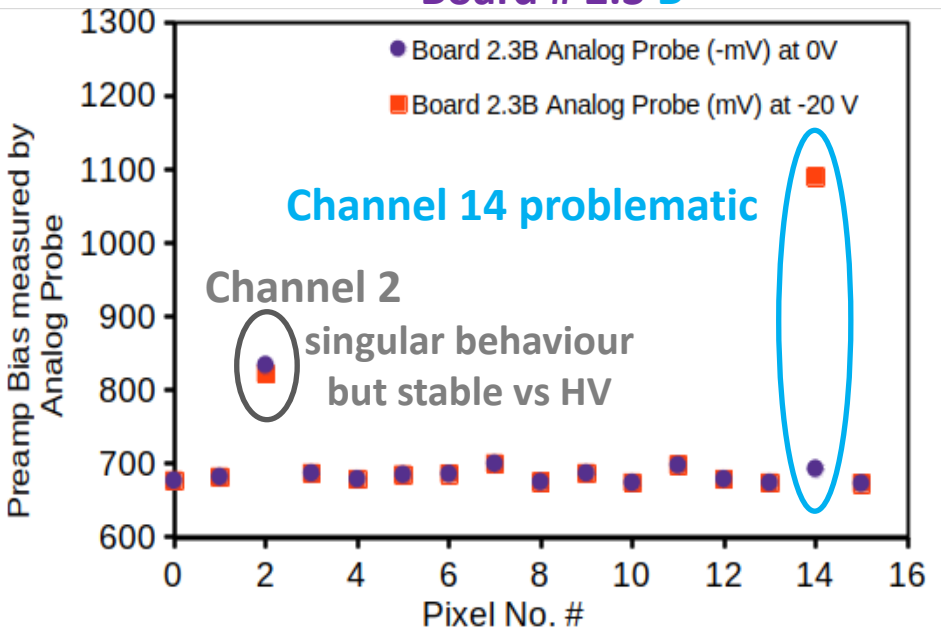
2.3 **A**: $I_{measured}$ at **-20 V** : **~ 15 µA**

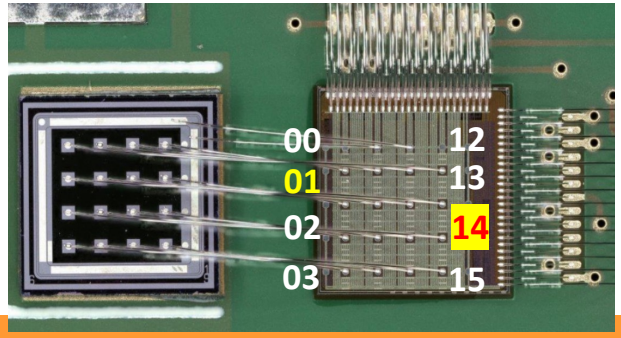
2.3 **B**: $I_{measured}$ at **-20 V** : **~ 48 µA**

Board # 2.3 A



Board # 2.3 B





Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

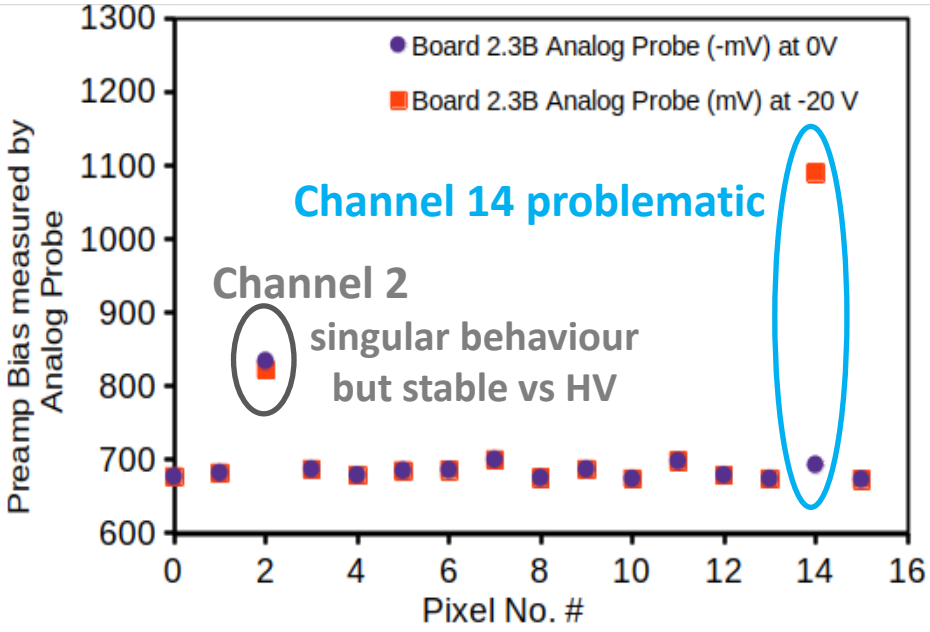
⇒ Chose **to disconnect** the wire associated to channel 14 (board # **2.3 B**)

[performed at OMEGA]

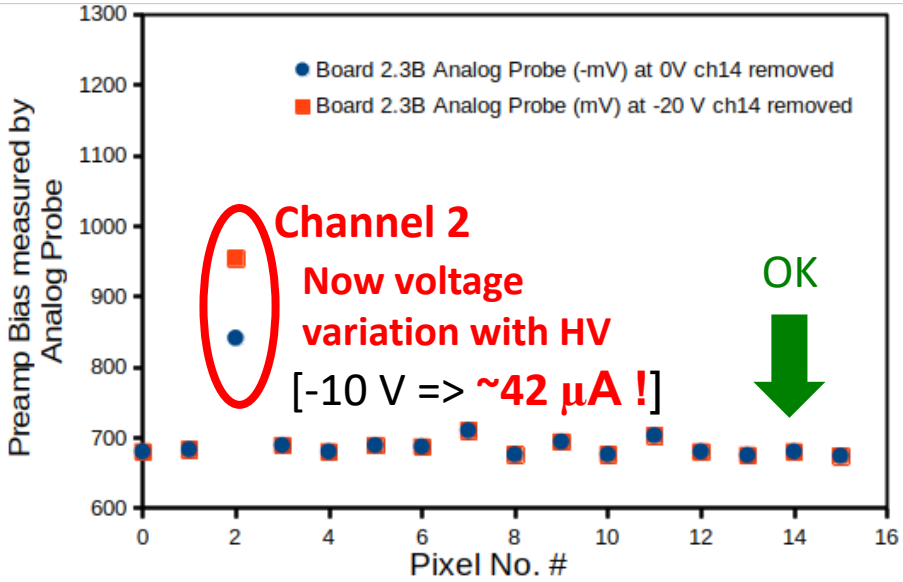
Analog probe (PA) DC level measurements for all channels varying sensor HV applied
After removal of wire connecting channel 14 on board # 2.3 B

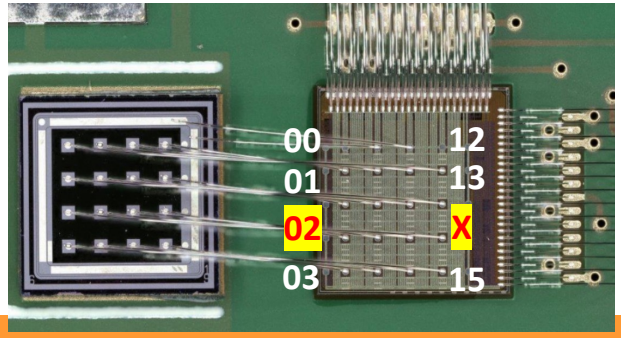
For each channel the measured PA DC level should not vary with the HV applied to the sensor

Board # 2.3 B before #14 wire removal



Board # 2.3 B after #14 wire removal





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Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

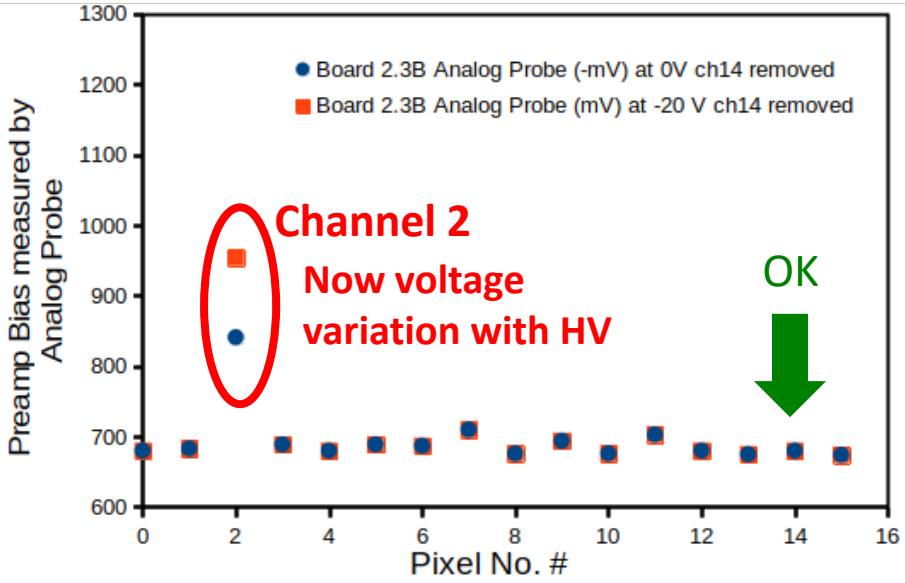
⇒ Chose **to disconnect** the wire associated to channel 2 (board # **2.3 B**)

[performed at OMEGA]

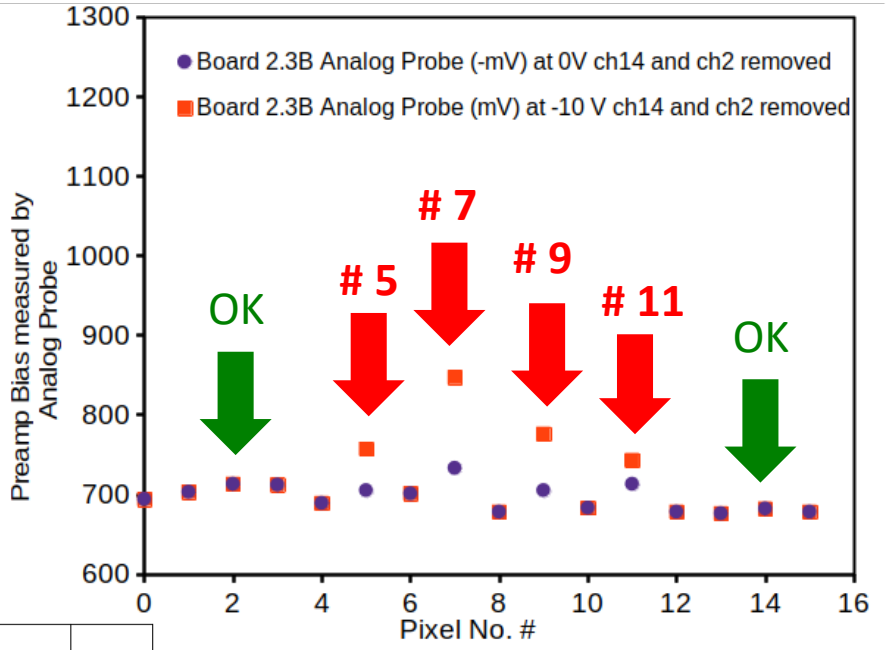
Analog probe (PA) DC level measurements for all channels varying sensor HV applied
After removal of wire connecting channel 02 on board # 2.3 B

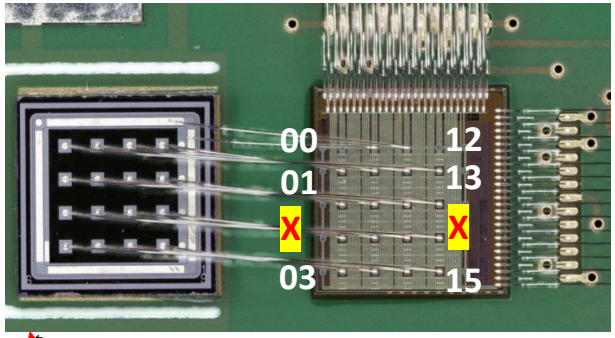
For each channel the measured PA DC level should not vary with the HV applied to the sensor

Board # 2.3 B before #02 wire removal



Board # 2.3 B after #02 wire removal





Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

⇒ Now 4 channels show singular behaviours …

No more wire disconnection

Status of boards with AC-LGAD in France

- **2 test boards (updated PCB) with 1 EICROC0 and 1 AC-LGAD: 2.3 A & 2.3 B**
  (wire-bonding at IPHC Strasbourg late June)
  - **# 2.3 B** : wires associated to channels **# 02** & **# 14 disconnected**
    PA DC levels of channels # 05, 07, 09 & 11 vary with sensor HV applied,
    Current reaches 40 µA for HV = - 10 V
  - **# 2.3 A** : **PA DC level of channel # 01 varies with sensor HV applied,**
    Current reaches 15 µA for HV = - 20 V

Wire-bonding issue? Pixel / sensor issues?

- **1 test board (previous version of the PCB) with 1 EICROC0 and 1 AC-LGAD:**
  - **I(V) curve OK**
  - **ASIC connection issues: PCB cabling and components under investigation**

We have no board holding an AC-LGAD to test ….
We are stopped in our tracks

=> We need your expertise

A parcel containing board **# 2.3 B** and **2 PCBs** (partially cabled) leaves IJCLab today for BNL
(Contact: Alessandro Tricoli)

Expectations

- **# 2.3 B** : diagnostic, lessons to learn, …
  Can another sensor be wire-connected using the second sensor location?

- **2 partially cabled PCBs (updated version):**
  - **Could you please wire-bond an EICROC0 + an AC-LGAD sensor?**
  - **Could you please wire-bond an EICROC0 flip chip?**

… and send (or deliver to CERN) at your earliest convenience

Extensive measurements with a sensor are essential in view of next ASIC iteration design and in view of Beta source, laser & test beam measurements.

EICROC Project within ePIC collaboration: Questions in view of the upcoming review by our institute

Exhaustive scientific document to be submitted Sept. 20th, 2024

After checking that EICROC2 performances are in agreement with specifications

- Number of EICROC2 per AC-LGAD sensor (4/1? or 1/1? or?: date of decision?
- Responsability / payer for EICROC2 production run for all pixelated?
- Responsabilty for EICROC2 + AC-LGAD assemblies (QA)?
- Overall realistic timeline up to Roman Pots (OMD) installation in EIC beam line?

Appendix

Analog probe (PA) DC level measurements for all channels varying sensor HV applied before disconnecting wires

(Measurements with preamplifier probes enabled)

Pix	Board 2.3A Analog Probe (-mV) at 0V	Board 2.3A Analog Probe (mV) at -20 V	Board 2.3B Analog Probe (-mV) at 0V	Board 2.3B Analog Probe (mV) at -20 V
0	666	666	677	677
1	871	961	682	682
2	677	677	834	822
3	678	678	687	687
4	671	671	679	679
5	683	683	685	685
6	676	676	686	686
7	681	681	700	700
8	668	668	675	675
9	675	675	687	687
10	675	675	674	674
11	676	676	698	698
12	672	672	679	679
13	669	669	674	674
14	666	666	693	1090
15	677	677	673	673