# Updates on AC-LGAD Testing @ BNL

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#### Overview

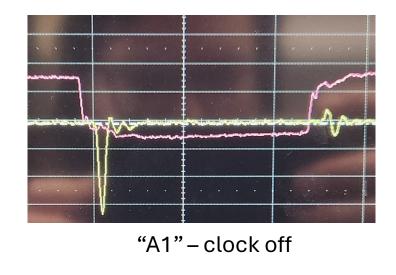
- New firmware provided by IJCLab at the end of July (right before the ePIC meeting in Lehigh).
  - Supposed to fix issues with the clock and the digital output.
  - Drastically speeds up data-taking → everything runs directly on FPGA, previously run on local laptop, commands sent serially to board. (e.g. previously 2k events took 60 seconds to run; now 200k events takes about 10-20 seconds)
- First bump-bonded sensor + ASIC provided by BNL.

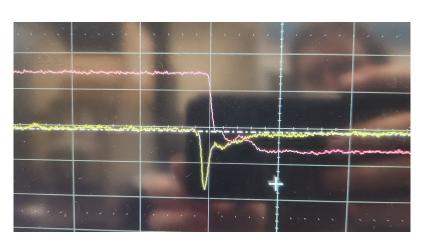
#### Goals from past few weeks:

- Test new firmware with old ("A1") board (wire-bonded) and reproduce <u>Adrien's results</u> shown at ePIC meeting in progress (see next slide).
- Fix issues with the new boards (B1 + B2) and test bump-bonded sensor package.
- Test B1 board with new firmware.
- Set up TCT scans for the "A1" boards.
- Send "B2" board to IO for bump-bonding with AC-LGAD in progress.

#### **New Firmware**

- New firmware is a complete overhaul required re-learning how to send configurations to the board, and (still) requires learning to analyze the output.
- Successfully able to use new setup to see charge injection and analog signals on scope (with both "A1" and "B1" boards).
- Analog output looks similar to before with charge injection.





"B1" - clock off

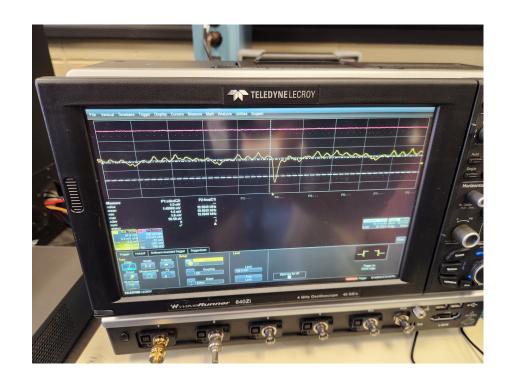
#### New boards

- New board had several issues with missing or incorrect components.
- BNL techs fixed the noted issues in June.  $\rightarrow$  boards still did not draw any current.
- Alex found missing jumpers on both boards, replaced them, and then had to adjust the potentiometers on the board until the correct voltages were read at test terminals.
  - Board B1 and B2 now both functioning properly.
  - B1 has bump-bonded assembly mounted, B2 in progress.

## Bump-bonded assembly (board B1)

- Basic charge injection tests carried out to check ASIC functionality.
- All 16 pixels tested with Sr-90 source to ensure bonding was successful. 

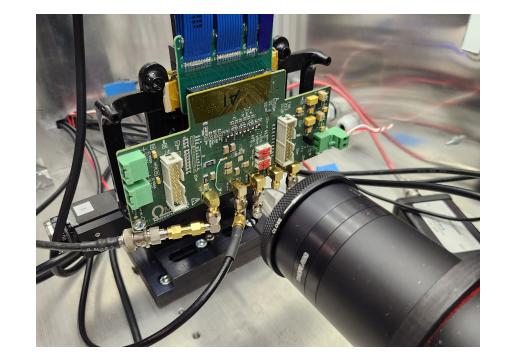
  all channels showed clean analog output via the ASIC!



 Next step is to use new firmware to extract digital information (TDC, ADC) from both A1 and B1 boards to compare.

#### TCT scans of A1 board sensor

- Alex and Enrico Rossi (expert in lab at BNL) setup TCT apparatus yesterday morning.
- Initial tests were successful\*.
- Work is now focused on scanning one column of pixels, second will be added today.
- B1 board cannot be used for TCT due to bump-bonding (AC-LGAD is upside down, backplane blocks photons).

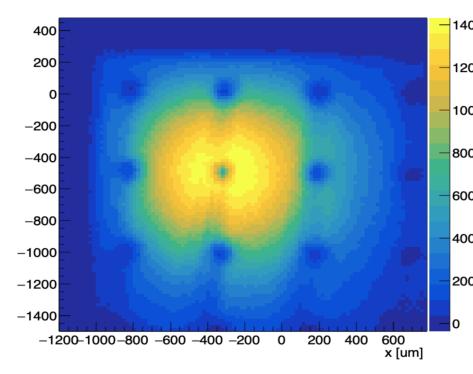


\*There is not a GUI to switch on the preamps on the board – we found that we can send a configuration to the board, and it stays in that state until the board is reset.

### TCT scans of A1 board sensor

- Still having issues with focusing the laser on the pixels.
- Should hopefully have issues solved this week.
- Need to figure out the best configuration of pixels for testing since we can only read out columns of 4.
- A1 board connected with ribbon cable to FPGA outside of the TCT box.
  - Initial testing was done to ensure no obvious issue with ribbon cable seemed okay.





## Next Steps

- TCT scans will continue over next few days → crucial to test performance with integrated AC-LGAD + EICROC0.
- Data analysis using new firmware (Ashik and Souvik are working on this).
  - · Will follow-up with Adrien on a few issues in the data analysis itself.
- When B2 board is ready, we will do same tests as for B1.
- Working on a QA procedure for new boards and fully-assembled setups to make troubleshooting more efficient.
- Ultimate goals are to ensure we have several bump-bonded assemblies which are well-understood to use in test-beam, and to provide feedback to IJCLab and OMEGA.