

From Novel Imaging Sensors to Advanced Tracking Devices

IJCLab
10/02/2025

FROM DELPHI AT LEP TO MIMOSIS AT FAIR AND BEYOND

Marc WINTER -- IJCLab (CNRS), Orsay, France
(20 years of R&D with the PICSEL team of IPHC-Strasbourg)



2024 ICFA Instrumentation Award

to

Walter Snoeys
Renato Turchetta
Marc Winter



for their vision and leadership in the development of low-mass and high-resolution particle physics detectors, based on commercial CMOS technology, the Monolithic Active Pixel Sensors (MAPS)



16th Pisa Meeting on Advanced Detectors, La Biodola – Isola d'Elba, 26 May -1 June, 2024

Monolithic CMOS pixel sensors for charged particle detection

CONTENT

- Introductory remarks on Semi-Conductor Pixel sensors
- The **proof of principle**: efficient detection of charged particles
- Establishing **charged particle tracking**
- **1st CMOS sensor based vertex detector** in a collider experiment
- Follow-ups: **ALICE-ITS2** at CERN-LHC and **CBM-MVD** at FAIR/GSI
- Kernel actors of > 20 years of CMOS sensors developpement
- Conclusion - Outlook

FROM HYBRID TO MONOLITHIC SENSORS

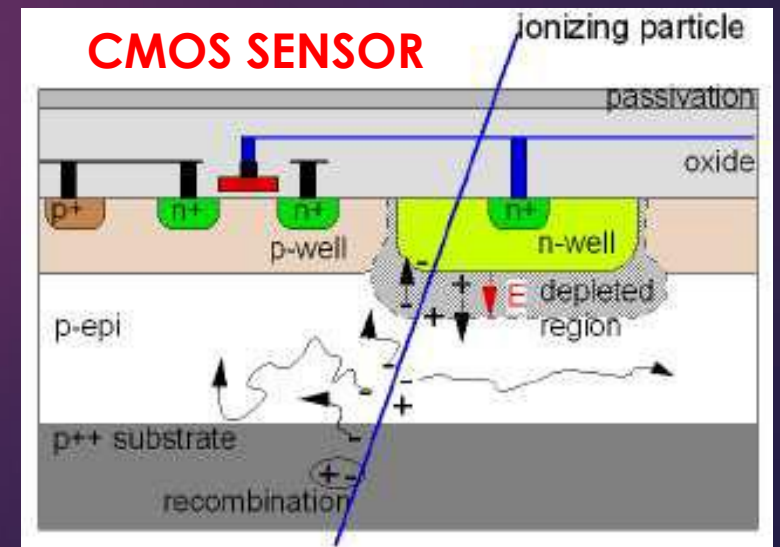
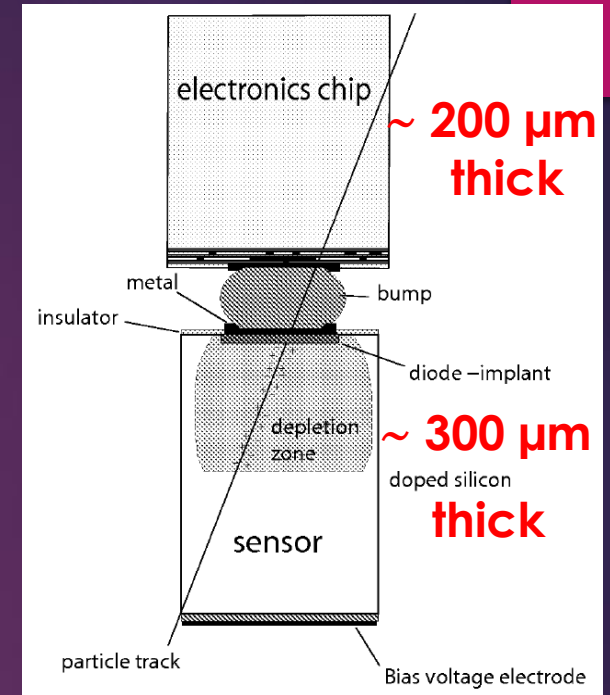
□ Limitations of Hybrid Pixel Sensors

- **Bump bonding** is expensive and is subject to industrial fabrication yield shortcomings (it is moreover fragile)
- Signal processing electronics is enough **power** consuming to require active cooling
 - **cooling pipes** on the way of particles to detect
- Electronics chips introduces substantial passive material on the way of the particles to detect
- Sensor is relatively thick
 - **material budget** (multiple scattering issue)
- **Pixels need to be relatively large** because of bump bonding and of read-out μ -circuit dimensions (e.g. in-pixel threshold dispersion correction)

→ HPS are not suited to high the precision physics programme anticipated at a future lepton collider

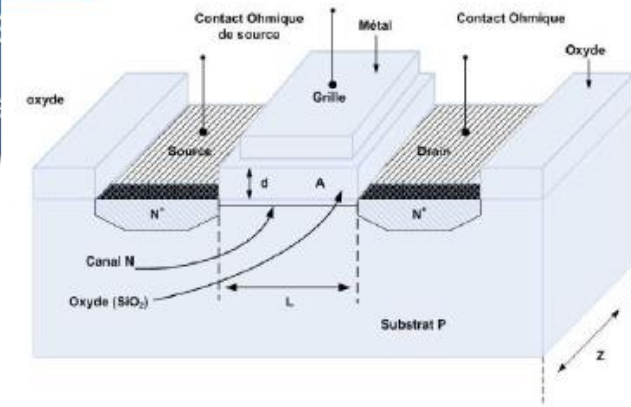
→ **SEARCH FOR MORE COMPACT AND TRANSPARENT PIXELATED STRUCTURE**

→ CDD too slow, needing cooling, radiation soft, ...



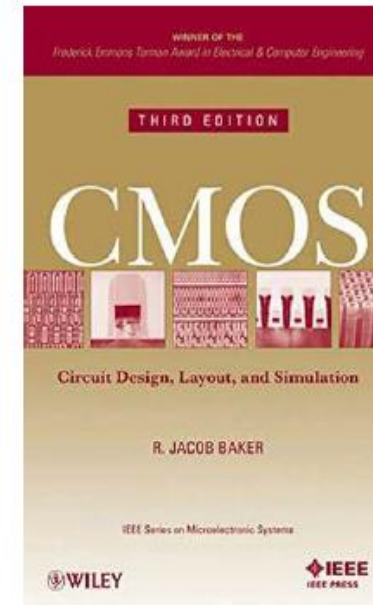
SEMI-CONDUCTOR DETECTORS: ORIGIN OF (MONOLITHIC) CMOS PIXEL SENSORS

- CMOS Pixel Sensors are derived from ASICS
 - ≡ Application-Specific Integrated Circuits
 - ASICs populate every day's life: e.g. credit cards, PC, cell-phones, cars, washing machines, ...
 - ⇒ industrial mass production item
 - (world revenue ~ several 100 billions USD/year)
 - key element: MOSFET transistors & conductive traces printed in **Silicon** (usually)



Substrat type P pour MOSFET canal N
Substrat type N pour MOSFET canal P

- C.M.O.S. ≡ Complementary Metal Oxyde Semi-conductor
 - widespread technology for constructing integrated circuits used in microprocessors, microcontrollers, memories, etc.

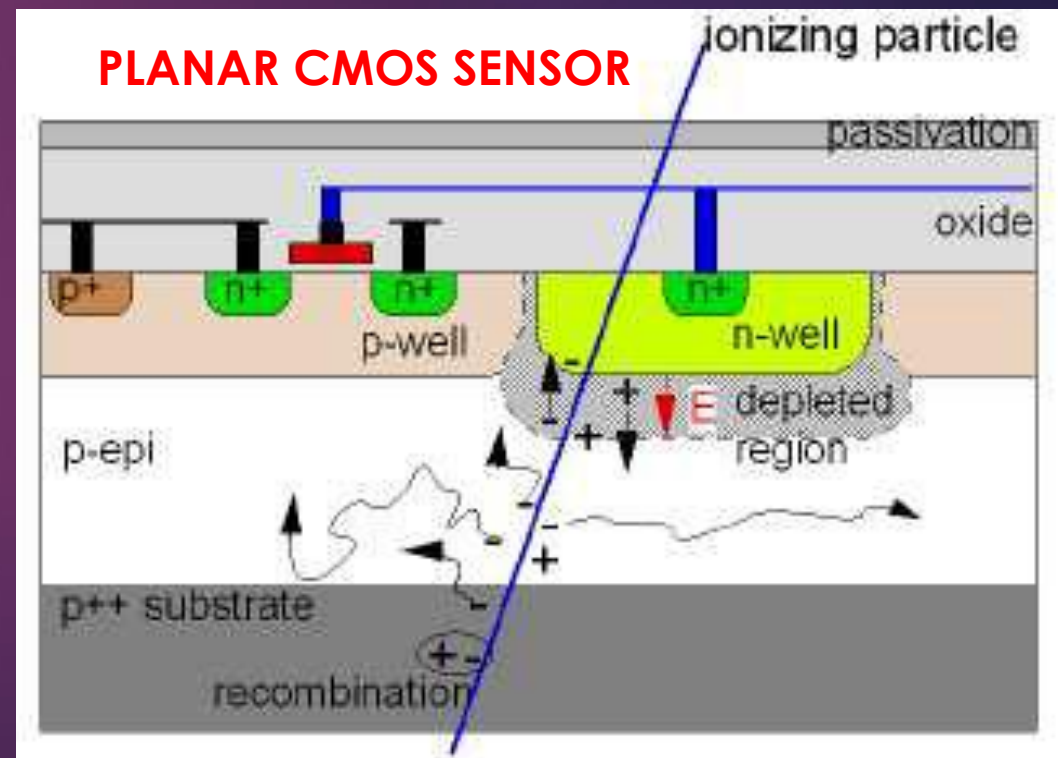




EMERGENCE AND RISE OF MAPS

INDUSTRIAL MONOLITHIC CMOS SENSORS: CONSTRAINTS

- ❑ First use of ASICs (Application Specific Integrated Circuits) for detection pioneered in the 1990's for light imaging (e.g. Eric Fossum et al. at NASA Jet Propulsion Lab)
- ❑ Industrial CMOS technology is not suited to particle detection by default:
 - Most commercial processes don't feature low doping epitaxial layer (= sensitive volume)
 - Thinning to $\sim 50 \mu\text{m}$ (default chip thickness is typically $700 \mu\text{m}$)
- ❑ First industrial CMOS process investigated: **AMS-0.6**
 - Feature size ($0.6 \mu\text{m}$) \equiv precision of lithography
 - dictates the transistor gate dimension
 - restricts the density of μ -circuits inside pixels
 - Planar process: only NMOS transistors may be integrated inside pixels since PMOS transistors would require dedicated n-wells, which would act as parasitic charge sensing nodes
 - restricted μ -circuitry inside pixels
 - EPI: $14 \mu\text{m}$ thick $\rightarrow \sim 1000 e^-$ signal charge
low resistivity \rightarrow thermal diffusion of signal e^-



ESTABLISHING A PROOF OF PRINCIPLE

LEP/e+e- coll./HF tagging with HAPS:
 Delphi: 200x200 μm^2 ; > 1% X0, > 1 W/cm²



> join TESLA collider project on VD (F.Richard)
 > contact LEPSI-Strasbourg: **Renato Turchetta**



March '99: 1st talk on MAPS for a VD
 at ECFA-LC workshop in Oxford

MIMOSA-1: fabricated in 2000 with
 AMS-0.6 μm commercial CMOS process

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI technology, NIM A458 (11 Feb. 2001), pp 677-689

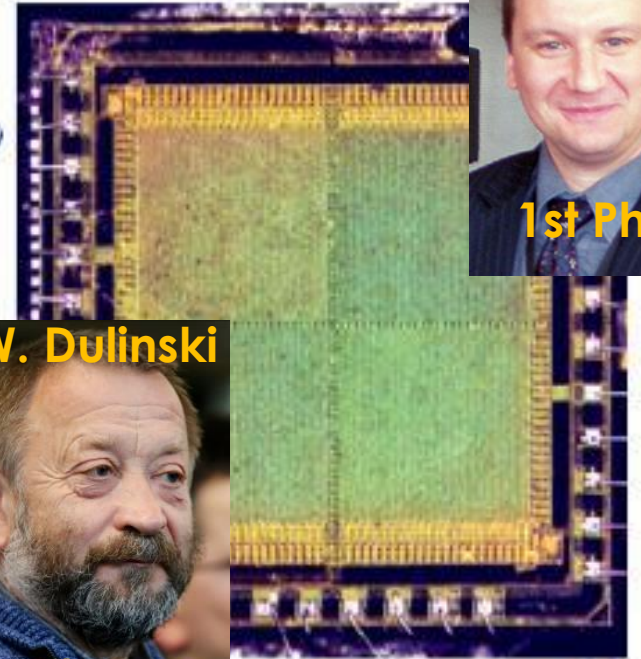
Simulation and Measurements of Charge Collection in Monolithic Active Pixel Sensors

Gregory Deptuch
 deptuch@epi.aps.fr

MIMOSA I (Minimum Ionising particle MOS Active pixel detector)

Goal of fabrication:

- feasibility study
- understanding/tests
 - standard 0.6 μm CMOS ($t_{ox}=12.7\text{nm}$)
 - 14 μm thick EPI layer (10^{14}cm^{-3})
 - 4 arrays 64x64 pixels
 - pixel pitch 20x20 μm
 - diode (nwell/pepi) size 3x3 μm - 3.1fF
 - readout clock $f < 10\text{MHz}$
 - readout - serial analog
 - die size 3.6x4.2mm²



G. Deptuch

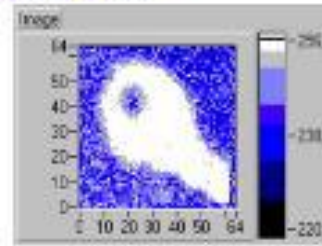


1st PhD

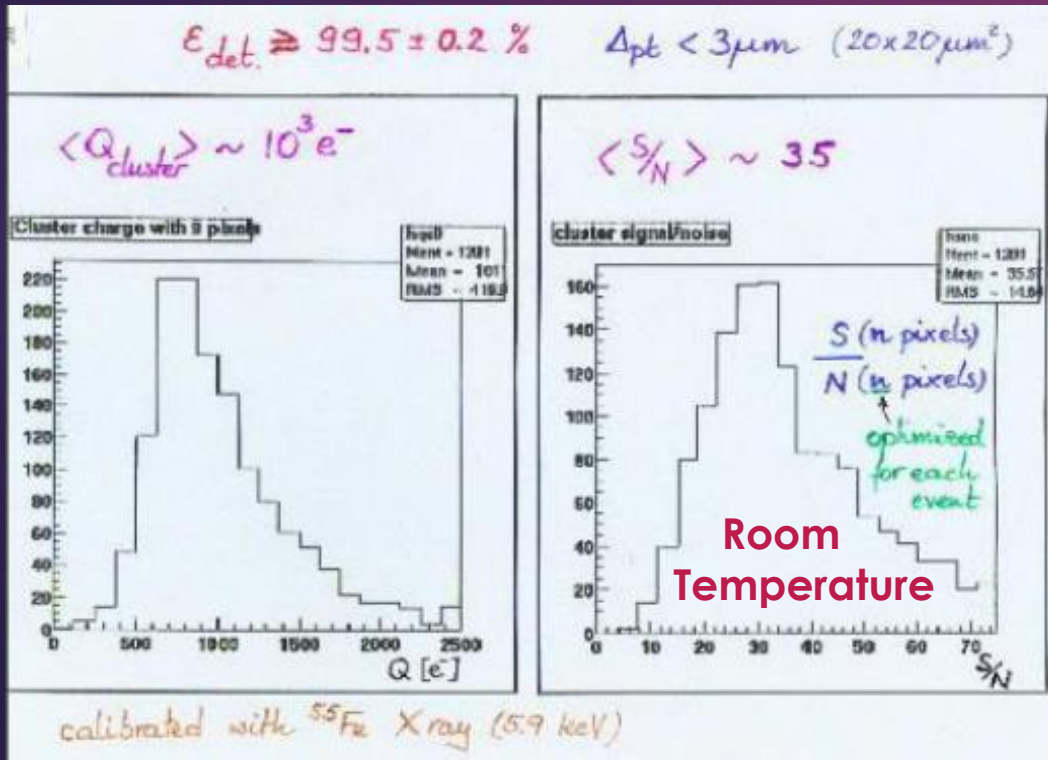
W. Dulinski



† '14



"Visible light photography with MIMOSA"



ESTABLISHING A PROOF OF PRINCIPLE



N° d'ordre : 4091

École Doctorale Physique, Chimie physique et Mathématiques
ULP – IReS – LEPSI et UMM

THÈSE

présentée pour obtenir le grade de

Docteur de l'Université Louis Pasteur – Strasbourg
Discipline : Physique (42000 02)
Spécialité : Micro-capteurs et leur électronique intégrée

par

Grzegorz DEPTUCH

Développement d'un capteur de nouvelle génération et son électronique intégrée pour les collisionneurs futurs

New Generation of Monolithic Active Pixel Sensors for Charged Particle Detection

Soutenue publiquement le 20 septembre 2002

Membres du jury

Directeur de thèse : M. Ulrich Goerlach, professeur, ULP Strasbourg, France
Codirecteur de thèse : M. Stanislaw Kuta, professeur, UMM Krakow, Pologne
Codirecteur de thèse : M. Renato Turchetta, docteur, RAL Didcot, UK
Rapporteur interne : M. Daniel Mathiot, professeur, ULP Strasbourg, France
Rapporteur externe : M. Christopher J.C. Damerell, professeur, RAL Didcot, UK
Rapporteur externe : M. Wojciech Kucewicz, professeur, UMM Krakow, Pologne
Rapporteur externe : M. Ryszard Wojtyna, professeur, ATR Bydgoszcz, Pologne
Examineur : M. Veljko Radeka, docteur, BNL Upton NY, USA
Examineur : M. Pierre Jarron, docteur, CERN Genève, Suisse
Examineur : M. Tadeusz Pisarkiewicz, professeur, UMM Krakow, Pologne

IReS UMR 7500
LEPSI EA N°3425

UMM Krakow



G. Deptuch



A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI technology, NIM A458 (11 Feb. 2001), pp 677-689

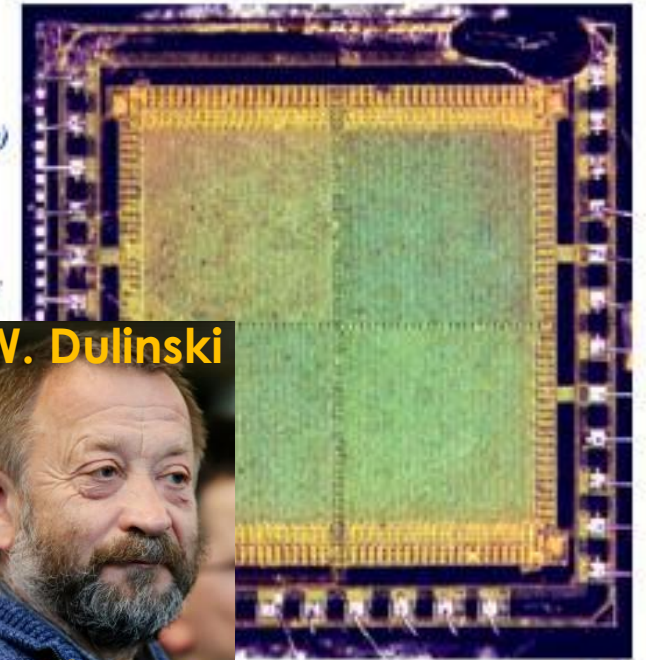
Simulation and Measurements of Charge Collection in Monolithic Active Pixel Sensors

Grzegorz Deptuch
deptuch@epi.ulp.fr

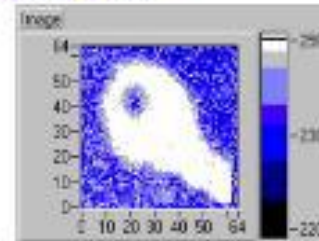
MIMOSA I (Minimum Ionising particle MOS Active pixel detector)

Goal of fabrication:

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- understanding/tests
 - standard $0.6\mu\text{m}$ CMOS ($t_{ox}=12.7\text{nm}$)
 - $14\mu\text{m}$ thick EPI layer (10^{14}cm^{-3})
 - 4 arrays 64×64 pixels
 - pixel pitch $20\times 20\mu\text{m}$
 - diode (nwell/pipi) size $3\times 3\mu\text{m} - 3.1\text{fF}$
 - readout clock $f < 10\text{MHz}$
 - readout - serial analog
 - die size $3.6\times 4.2\text{mm}^2$



W. Dulinski



Visible light photography with MIMOSA I



ESTABLISHING A PROOF OF PRINCIPLE

SUCIMA
EU-FP5
project

MIMOSA-5
Fab. In 2003

P.I. M. Caccia

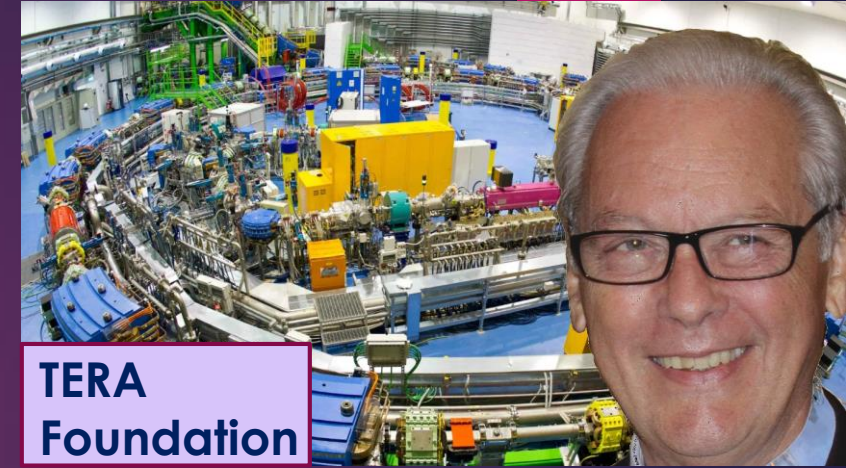


SUCIMA for TERA: Hadrontherapy

MIMOSA-5 = proton beam monitor

CMOS technology:

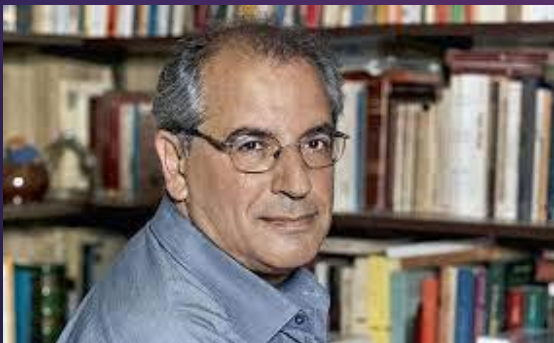
- AMS 0.6 μm feature size
- 14 μm thin sensitive volume
- planar: only NMOS T inside pixels



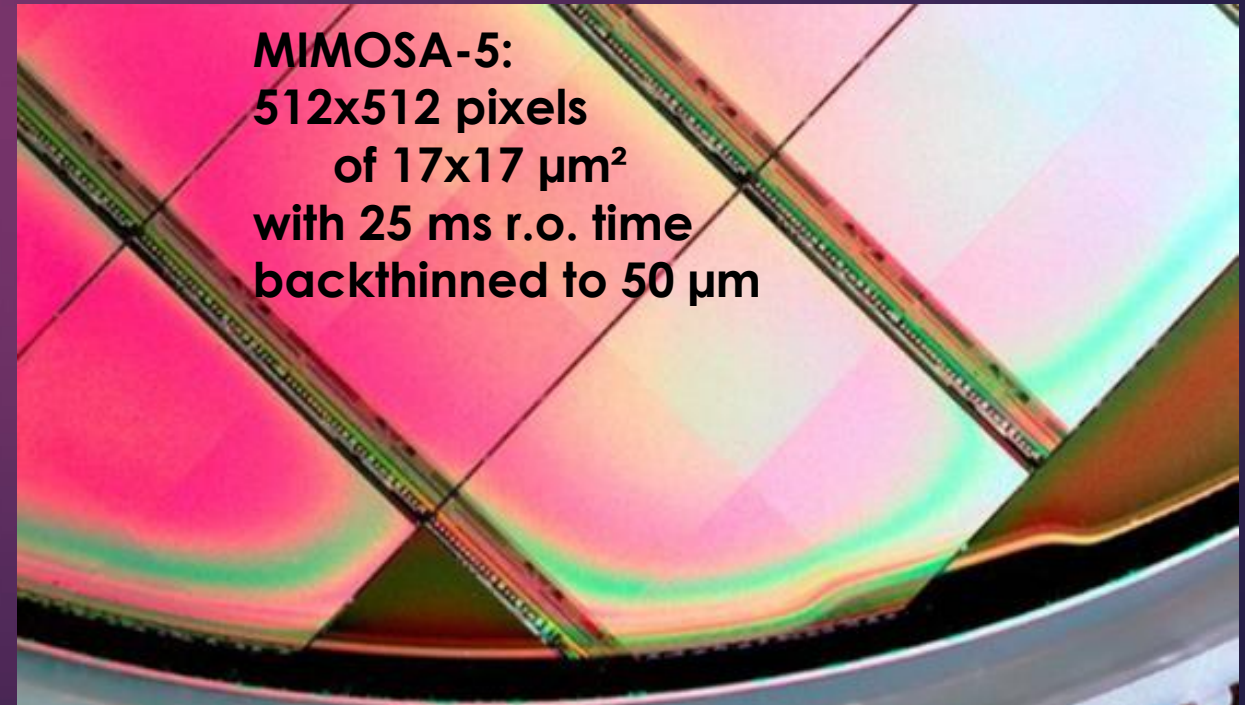
Numerous spin-off
applications



S. Katsanevas † '22



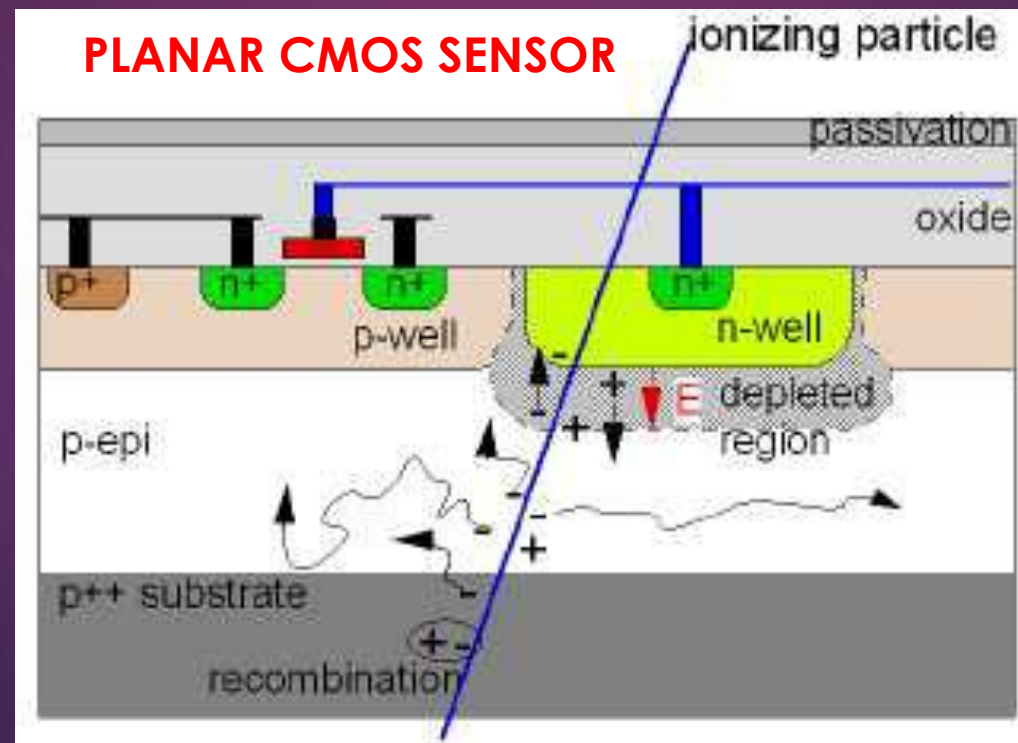
MIMOSA-5 in HPD
Photonis / Antares



MIMOSA-5:
512x512 pixels
of 17x17 μm^2
with 25 ms r.o. time
backthinned to 50 μm

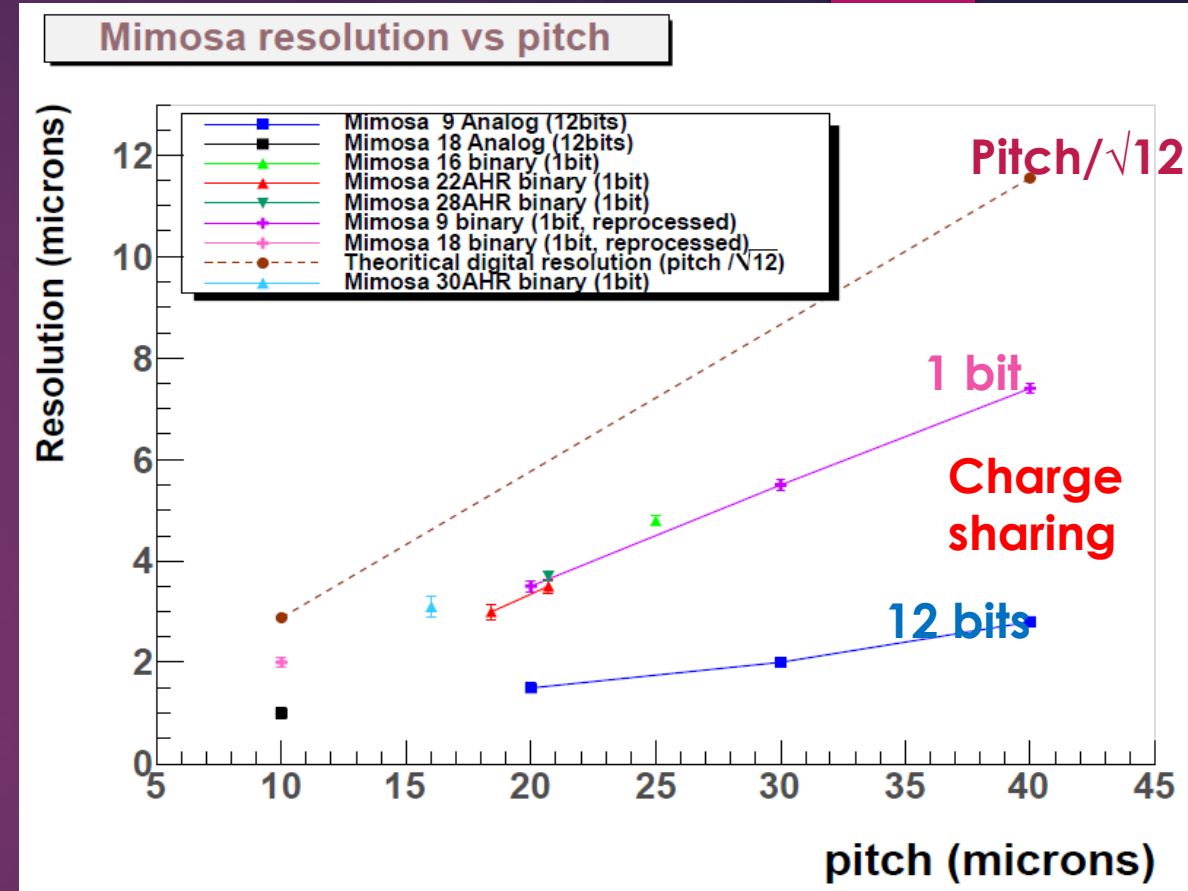
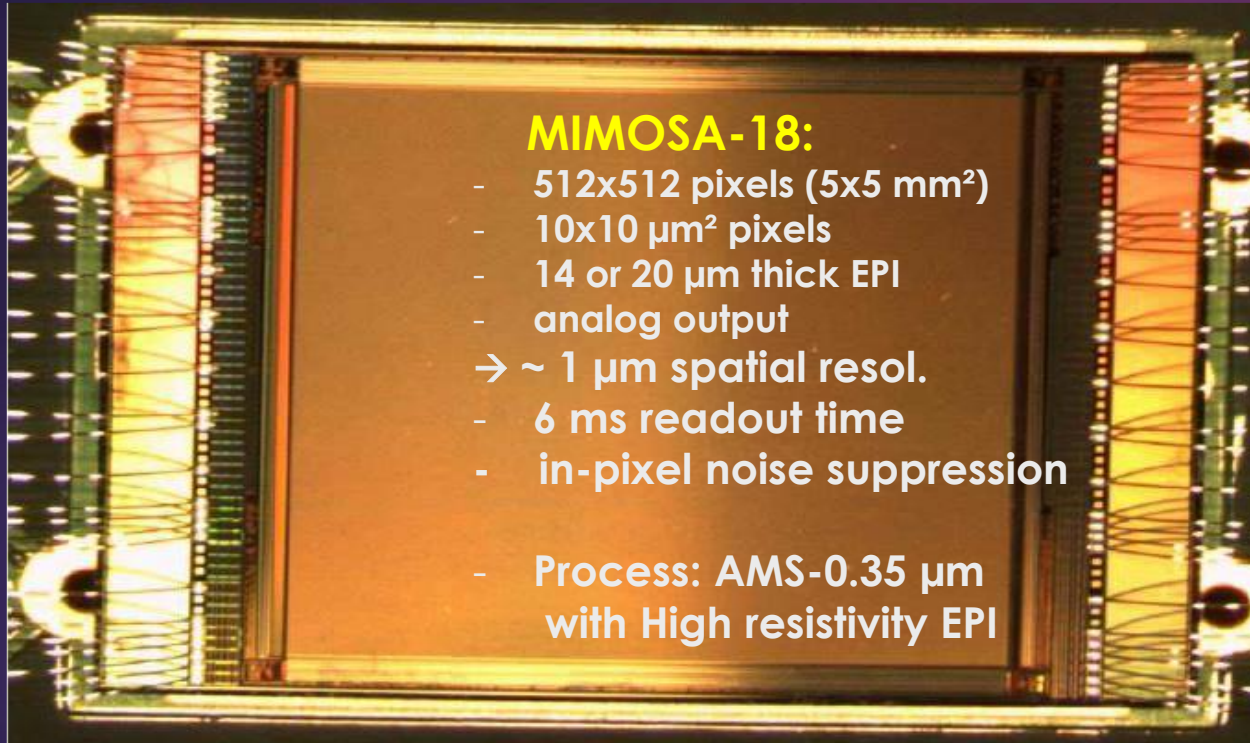
INDUSTRIAL MONOLITHIC CMOS SENSORS: 2nd GENERATION

- Second industrial CMOS process used: **AMS-0.35**
 - Still a planar process
 - Feature size (0.35 μm) allowed to integrate noise-suppression μ -circuits inside pixels
 - correlated double-sampling
 - EPI: 12 & 15 μm thick → $\sim 10^3$ e- signal charge
 - low resistivity → thermal diffusion of signal e-



ESTABLISHING CHARGED PARTICLE TRACKING

Achieving micron level spatial resolution



$O(1)$ μm resolution exploiting charge sharing with read-out time > 1 ms (4 sub-arrays read out in //)

But a Higgs-Factory Vertex Detector requires < 10 μs

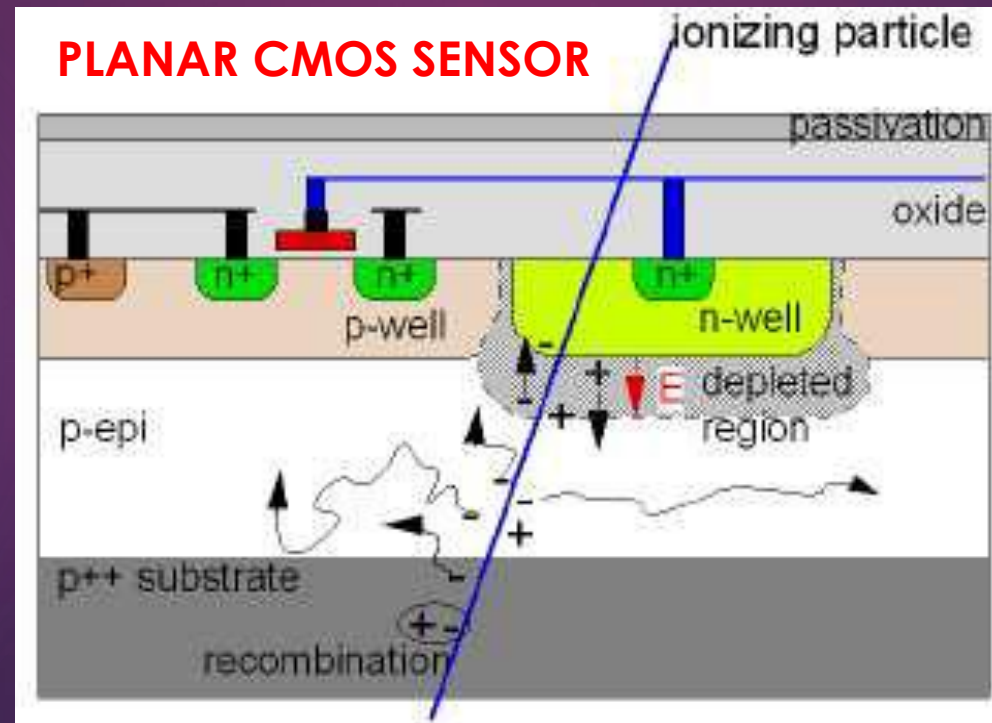
→ much more // read-out necessary

→ less bits for charge encoding mandatory

INDUSTRIAL MONOLITHIC CMOS SENSORS: 3rd GENERATION

- Second industrial CMOS process used: **AMS-0.35**
 - Still the same planar process
 - Same integrated μ -circuitry as previously
 - EPI: 12 & 15 μm thick $\rightarrow \sim 10^3$ e- signal charge
 - high resistivity** \rightarrow part of signal e- collected by drift \rightarrow enhanced seed pixel signal
 - \rightarrow improved radiation tolerance
 - \rightarrow improved cluster multiplicity

400 – 800 $\Omega\cdot\text{cm}$ \rightarrow

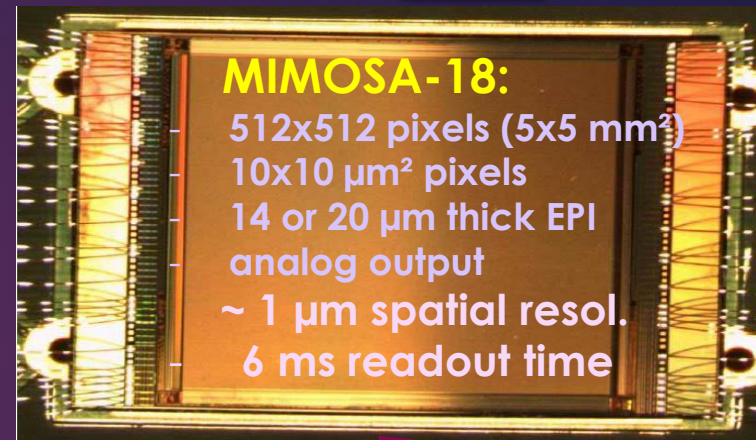


ESTABLISHING CHARGED PARTICLE TRACKING

EUDET: 6th Framework Programme of E.U.: MAPS for Beam Telescope

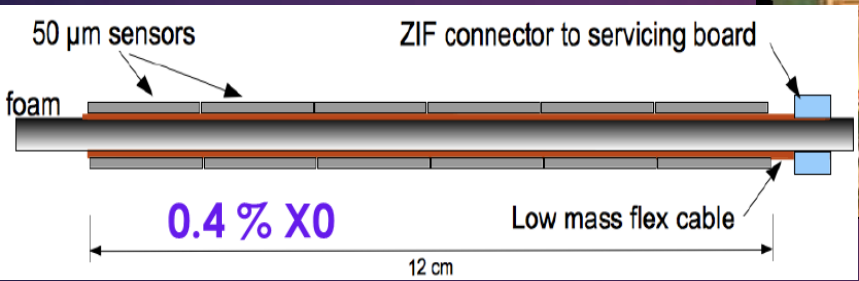
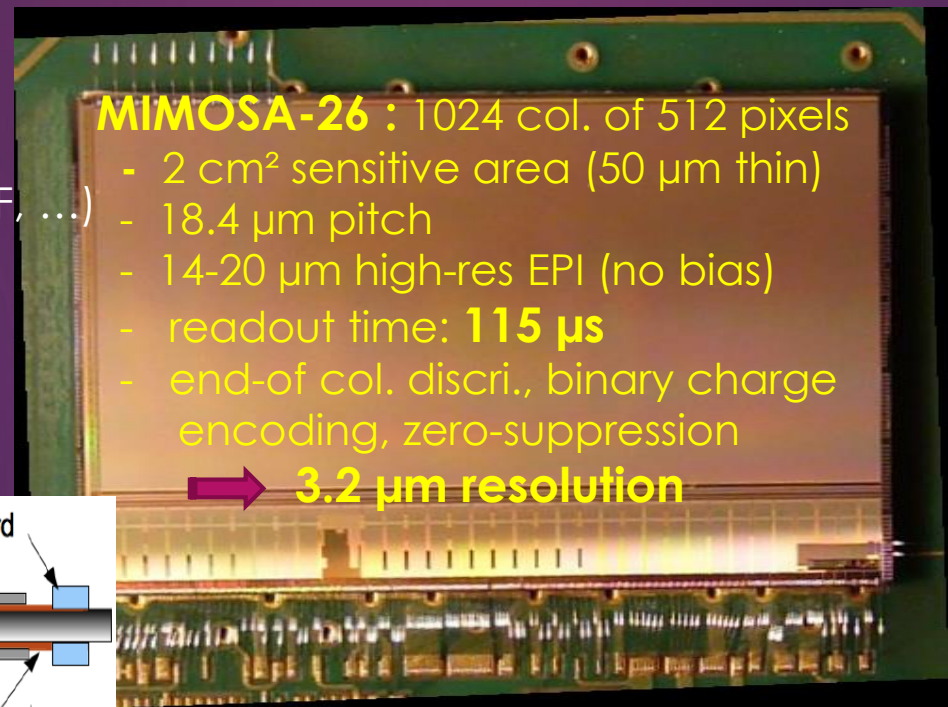
Introducing on-chip signal discrimination & 1 bit charge encoding

- MIMOSA-8 proto. (TSMC-0.25): 2004/5 end of col. discri. (Yavuz Degerli/Irfu)
- MIMOSA-16/22 proto. (AMS-0.35 OPTO)
- MIMOSA-26 final sensor (EUDET-FP6): High resolution beam telescope



Numerous applications:

- > 10 BT (DESY, CERN, SLAC, TRIUMF, ...)
- Fixed target expts (NA61, ...)
- Hadrontherapy
- Industrial imager
- Research in biology
- PLUME 2-sided ladder



MIMOSA-26/-28 GEOGRAPHICAL DISTRIBUTION



APPLICATION TO A VERTEX DETECTOR

COMPOSING A COLLIDER EXPERIMENT

STAR
AMS-0.35

A new Inner Vertex Detector for STAR

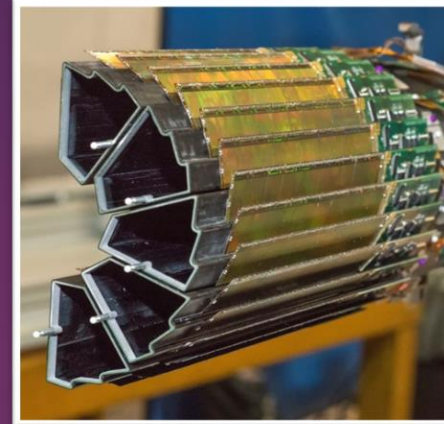
H. Wieman
Vertex 2000



MONOLITHIC ACTIVE PIXEL SENSORS FOR A LINEAR COLLIDER

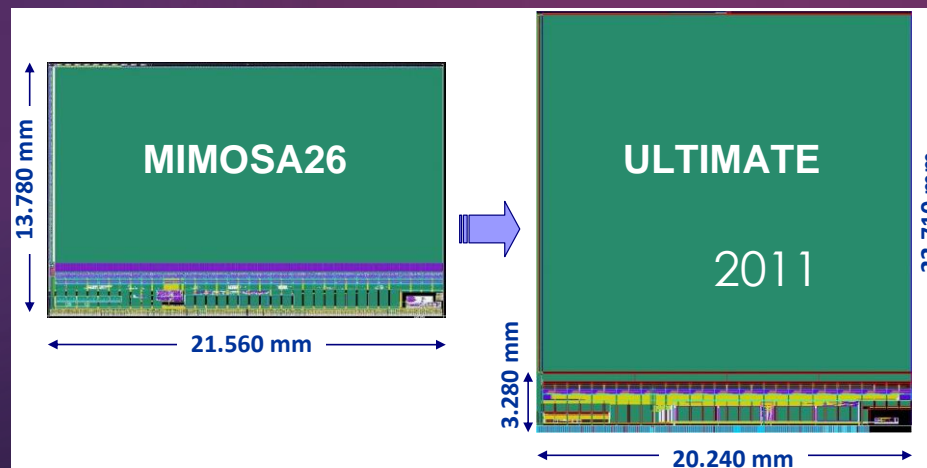
(Marc WINTER - IReS (Strasbourg))
on behalf of IReS+LEPSI coll.

- ▶ Physics Motivations
- ▶ Principle of Operation of M.A.P.S.
- ▶ Characteristics of 1st MAPS prototype
- ▶ Beam test Results (preliminary)
- ▶ Outlook

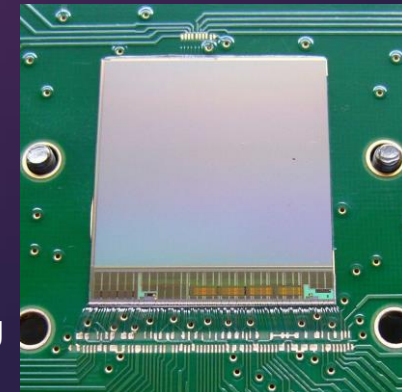


Data taking campaigns:
2014 & 2015

STAR-PXL: 2 layers (~ 0.4 % X0/layer),
400 ULTIMATE sensors (1600 cm²),
back-thinned to 50 μm
170 mW/cm², air-cooled (10 m/s)



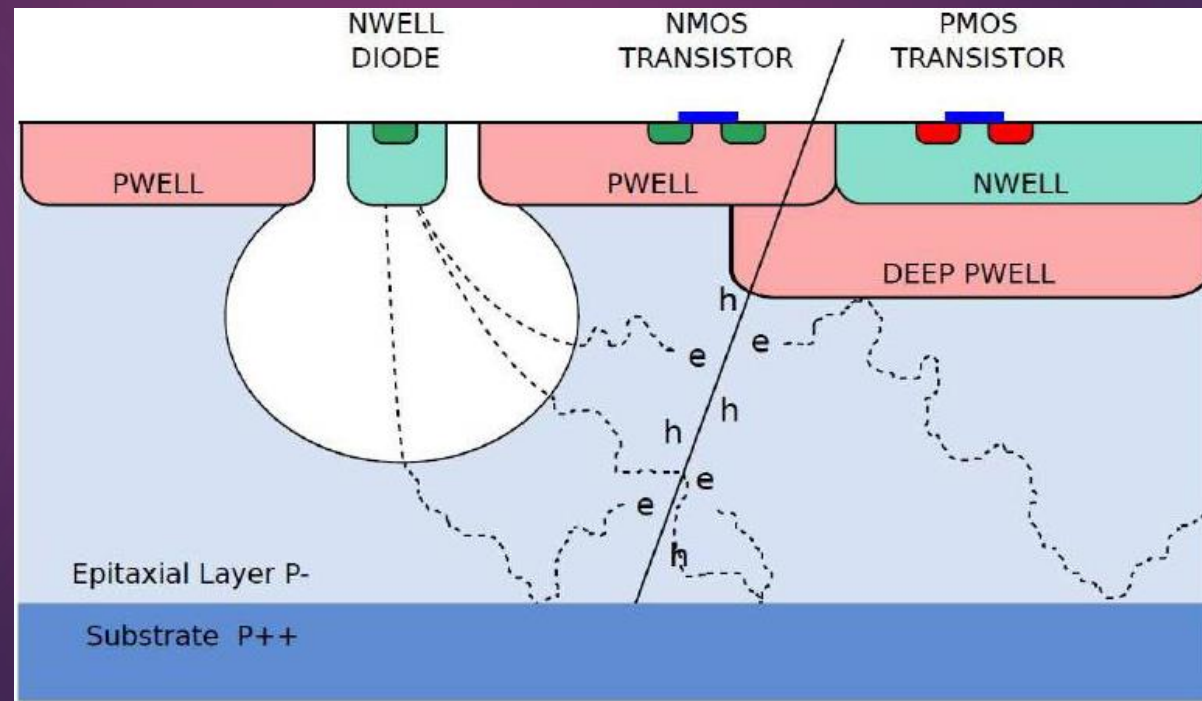
AMS-0.35 OPTO (twin-well process)
Customised EPI: 15 μm, **High Res.**
960 x 928 pixels (pitch = 20.7 μm)
Spatial resolution < 4 μm
Readout time: 185 μs
In-pixel Amp. & Corr. Dble Sampling
Deep Reactive Ion Etching (DRIE)



INDUSTRIAL MONOLITHIC CMOS SENSORS: 4th GENERATION

- Third industrial CMOS process used: **TSMC-0.18** (Tower-Jazz CIS)
 - INMAPS process pioneered by Renato Turchetta at RAL
 - Quadruple well technology → in-pixel N-MOS and P-MOS transistors
→ more in-pixel functionalities or smaller pixels with less μ -circuits
 - EPI: thickness of 18/25/30/40 μm → up to $2.5 \cdot 10^3$ e- signal charge
 - high resistivity** → **substantial part of signal** e- collected by drift
 - fast charge collection, enhanced radiation tolerance
 - reduced cluster multiplicity → degraded spatial resolution

> 1 $\text{k}\Omega\cdot\text{cm}$ →



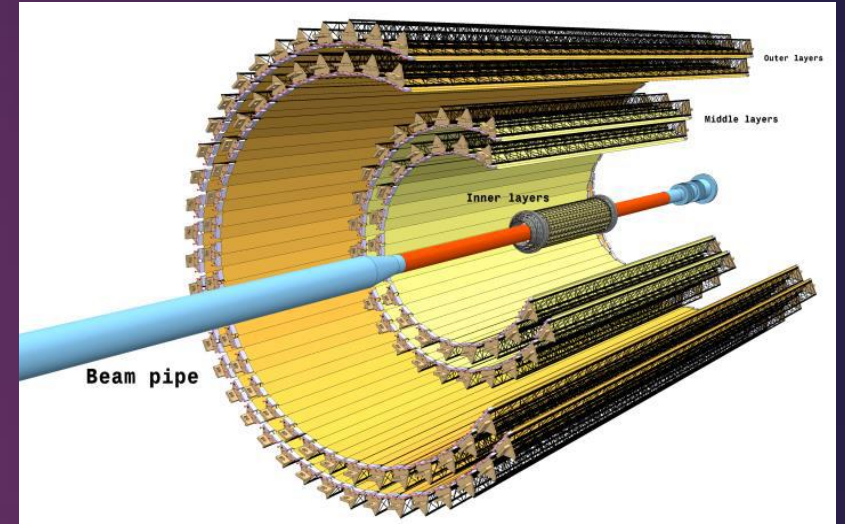
APPLICATION TO AN INNER TRACKER

COMPOSING A COLLIDER EXPERIMENT

ALICE
TJsc-0.18

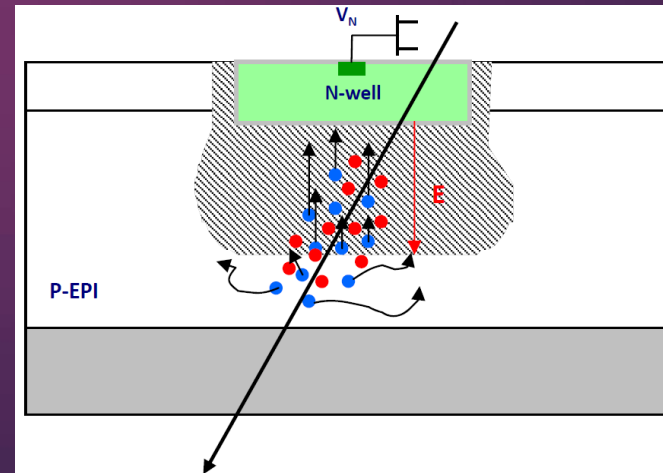
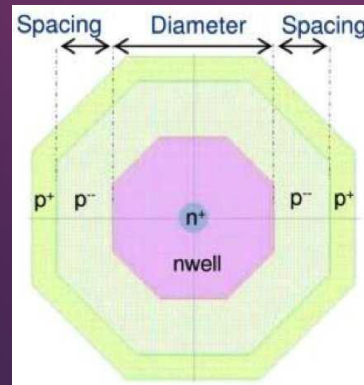
2010/11: proposal to consider CMOS pixel sensors for the upgrade of the ALICE vertex detector, based on the same readout architecture (**rolling shutter**) as MIMOSA-26/-28, customised for the ALICE physics goal & more demanding running conditions

ALICE coll. approved the proposal in 2011/12, promoted by Luciano Musa, who extended the concept to the whole ITS (10 m²)



PICSEL Team (IPHC-Strasbourg):

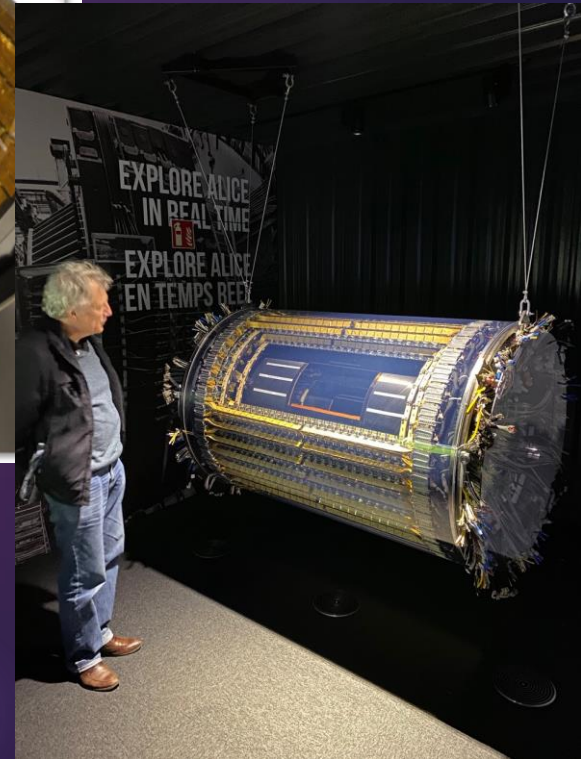
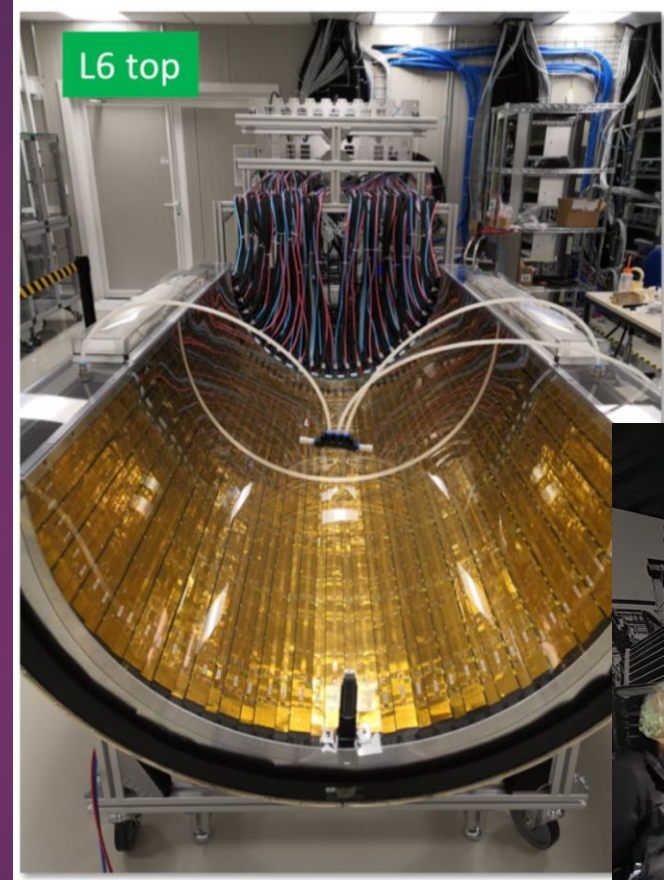
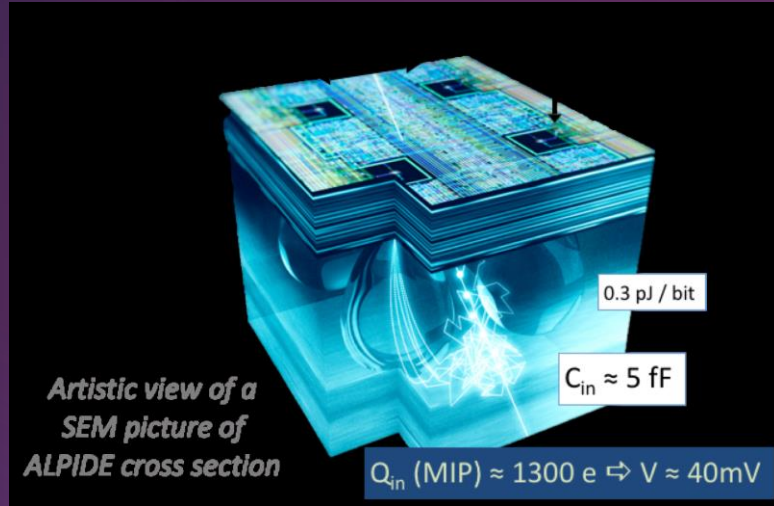
- extensive study of the techno. charge collection & sensing node characteristics
 - find out an **optimal sensing system** (EPI, diode, etc.)
 - MISTRAL (ASTRAL):
 - rolling shutter, column // read-out
 - end-of-column discriminators
- 30 (15 ?) μ s read-out time, power \leq 200 mW/cm²



AIDA – FP6 EU support

APPLICATION TO AN INNER TRACKER COMPOSING A COLLIDER EXPERIMENT

ALICE
TJsc-0.18



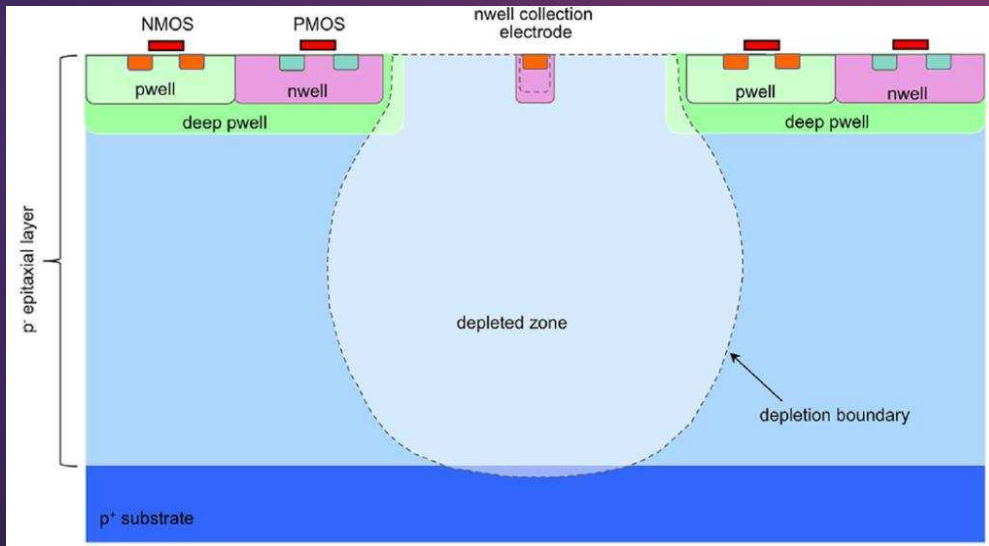
CERN Team (Walter Snoeys & coll.): ALPIDE sensor

- design based on hybrid pixel sensor read-out architecture
 - in-pixel discriminator, priority encoding, active EPI depletion
 - advantage:
 - suppressed power consumption : $\leq 50 \text{ mW/cm}^2$
 - faster read-out : $\leq 10 \mu\text{s}$
 - improved radiation tolerance
 - less periphery (insensitive) area devoted μ -cricuits
 - ...
- 24120 sensors ($\sim 12.5 \text{ Gpixels}$) equipping $\sim 10 \text{ m}^2$

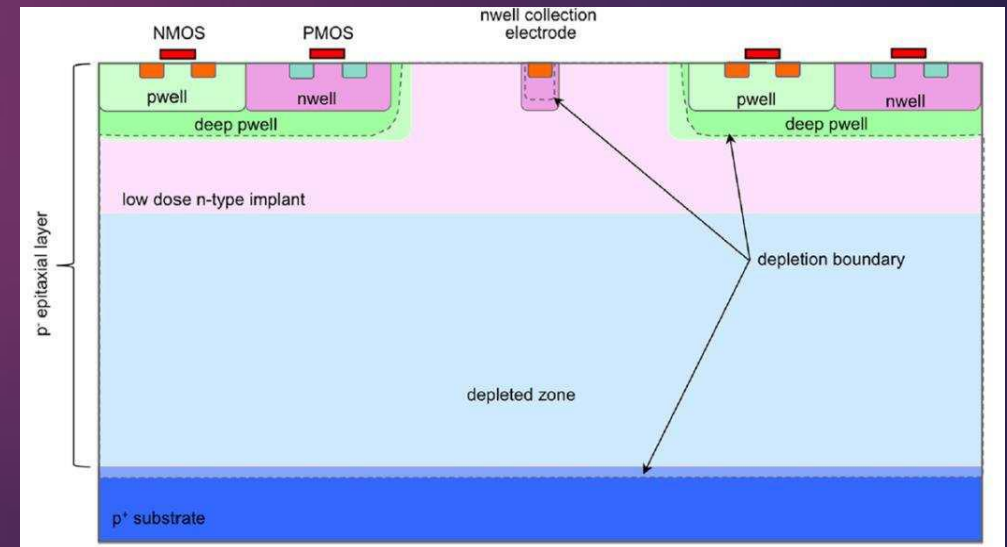
INDUSTRIAL MONOLITHIC CMOS SENSORS: 5th GENERATION

- ❑ Third industrial CMOS process used: **TSMC-0.18** (Tower-Jazz CIS)
- ❑ EPI: **foundry accepted to modify the doping profile** (film of n-type dopant introduced on top of EPI)
 - drift field extended laterally underneath sensing nodes
 - benefit: faster charge collection, enhanced radiation tolerance
 - drawback: reduced cluster multiplicity → somewhat degraded spatial resolution

Standard EPI



Modified EPI profile
(introduced by Walter S.)



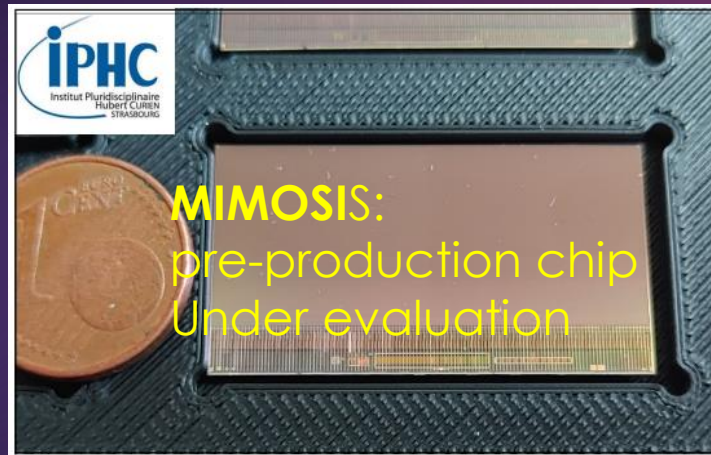
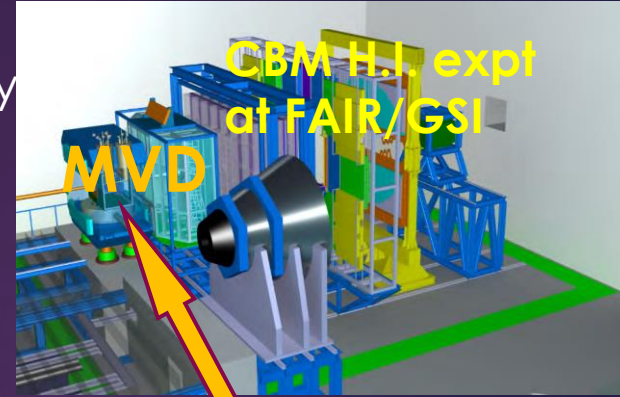
APPLICATION TO A VERTEX DETECTOR

COMPOSING A FIXED TARGET EXPERIMENT

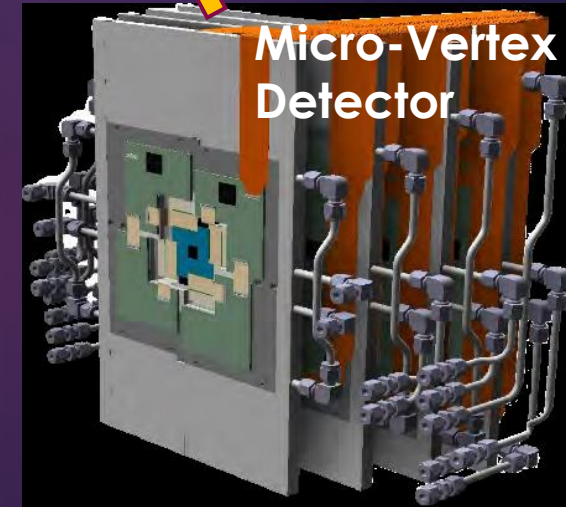
CBM
TJsc-0.18
modified

March 2003: 1st seminar on CMOS pixel sensors at GSI (invited by H. Gutbrod)
CBM \equiv H.I. fixed target expt \rightarrow Micro-Vertex Detector faces very high hit density
 \rightarrow more demanding running conditions than ALICE-ITS2

Stretched timeline allowed to benefit from evolution of CMOS industry
(Tower-Jazz 180 nm) and progress on CMOS sensor design (ALPIDE, mod. EPI)



Priority encoder & pixel design
derived from ALPIDE EPI layer
doping profile modified for
improved radiation tolerance



20 yrs of steady support and trust
from GSI / Darmstadt &
Univ. Goethe / Frankfurt, with
highly appreciated collaborators



EXTENSIVE STUDY OF KEY PARAMETERS RULING CHARGED PARTICLE DETECTION

PICSEL:
Physics
with
Integrated
CMOS
Sensors
and
Electron
machines



Support from IN2P3/CNRS Dir.:

→ PICSEL & CMOS sensor devt:

- ≈ 10 engineer positions created
- ≥ 6 post-docs, 2 phys. positions
- funding: foundry submissions, test equipment

& Support from IPHC-Strasbourg

Strasbourg **PICSEL** team (≤ 25 FTE):
3-5 physicists, O(10) ASIC designers,
4-5 electronics, ≤ 5 PhD students
> 20 PhDs on CMOS sensor R&D

Essential Partners (incomplete):

- Irfu-CEA (Y.Degerli): end-of-col. discri. (MIMOSA-8)
- DESY/Univ.Hamburg (I.Gregor): EUDET Beam Tel., AIDA
- STAR coll. (Berkeley, BNL): STAR-PXL/HFT
- Univ. Frankfurt (J.Stroth), GSI: CBM-MVD, Hadron-Physics-2
- ALICE-ITS2/CERN (L.Musa): → ALPIDE (Walter S.)

Charge collection & signal sensing:

- EPI: thickness, resistivity doping profile
- junction: dimensions, insulation
- depletion: top vs back vs field amplitude
- impact of/on pixel dimensions
- ISE/TCAD simulations

In-pixel signal processing:

- pre-amp T: size & shape vs gain & RTS
- noise suppression: double-corr. sampling, ...
- junction to preamp: DC vs AC

Read-out architecture:

- charge encoding: binary, ADC (4-5 bits, ...)
- zero-suppression, elastic buffering, ...)

Particle detection performance assessment:

- lab tests: noise, steering param., threshold dispersion, ...
- beam test: det. eff., cluster characteristics, spatial resol.
- radiation tolerance assessment: TID, NIEL, SEE, ...

Determination of requirements:

- ILC vertex detector and inner track
- optimisation of conflicting design param.
- investigate charge coll. system variants

Comparison of CMOS processes:

- impact of feature size, design rules, IP μ circuits
- planar vs triple-well vs quadruple-well
- nb of ML
- intrinsic radiation tolerance

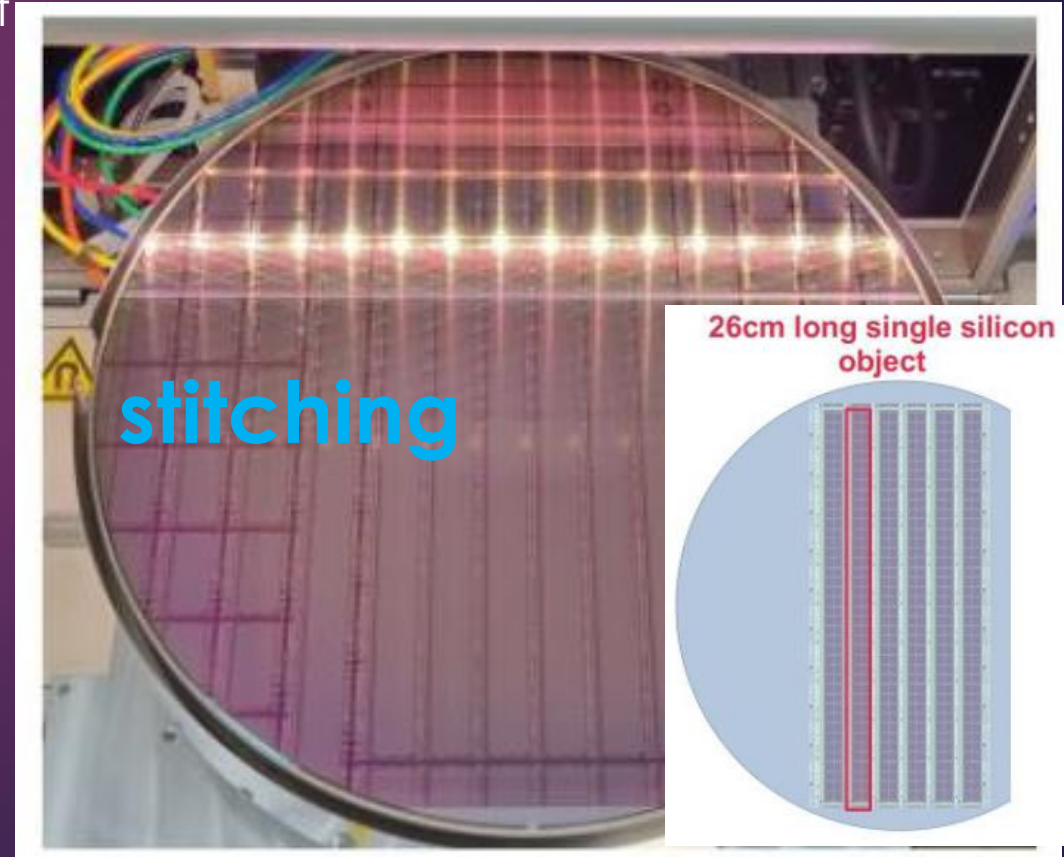
INDUSTRIAL MONOLITHIC CMOS SENSORS: 6th GENERATION

- ❑ Fourth industrial CMOS process used: **TPSco-65**
 - Access based on close contact between CERN (Walter Snoeys) and Tower-Jazz foundry
 - Feature size : 65 nm ($V_{ref} = 1.2$ V)
 - Quadruple well technology → in-pixel N-MOS and P-MOS transistors
→ feature size: 65 nm
 - EPI thickness: less than with previous CMOS processes → **modest (< 1000 e-) signal charge**
 - **high resistivity** → **nearly all signal e-** collected by drift
 - fast charge collection, enhanced radiation tol.
 - BUT smallest cluster multiplicity
 - degraded spatial resolution
 - partially recovered with smaller pixels ?

New step toward passive material suppression →



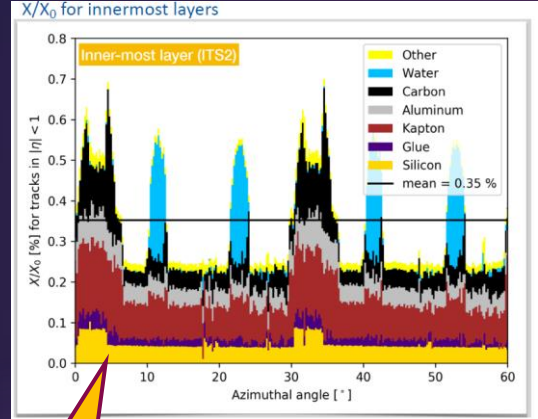
Flagship: **ALICE-ITS3 Vertex Detector**



FLAGSHIP PROJECTS BASED ON CMOS SENSORS

**FUTURE
TPSco 65 ?**

ALICE-ITS2 material budget.

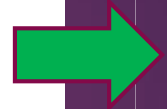
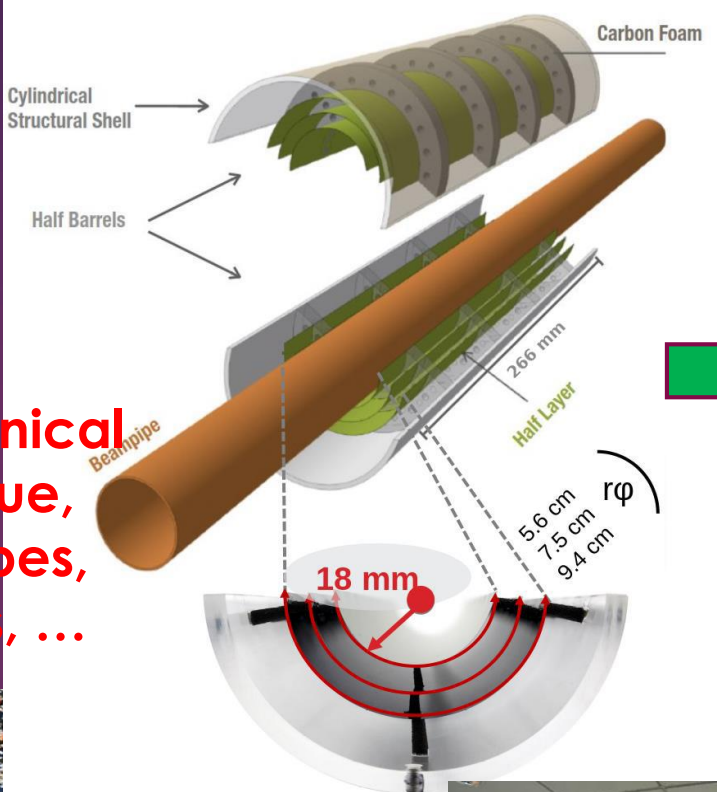


Most material is passive (services)

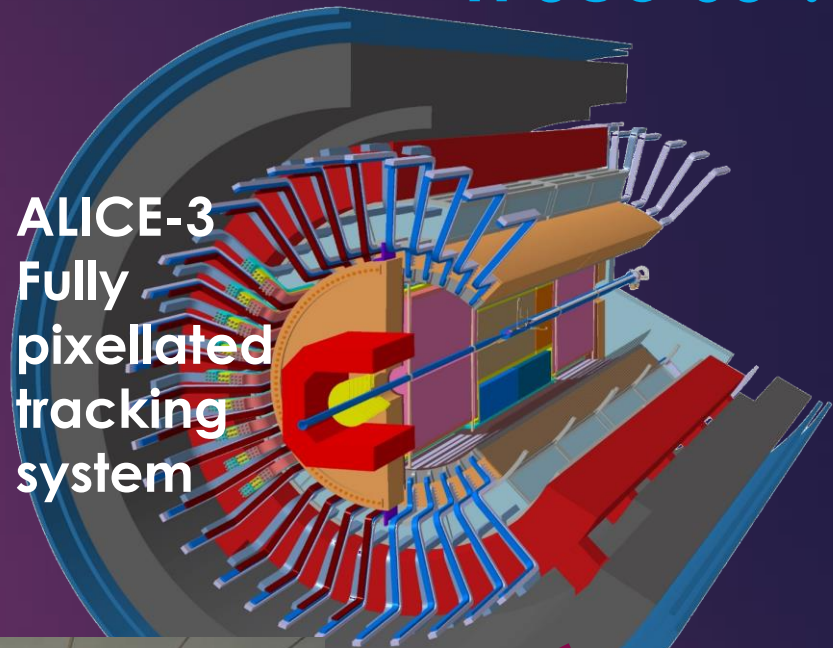
Si

ITS3

NO mechanical support, glue, cooling, pipes, flex cables, ...



**ALICE-3
Fully
pixellated
tracking
system**



**ECFA
DRD-3**

**Expts at
a future
lepton
collider**

CONCLUSION & OUTLOOK

My involvement in the birth and devt of CMOS pixel sensors for charged particle tracking stems from an **idea proposed by Renato T.** and benefited from **R&D realised/supervised by Walter S.**

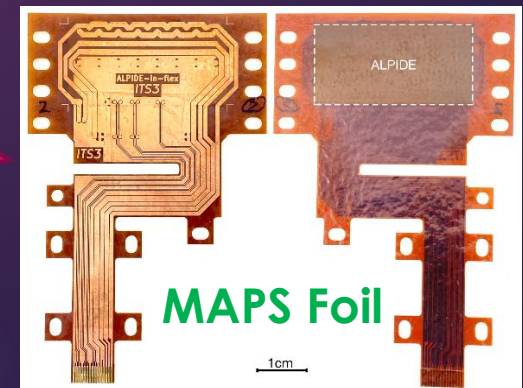
Monolithic CMOS Pixel Sensors for charged particle tracking are born 25 years ago. They have evolved in numerous aspects, relying on an industrial market which was not anticipated to preserve characteristics essential for charged particle detection

Toward a future (e+ e-) Higgs Factory:

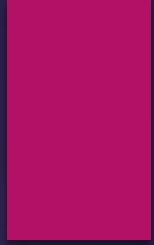
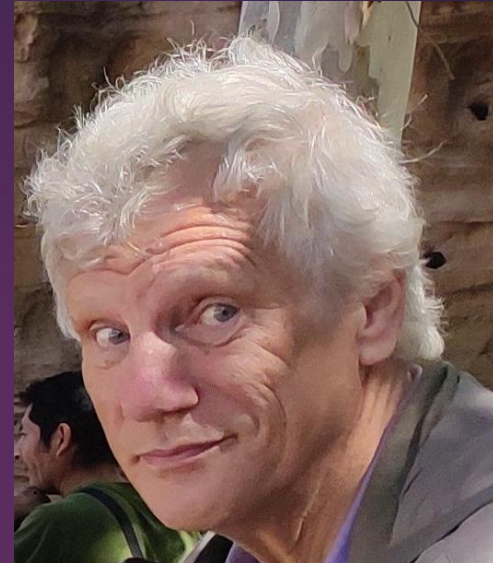
- the challenge is still to concentrate in a single, thin, low power sensor the ambitionned spatial and time resolution
- on-going & emerging projects pave a promissing path:
CBM-MVD (& STS upgrade), ALICE-ITS3 (& eIC expts), Belle-II ?, ALICE-3
-

Numerous pending questions:

- which CMOS technology: TPSCo 65 nm ?, XXX 28 nm ? ... or TJsc 180 nm ?
- with/without stitching (e.g. what about sensors embedded in mylar foils ?)
- why restricting to processes featuring an EPI layer ?
- what about stacked sensors ?
- etc.



THANK YOU FOR
YOUR ATTENTION !

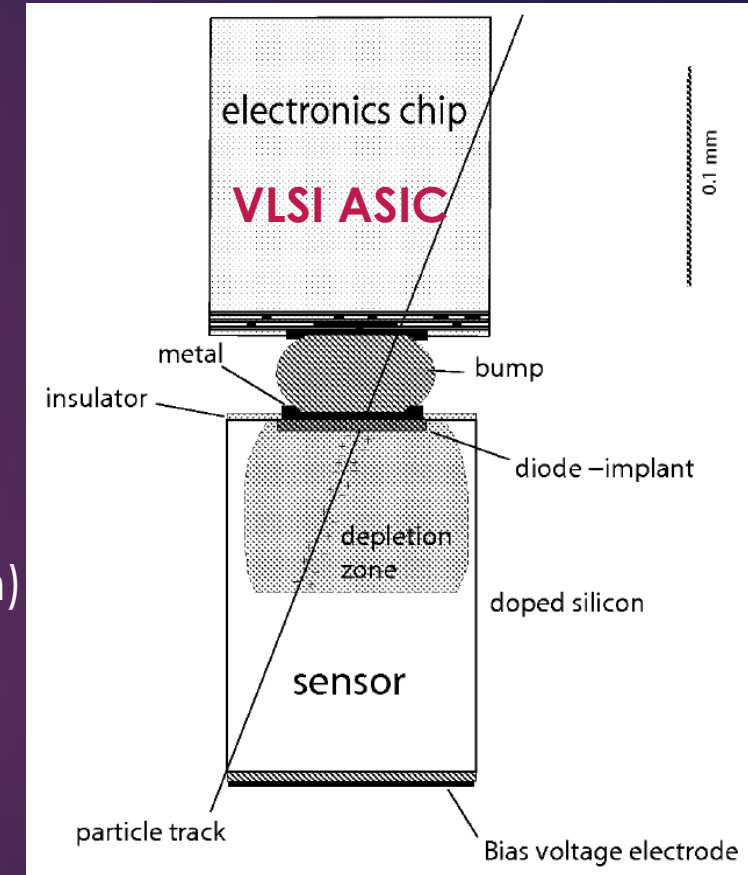


THE TRIGGER FOR CMOS PIXEL SENSORS: HYBRID PIXEL SENSORS

VOCABULARY:

- **PIXEL:** short term for **PICTure Element**
- **PIXEL DETECTOR:** device able to detect an image with a resolution power expressing the size of the pixels
- **PIXEL DETECTOR FOR PARTICLE PHYSICS:**
 1. an image is generated in a semi-conductor by ionisation,
 2. the charge generated is converted in an electronic signal,
 3. which is processed electronically (VLSI: Very Large System Integration)
 4. the resulting signals are read out and transferred to the DAS
- 1st generation of pixel detectors with on-pixel electronics
Hybrid Pixel Sensors, first used at CERN in DELPHI/LEP and in the WA-97 Heavy Ion fixed target expt (1996/97)
→ **Hybrid:** sensing element & read-out μ -circuits are fabricated separately and interconnected via bump-bonding

Hybrid Pixel Device

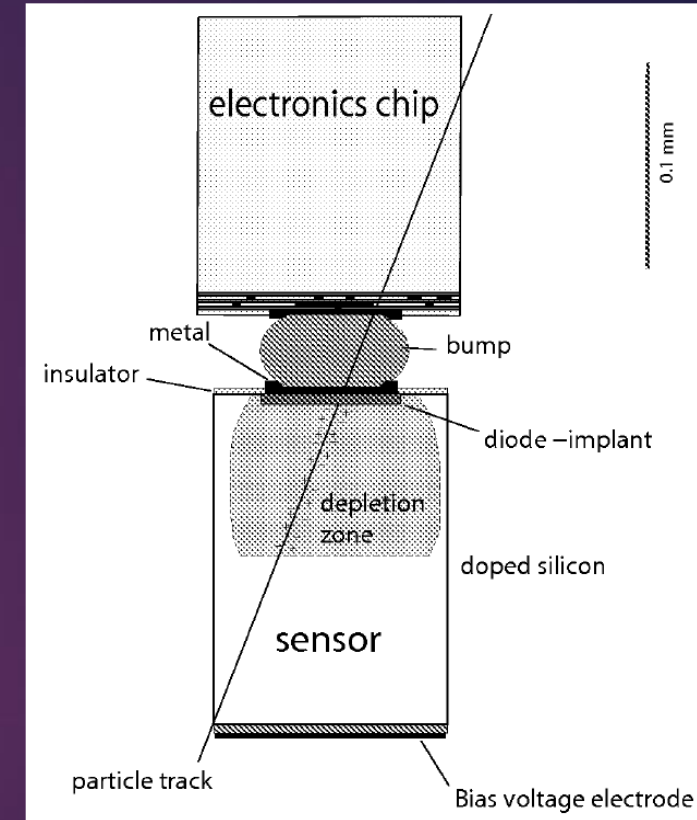


SEMI-CONDUCTOR DETECTORS: HYBRID PIXEL SENSORS

FUNCTIONING:

- When a charged particle crosses the sensor, it liberates about 70 eh pairs/ μm (3.6 eV / eh pair) \rightarrow Landau fluctuations !
- The ionisation electrons and holes diffuse thermally (by default)
- Sensor material: usually P-type silicon (dopant with 3 electrons populating valence band, while Si has 4 valence electrons)
- The dopant is integrated into the lattice structure of the semiconductor crystal, the number of outer electrons defining the type of doping: Elements with 3 valence electrons (e.g. Bo, In) are used for p-type doping, while 5-valued elements (e.g. P) are used for n-doping. The conductivity of a deliberately contaminated silicon crystal can be increased by a factor of 10^6 .

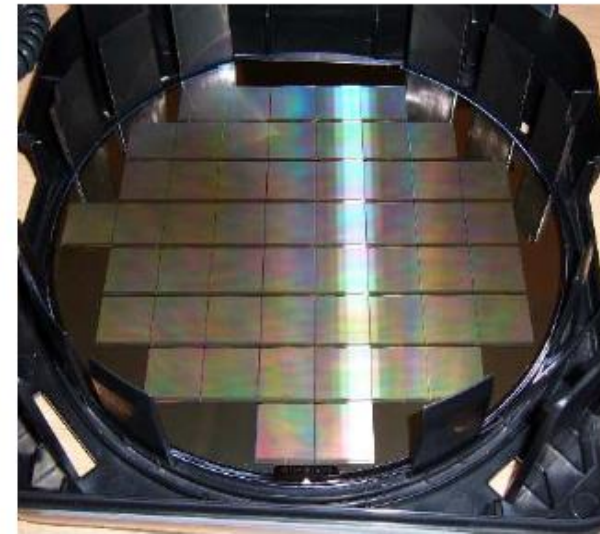
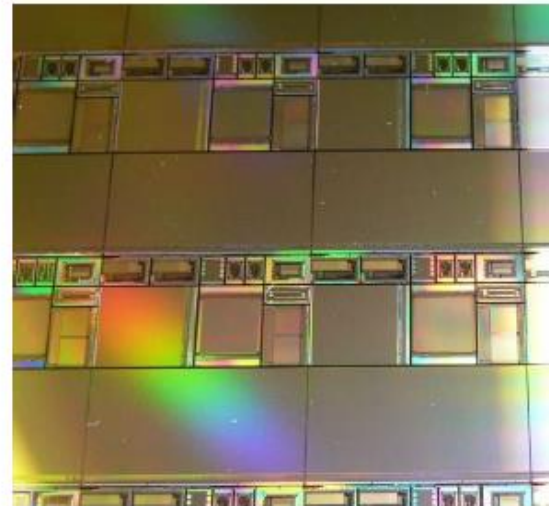
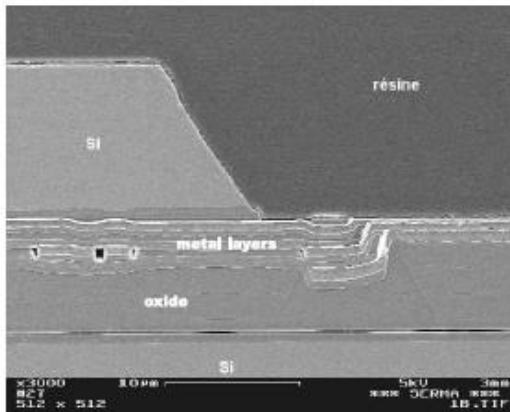
Hybrid Pixel Device



SEMI-CONDUCTOR DETECTORS: CMOS TECHNOLOGY

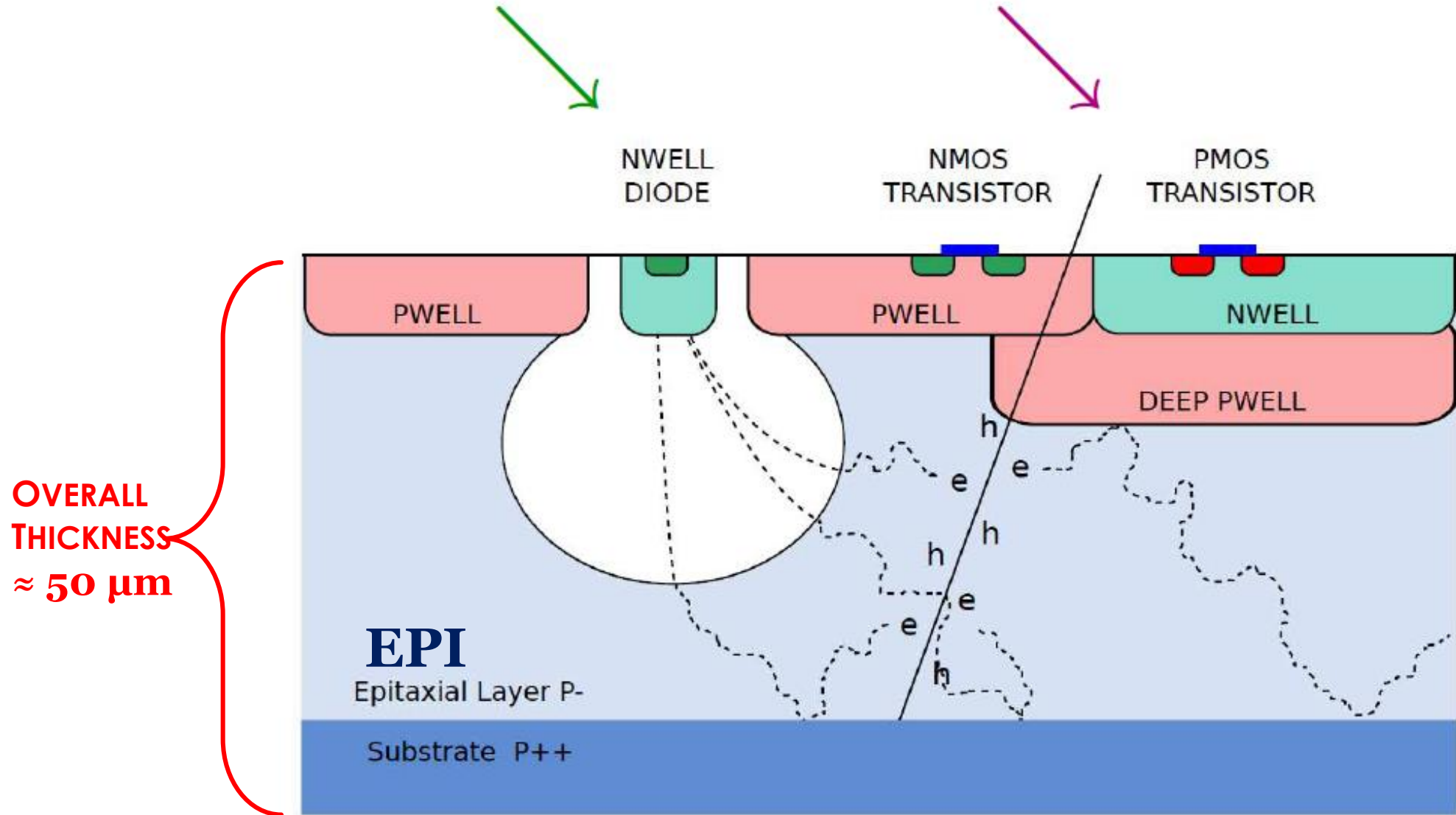
- CMOS fabrication mode :

- * μ circuit lithography on a substrate sliced from a crystal ingot (or *boule*)
- * proceeds through reticules (e.g. 21x23 or 25x32 mm²) organised in wafers



SEMI-CONDUCTOR DETECTORS: CMOS TECHNOLOGY

- CMOS Pixel Sensors \equiv **Detector** \oplus **Front-End Electronics** in same die



SEMI-CONDUCTOR DETECTORS: CMOS TECHNOLOGY

- R&D addresses

Sensing Element



Read-Out μ circuitry

OVERALL THICKNESS $\approx 50 \mu\text{m}$

