High resolution time measurement on the LHC with the SPIDER ASIC

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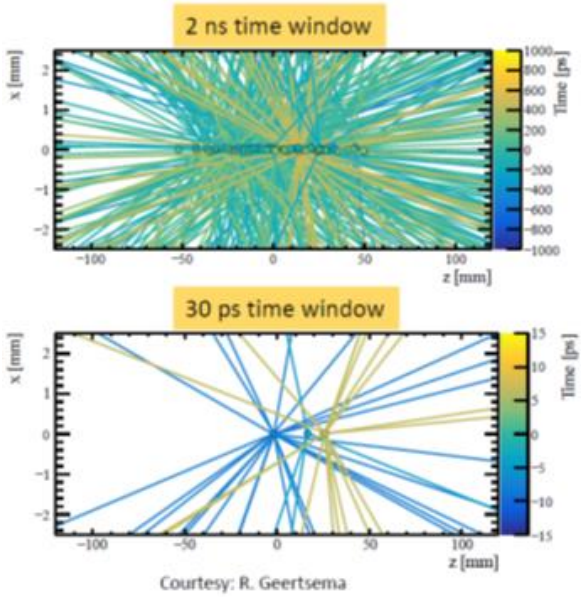
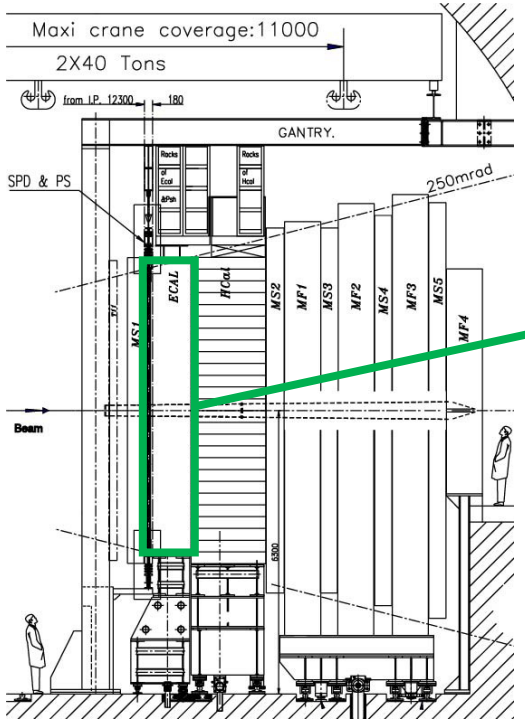
DRD6 meeting

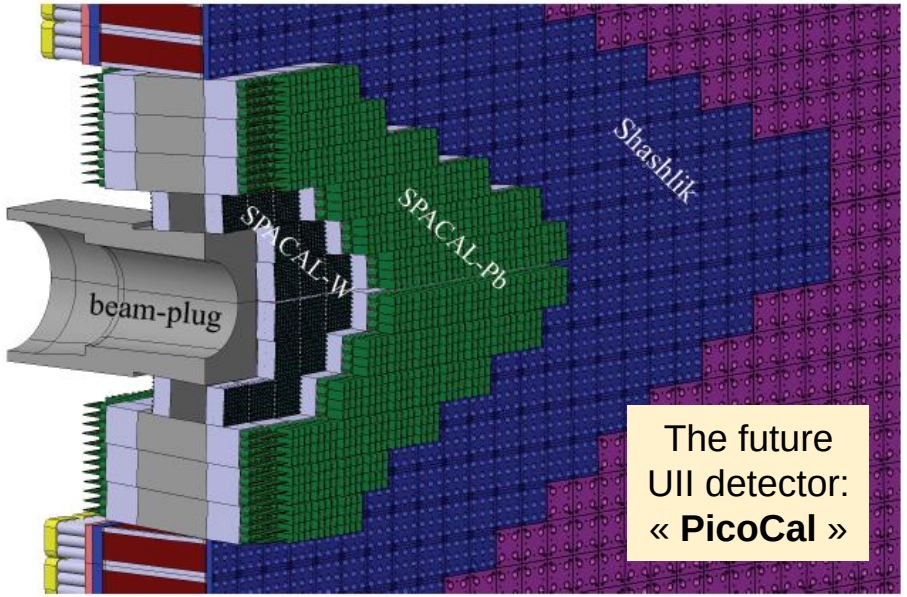
Orsay – April 2nd 2025

The Ecal of LHCb

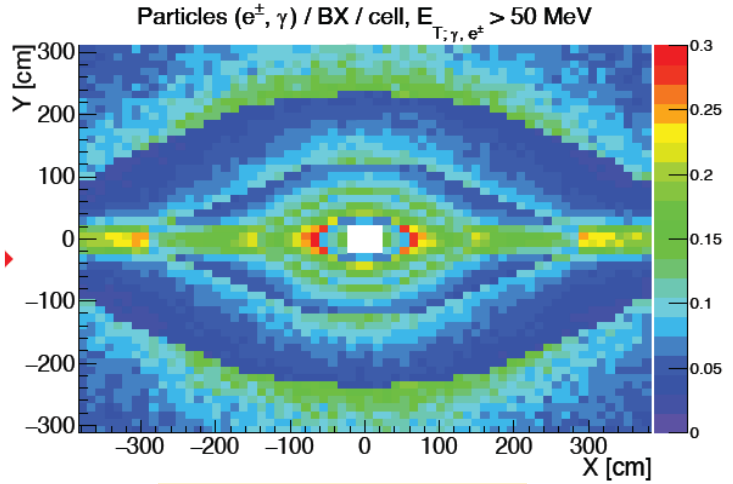


Courtesy: R. Geertsema



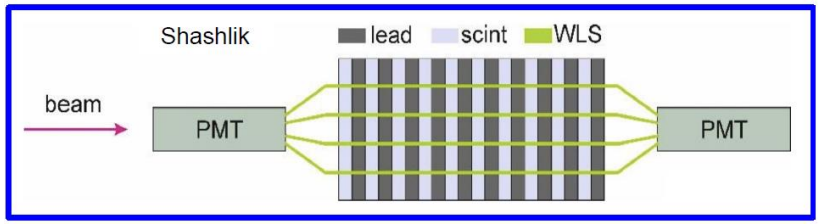


- For the phase 2 upgrade, the central part of the detector will be equipped with **SPACAL modules** to deal with radiation levels (up to 1MGy).
- **Shashlik** will remain in the outer part (< 40kGy).
- In order to limit the occupancy, the size of the modules will be reduced thus their number increased => **from 6,000 to ~ 15,000 modules**
- Introduction of longitudinal segmentation and double sided readout => **~ 30,000 channels** (baseline option)
- In order to filter the luminosity-induced event pile-up, timing of signals should be measured with a resolution **better than 30 ps rms** between 50MeV and 5GeV

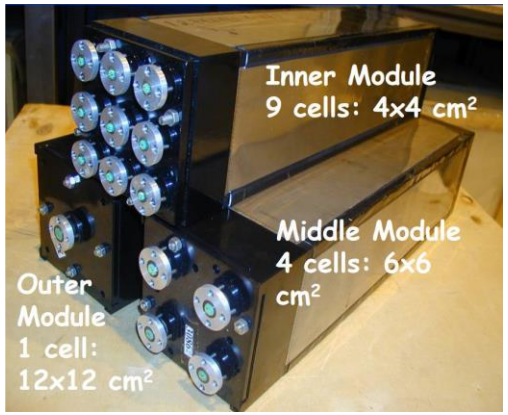


UII detector occupancy

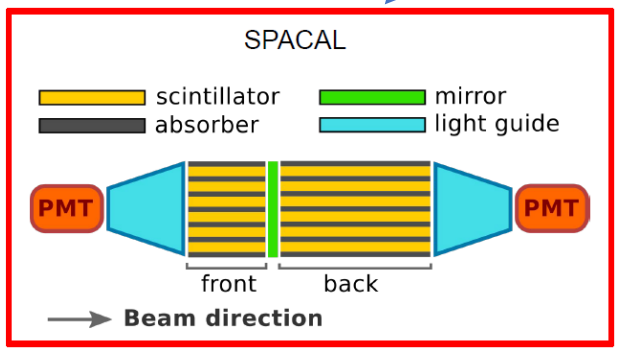
Technologies for PicoCal R&D

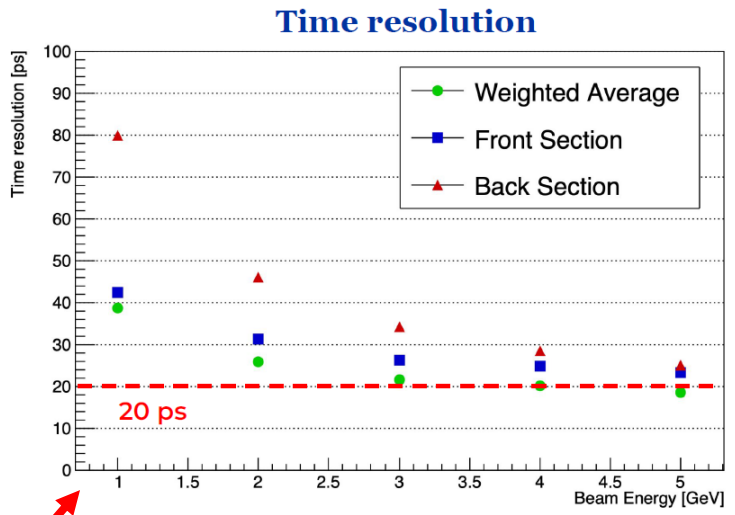


Shashlik
20ps@40GeV



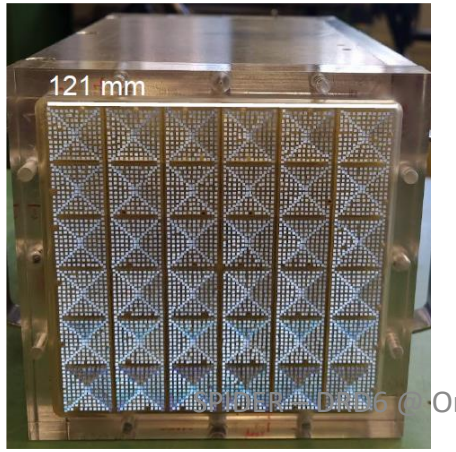
Optional dedicated timing layer

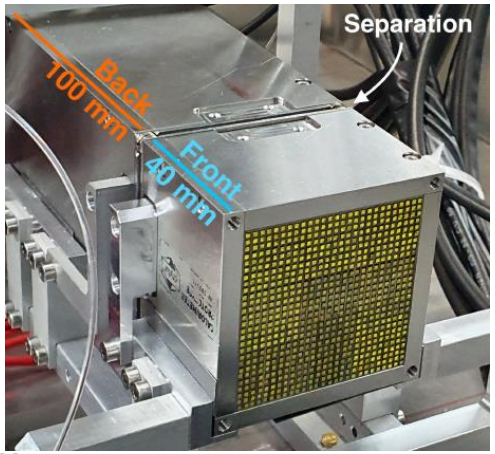




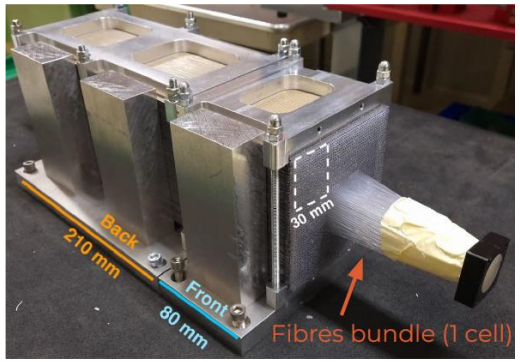
SPACAL W-GAGG
20ps@5GeV

SPACAL W-Polystyrene
20ps@20GeV, 10ps@100GeV



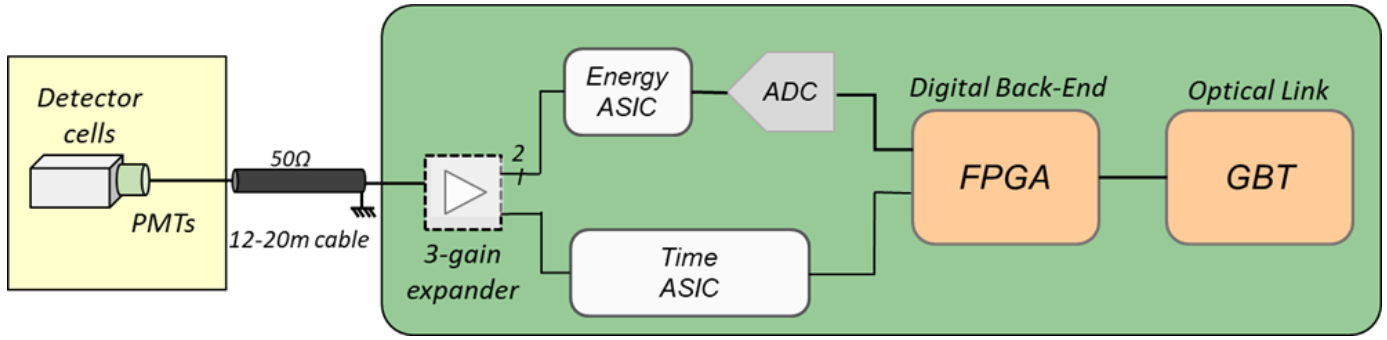


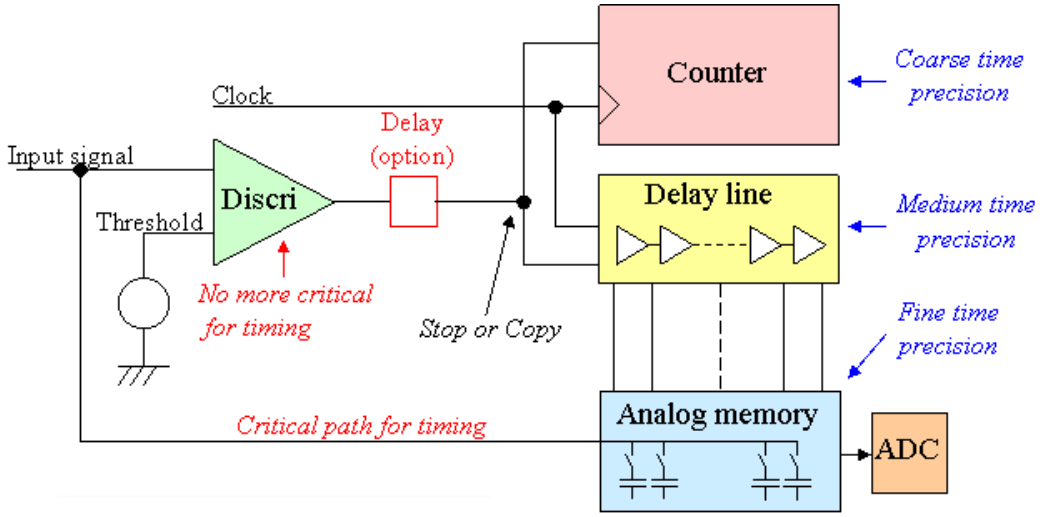
SPACAL Pb-Polystyrene
20ps@20GeV, 10ps@100GeV

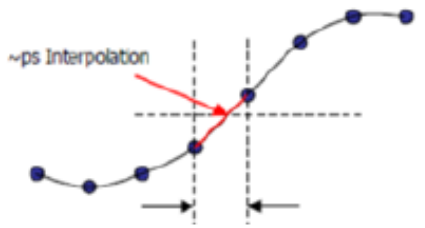


Readout chain for PicoCal

- **Requirements**
  - **Energy**
    - Large dynamic range: **50 MeV to 100 GeV**
    - Dual gain ASIC (evolution of **Icecal** with 2 gains)
  - **Timing**
    - Time resolution target **15 ps for E_T = [1-5 GeV]** to distinguish multiple interactions
    - Rise time between **1.5 ns and 2.5 ns**
    - Time measurement in range **E_T = [50 MeV - 5 GeV]**
    - Max occupancy up to **50% per channel** (20 MHz average rate)
- **Chosen solution for timing: a « waveform TDC » called SPIDER**
  - Waveform TDC architecture was originally developed by LAL/IRFU (SAMPIC ASIC family) as a circular memory with time resolution of a few ps rms
  - Switched capacitor sampler
  - Fast A/D conversion (Wilkinson)
  - Digital “constant fraction discriminator” based on ~5 samples on rising edge







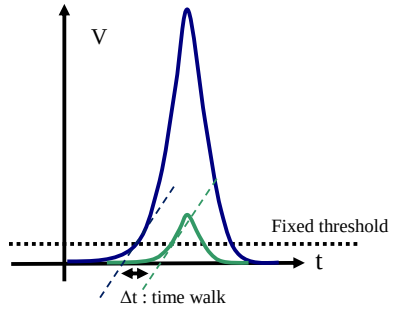
Architecture of a Waveform TDC

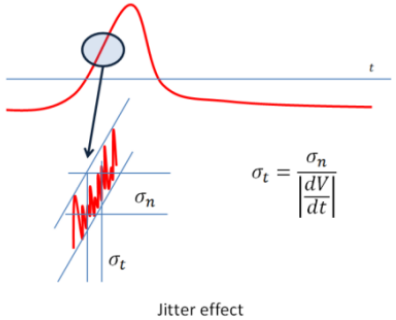
Why using a waveform digitizer ?

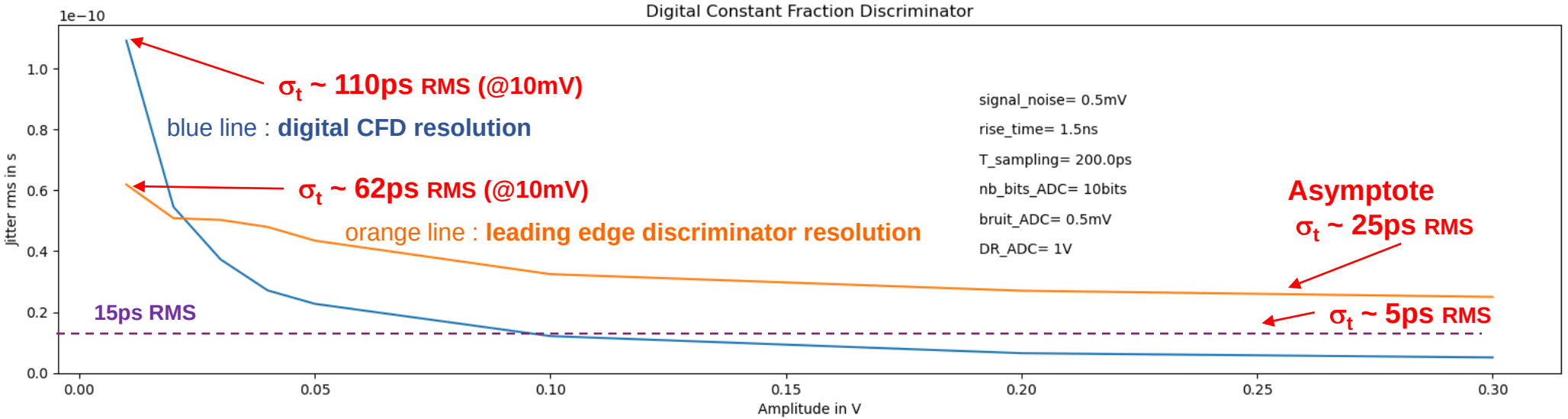
➢ Estimate of time jitter vs input signal amplitude

Dynamic range = 100 → V_{in} : 8mV - 800mV

→ discriminator threshold level set to 4mV (half of minimal amplitude)







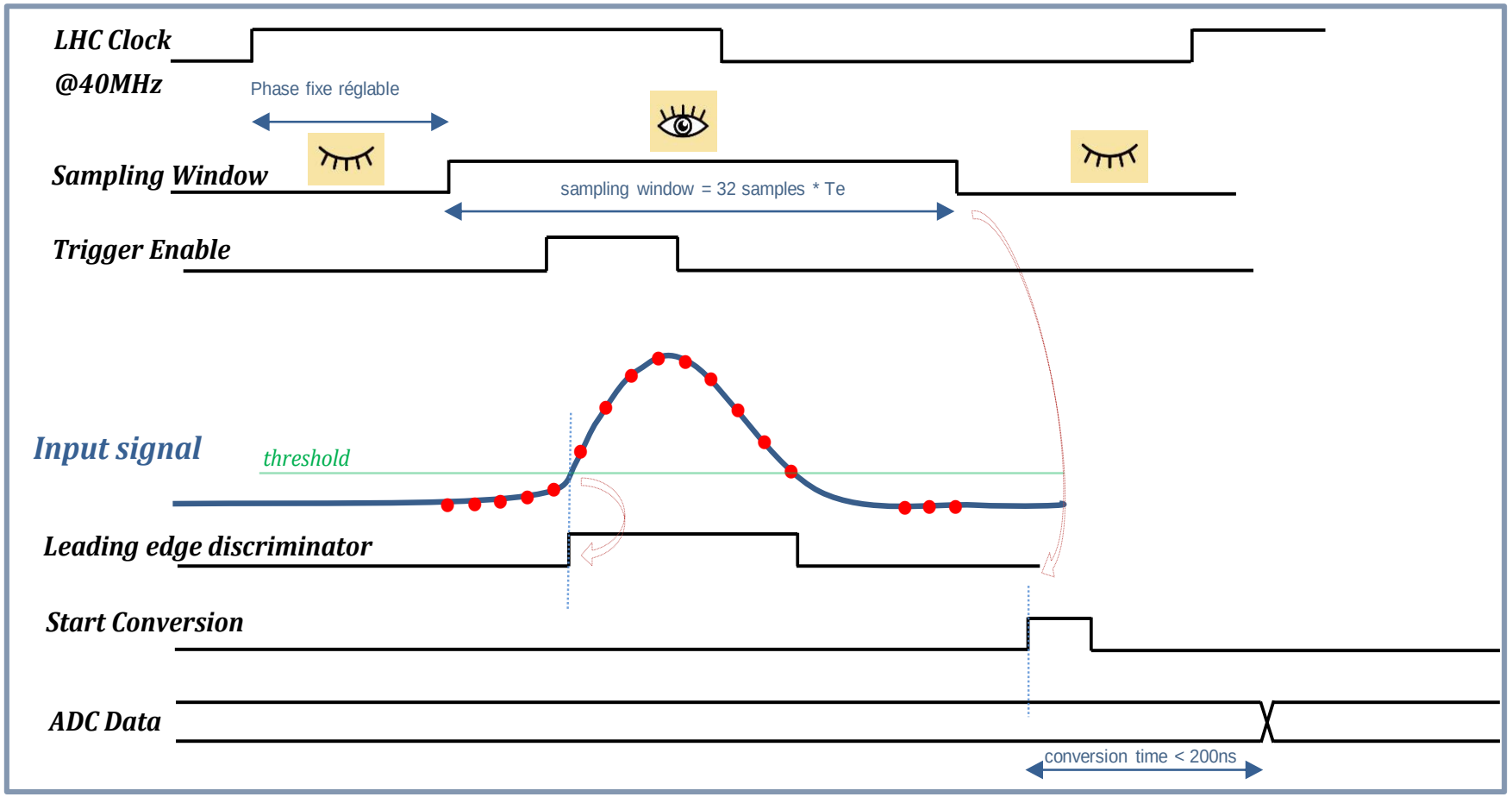
Digital CFD based on a waveform TDC → time resolution better than 15ps above 500MeV and 5ps above 1GeV

Time resolution for low amplitude is degraded by pure SNR and ADC quantification step

Even with ideal time walk correction, leading edge discriminator is affected on large signals by non-optimal threshold (constrained by smallest signals)

How does SPIDER work …

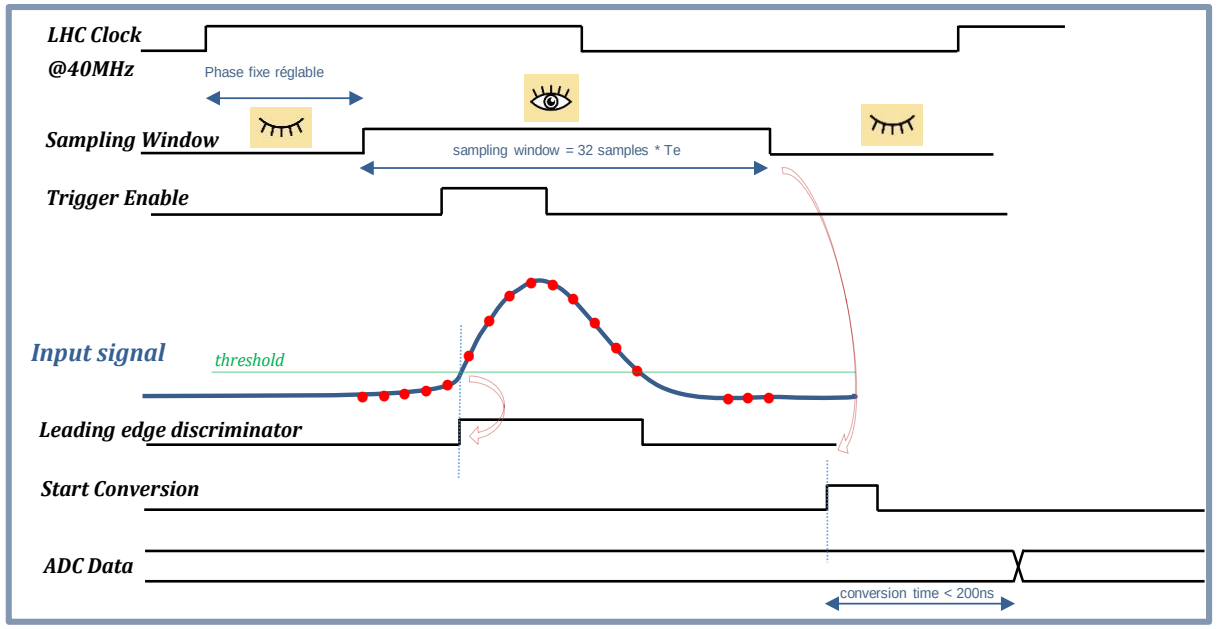
Instead of being a circular memory, SPIDER is dedicated to colliders and finely records the signal during a programmable time slice after each beam crossing

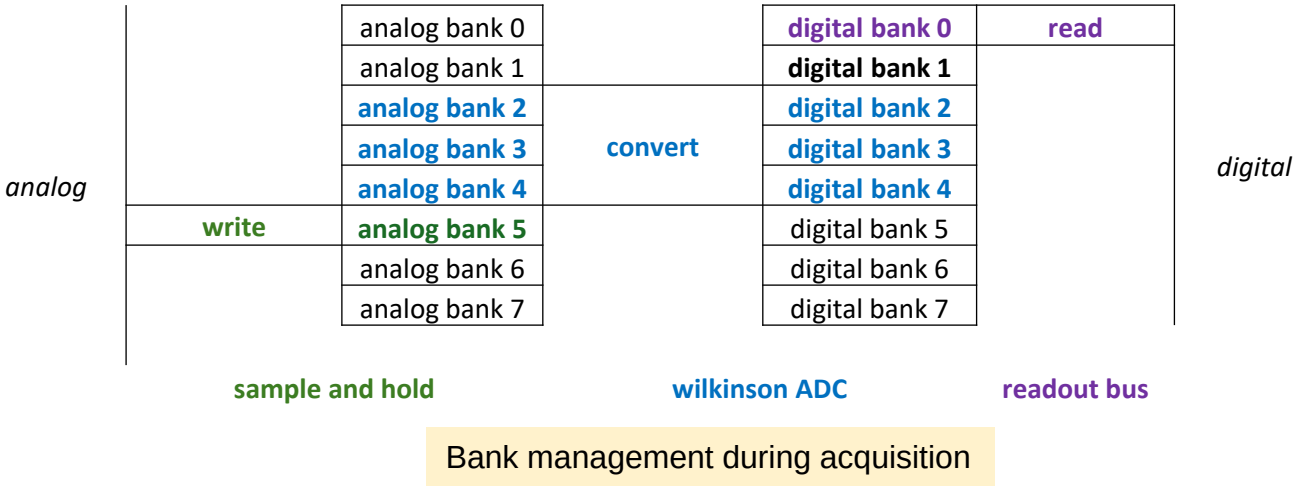


- It takes benefit of the given **Time Of Flight** between the vertex and each detector cell
- **Strong decrease of the number of samples wrt circular memory**
- Idea of the “samples of interest”
- Adjustable phases wrt LHC clock:
  - **sampling window**
  - **Trigger enable window**

SPIDER charactistics

- Analog sampling of input signals
  - in configurable time window w.r.t. LHC clock, adjustable per channel, by steps of 200ps
  - Sampling period adjustable from 50ps to 600ps
  - Sampling window of 32 samples, duration: 1.6ns to 19.2ns
  - Analog bandwidth compatible with minimal rise time ~250ps
- Self-triggered digitization on 10 bits, voltage range 0-800mV
  - Memory bank with bootstrap for range and linearity
- Noise target < 0.5mV rms
- Pipelined operation:
  - 8 banks of 32 samples
  - write/convert/read simultaneously on different banks
- Readout can be restricted to a few samples (typ. 8)
  - Built-in "peak finder" locates the analog cell with max value
  - Cells to be read are relative to the peak (smart read)
- On-chip calibration generators (ADC, timing)
  - ADC and time calibrations (asynchronous for time INL and synchronous for phase vs LHC clock) are required



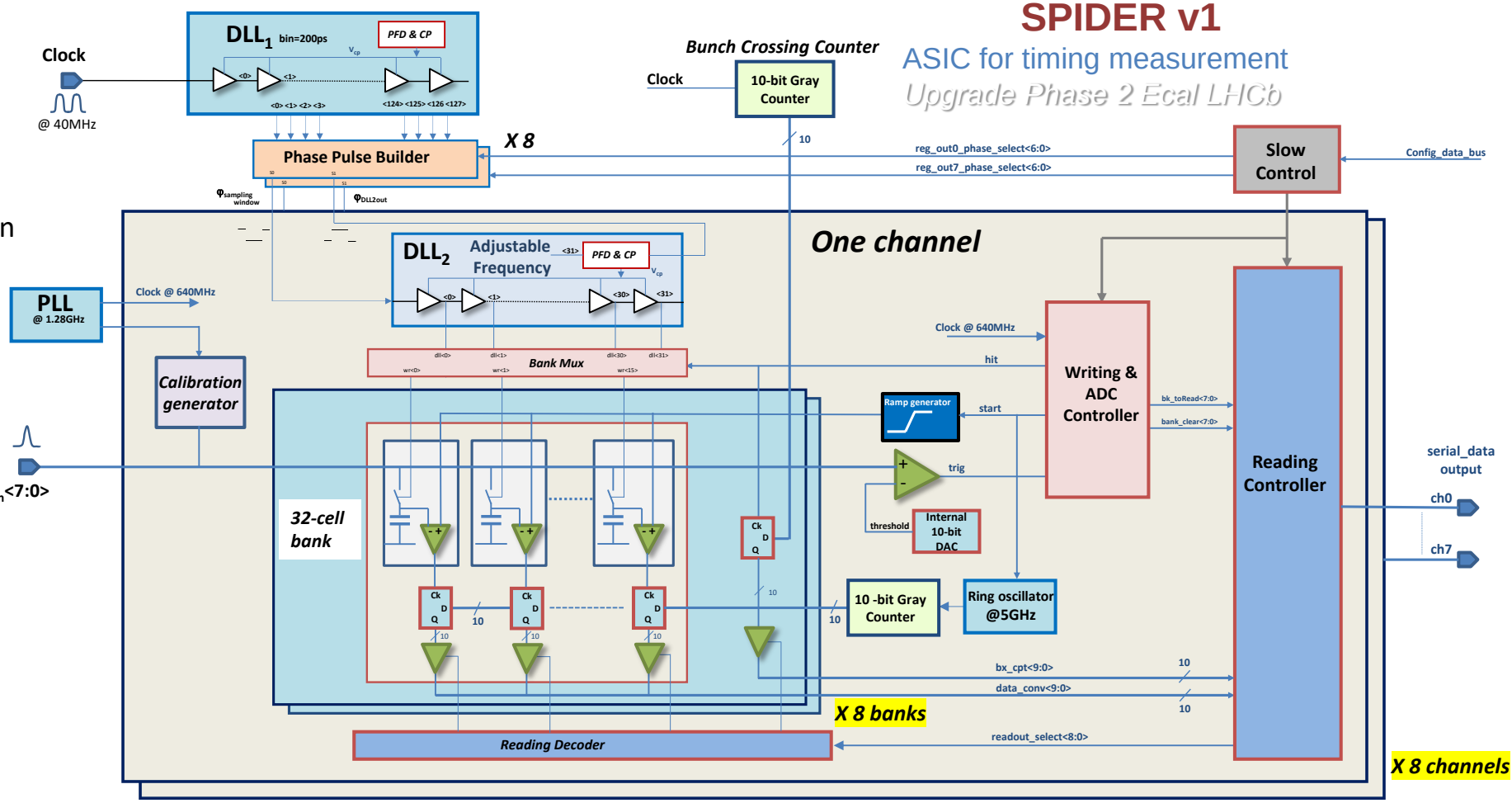


Bank management during acquisition

SPIDER architecture

Architecture specifications – standard version with 8 channels (“V1”)

- TSMC 65nm, VDD 1.2V
- 8 self-triggering channels
- Clock distribution & DLLs
- Memory cell
  - Sample & hold with bootstrap, built-in Wilkinson ADC
  - Noise < 0.5 mV
- Multi-bank system
  - Derandomization buffer
  - 8 banks of 32 cells, sequencing logic
- 10-bit Wilkinson ADC @5 GHz
  - Fast counter to limit conversion time (max 200 ns for 10 bits i-e 8 LHC periods, for 800 mV signals)
- PLL and DAC + buffer for calibrations
- Serial readout interface
  - Digital buffers
  - Up to 2.56 Gb/s on each channel, ASIC-driven (“push” mode)

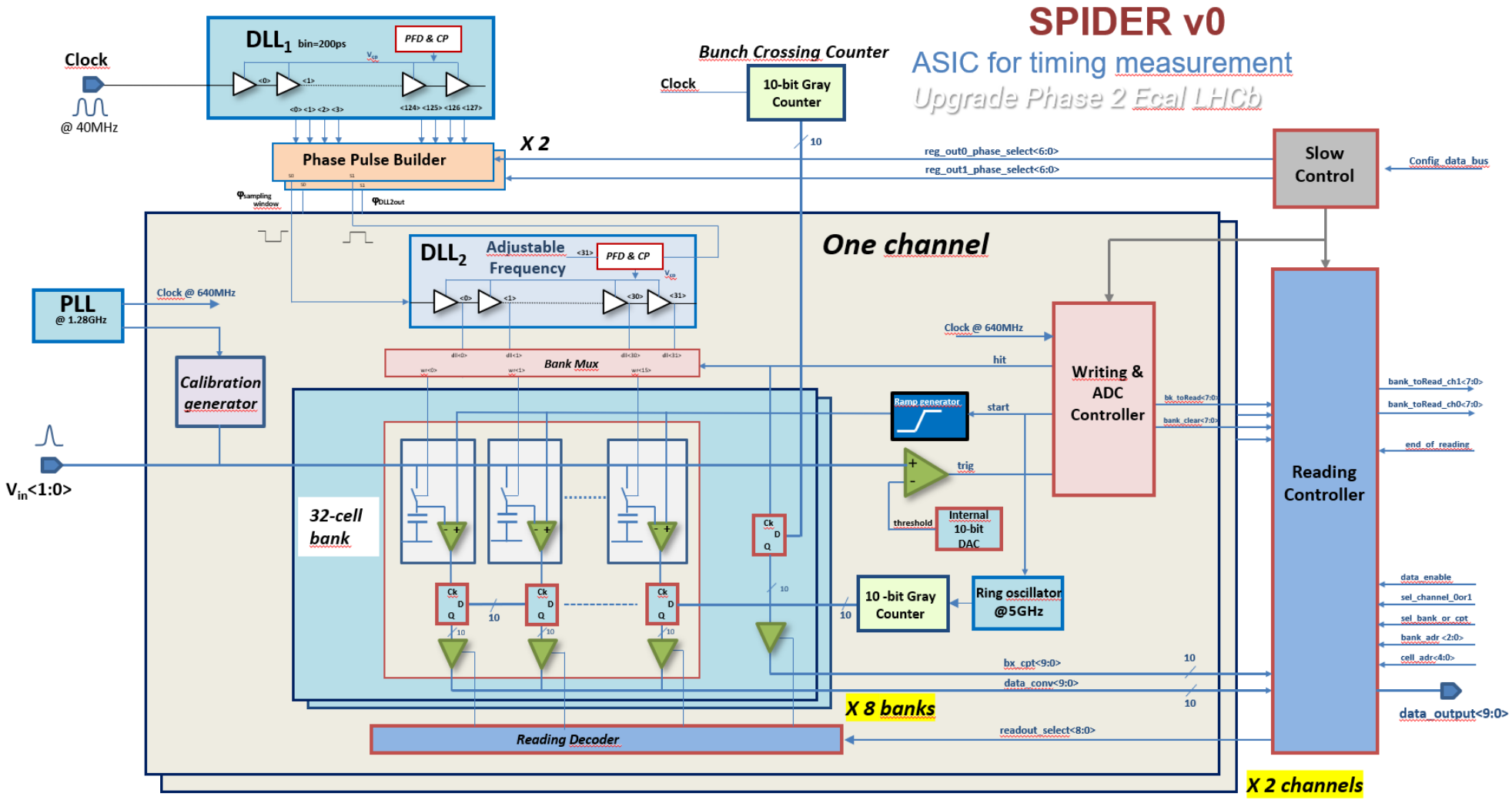


SPIDER first prototype

Architecture specifications – first prototype with 2 channels (“V0”)

Differences with V1:

- Only 2 channels
- Parallel readout interface
  - Simplified logics
  - **FPGA-driven** (“pull” mode)
  - Permits easy and modular access to SPIDER



SPIDER collaboration

- "R&T Projet" @ IN2P3, 2021-2023, will be extended to 2029 (*RS: P. Robbe & RT: C. Beigbeder*)
- Co-coordinators for SPIDER ASIC development *: P. Vallerand & B. Joly*
- Organisation in 7 WPs
- Project started in 2021
- Regular meetings
- Prototype 0 submitted in February 2025 for ~50 k€

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

- C. Beigbeder
- D. Breton
- R. De Neeff
- J. Maalmi
- P. Robbe
- C. Sylvia
- P. Vallerand

LPC Particules Plasmas Univers applications Laboratoire de Physique de Clermont

- N. Arveuf
- G. Blanchard
- B. Joly
- F. Jouve
- S. Manen
- V. Tisserand
- R. Vandaële

lpc caen

- L. Alvado
- L. Leterrier

iP2I LES 2 INFINIS LYON

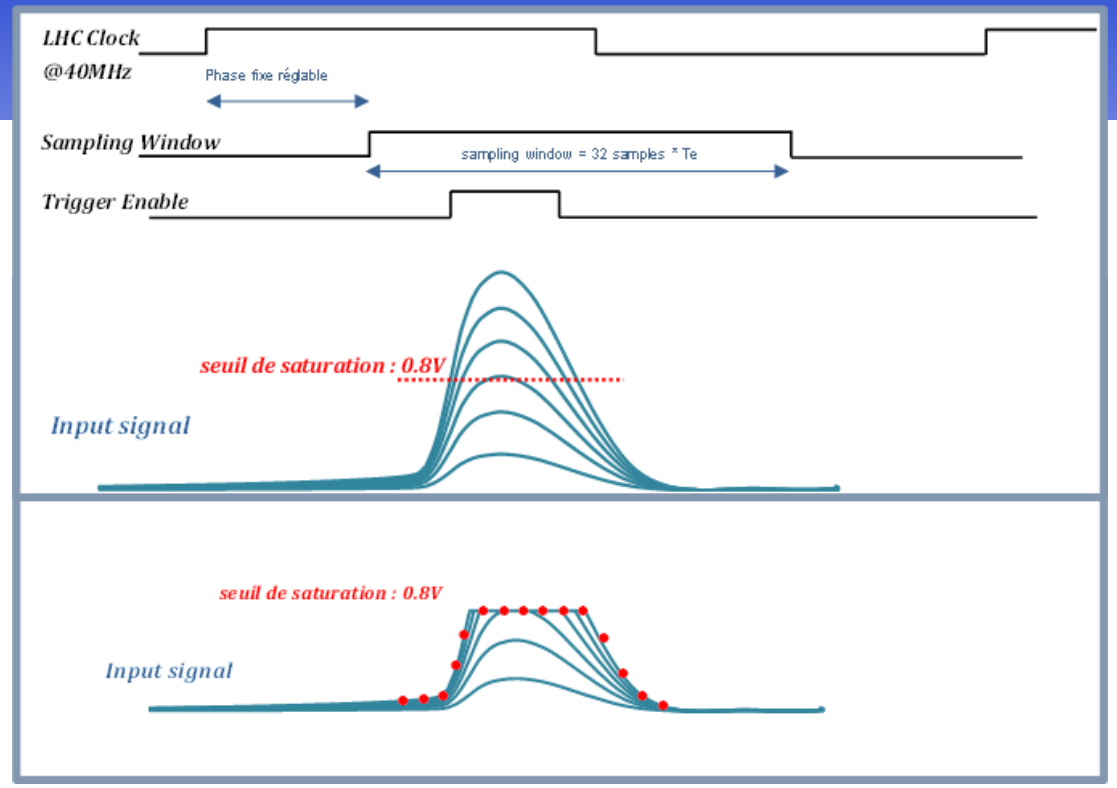
- E. Béchetoille
- H. Mathez

Mi2i Micro électronique des deux infinis

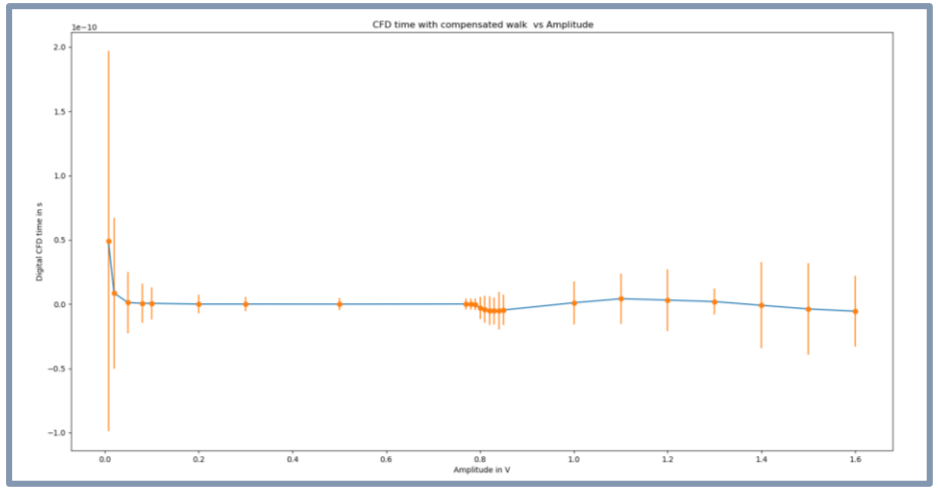
Dealing with saturation

Design difficulty: time measurement must be performed in the lower part of the dynamic range

- This implies we'll have to deal with saturated signals (saturation is performed by electronics in front of SPIDER)
- Digital CFD not directly valid for such signals
  - Timing threshold becomes constant
- Energy can be used to correct for time walk of saturating signals
- Nb of saturated cells can be used to correct for time error
- Logics implemented to extract saturated cell addresses (min-max)

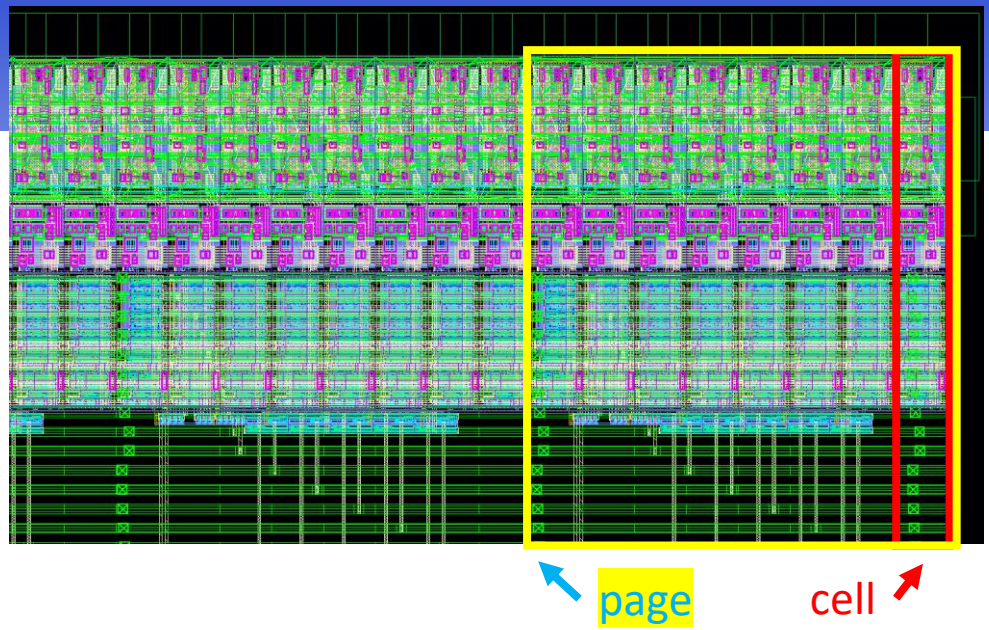


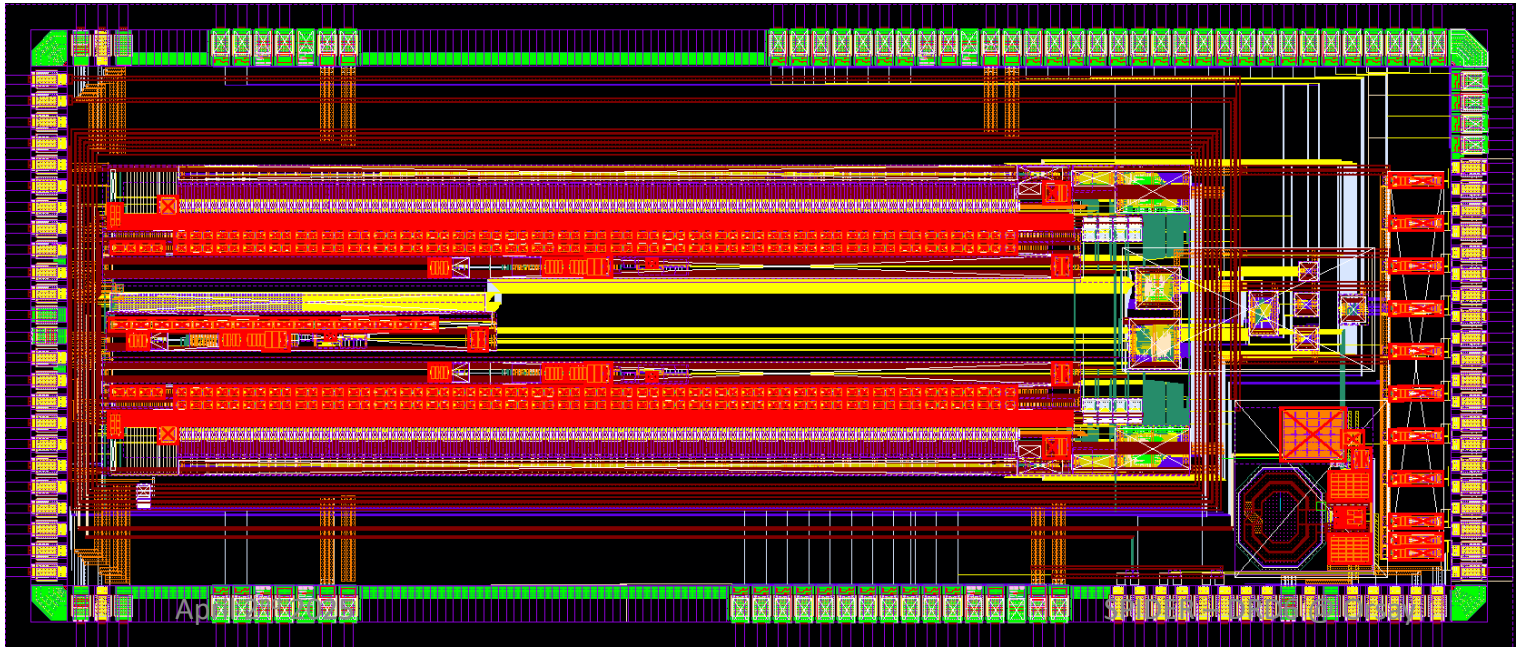
Walk error reduced from 500ps to ~20 ps after compensation (2nd order polynom based on nb of saturating cells)

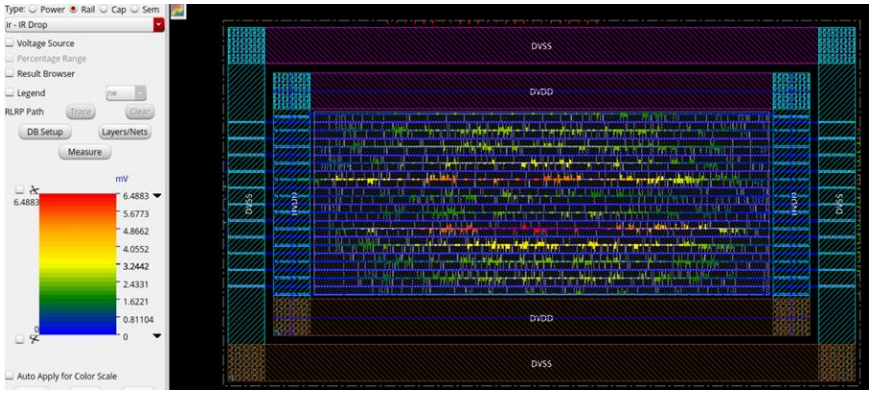


Layout design

- 1 channel => **32*8 = 256 sampling cells**
- Based on **pages** where the 8 banks are interleaved. Total memory length of 2.8 mm.
- Channel layout designed in bottom-up order, many hierarchical levels
- Many post-layout simulations performed (signal integrity, timing, couplings,…)
- Optimizations to reduce power consumption, current transients on VDDs
- Our philosophy: no submission before **thorough functional simulation**







- **V0 submitted in Feb 2025: 2 x 5 mm²**
- **First tests expected from June 2025:**

2 test benches currently being designed in parallel in 2 different labs (IJCLab and LPC Clermont)

Design & verification methodology

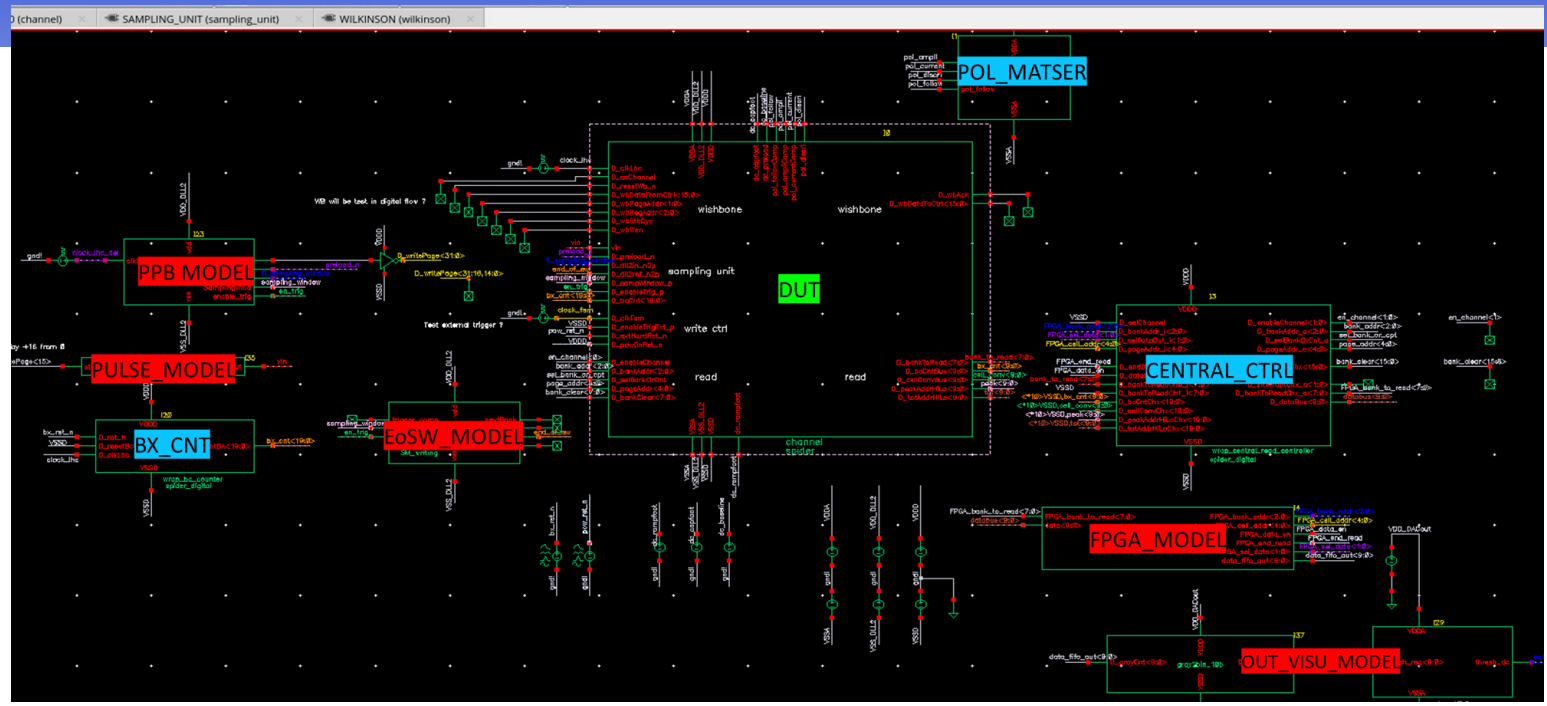
- Complex design => high risk of critical fault
- Analog on top methodology chosen for v0 (top cell is schematic as well as a large part of the design)
- Thorough verification strategy required at *cell level* and *system level* with simplifications (mandatory)
- Test bench (TB) per design cell
  - schematic or digital
  - Post-layout

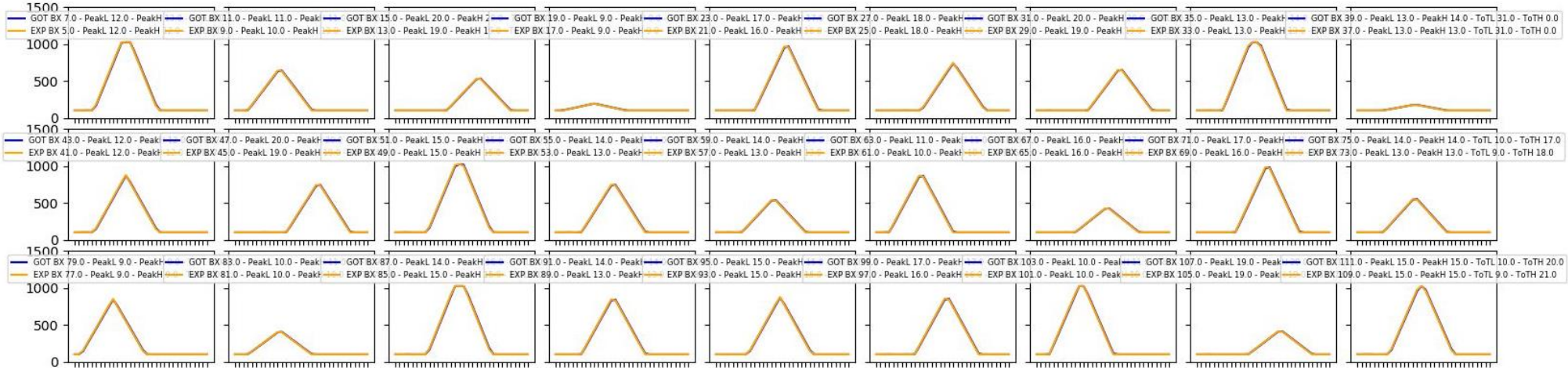
simulation	Device under test		
	hierarchy	top view	sub-cells
analog	cell	schematic, post-layout	
digital	cell	verilog, SystemVerilog	
analog / mixed	subsystem	schematic, post-layout	
digital	subsystem	verilog, SystemVerilog	
analog/mixed	channel / top cell	schematic	schematic, Verilog-A(MS), Verilog, SystemVerilog
digital	top cell	SystemVerilog	Verilog, SystemVerilog

- Digital TBs per subsystem (slow control, readout…)
- Mixed TBs for sampling subsystem
  - Sampling cell, bank, full array of 8 banks => schematic or post-layout
  - Behavioral models for environment (DLL, Wilkinson counter…)
- Full system verification
  - **UVM (Universal Verification Methodology)**, **digital-oriented**, in SystemVerilog, with "Real Number Models" (discrete time, continuous values) for analog parts
  - **schematic**, **mixed** TB for "**channel**" and for **top view** with behavioral models for some cells (Verilog-A, Verilog-AMS) or functional models (Verilog, SystemVerilog)

Channel test bench

- **Behavioral** models designed for some blocks (internal and environment)
- Check multi-bank operation (write, convert, read)
- Schematic-level verification of sampling array
- Signal amplitude and time with random distributions.
- Checker cell for automatic comparison of expected data *vs.* digital output => match
- Validates the functionality of sampling, conversion, readout in full mode and “smart read” mode (8 samples) with peak finder

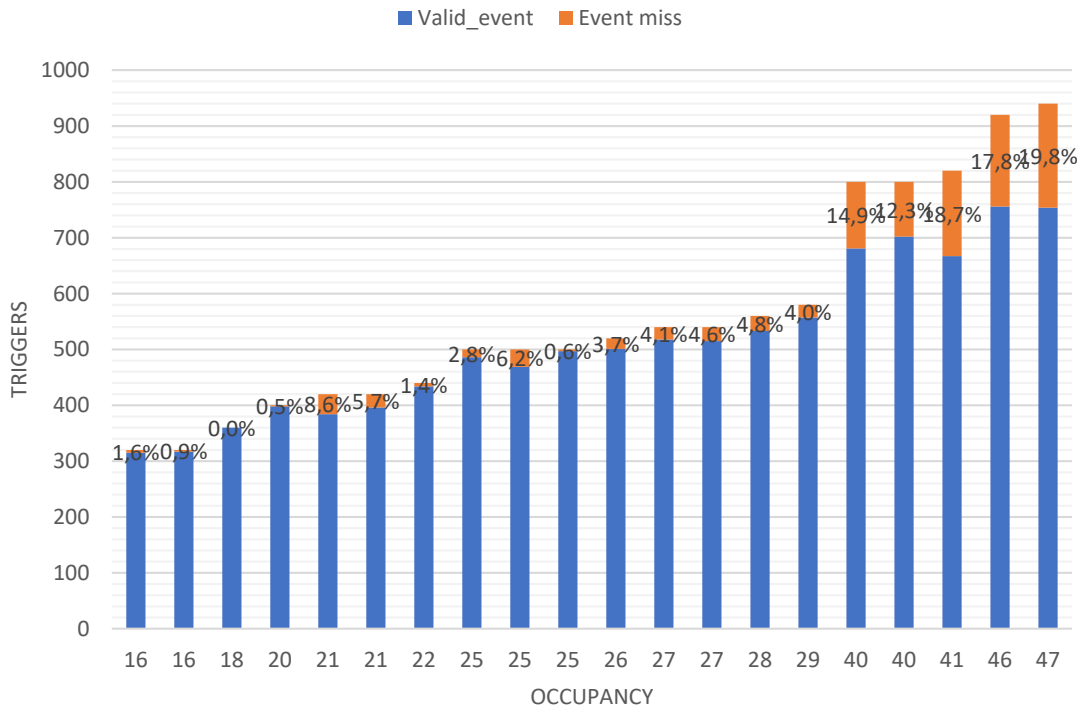




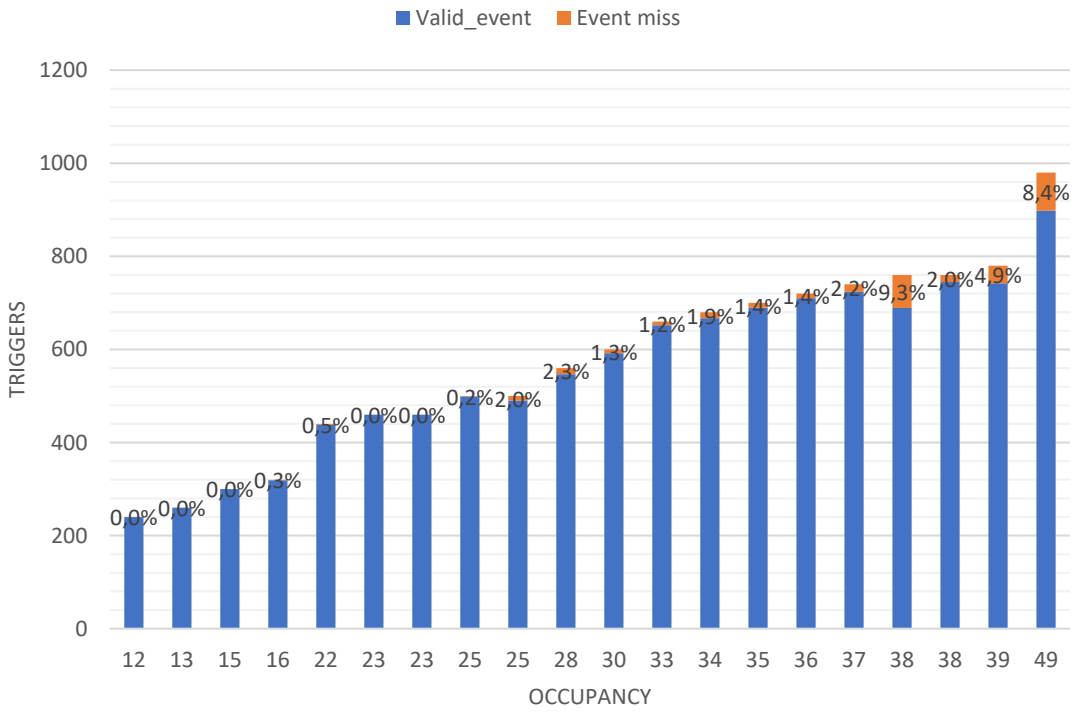
Writing & ADC Controller occupancy stats

- Based on 40 ns readout time with 2,56 Gbits/s channel serializers (BCID + Peak location + 8 Samples)
- Random trigger distribution for a given occupancy
- Equiprobable (10 to 200ns) or Poissonian (90% < 20ns) conversion time

Equiprobable conversion time



Distribution 90% of low conversion time

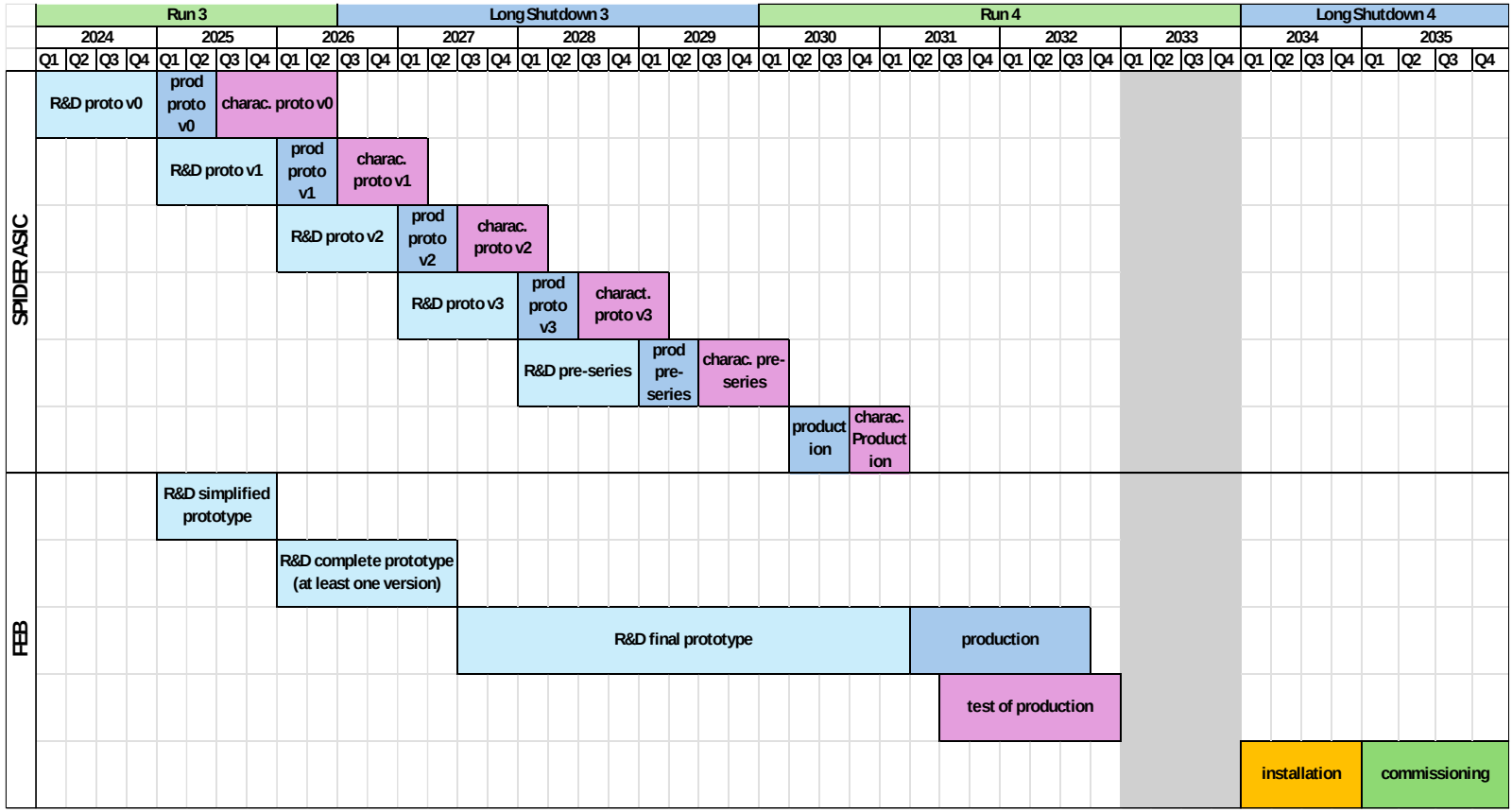


Development schedule

Basis: ~1 engineering run per year 2024-2029

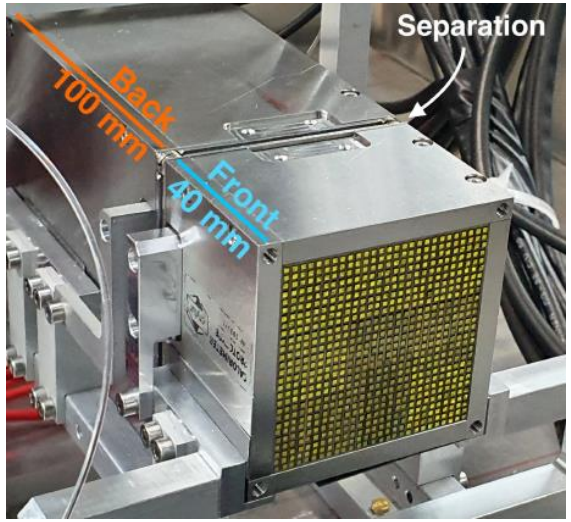
2 x 2-channel and 3 x 8-channel prototypes

- SPIDER V0 (2 channels prototype), design 2023-24, test 2025-2026
- V0+ if required (2 channels prototype with corrections)
- V1 (8 channels + radiation tolerance)
- V2 (8 channels + radiation tolerance + optimisations)
- V3 (+ target « yield »)
- 2028: test of V3; preproduction design
- 2029: preproduction characterisation
- 2030: SPIDER production (30k channels, Front-end card production
- 2031-2032: Card production and test
- 2034: installation
- 2035: commissioning

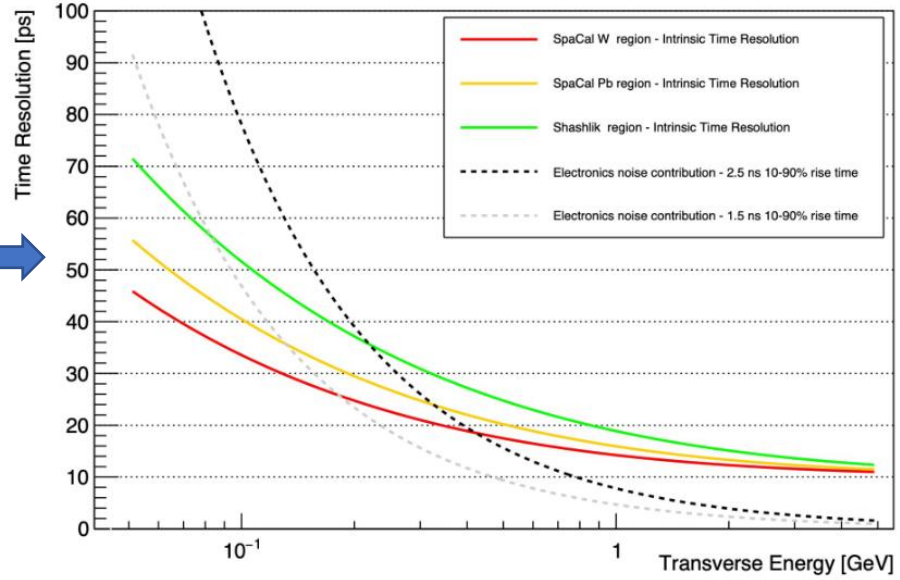


Conclusion

- Detector technology is improving and getting close to the targets in terms of radiation hardness and timing performance
- The large dynamic range and the fact of using the lower part of the energy range present a double challenge for timing
- We tried to optimize the use of waveform digitizing wrt rates, occupancy, and readout dataflow: **new architecture of SPIDER**



- SPIDER should be usable with **any kind of fast detector on a 40 MHz collider**.
  - Sampling can go up to **20 GS/s** for very fast signals
  - We just target the best possible time resolution
  - For Picocal, it will directly depend on the signal rise time



- Still a long way to go …
  - But already a big step forward!