CALICE / DRD6

SiW-ECAL Status

Vincent Boudry

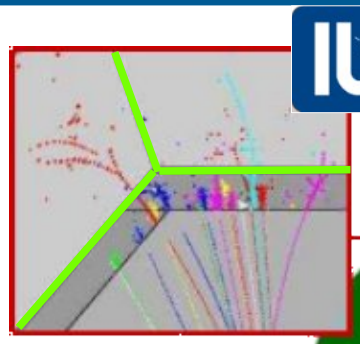
LLR

Institut Polytechnique de Paris

for the SiW-ECAL groups

DRD6 3rd collaboration meeting
01/04/25 @ IJCLab

Design Constraints



HCAL

Endcap2

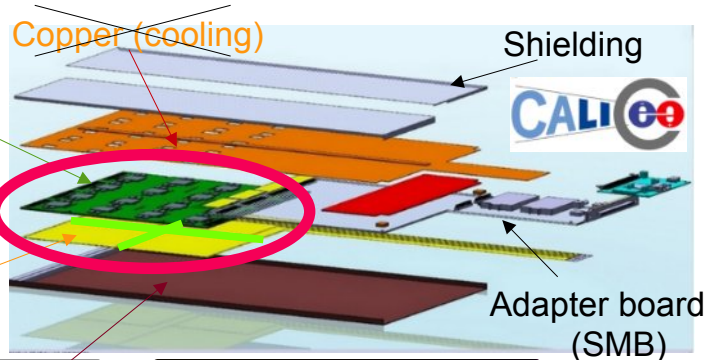
Endcap1

Barrel

ECAL

B = 2 – 3.5 T

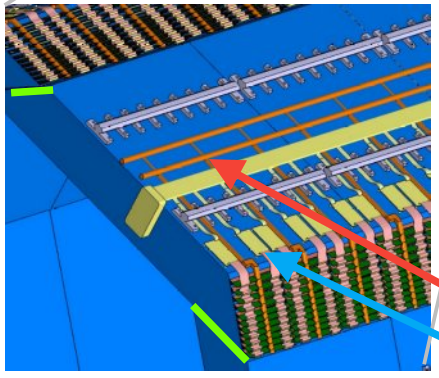
PCB (FeV)
16 SK2 ASICs
1024 channels
ASU
Wafer (4)
Carbon+W

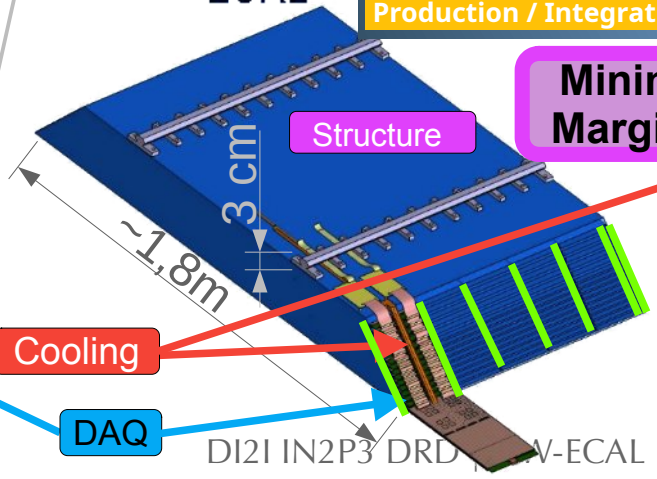


U layout of a **short slab**

- Physical
- Instrumental
- Electronics
- Mechanical
- Thermal
- Production / Integration

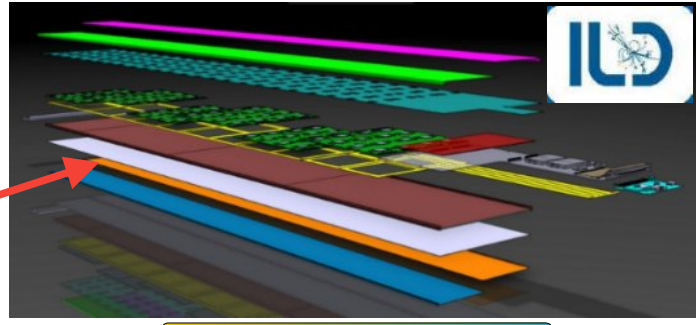
Mininal Margins





Cooling

DAQ

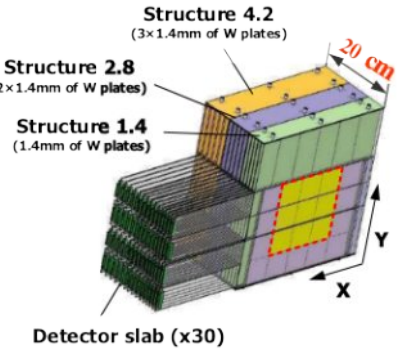


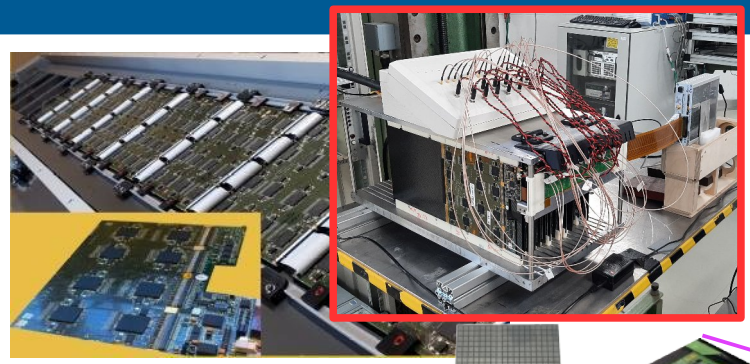
U layout of a **long slab**

+ timing

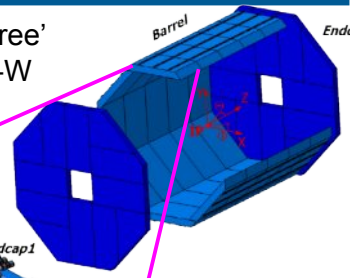
PP ↔ Cont

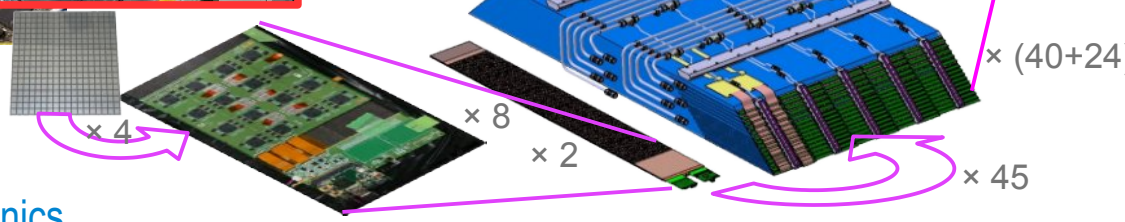
Timeline of SiW-ECAL Prototypes





'dead space free'
Carbon Fibre-W
Structure





Physical (2005-11)

- 1×1 cm² on 500µm 6×6 cm² Pad glued on PCB Floating GR
- × 30 layers (10k chan).
- External readout
- Proof of principe

Technological (now)

- Embedded electronics
  - Power-Pulsed, Auto-Trig, delayed RO
  - S/N = (MPV/σ_{Noise}) ≥ ~12 (trig)
- Compatible w/ 8+ modules-slab
- 5×5 mm² on 320–650m 9×9 cm² × 26–30 layers
  - 8k (slab) ~ 30k (calo) channels

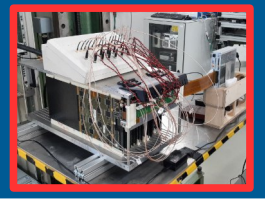
We are here

Pilote ➡ Full Detector

- 1M ➡ 70M channels
- on 725µm 12×12 cm² 8" Wafers ?
- Pre-industrial building
- Full integration (⊃ cooling)
- **Final ASIC**

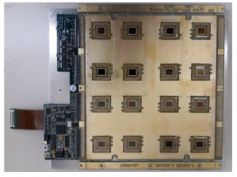
'Almost ready' for LC
To be revisited for CC

Technological Prototype Beam test at DESY & CERN



FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014



FEV-COB

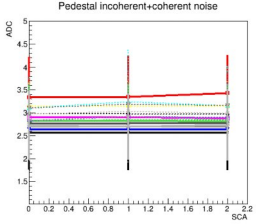
- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

FEV13

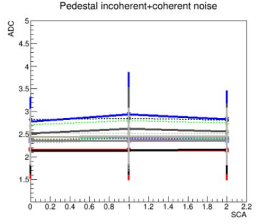
- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

Pedestal widths, 1st memory cells, per asic

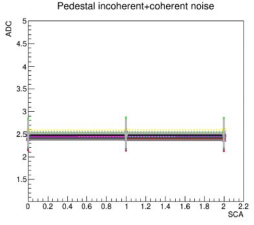
COB



FEV12

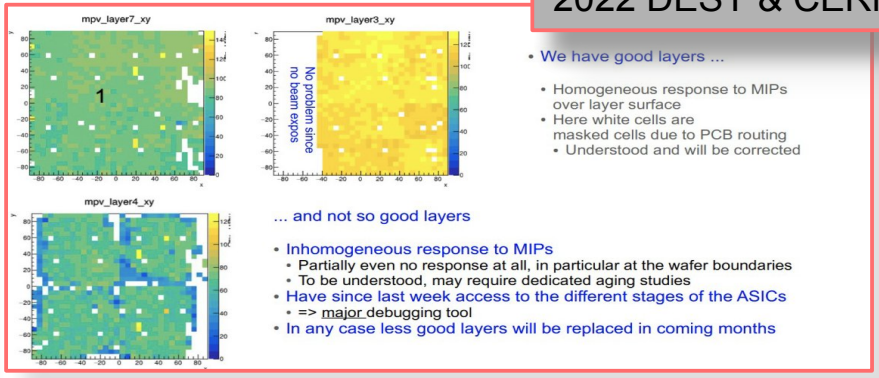


FEV13



- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors

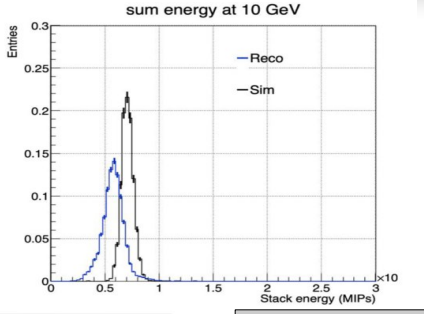
2022 DESY & CERN BT



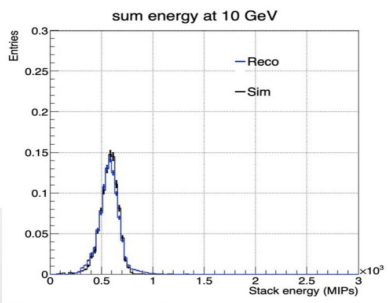
- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
  - Understood and will be corrected

... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months



Masking
Beam
profiling



Yuichi Okugawa (PhD in Feb. 2024)

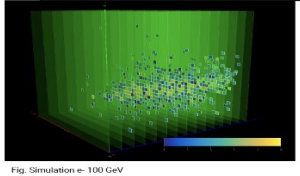


Fig. Simulation e- 100 GeV

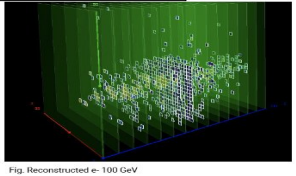
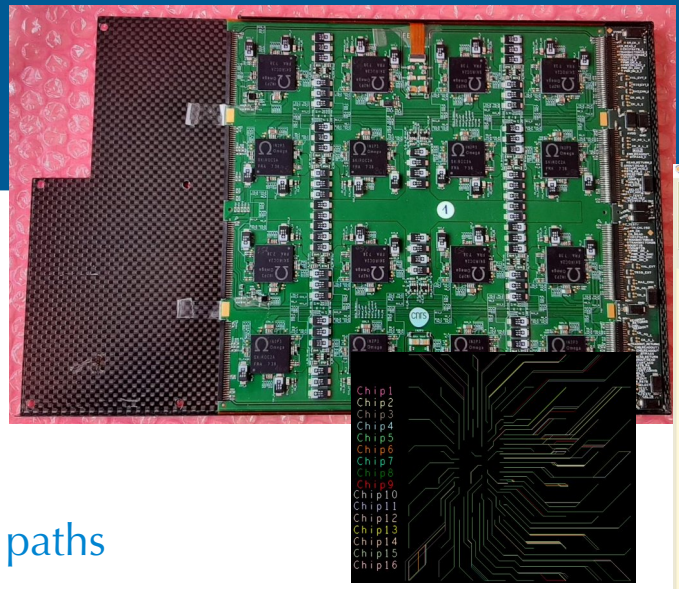
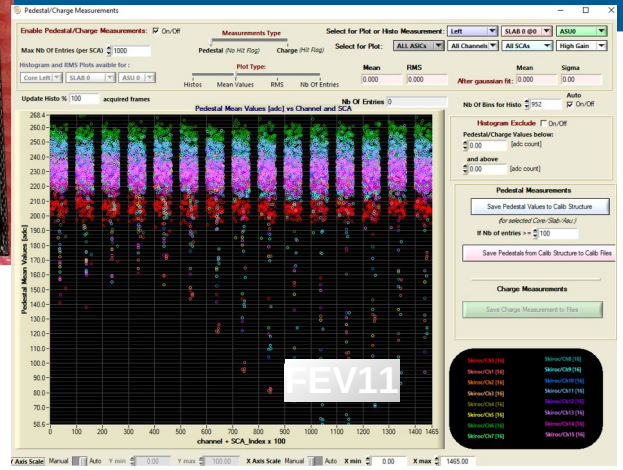


Fig. Reconstructed e- 100 GeV

New FE boards (2023)





Pedestal measurements vs. Ch# + Mem#×100)

SIngle channel → the fault on the ASIC/packaging

Improvements:

- Power distributions
  - Local LV power regulation: LDO's
  - Local HV filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing

Status:

- Noise uniformity dramatically improved (ex: outliers in thr. / 20)
- version 2.1 produced
  - 4 cabled, 2nd metrology, 2 equipped with sensors (Fev'25)

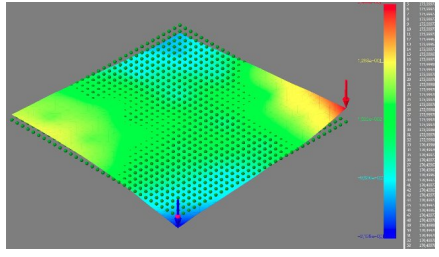
Hybridization studies (2024): How to assemble silicon sensors & PCB ?

See Adrián's presention in side SiW-ECAL meeting for a complete overview

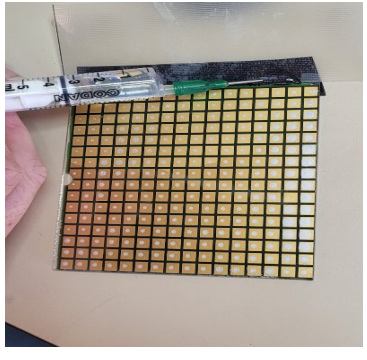
Revisiting gluing (IFIC, IJClab, DMLAB)

- PCB metrology
  - Bef. & After curing & soldering
- Glue formula & preparation
- Gluing methods
  - Robot
  - Stencil
- Reenforcement
  - Filling glue
  - Adhesive films

IJClab (méca)

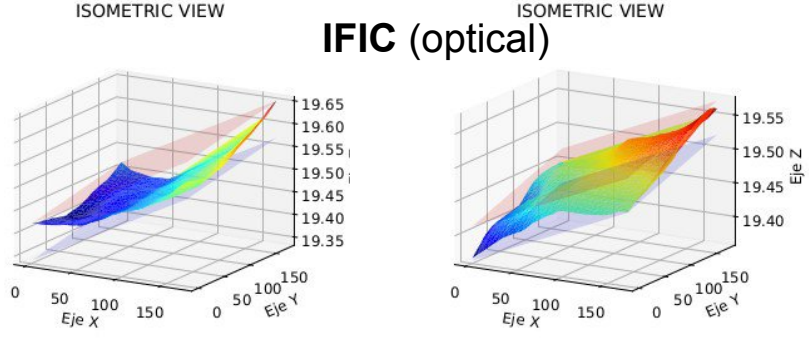


Conductive glue + filling (~invisible) on a glass plate



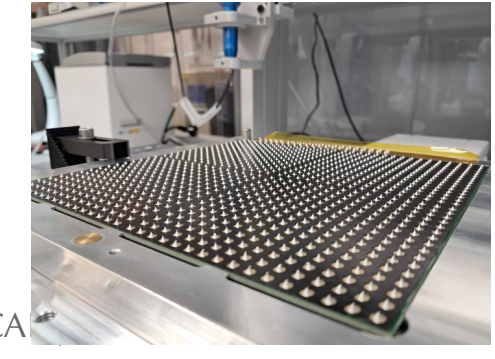
Flatness of PCB

IFIC (optical)



Same PCB before / after 10-day dry storage

Measurements by C. Orero, IFIC



Puncturated adhesive film (**DMLab**) + conductive glue dots

ASU2025_001 + 002 (2025)

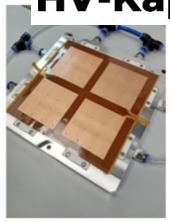
Metrology of PCBs

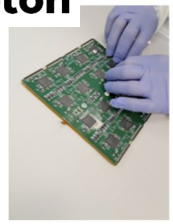
IFIC INSTITUT DE FÍSICA CORPUSCULAR

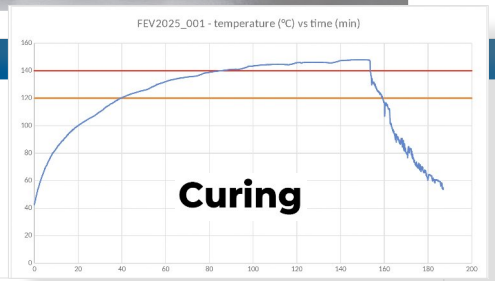
▷ **We could not do conclusive metrologies of the PCBs upon reception**

- Small differences between FEV2.0 and 2.1 and w/ w/o components which make the tools available not suitable… we aim for precision mechanics, we require detailed mechanics models and designs
- At arrival + after drying, requires at least 1 month of time for the full process. → so we decided to dry them before having the definitive tooling (which took some time to be produced)

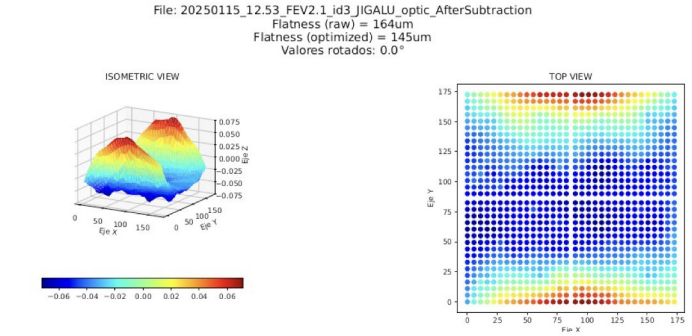
HV-Kapton



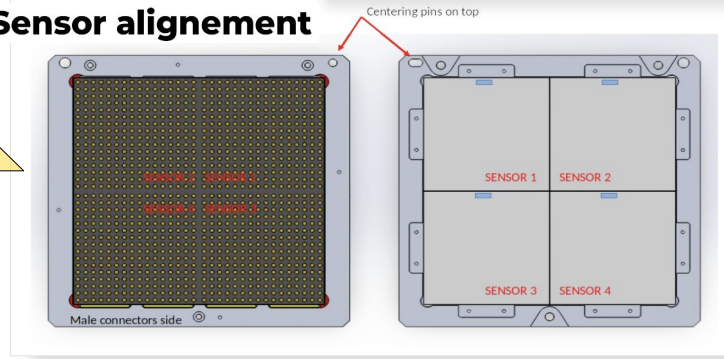




▷ **Metrologies after drying them – FEV2.1 id3 – "flatness" of 145um**



Sensor alignement



PROCEDURE - 3D robot and precifluid v0.odt

PROCEDURE - CALICE ASU gluing_alignment v0.odt

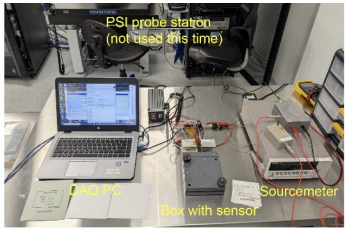
PROCEDURE - CALICE ASU gluing v0.odt

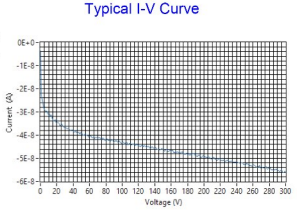
PROCEDURE - H20E preparation v2.odt

PROCEDURE - HV-K… to ASU v0.odt

Sensor and electronics cleaning

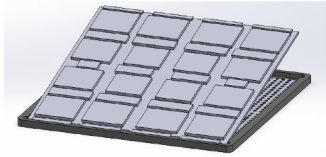
Sensor characterization

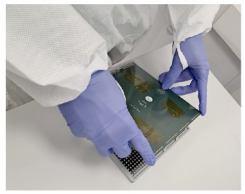


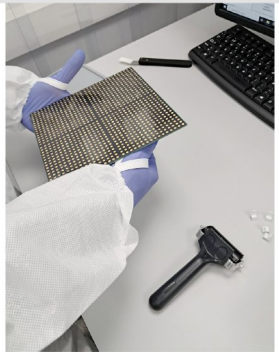


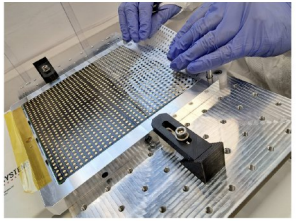
- Reasonable I-V curve though leakage current ~ factor two lower than in HPK data sheet
- Tests allow to validate that there is no major problem with sensors

J. Jeglot, A. Torento, R.P., (R. Cornat)







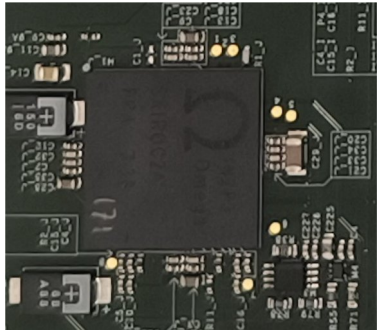


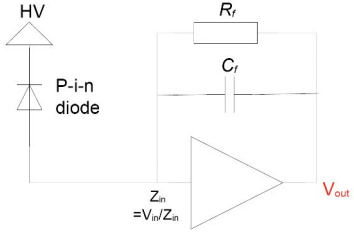
3M tape

Commissioning: Analogue Probes

See Roman's presention in side SiW-ECAL meeting for a complete overview

Analogue Probes

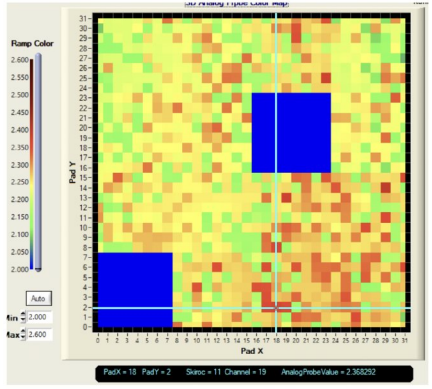




$$V_{out} = V_{in} - I_{in} Z_f$$
$$Z_f = 1/\omega C_f + R_f$$

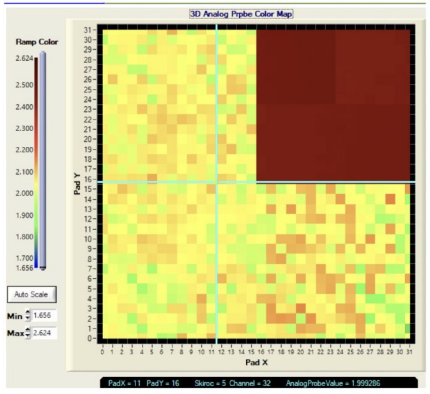
1 value (LV, Channel, …)
→ common line

Two ASICs with short cut diode on input



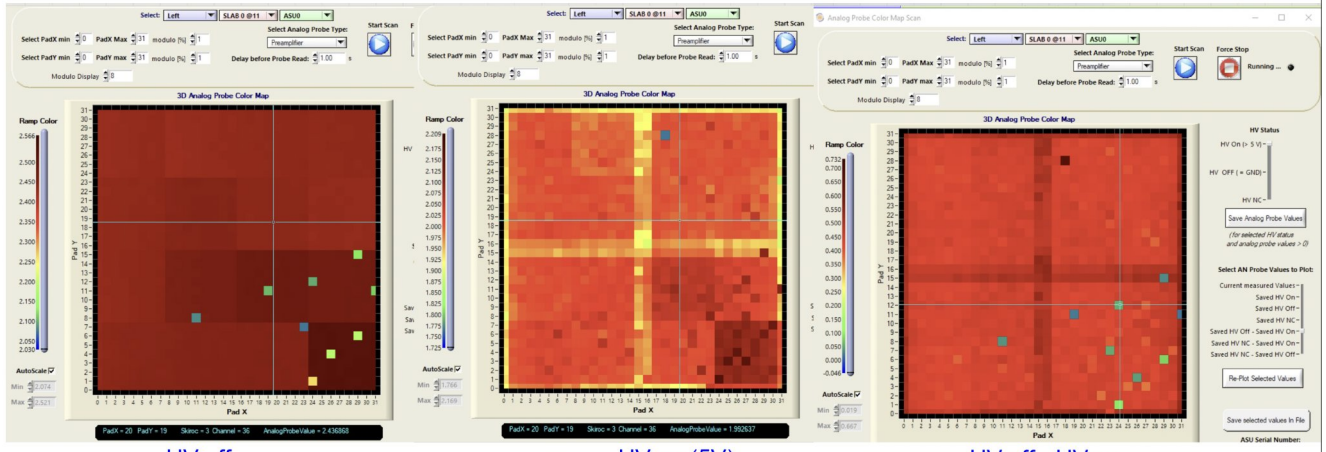
Repaired by Dominique

Badly powered sensor



Replugging of HV Connection helped

- Automatic scan over all 1024 cells (~15 minutes)



HV off | HV on (5V) | HV off - HV on

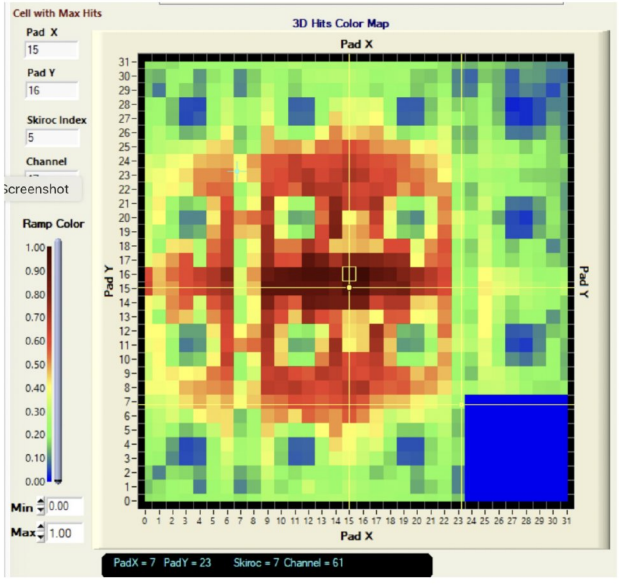
Commissioning: ^{90}Sr

Tests made one week before BT at DESY

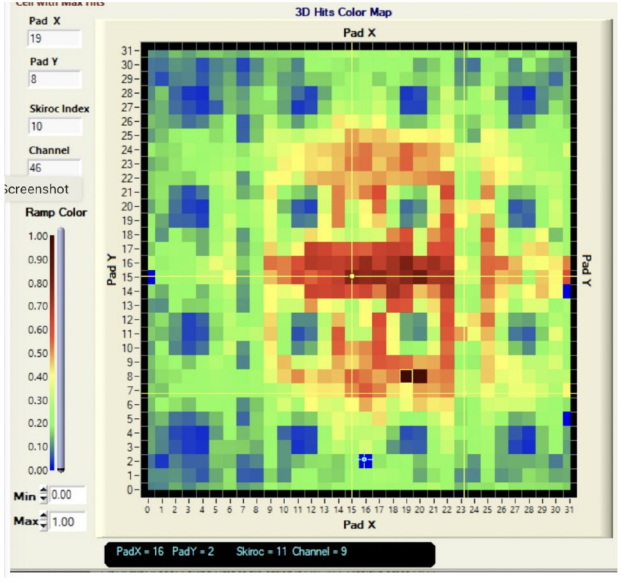
Beam test reports:

- See (next) Yukun's presentation

ASU2025_001

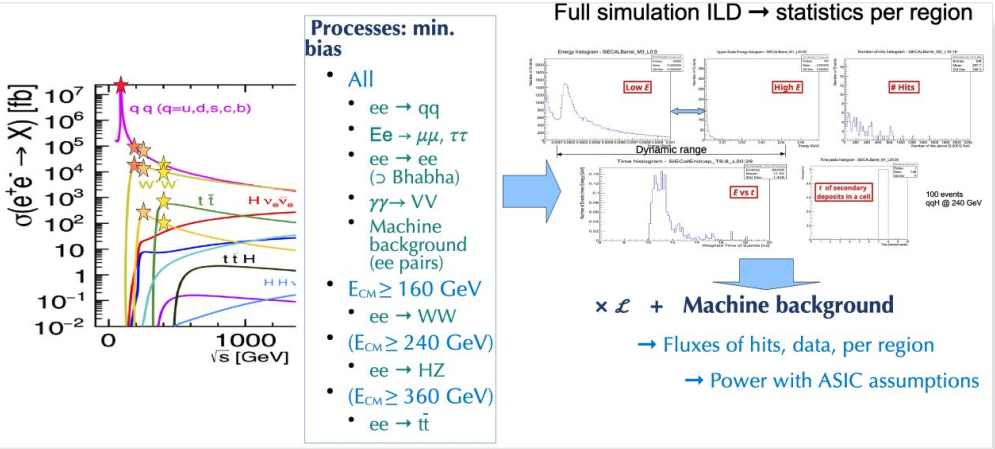


ASU2025_002



- Source tests allow to validate functionality of all cells (or identify further problematic cells)
- Small blue regions ASIC packaging (-> ok), large blue region one faulty chip

Fluxes in Calorimeters

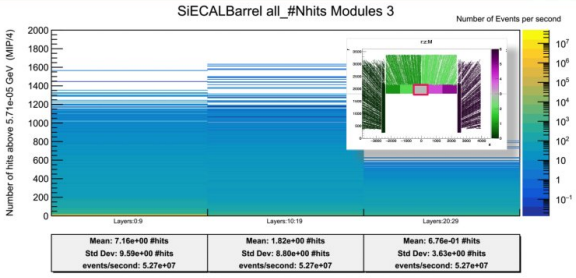


Take Home:

- Even at Z peak power dominated by pre-amp (⇔ conversion power in negligible)
- Tool is there, missing:
  - Digitization (easier way in Key4HEP ?)
  - Mapping needs to be adapted for each calorimeter readout topology

Results : Rates in Silicon ECAL Barrel, Central Module vs depth

Similar results for ScECAL, SDHCAL, AHCAL



Distributions of the number of hits crossing (MIP/4) energy threshold of all the physics processes and machine background at 91.2 GeV (FCC-Z4)
The z scale is the number of event/s

From the $\langle f_{Nhits} \rangle$ in one region one can extract :
- The data rate, knowing the number of bytes per hits (here 7 as a landmark)
- The occupancy, knowing the number of cell in the region.
- The power dissipated on elec. power (here for SKIROC2 like chip)

M3 all staves	L0:9	L10:19	L20:29
Average #hits/s	302E+6 hits/s	65E+6 hits/s	8E+6 hits/s
Max	2000 hits/event	2500 hits/event	1000 hits/event
Data rate	2,11E+9 B/s	458E+6 B/s	54E+6 B/s
Ncells	4 026 764	3 767 273	3 378 036
Occupancy/BX	**1,4 E-06**	**3,3 E-07**	**4,3 E-08**
Base power/W	18,2 E+03	17,1 E+03	15,3 E+03
Conversion power/W	271,4 E+00	58,9 E+00	6,9 E+00
Total power/W	**18,5 E+03**	**17,1 E+03**	**15,3 E+03**
% conv.	1,5 %	0,3 %	0,05 %

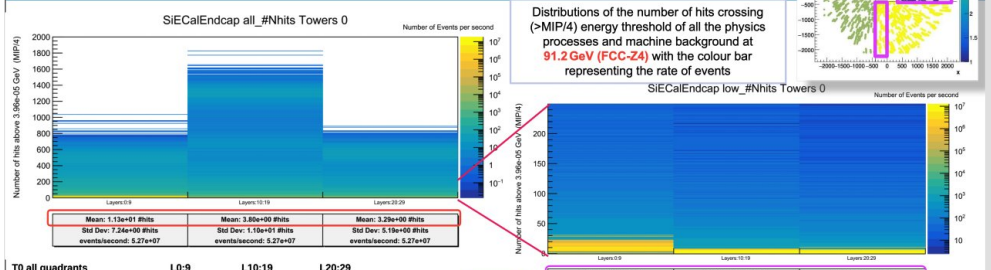
cell size	5,5
Bytes/hit	7
powa (W/cell)	4,5 E-03
powb (J/hit)	8,7 E-10
Conv & RO E/hit/μJ	9,0 E-01
Δt/s	19 E-09

- **Most of the hits are in the first third of the calorimeter.**
- **Highest average rates L0:9**
- **Highest max rates in L10:19**

Note 1 : (still) **preliminary**
Note 2 : Rates & Power for all M3 modules
→ 8 per module, 10 per layer for 1 slab
→ ~ 50 W/slab

Results: Rates in SiECAL EndCaps, Tower 0 vs depth

Similar results for ScECAL, SDHCAL, AHCAL



Distributions of the number of hits crossing (>MIP/4) energy threshold of all the physics processes and machine background at 91.2 GeV (FCC-Z4) with the colour bar representing the rate of events

T0 all quadrants	L0:9	L10:19	L20:29
Average #hits/s	572E+6 hits/s	176E+6 hits/s	147E+6 hits/s
Max	2000 hits/event	2500 hits/event	1000 hits/event
Data rate	4.00E+9 B/s	1E+9 B/s	1E+9 B/s
Ncells	1,161,775	1,161,775	1,161,775
Occupancy/BX	**9.4E-06**	**2.9E-06**	**2.4E-06**
Length/Width	2496		565
Base power	5E+03	5E+03	5E+03
Conversion power	515E+00	159E+00	132E+00
Total power	**6E+03**	**5E+03**	**5E+03**
% conv.	8.9 %	2.9 %	2.45 %

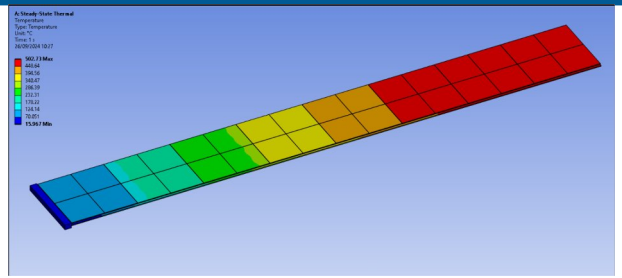
cell size	5.5
Bytes/hit	7
powa (W/cell)	5E-03
powb (J/hit)	870E-12
Conv & RO E/hit/μJ	0.9
Δt	19E-9

- **Machine background in first layers**
- **High E ee→ee in middle of ECAL**
- **Power driven by the continuous part (Pre-Amps)**

Note 1 : (still) **preliminary**
Note 2 : Rates & Power for all T0 modules
→ /8 per quadrant, *10 per layer for 1 slab* → 75W / slab

ECAL adaptation : flat cold plate, preliminary thermal studies

Uniform solutions:



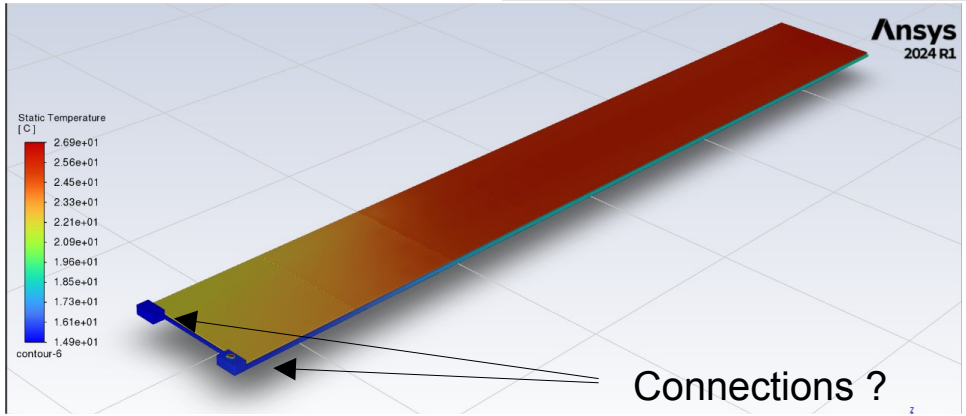
“Standart Slab”:

- 8 ASU (1440mm)z, 8192 ch / 128 ASICs
- 100 W

Passive cooling: Cu of 2mm (W, C ignored)

Adiabatic, but for heat bridge at the end

ΔT = 500°C on Wafer surface at $t = \infty$



Status:

- Limited flow of water seems enough…
- Now looking into pipe in 4-mm Cu layer
  - Replaces W in 1st half of SiW-ECAL
  - Replaces ½ the W in the second part
- To be validated on simulations

“Standart Slab”:

- 8 ASU (1440mm), 8192 ch / 128 ASICs
- 128 W (1W/ASIC ~16 mW /ch)

Active cooling:

- Hollowed Cu of 4mm, with 1 ℓ/min of water @ 15°C

Adiabatic, but for heat bridge at the end

ΔT = 12°C on Wafer surface at $t = \infty$

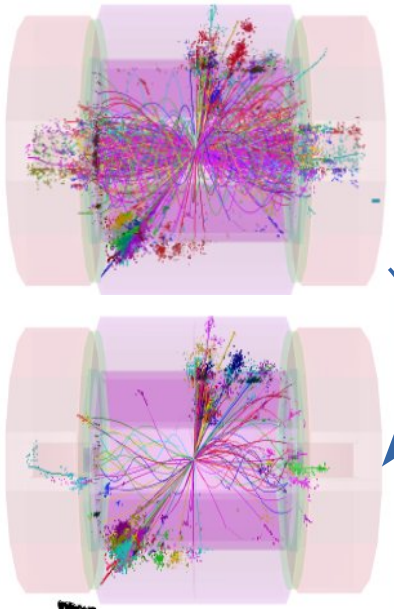
Centimetric Timing

Timing in Calorimeters: 0.1–1 ns range

1 cm/*c* = 30 ps

Started in KIT, JGU, IJClab, LLR and IP2I (Lyon): Calo5D & T-Calo

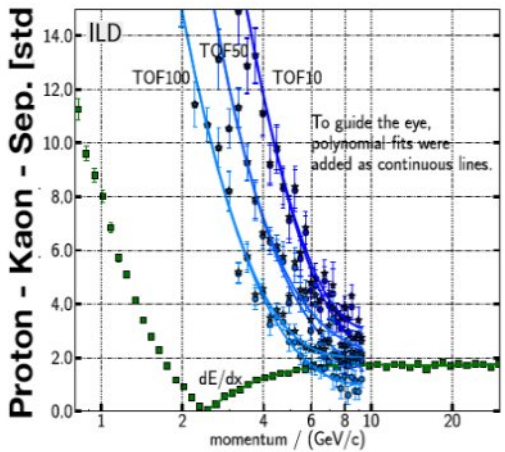
Cleaning of Events



[CLIC CDR: 1202.5940]
adapted from L. Emberger

Particle ID by Time-of-Flight

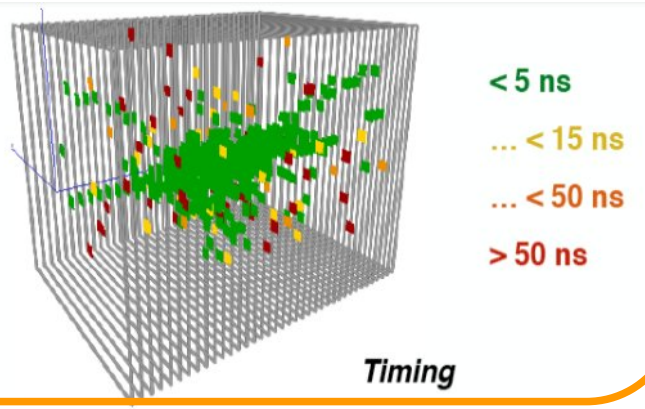
- Complementary to d*E*/d*x*
  - Here with 100 ps on 10 ECAL hits



S. Dharani, U. Einhaus, J. List

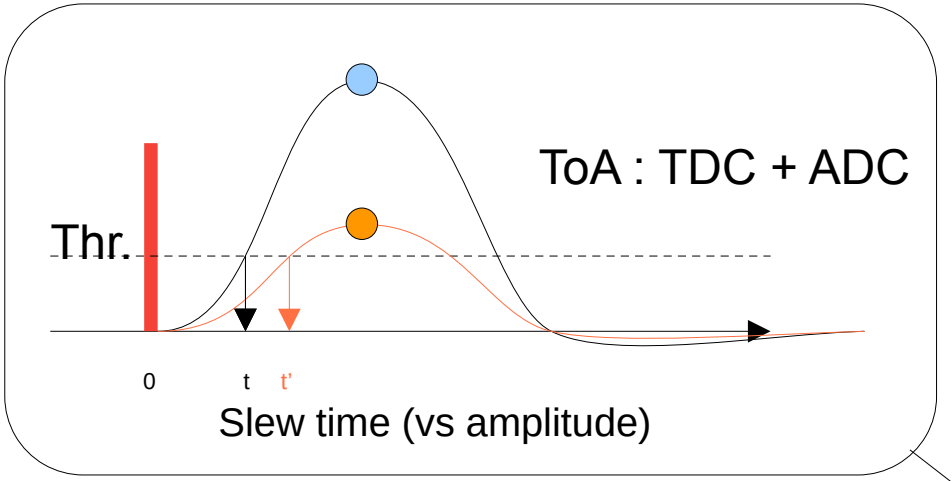
Ease Particle Flow with $\mathcal{O}(30)$ ps ?

- Cleaning of late neutrons & back scattering (ns)
- $\mathcal{O}(30)$ ps for mips… HGCAL / 100!
- Identify primers in showers
- Help against confusion *better separation of showers*
  - Requires '4D clustering'

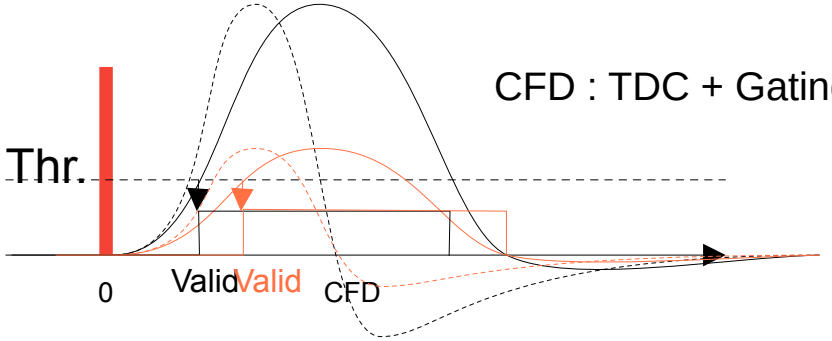


Ch. Graf

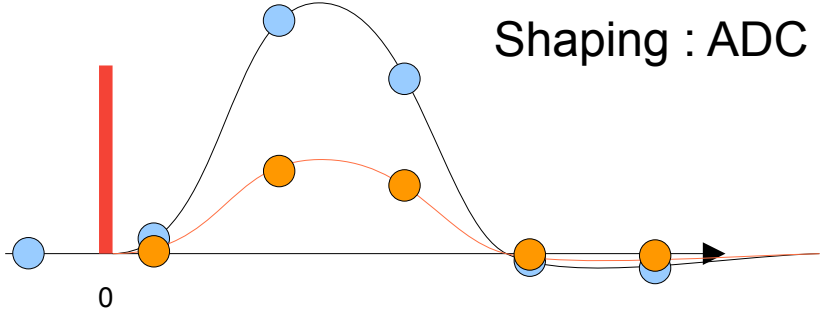
Time measurement methods



Slew time (vs amplitude)



Time ~ cst (vs pedestal, noise)



Time fit (vs shaping)

In SKIROC2. Validation of digi on beam tests…

Conclusions

SiW-ECAL technological prototypes

- **2022:** Heterogeneous 15 layers
  - 1st full calorimeter working [DESY22, CERN22]
    - Shower seen, Detailled simulation ready
    - Analysis on-going ➞ resolutions, …
  - Numerous emerging issues
    - gluing, HV filtering at high energy
- ~~**2024**~~ **2025–26:** Uniform 15 layers
  - ➞ New VFE boards
    - Cleaner PS & Clock distributions; more uniform
  - Gluing being revisited
  - Material available.
  - To be tested in 2025
    - ➞ Provide reference sample for GEANT4
    - ➞ With funding ➞ "full" **LUXE**, **EBES**, Lohengrin ?, **SHiP** ?
  - Start FE board on HKROC ?

SiW-ECAL design for HET factories

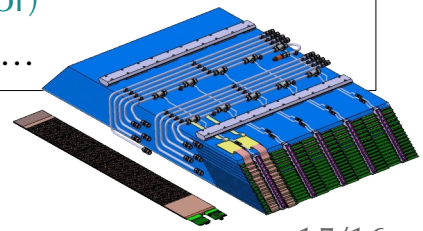
– **2023–25**: Power budget & performances to be re visited

- Occupancy, power, data fluxes (on-going)
  - ➞ Granularity; Passive or Active cooling
  - ➞ new ASIC attributes (← CALOROC Pres Dulucq)
- 2025–27: PFA & Timing & Physics performances

2025–27 : Blue-print for a SiW-ECAL detector for the next ee collider

➞ planning for a **pilote module** @ T_0 collider-8y -5y (1 Mch, 1/60th of real detector)

semi-industrial, quality, ASICs, …



DRD 6: Calorimetry

Proposal Team for DRD-on-Calorimetry

November 15, 2023

	Milestone	Deliverable	Description	Due date
Task 1.1: Highly pixelised electromagnetic section				
Subtask 1.1.1: SiW ECAL		D1.1	Revised 15 layer stack	2024 +1
	M1.1		Specifications for timing and cooling	2025 +1
		D1.2	Engineering module for Higgs factory	>2026 +1

Planning towards a pilot module… *just in case*