The IDROGEN System

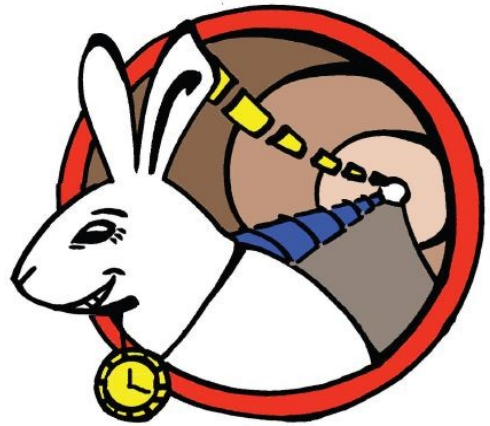
A high data rate acquisition system synchronized by an enhanced White Rabbit node

- IJCLab : Scientific themes : Astroparticles, Astrophysics & Cosmology, Nuclear physics, High Energy Physics, Accelerator Physics, Theory, Heath, Energy
  - Daniel Charlet, Antoine Back, Cédric Esnault, Christelle Soulet, Monique Taurigna, Chafik Cheikali, *Gaetan Seuillot, *Mathias Vecchio, *Sid Ali Cherrati
- Paris Observatory : Scientific themes : Time and frequency metrology, time and frequency transfer, inertial sensors, space-time reference frames, theory, epistemology
  - LTE : Paul-Eric Pottie, Michel lours
  - Obs Nancay : Cédric Viou

Agenda

- The functioning of the White Rabbit
- The IDROGEN System
  - Master board
  - Additional functionalities
- Last results on different setup

Timing and synchronization solution : WhiteRabbit

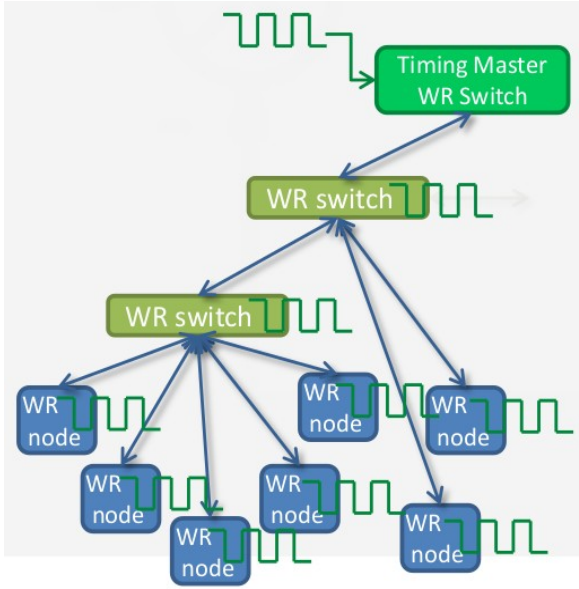


- Optical link
- System synchronization
  - Precision Time Protocol (IEEE1588)
  - Synchronous Ethernet
  - DDMTD Phase tracking (Digital Dual Mixer Domain)
- Time propagation compensation
- Large area and node number (+1000)
- Jitter stability:
  - Our work: hardware and firmware re-design
  - Special care on every clock signals

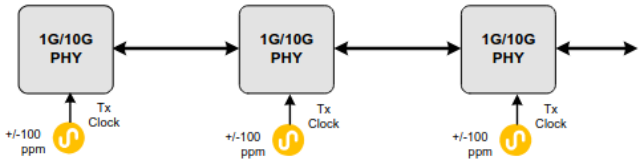
- Delivering signals
  - Synchronous clock : 10MHz
  - Pulse Per Second
  - Absolute Time Tagging : 1s

TECHNOLOGY OVERVIEW : Synchronous Ethernet (Sync-E)

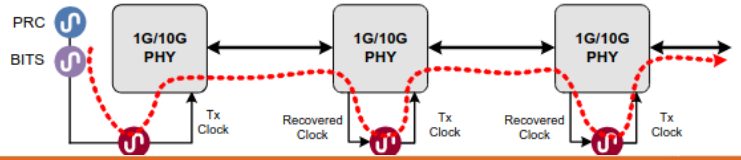
- All network nodes use the same physical layer clock
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip (PHY)
- A master and unique clock for the whole network
- High precision clock definition, 20 times better than standard Ethernet
  - ~ 10ns of StdDev at 10MHz no SynchE
  - ~ 400ps of StdDev at 10MHz with SynchE



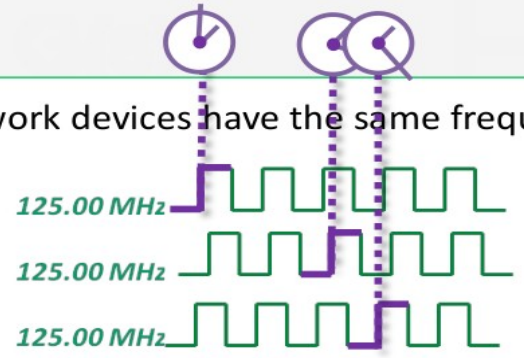
Packet Transmission using Asynchronous Timing



Packet Transmission with SyncE Physical Layer Timing Distribution

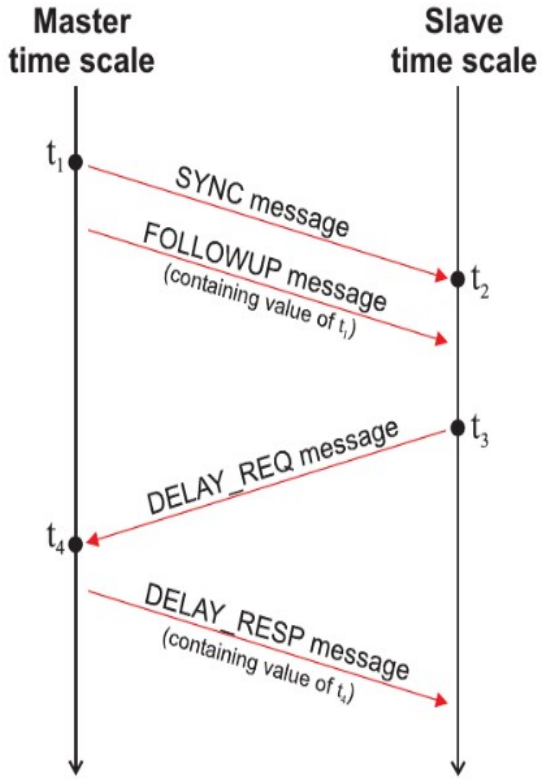


- All the network devices have the same frequency!



TECHNOLOGY OVERVIEW : Precision Time Protocol (PTP)

- Packet-based synchronization protocol
- Synchronizes the local clock with the master clock by measuring and compensating the delay introduced by the link
- Link delay evaluated by measuring and exchanging tx/rx timestamped packets
- PTP is used only for clock offset compensation



Having the values of t1 … t4 , the slave can:

- calculate the one-way link delay:

  $\delta ms = ((t4 - t1) - (t3 - t2)) / 2$

- syntonize its clock rate with the master by tracking the value of

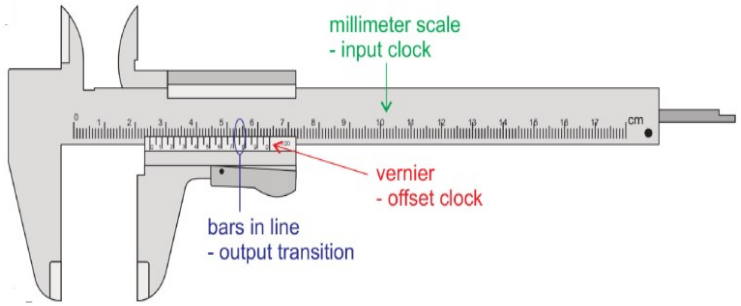
  $t2 - t1$

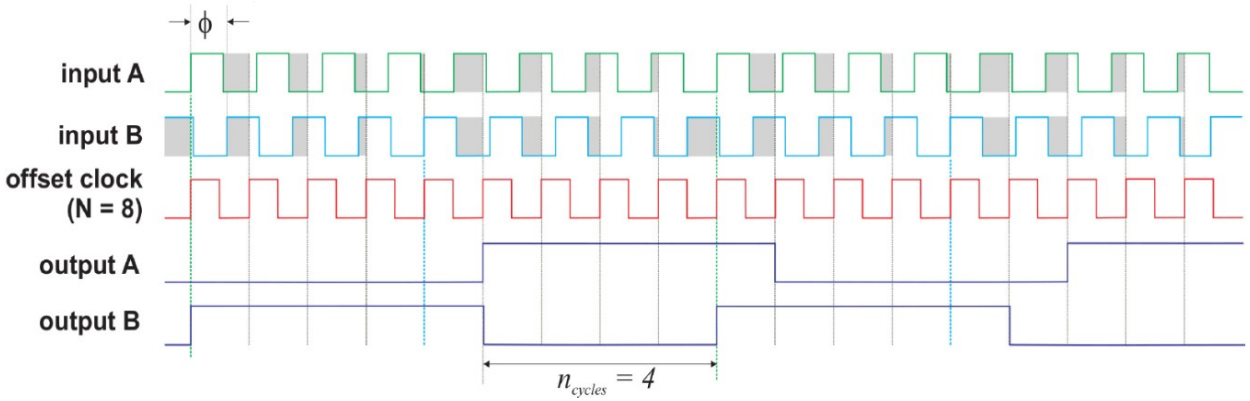
- compute the clock offset:

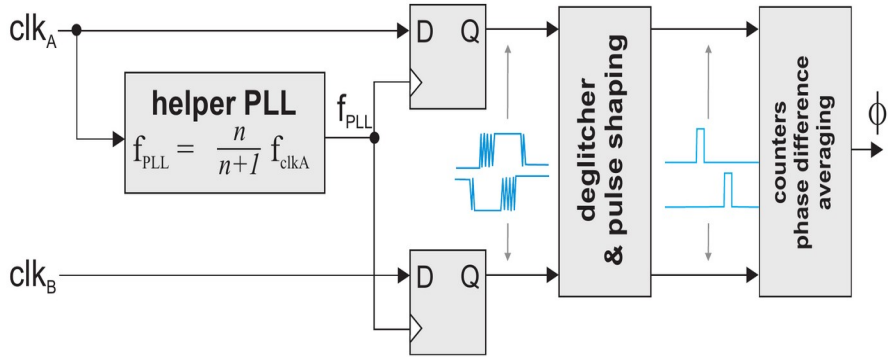
  $offset = t2 - t1 + \delta ms$

TECHNOLOGY OVERVIEW : Digital Dual Mixer Time Domain

- Measurement of the phase shift between transmit and receive clock on the master side, taking advantage of Synchronous Ethernet
- Continuous phase monitoring of bounced-back clock
- Phase-locked loop in the slave follows the phase changes measured by the master packet-based synchronization protocol







On the shelf White Rabbit solution

https://safran-navigation-timing.com/solution/white-rabbit-solutions/

Safran technology ensures deterministic Ethernet performance across large networks, making it ideal for applications, such as FinTech and Data Centers, that require real-time data transfer. With Wavelength Division Multiplexing (WDM), our solutions provide scalability and efficiency in synchronization.

White Rabbit Z16

- Sub-nanosecond Time Accuracy
- Multi-Source Time References
- 16 Optical Timing Ports for WR, PTPv2 and NTP

White Rabbit ZEN TP-FL

- Sub-nanosecond Time Accuracy
- 4x1PPS expansion / 8x1PPS expansion boards
- Remote configuration and monitoring

White Rabbit ZEN TP-32BNC

- Sub-nanosecond Time Accuracy
- Robustness & Redundancy
- 32 BNC configurable outputs

WR0X

- Adds White Rabbit interface to SecureSync
- PTP: Compliant with IEEE1588v2
- 1 G and 10 G configurations

High Accuracy Timing IP Core (HATI)

- Sub-Nanosecond Time Accuracy
- Easily Integrable and Compatible with Multiple FPGA Families
- Deterministic Delivery of Timing Information

White Rabbit PTP License

- WR to PTP Protocol Interoperability
- Synchronize Network Via WR & PTP Timing Protocols
- Sub Nano Second Accuracy

White Rabbit Switch – Low Jitter

- Sub-Nano Second Time Accuracy
- Time & Frequency Distribution
- Improved Clock Jitter and Phase Noise

White Rabbit Switch v3.4.

- Sub-Nano Second Time Accuracy
- Time & Frequency Distribution
- 18 SFP 1GbE ports

White Rabbit LEN

- Sub-Nano Second Time Accuracy
- Distance Range: Over 80km Using Fiber
- Dynamic Calibration

http://www.synctechnology.cn/en_detaile.aspx?ClassID=1

信科太 SyncTechnology Sync (Beijing) Technology

Tel：0086-13070165776

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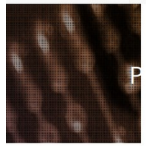
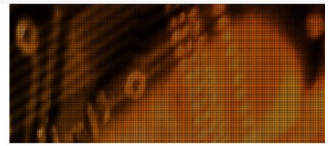


WRS-18

WRS-CM

Cute-WR-A7

WR-TB-410



PRODUCTS

- WRS-18
- WRS-CM
- Cute-WR-A7
- WR-TB-410
- WR-PKG

WRS-18 LOCATION: HOME > PRODUCTS

信科太 SyncTechnology

WRS-18

Introduction

WRS is the central element of a WR network, it can connect multiple WR nodes or WR switches.

Features

IDROGEN mother board

IDROGEN Key concepts

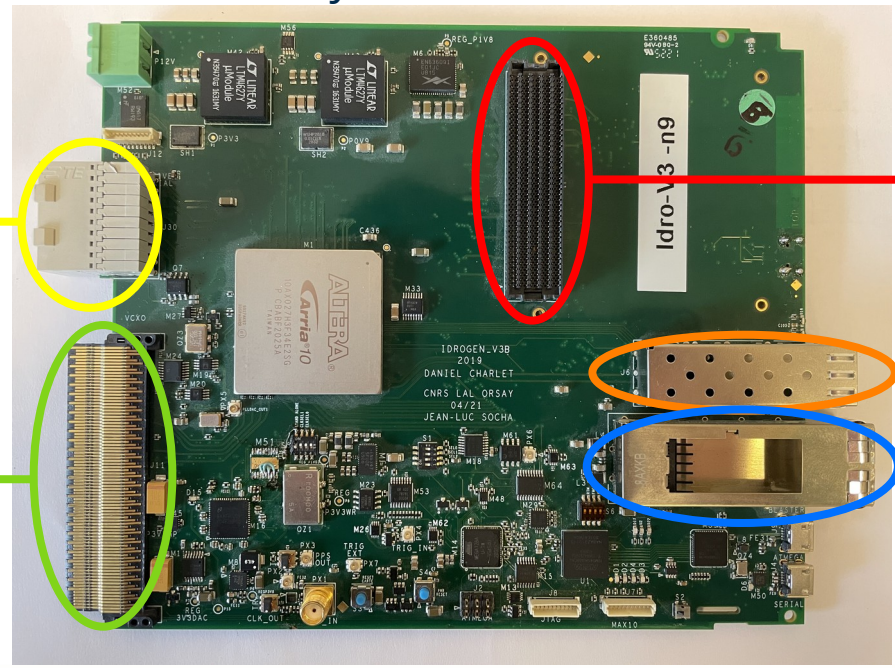
- A new architecture where all signals generated by the board are synchronous with the master clock.
- In addition, the master clock can be synchronized by the WR protocol.
- In a network, all the boards are therefore synchronized to the grand master.
- High data rate acquisition system using standard protocols.
- Frequency generator.
- Fully re-configurable.

IDROGEN board v3

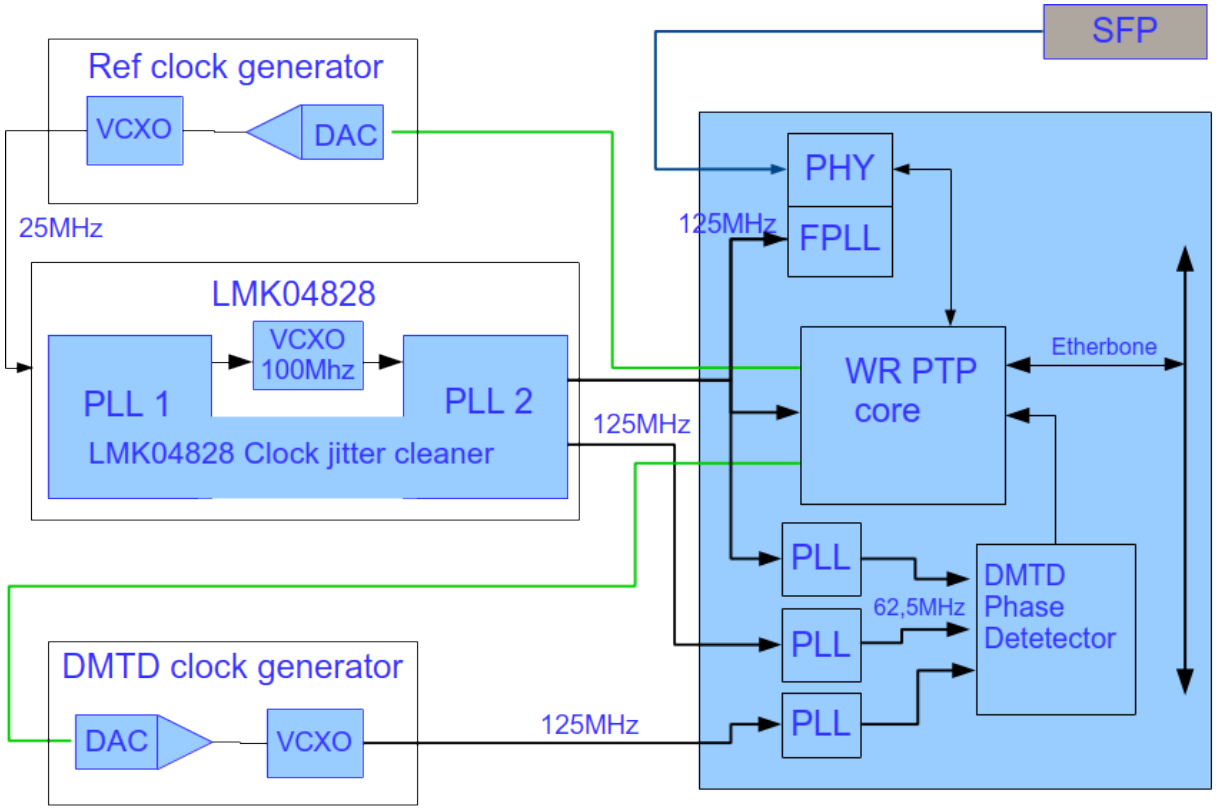
High speed data acquisition & Low phase noise WR node

- White Rabbit Design & development done by IJCLab (based on CERN schematic): Component upgrade and EMC design rules compliant → High stability timing distribution
- xTCA4.0 form factor board → Modularity

- Base on ARRIA 10 FPGA → High data rate transfer
- Standalone capability
- RTM extension boards
- FMC carrier board



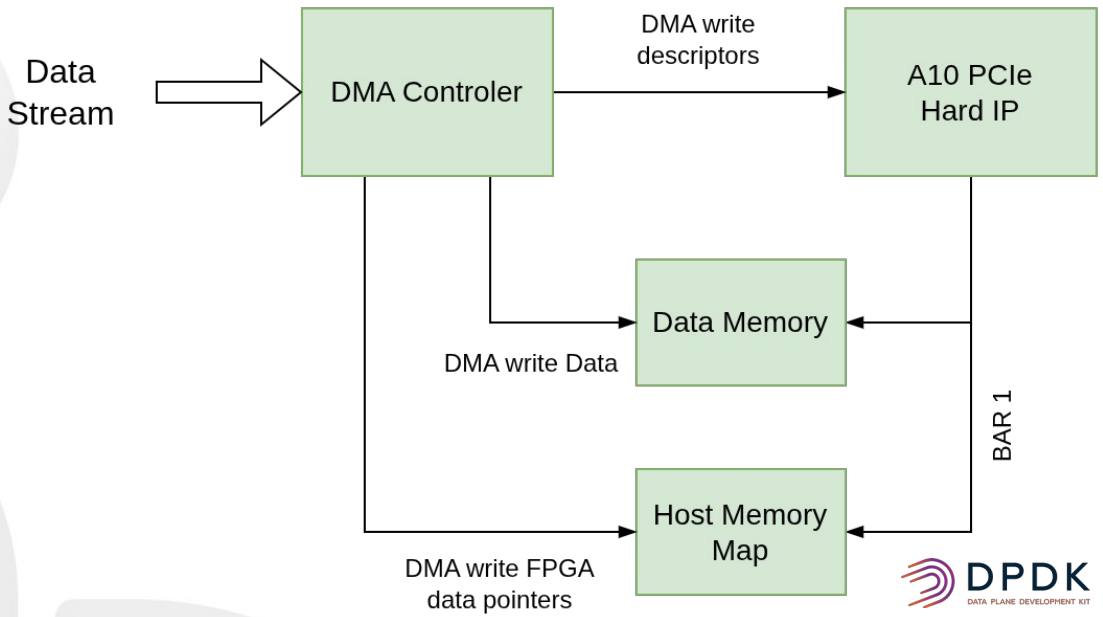
IDROGEN board : WhiteRabbit implementation



- Based on CERN open hardware with Enhancements
- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
  - Tx/Rx routing equalisation

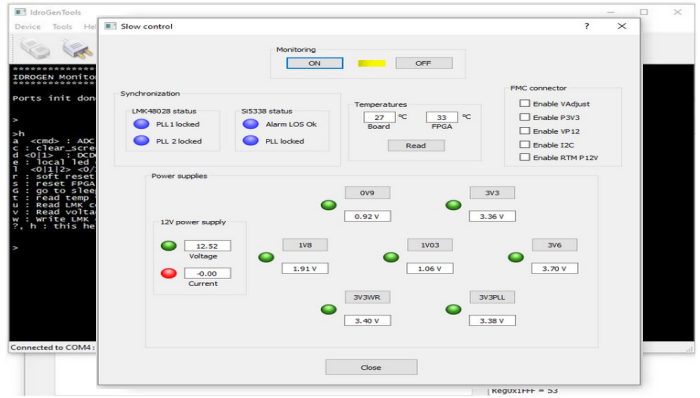
IDROGEN: Firmwares

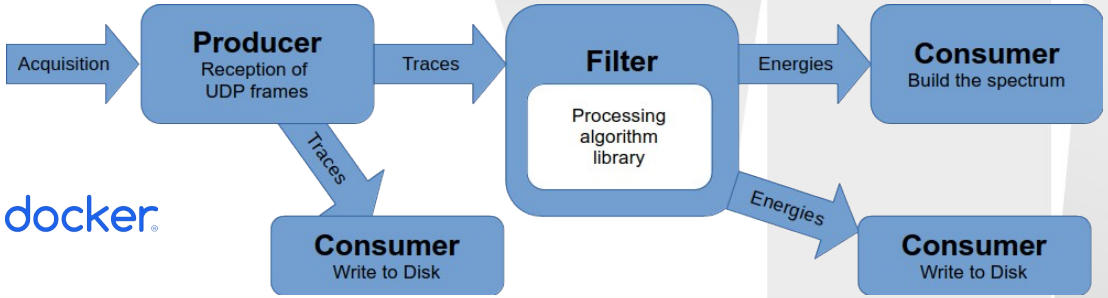
- Data transfer firmware
  - PCI-Express with DMA Gen3x4 (~25Gb/s)
  - GBT protocol (CPPM development for PCIe40)
  - IpBus 1G & 10G portage on Arria 10, from LPSC laboratory developments
  - UDP streamer 1G & 10G
    - Software C, Multi Jumbo frame by event
  - 2 x 10 Gb available, 40 Gb future development
- High speed ADC acquisition
  - JESD204B for (1G/500M/250M)
- Parallel 64 data acquisition
- White Rabbit core v4 & v5 porting on Arria 10
  - Master & Switch (on development)

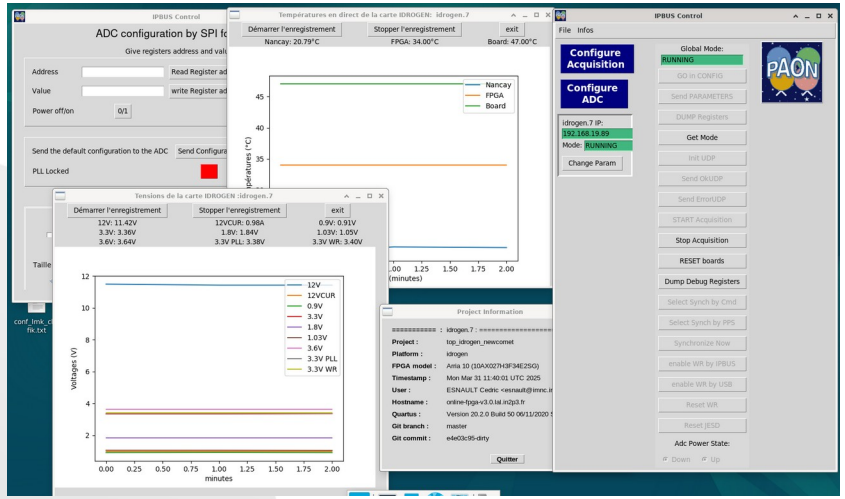


IDROGEN: softwares

- Configuration GUI tools over USB and Ethernet
  - Power, PLL, FMC and ADC configuration
- Monitoring GUI for power supplies and temperature monitoring
- Slow control library and tools (I2C, SPI, WR diagnostic, …)
- Frame viewer
- Acquisition software
  - Based on DCOD framework
  - Implement a generic processing algorithm interface (loading a dynamic library)
  - Based on widely used technologies (Docker, DPDK)





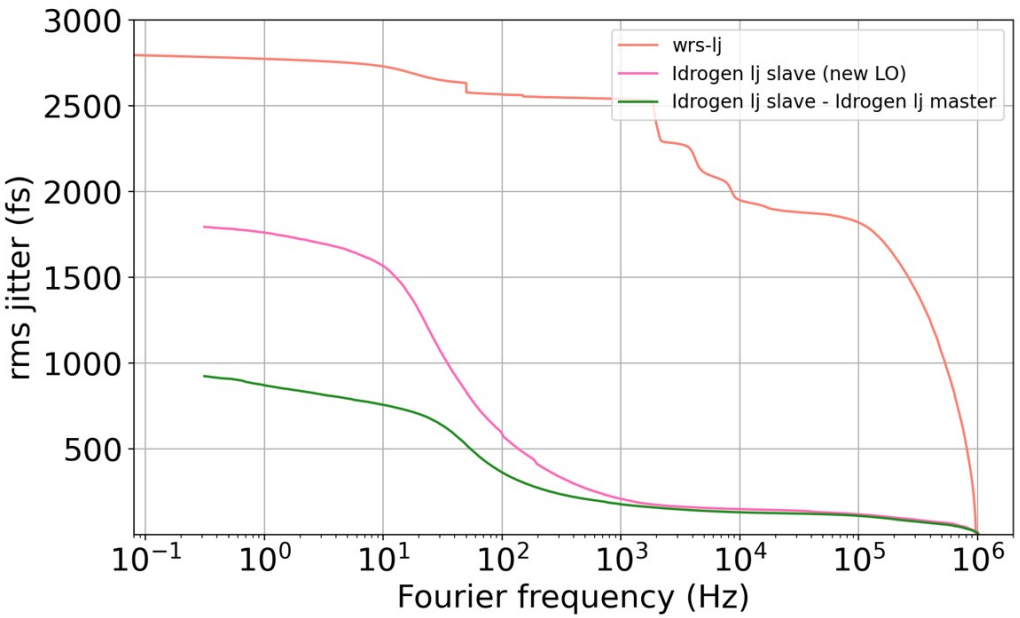


IDROGEN board: Timing performance

IDROGEN board performance

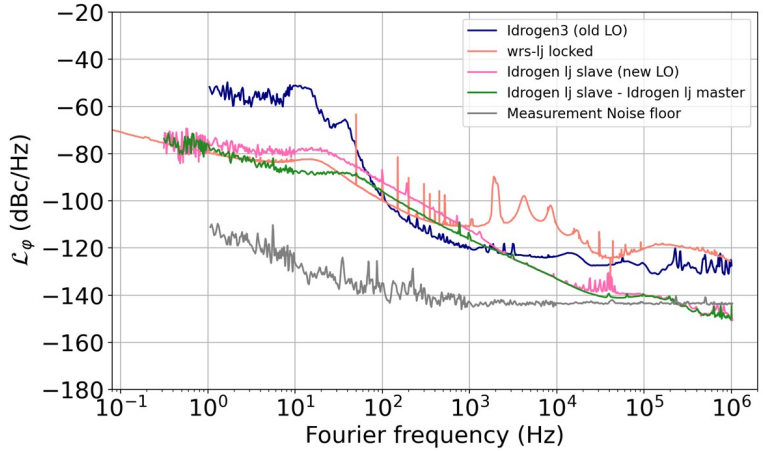
Phase noise measurement

Integrated jitter according to integration range



Variation of lower bound of integration range.
Upper bound fixed at 1 MHz

Phase noise measurement

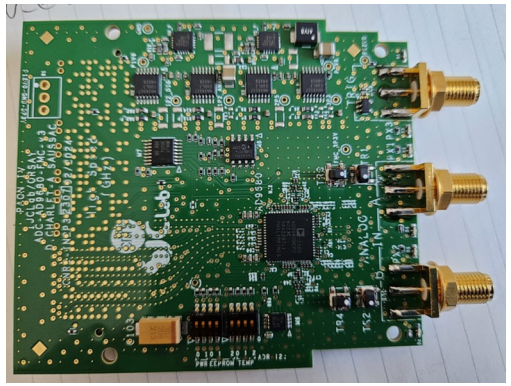


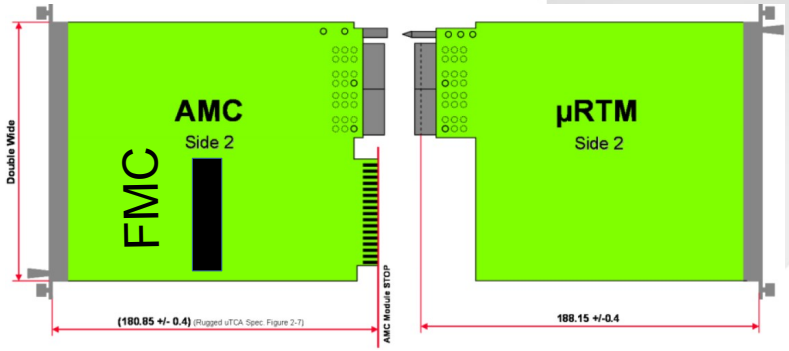
	1	10	100	1,000	10,000
wrs-lj	2 246	2 191	1 984	1 075	1 075
S	1 757	1 557	563	110	110
S-M	866	751	351	94	94
GM	445	439	432	129	129

Table 1: Integrated rms jitter expressed in fs for Idrogen and a wrs-lj, for integration bandwidth up to 100 kHz

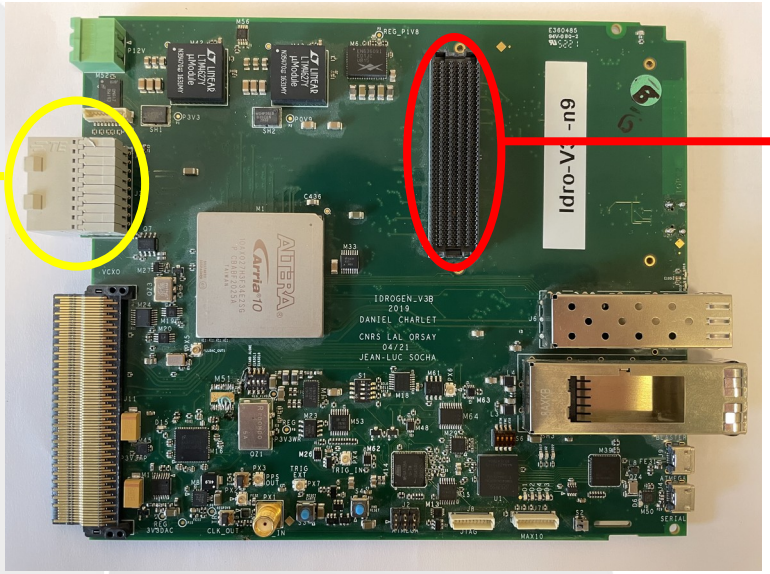
IDROGEN BOARD: 4x better than Switch
Low Jitter from Safran/Seven Solution

IDROGEN extension boards





RTM Connector

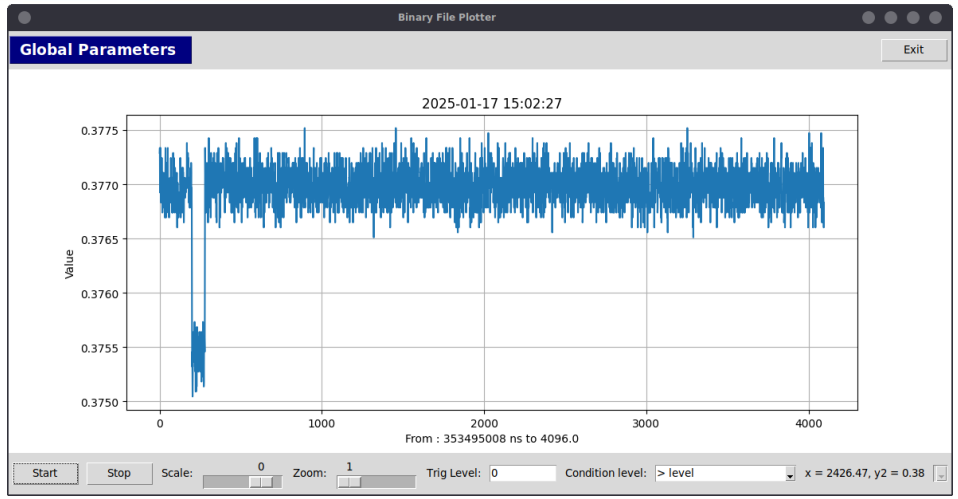


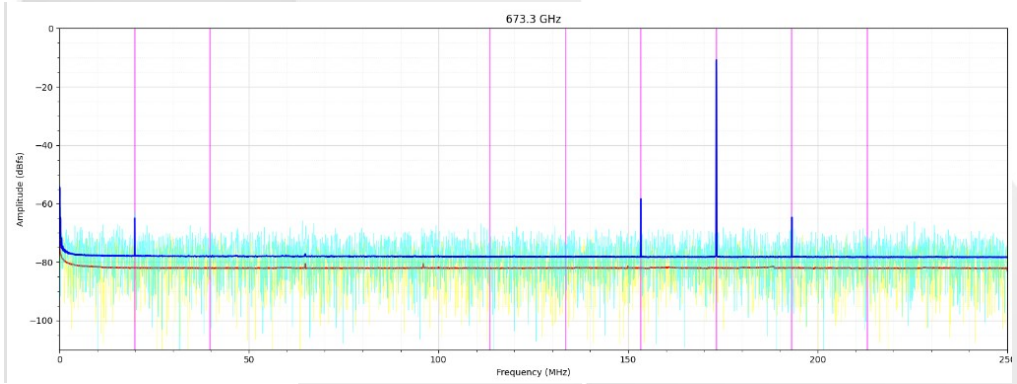
FMC Slot (ADC, DAC, clock synthesis, ...)

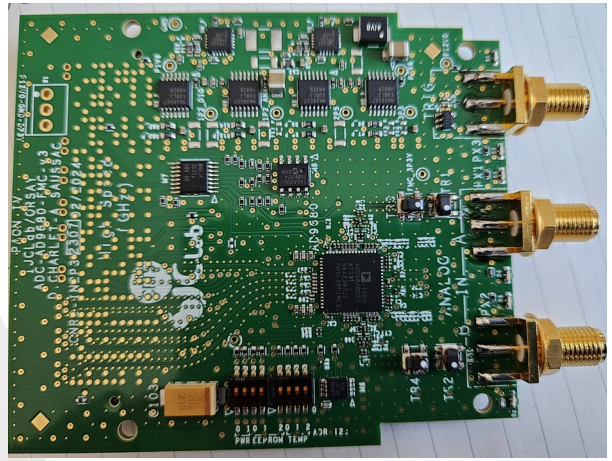
ADC acquisition board

Development of custom ADC board: Using the IDROGEN on board low jitter WhiteRabbit clock

- **FMC ADC9680_V1** **(**2022)
  - 2 channels, 500 MSPS, 14 bits
  - 2GHz analog bandwidth
  - Clock provided by Idrogen board
- **FMC ADC9680_V3** (2024)
  - 2 channels, 1 GSPS, 14 bits
- **FMC ADS42JB69** (2025)
  - 4 channels, 250 MSPS, 16bits
  - One external trigger
  - Analog input 900MHz
  - 2.5V inputs voltage







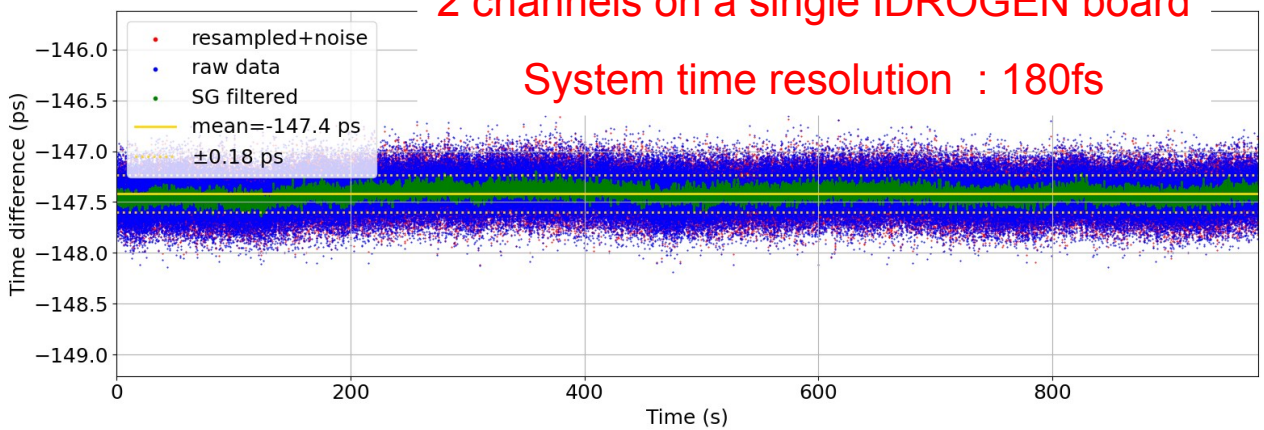
1GSPS ADC board: Synchronization performance

- Bandwidth (single board):
  ~500Mhz (1GHz → 1.5GHz)

- 2 IDROGEN boards synchronized by WR
- 2 channels 1GSPS 14b ADC
- Same RF signal (312.5MHz) split on boards
- FFT 8k point
- Cross correlation

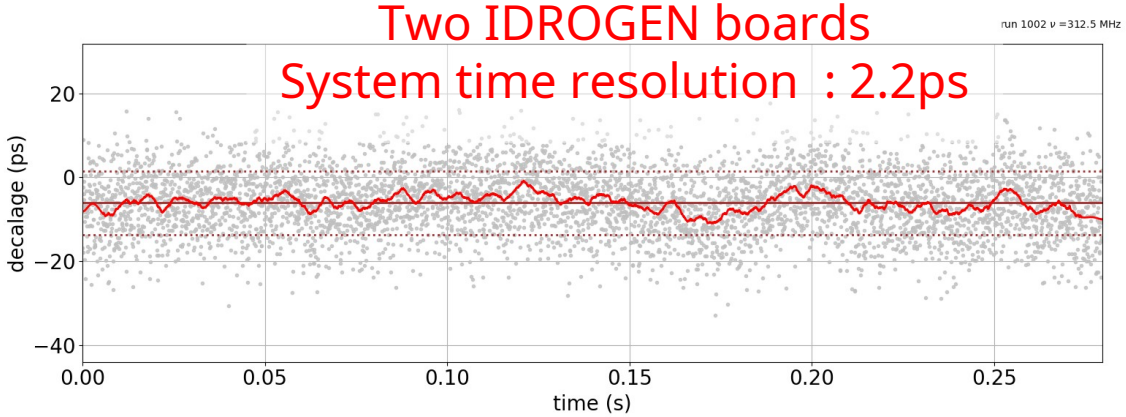
2 channels on a single IDROGEN board

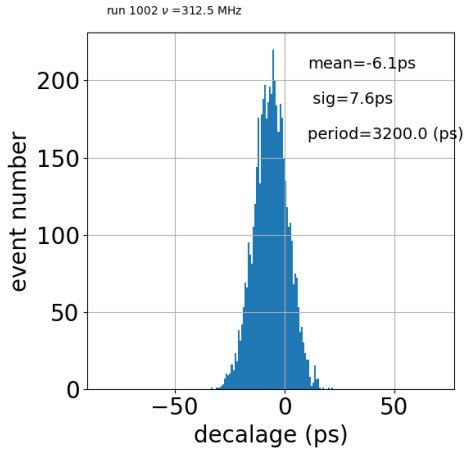
System time resolution : 180fs

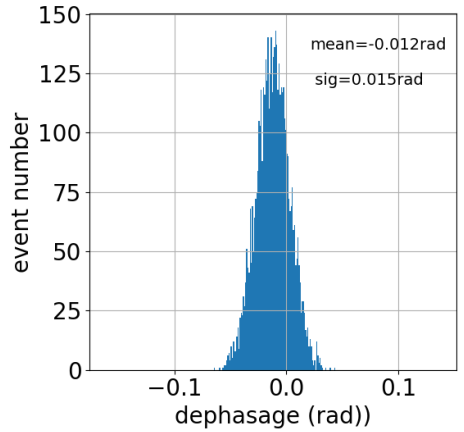


Two IDROGEN boards

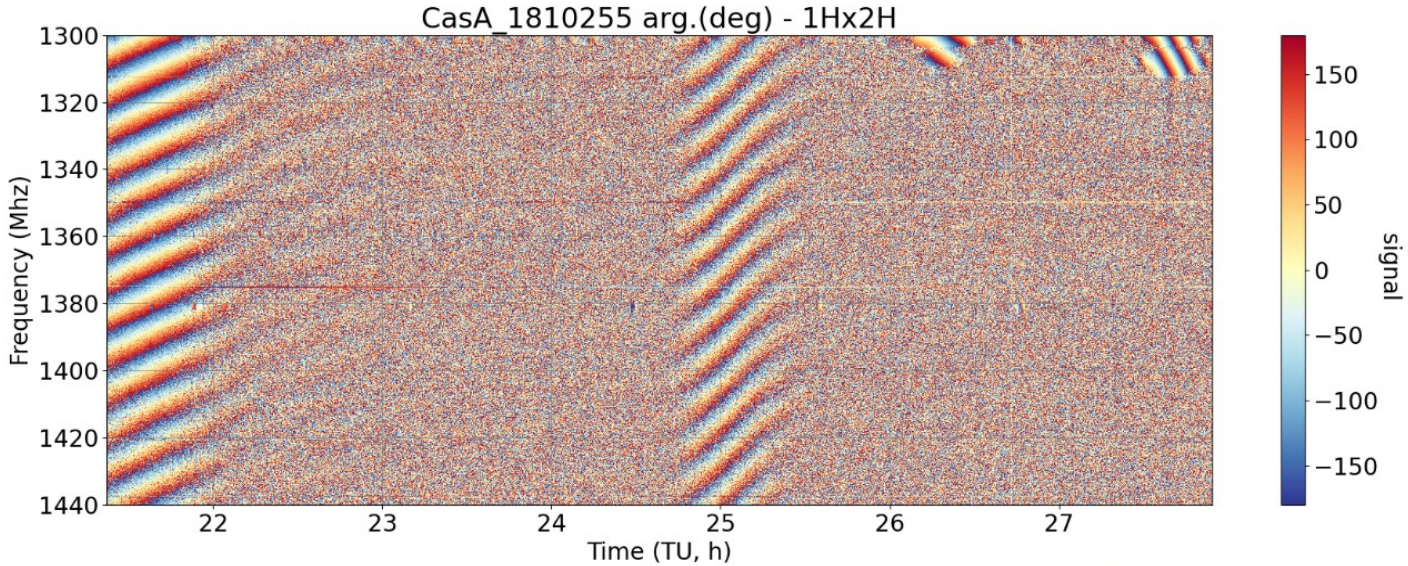
System time resolution : 2.2ps







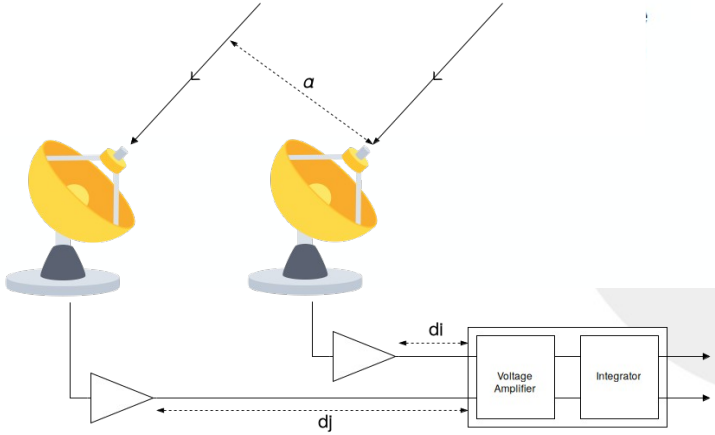
Radio Interferometer



Première acquisition astronomique directement raccordée à UTC(OP).

Au pied de deux antennes radio de l'Observatoire de Nançay (PAON IV), Idrogen3 est disciplinée par White Rabbit aux références temps-fréquence de l'Observatoire de Paris avec un lien de +300 km sur une paire de fibres partagées du réseau de télécommunication de RENATER (REFIMEVE). Une carte d'extension sur Idrogen3 réalise l'acquisition syntone et synchrone à 1Gb/s.

Crédits image : Olivier Perdereau.

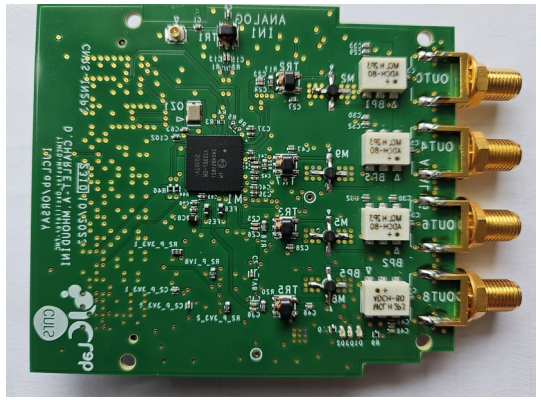


Typical configuration of radio interferometer

Accelerator synchronization: Arbitrary clock signal synthesizer

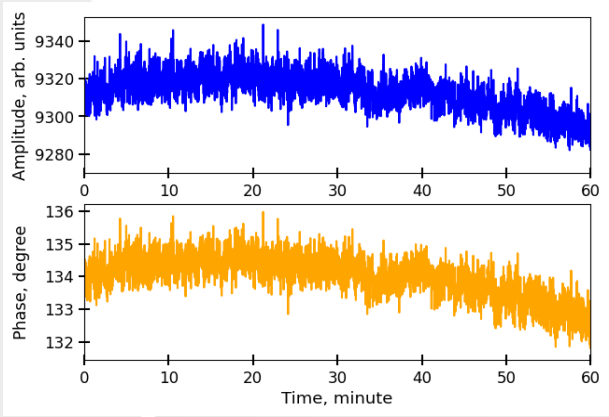
Fractionnal PLL (FPLL) FMC (on test)

- Replace very expensive system with recent, 30€ component
- Generate arbitrary frequency disciplined by WR clock
  - Frequency resolution 1 Hz
  - Phase noise system: 1.7ps (1 Hz, 10 MHz)
  - ~0.3° RMS phase jitter at 375MHz below 1Hz
  - 4 outputs 10KHz to 1.3GHz (2.75GHz: SI5361H chip)

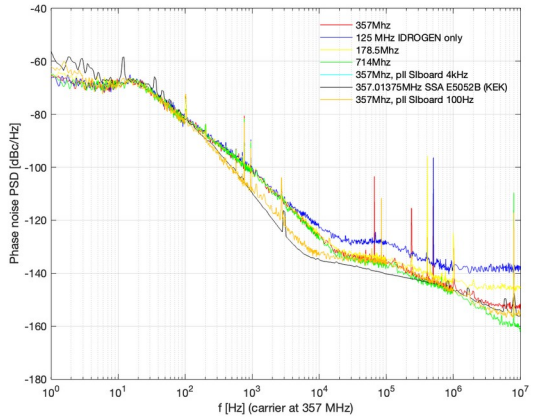


RTM board extension (under test)

- Arbitrary synthesizer
- High performance extension for optical time transfer (White Fox)



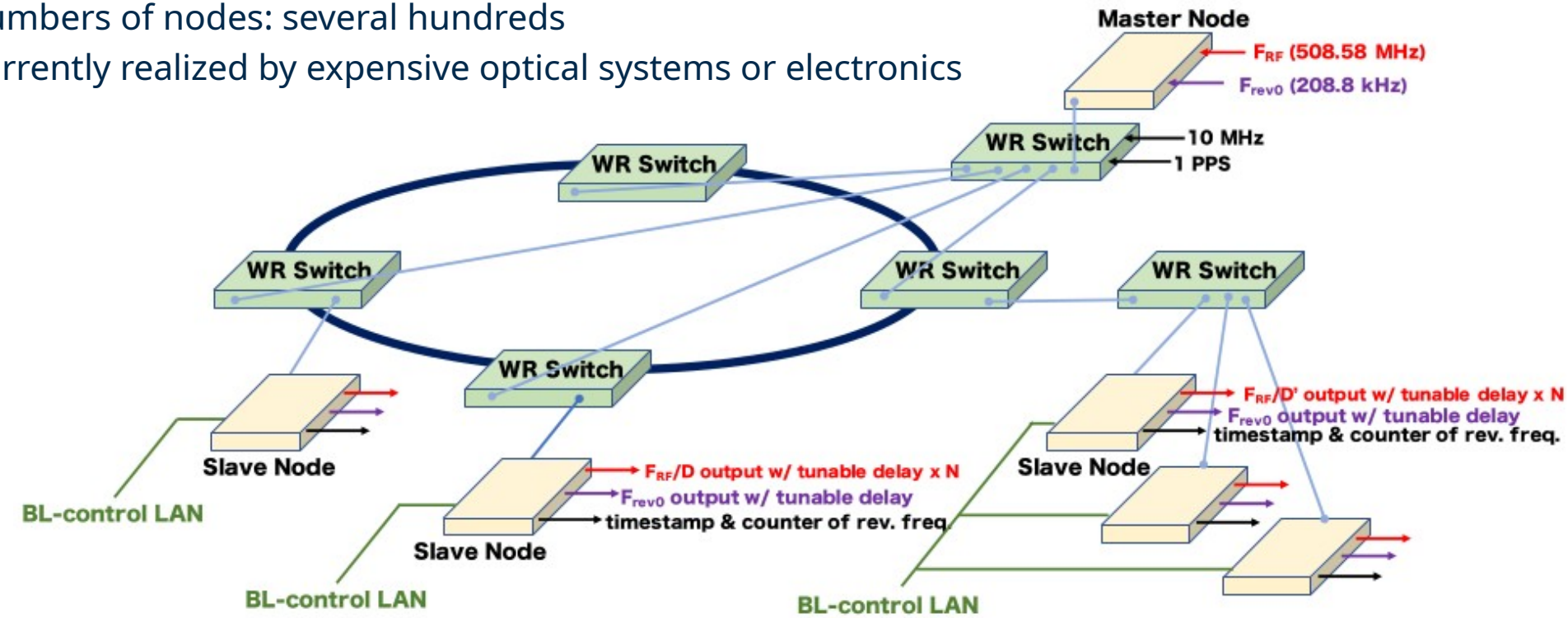
Long term drift



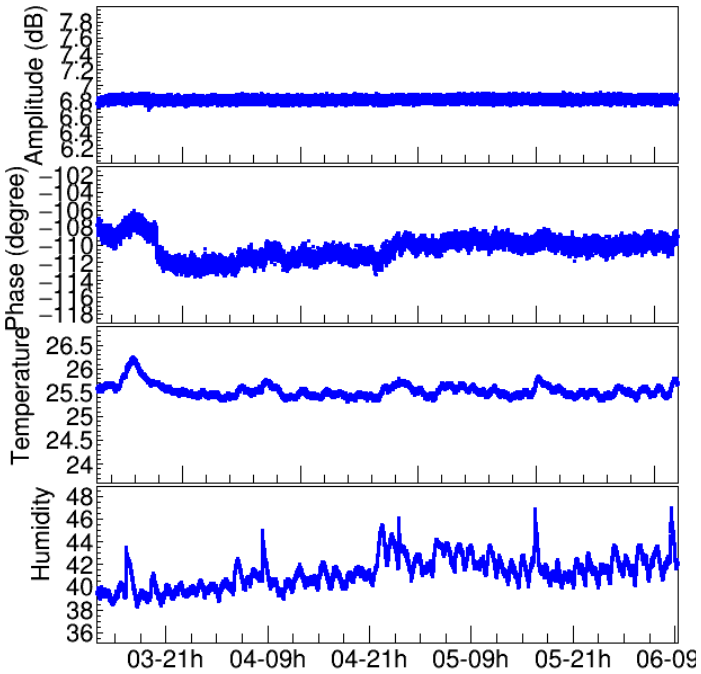
Phase noise for various different output frequencies

Accelerator : Master oscillator distribution

- Real-time communication system: tight time constraints
- Jitter stability (< 1ps)
- Monitoring synchronization
- Long distances between nodes (> 1km): long transmission delays
- Numbers of nodes: several hundreds
- Currently realized by expensive optical systems or electronics

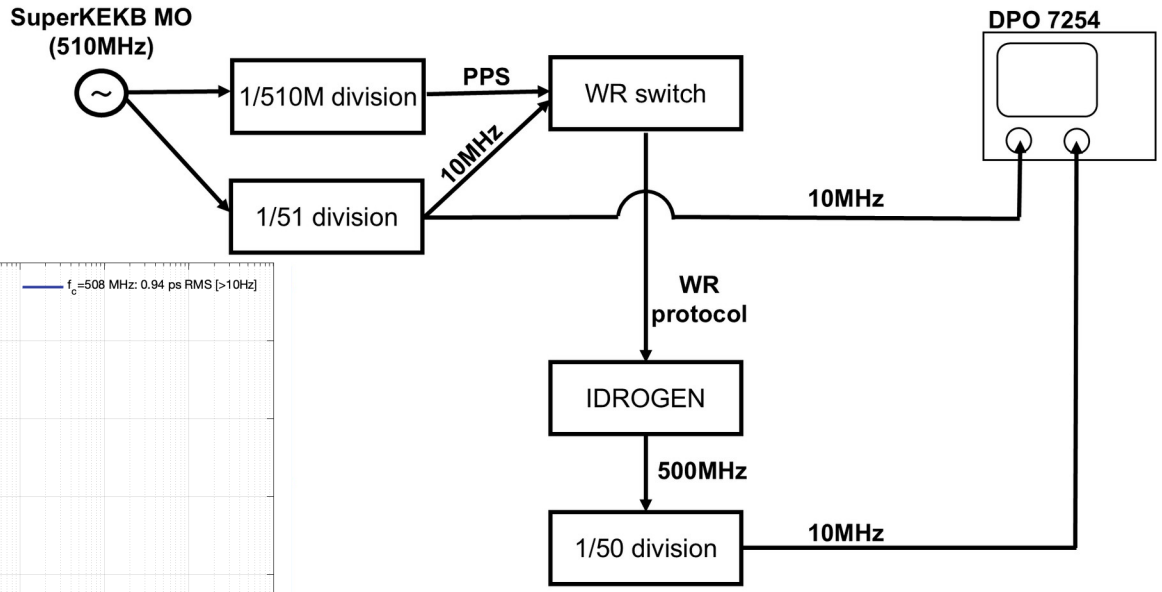


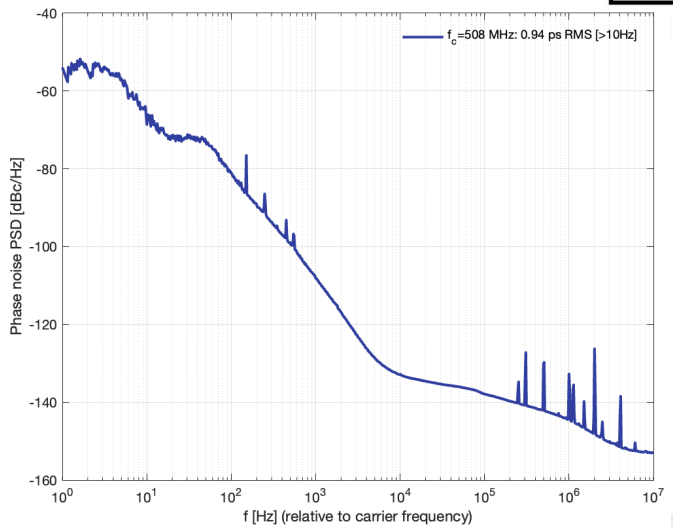
SuperKEKb : Master oscillator distribution



509Mhz

IDROGEN synchronization setup





Data taken from Sep22 19:10 to Sep24 12:00

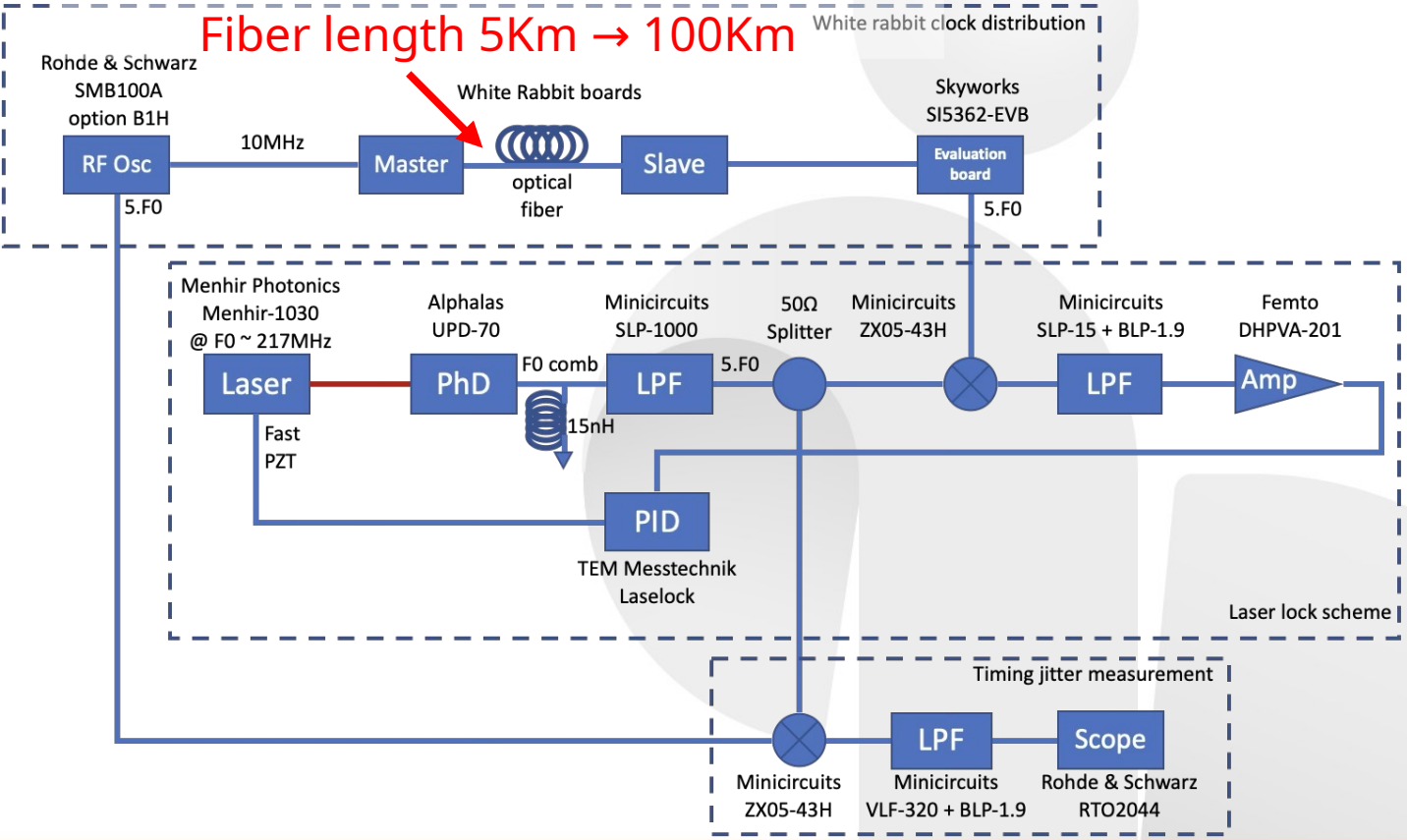
RMS jitter 10HZ → 10MHz

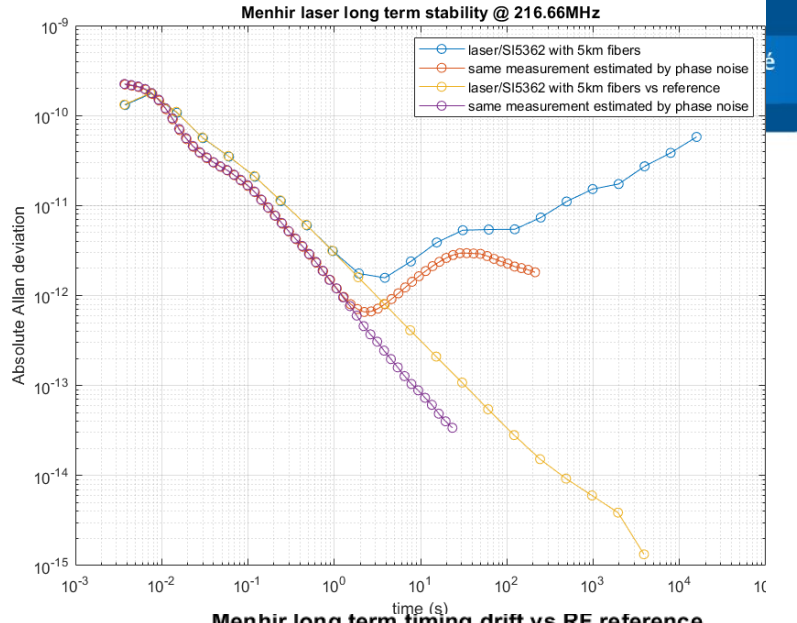
940Fs at 508 MHz

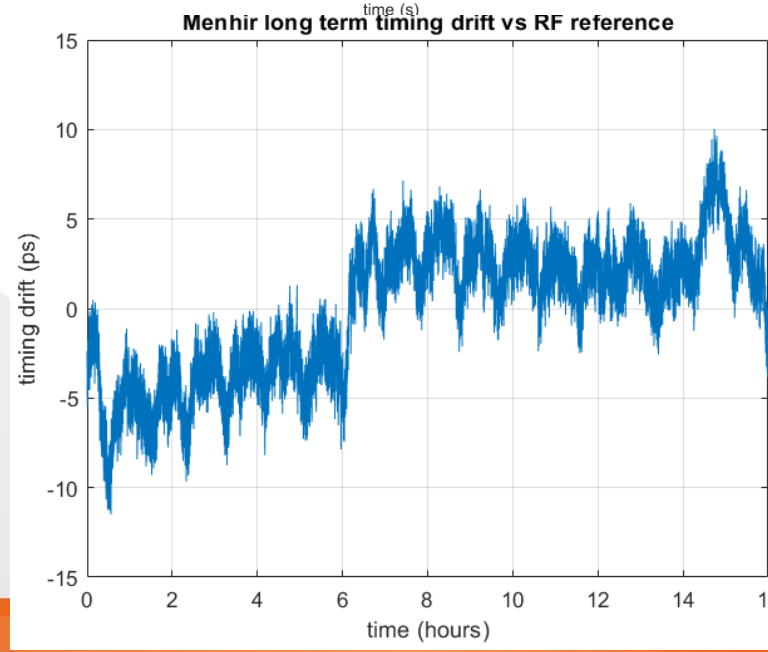
Lazer synchronisation

IDROGEN 1 : GM → IDROGEN 2 slave

Fiber length 5Km → 100Km







IDROGEN: roadmap and future directions

- IDROGEN_V4
  - Development for Q4 2025, mass production mid 2026
  - Replacement of obsolete components
  - Versatility Improvement
- FMC-AD42JB69 (in development)
  - 4 channels 250MSPS 16bits
- FMC-ADC 3GSPS
- White Fox (Highly improved White Rabbit)
  - Development with LTE
  - Sub 100-fs performance (prototype in development)
- Improve short term performance (ongoing development)
- 10Gb/s White Rabbit firmware
- IDROGEN_v5
  - New FPGA familly AGILEX

Conclusion

- Very promising results with IDROGEN board (sub-picosecond RMS jitter)
- New board version (v4) to address component obsolescence
- New projects: CTAO-MST, NENUFAR (Nançay observatory), ATF LLREF, KEK accelerators, New Comet (Nuclear physics @ IJClab),....
- Focus on essential hardware development
- Development:
  - low-frequency phase noise (low frequency)
  - White Fox project (jitter < 100fs) for future applications (FCC, Einstein Telescope,...)