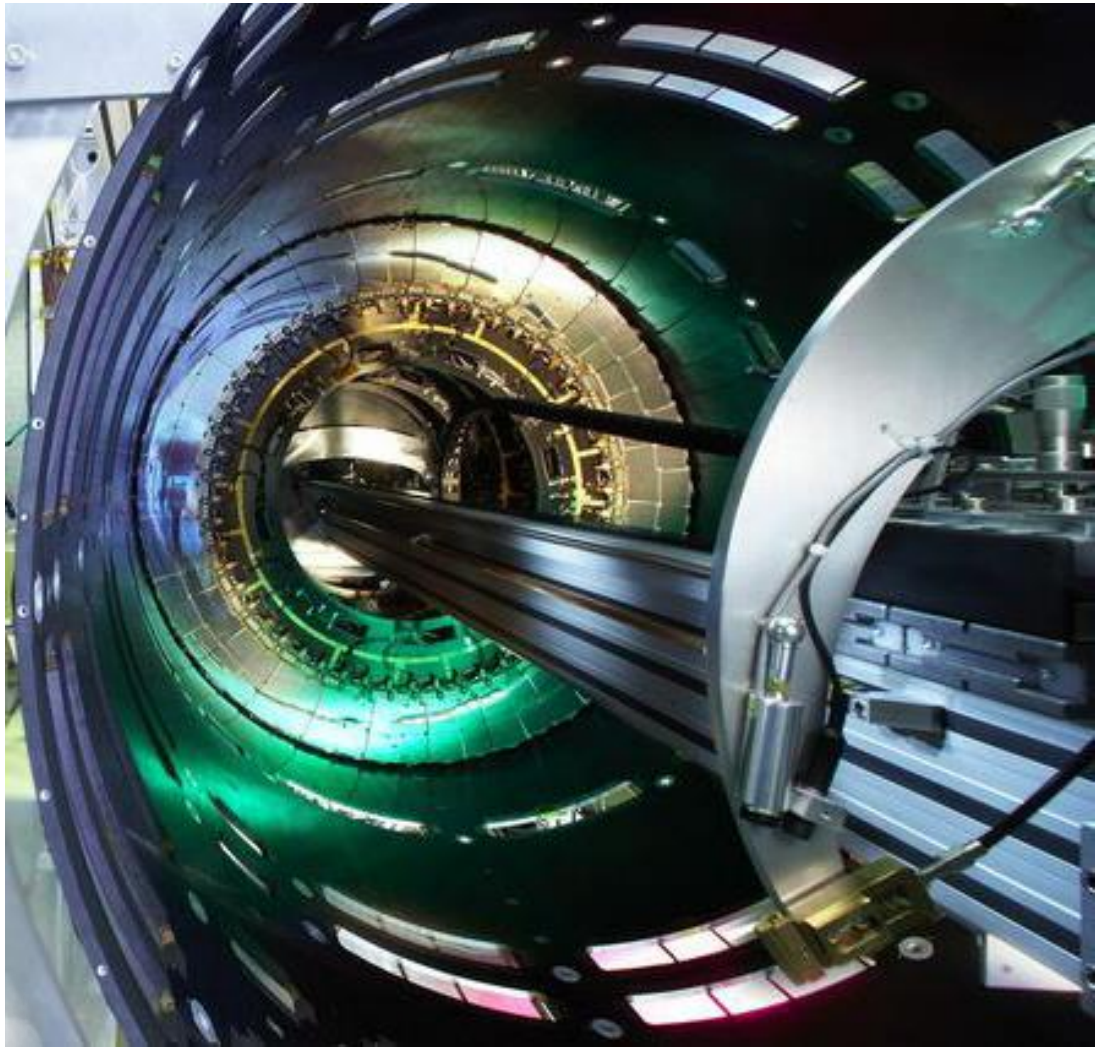
Silicon pixel detectors and module production for the ATLAS Inner Tracker (ITk)

Dmytro Hohov on behalf of the IJCLab-ITk team

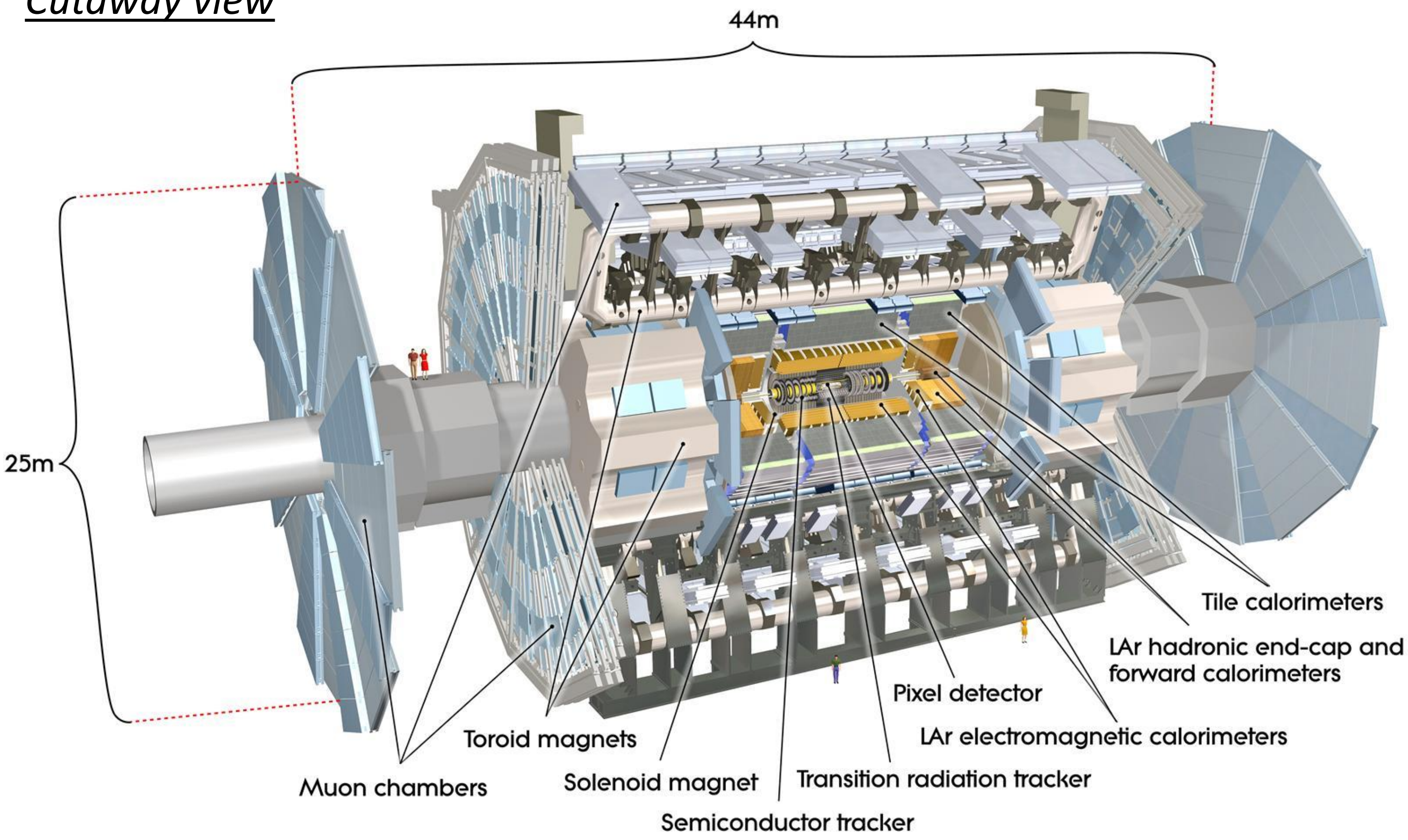
Outline

- ATLAS Detector and motivation for the ITk upgrade
- Silicon pixel detector technologies
- Towards ITk construction
- Module Assembly
- Module Testing
- Summary



ATLAS (A Toroidal LHC ApparatuS) Detector

Cutaway view



ATLAS multipurpose detector is 46m length, 25m diameter and 7000 tons, 100m below ground.

Sub-Detectors:

- **Inner Detector** (records tracks, measures momentum, vertices reconstruction)
- **Electromagnetic calorimeter (LAr)** (measures electrons and photons energy)
- **Hadronic calorimeter (TileCal)** (hadrons energy)
- **Muon spectrometer** (measures muon trajectories)

Upgrades for HL-LHC:

- **New muon chambers at the innermost part**
  - Trigger efficiency and momentum resolution improvements
- **High Granularity Timing Detector (HGTD)**
  - Improved pileup suppression at the forward region
- **Upgrades on calorimeter and muon chambers off-detector electronics and Trigger**
- **New Inner tracker (ITk)**

Motivation for the tracker upgrade

- Increased **instantaneous luminosity** up to $7.5 \times 10^{34}\ cm^{-2}s^{-1}$

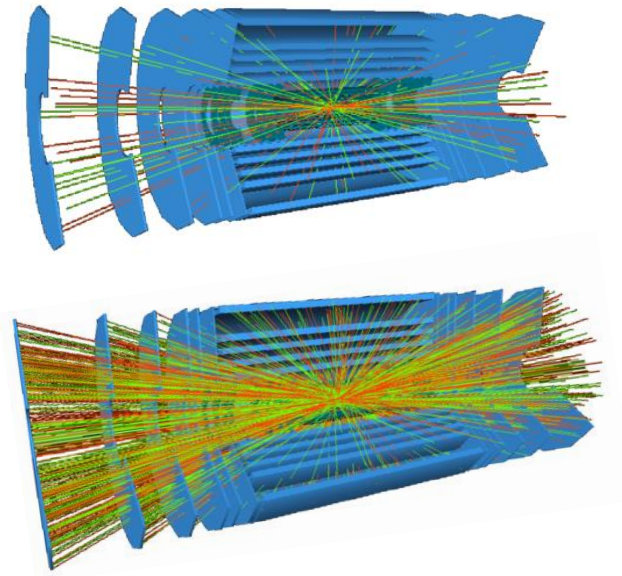
integrated luminosity will reach **4000fb^{-1}**

- approx. 200 simultaneous inelastic ***p*-*p*** collisions per bunch crossing , increase of overlap of events. → **High detector occupancy**
- High particle densities and rate → **Radiation dose $2\text{x}10^{16}\ n_{eq}/cm^2$**

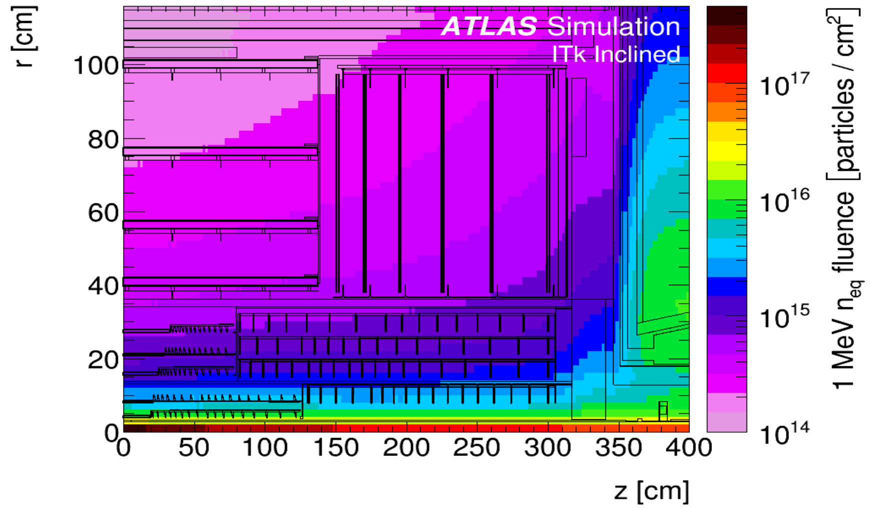
Keep the same or better tracking performance → The **ID** will be replaced by **all-silicon tracker** Inner Tracker **ITk.**

Average pile-up events

13,4 – (2015)
25,1 – (2016)
37,8 – (2017)
36,1 – (2018)
50-60 – (2022-2024)
~200 – (2030)

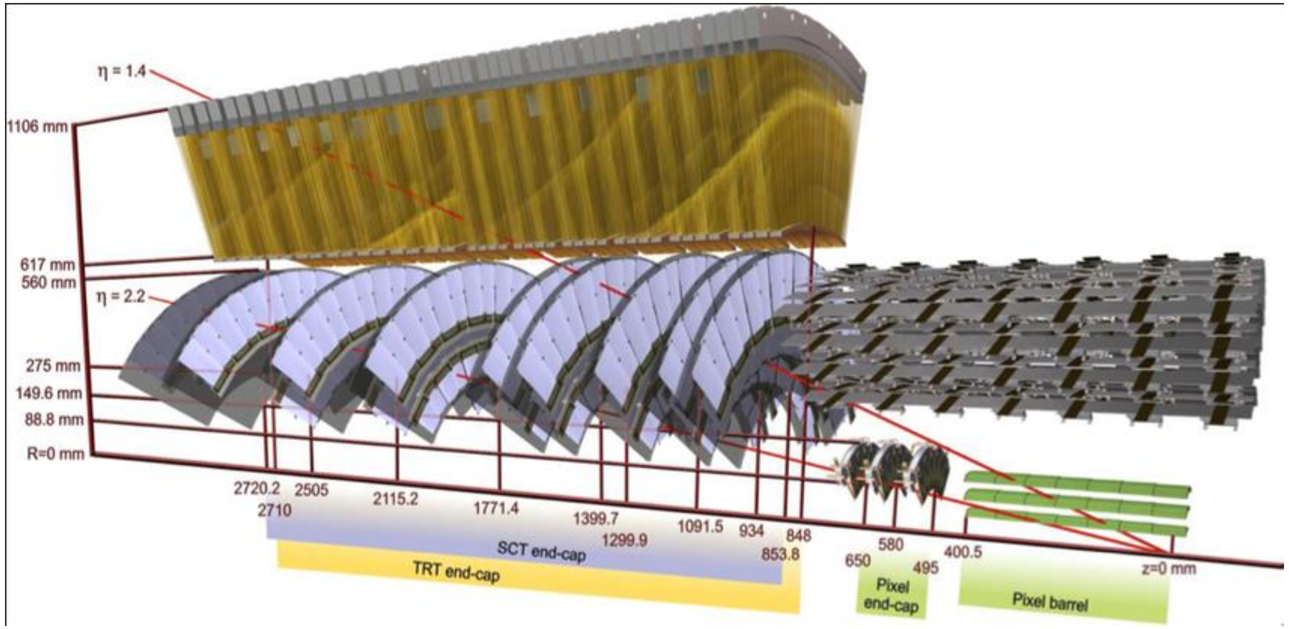


Radiation fluence



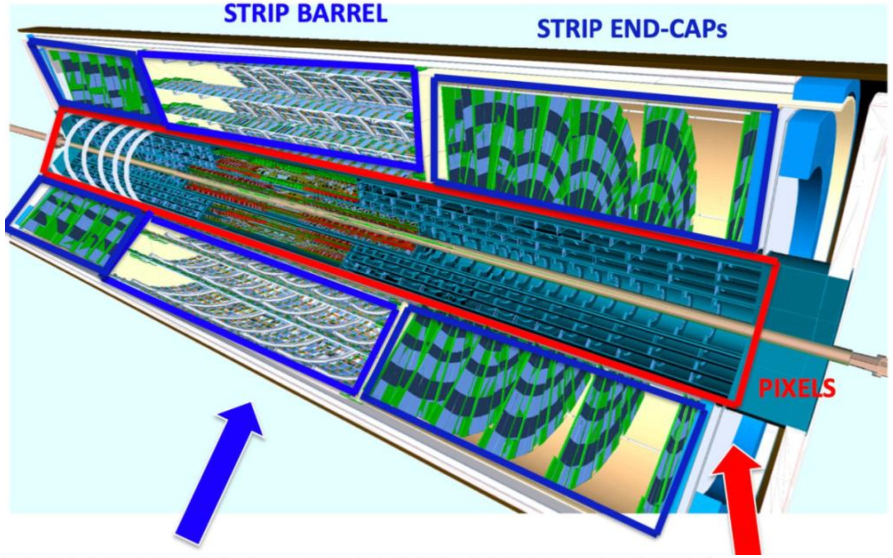
Inner Detector -> Inner Tracker

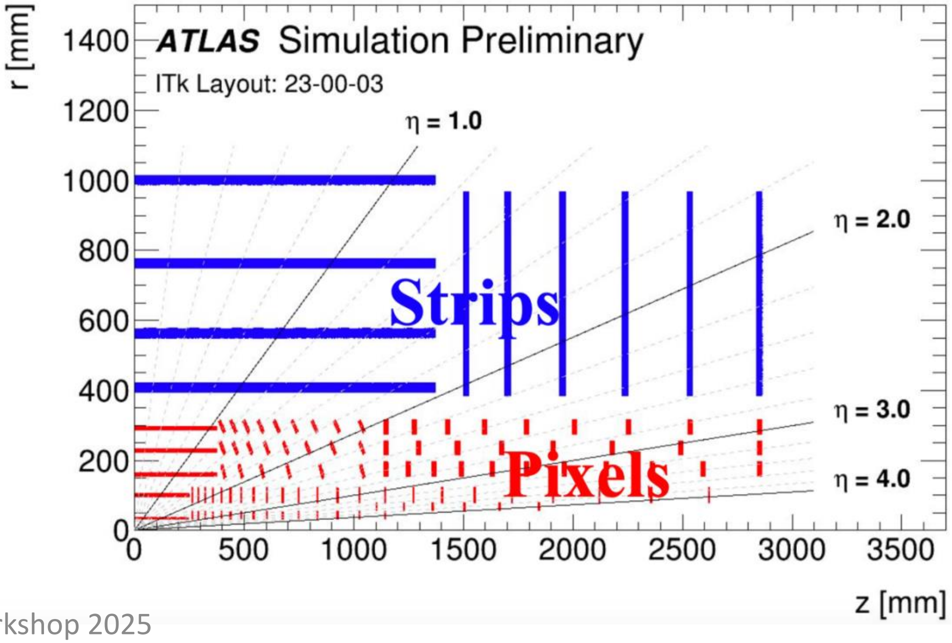
ID is an innermost detector, 6.2 m long and 1.2 in radius.
Composed of **TRT, SCT and Pixel Detector**



<u>Pixel Detector:</u>

composed of 4 barrel Layers (IBL, B-Layer, L1, L2) 3 disks in two end caps
2m^2 of active area, 92 millions of pixels





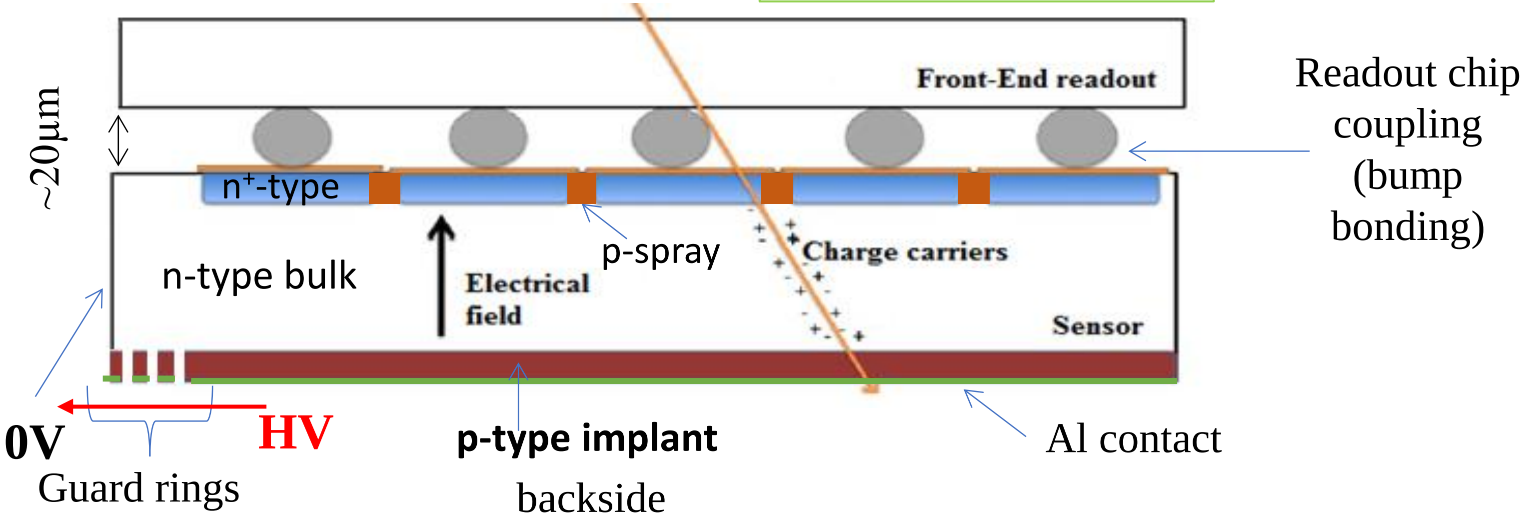
Silicon Strips
Outer layers
165 m²
17 888 modules
60 Million channels

Silicon Pixels
Inner layers
13 m²
8372 modules
5 Billion channels

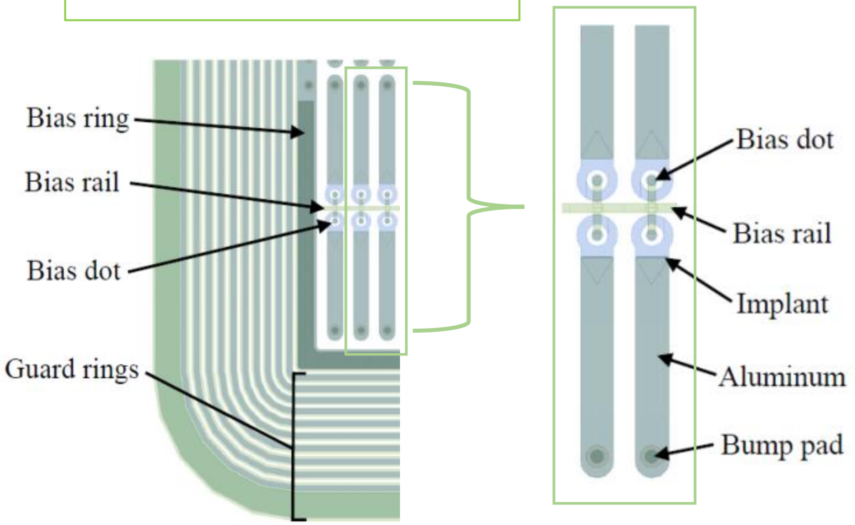
Silicon pixel detector technologies

Current ATLAS pixel detector:

Cross view



Front view



- Segmented pixel surface -> precise two dimensional spatial information
- **p-spray** for inter-pixel insulation and to compensate the accumulating electrons
- **Guard ring** structure to smoothly drop the potential at the edge of the sensor
- Reverse biasing is applied to deplete the sensor (Full charge collection)
  - Depletion starts from the backside (p-n junction): **depleted region = sensitive region**
- A particle creates **electron-hole pairs** which drift to the electrodes

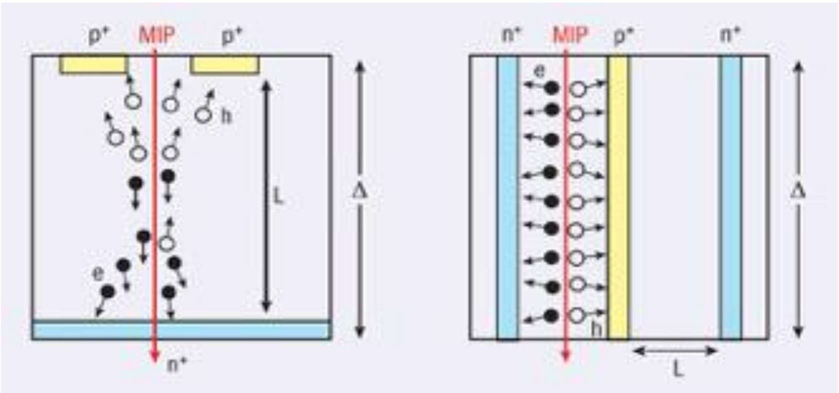
✓ Fast: O(few ns)

✓ Precise: O(~10um)

✓ Compact

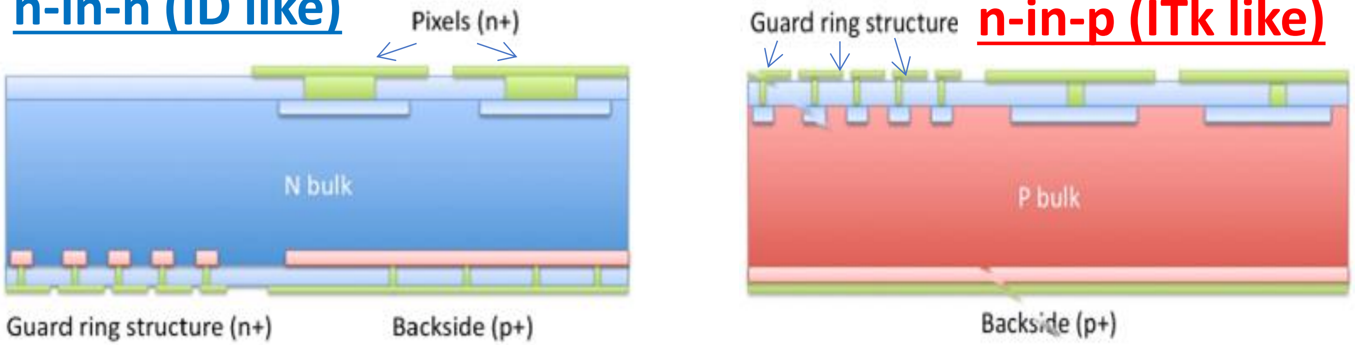
Silicon pixel detector technologies

- **<u>Planar sensors</u>**: highly doped implant on top of low-doped Si bulk **n-in-n** (ID), **n-in-p** (ITk)
  - ✓ less costly than 3D
- **<u>3D sensors</u>**: highly doped Si columns through low-doped Si bulk (ITk L_0)
  - ✓ high radiation hardness
  - ✓ low yield



Planar **3D**

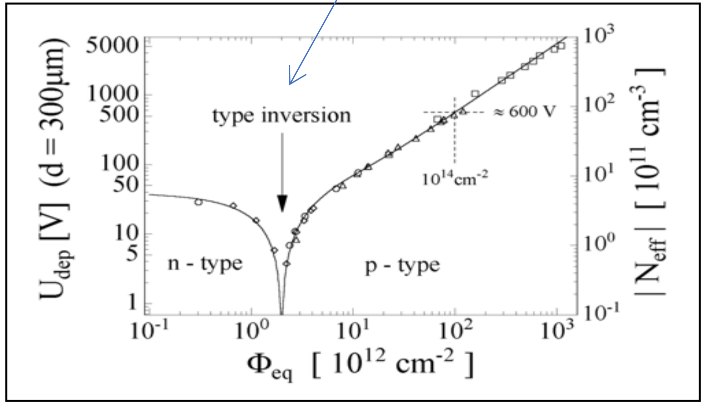
<u>n-in-n (ID like)</u> **<u>n-in-p (ITk like)</u>**



n-in-n:
- Collect electrons
- Guard rings are not on a front side
- Double-sided processing
- <u>Type inversion</u> of a bulk

n-in-p:
- Collect electrons (3 x faster than holes)
- No <u>type inversion</u>
- Can be operated partially depleted
- Single–sided processing
- Guard rings are on a front-end side

DESY-THESIS-1999-040



space charge sign inversion (**SCSI**)

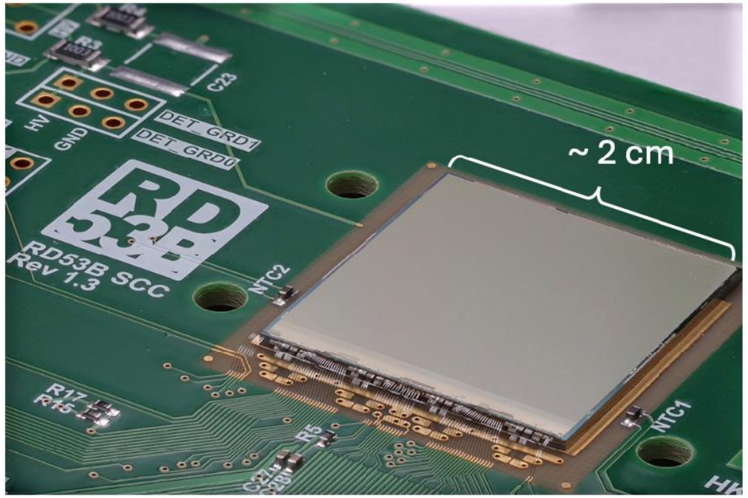
Silicon pixel detector technologies

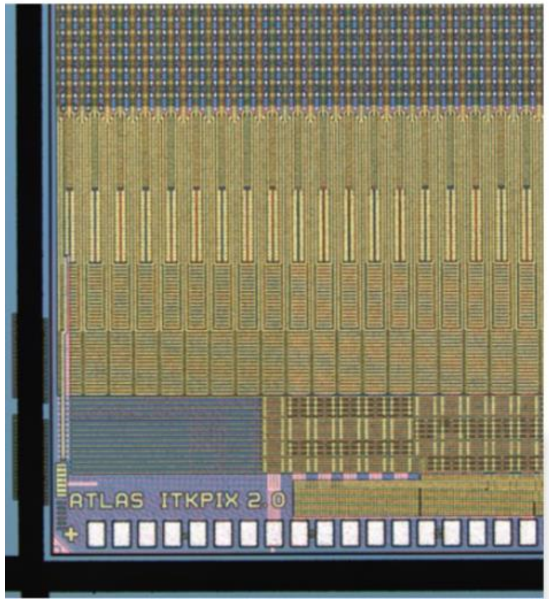
- Improvement FE-I4 chip -> RD53B chip

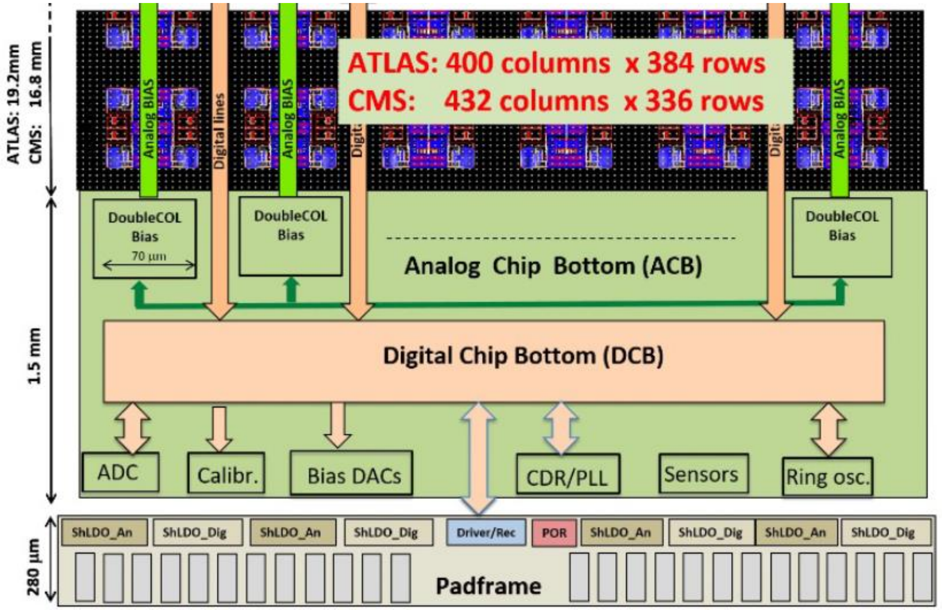
	FE-I4 chip	RD53B chip
Technology	CMOS 130 nm	CMOS 65 nm
Size	20.2x19.0 mm^2	21.0x20.0 mm^2
Pixel size	50x250 μm^2	50x50 μm^2
Pixel array	80x336	400x384
Pixel capacitance	<500 fF (700 edge)	<100 fF (200 edge)
Hit rate	400 MHz cm^{-2}	3 GHz cm^{-2}
Trigger rate	200 kHz	1 MHz
Trigger latency	6.4μs	12.8μs
Current consumption	20 μA/pixel	8 μA/pixel
Radiation tolerance	300 Mrad	1 Grad
Min stable threshold	1500 e	600 e
Readout data rate	160 Mb/s	1.28 Gb/s

Designed by RD53 collaboration
https://rd53.web.cern.ch/
R&D over 10 years

✓ High Granularity
✓ Radiation tolerance
✓ Power dissipation
✓ High readout data rate





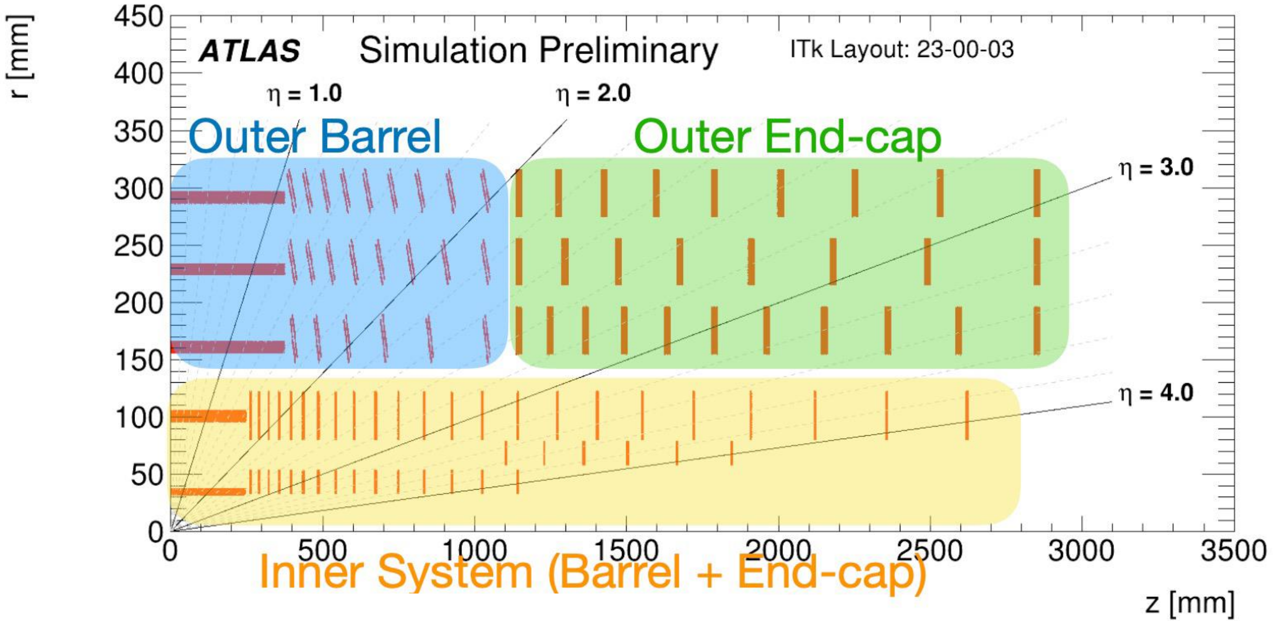


Pixel detector technologies in ITk

- **ITk-Pixel detector composed by 3 parts:**

Outer barrel: 3 barrel layers, 2x23 inclined disks
→ CERN, **France**, Germany, Japan, Switzerland

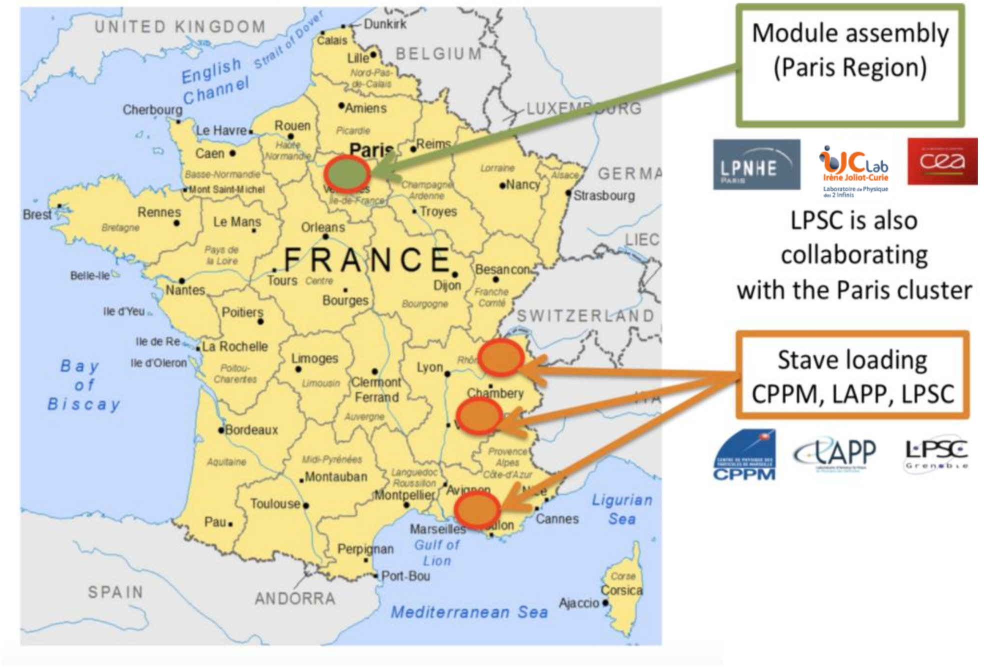
- **Outer endcap:** 2x28 outer disks
→ UK, Italy, Japan



Inner system: 2 barrel layers and 2x44 disks
→ USA, Germany

Sensors
- **L2, L3 and L4 planar sensors,** 150 μm thick
- **L1 planar sensors,** 100 μm thick
- **L0 3D sensors,** 250 μm thick

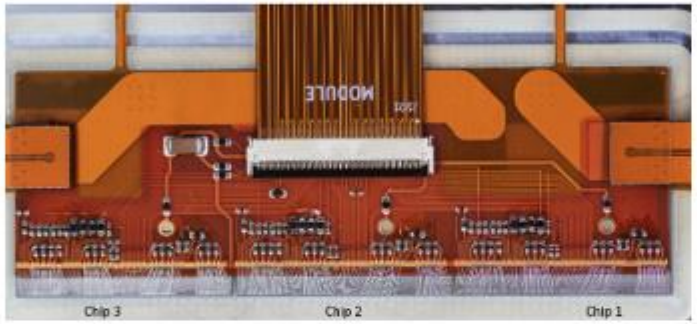
- **Outer barrel** is the **largest system** of ITkPixel detector
- ~4.5k modules, more than half of total ITkPixel
- **French** activities are organised in **two clusters**
  - **Paris cluster** for module assembly and testing: **IJCLab, IRFU, LPNHE**
  - **Alpaca cluster** for loading and integration: **CPPM, LAPP, LPSC**



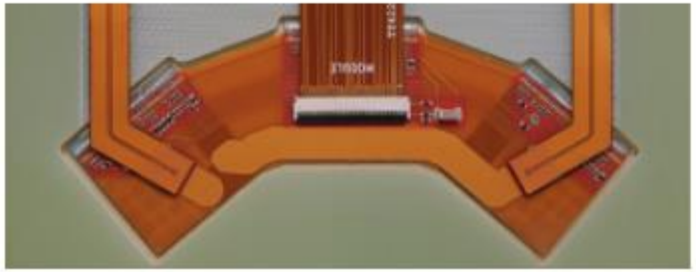
ITk Pixel Modules

>> Two types of modules:

- **Quad** modules: 4 FEs bump bonded to one sensor
- **Triplet** modules 3 single FE bare modules connected to the same flex

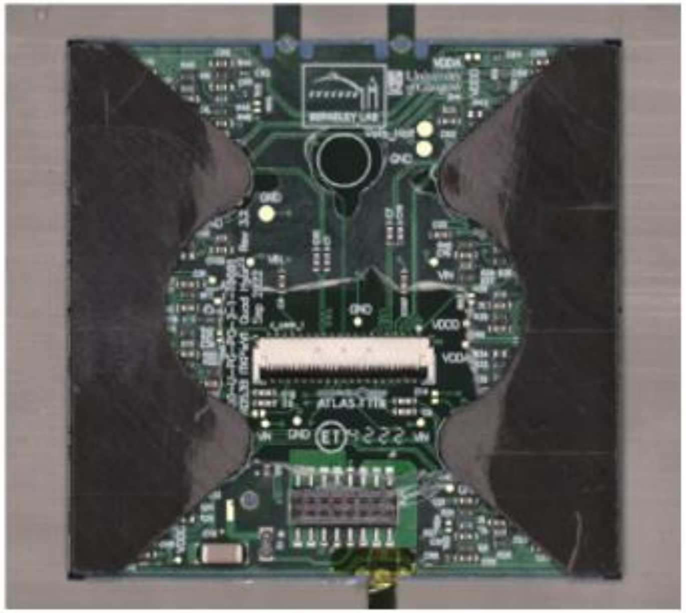


a) 3D triplet for the Inner System barrel stave



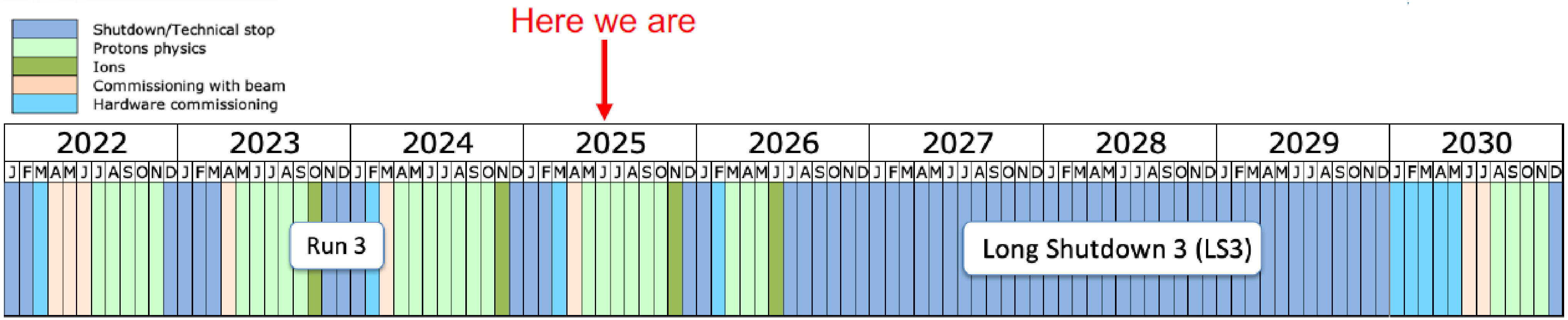
b) 3D triplet for the Inner System endcap ring

c) Inner System and Outer Endcaps quad module with data and power pigtails connected



d) Outer Barrel quad module with carbon fibre wire bond protection

Towards ITk construction

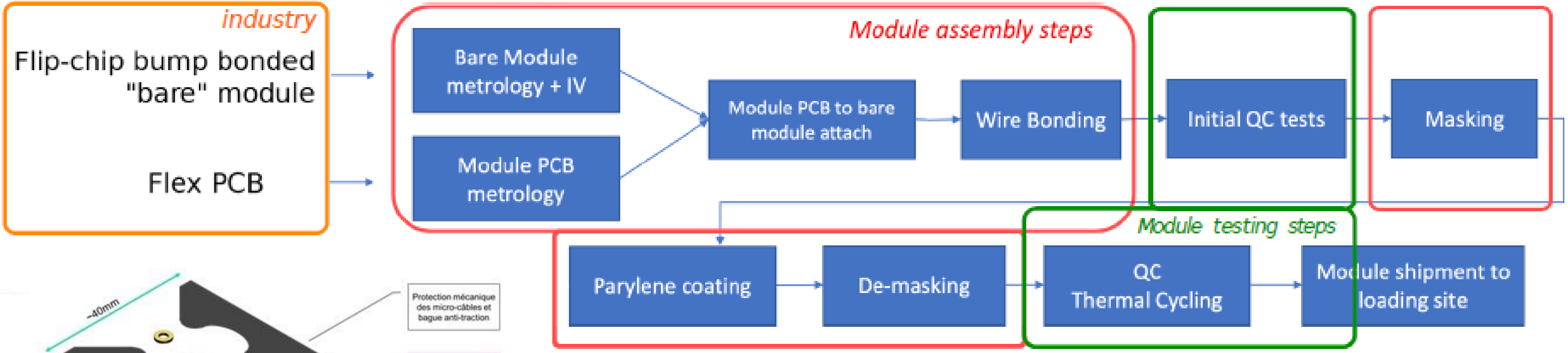


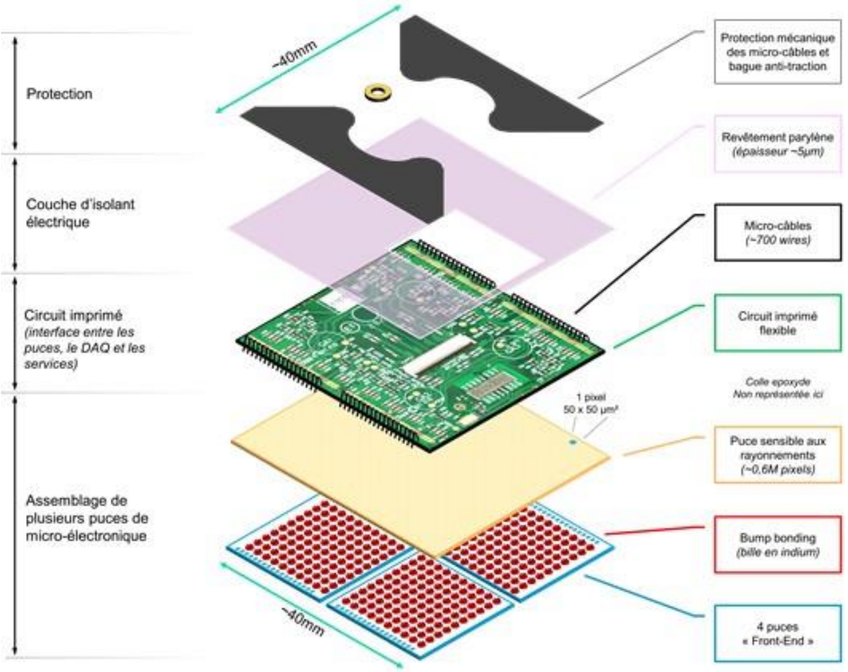
Milestones:

- **2021-2022:** production of about 160 prototype modules
- **2023-2024:** site qualifications (Lab infrastructure, Database, Parylene coating, Assembly , Testing setups, Full QC)
- **2023-2024:** pre-production of about 800 modules
- **2024:** beginning of module production (~ 12,000 modules)
- **2026-2027:** module production complete

Huge assembly load, shared among **14 assembly institutes** (USA, UK, **France**, Germany, Italy, CERN, Japan) ⇒ important effort in ATLAS to **develop common procedures** as much as possible

Module Production Chain (Paris Cluster)





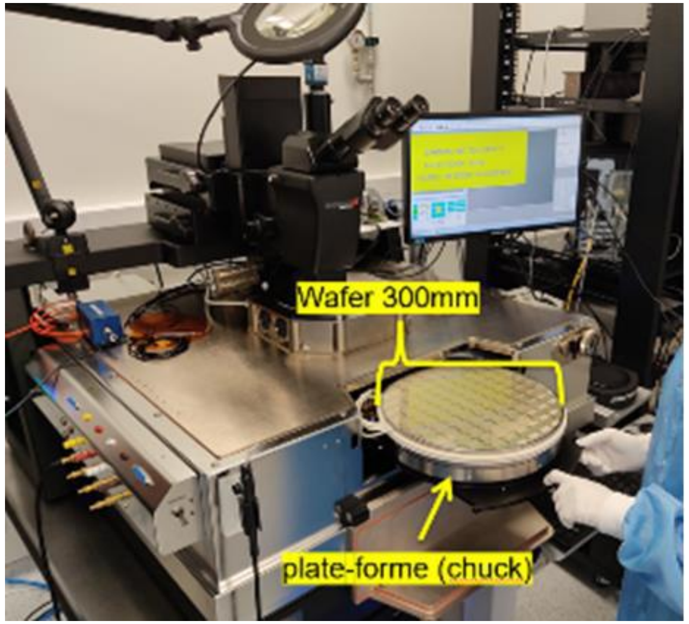
- In Paris cluster, we maintain **two** assembly lines
  - A. IJCLab (gluing/metrology/visual inspection) – CEA (Wire bonding/metrology/visual inspection)
  - B. LPNHE (all assembly steps).
- And **three** testing lines

80 weeks to build 2100 modules Need to be producing **27 modules / week !**

Module Assembly

Clean Room (PSI, IJCLab)

Clean room ISO-7, 70 m^2. Semi-automatic probe station, High precision numerical microscope, confocal profilometer, 3D automated measuring system



Pixel sensor electrical tests infrastructure

- probe station Signatone
- vortex cooling system up to -40^{0}C (irradiated sensor)
- Keithley provides comprehensive device-level characterization IV -CV
- up to 3kV of biasing voltage
- allows creating the map for automatic measurements of periodically repeating structures on the test wafer

Visual Inspection and Metrology

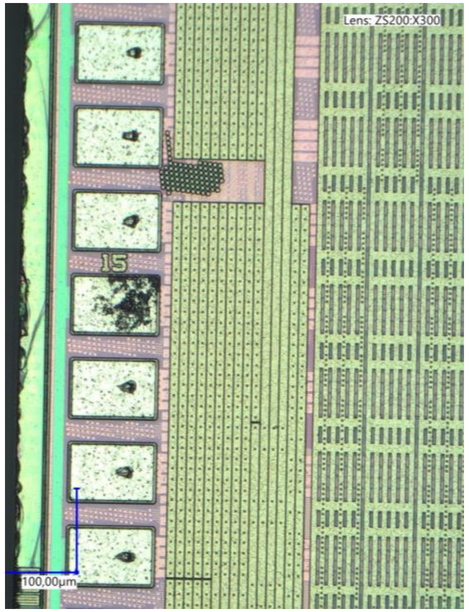
>> Prior to assembly

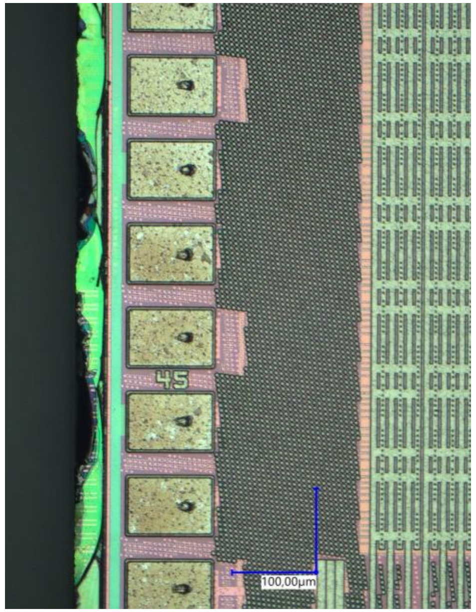
- **Bare module**
    - Bare module IV
    - Visual inspection
    - Mass/metrology

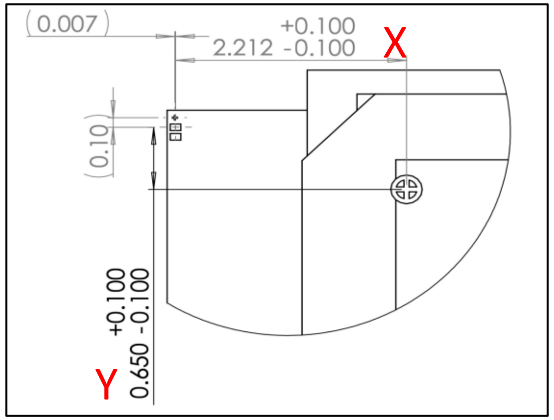
- **Flex PCB**
    - Visual inspection
    - Mass/metrology

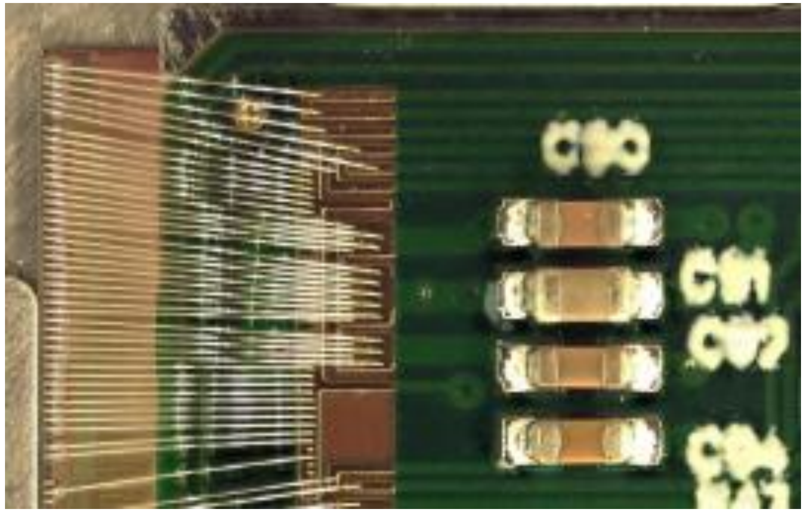
>> After assembly

- **Module**
    - Thickness and mass
    - Flex to bare module alignment

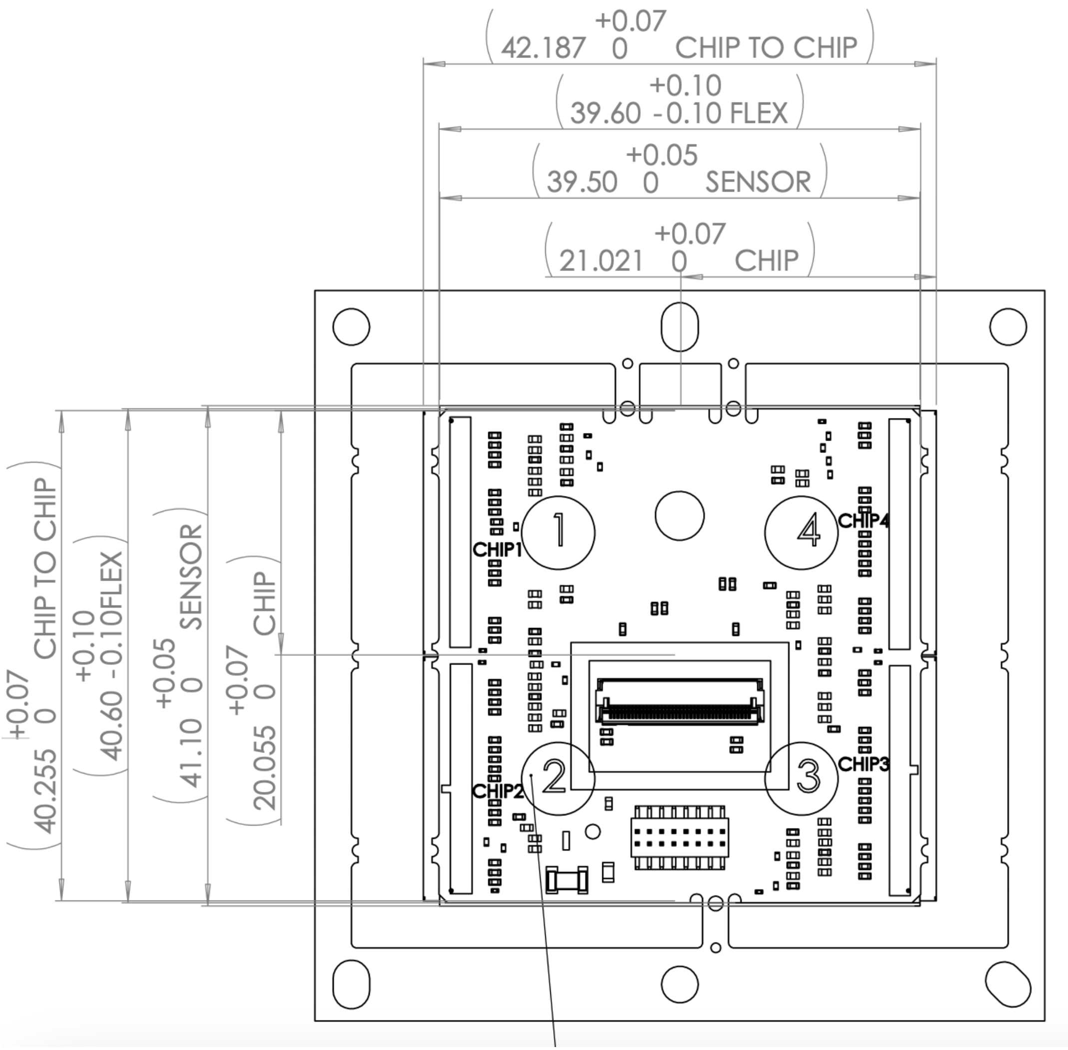


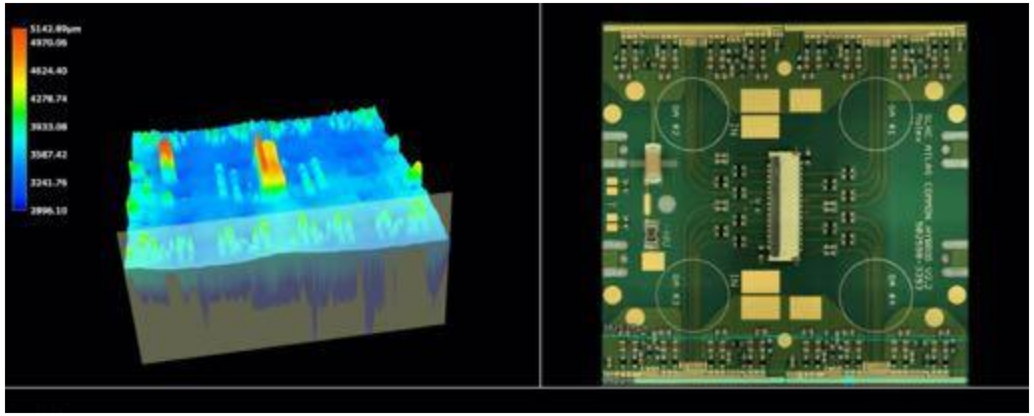






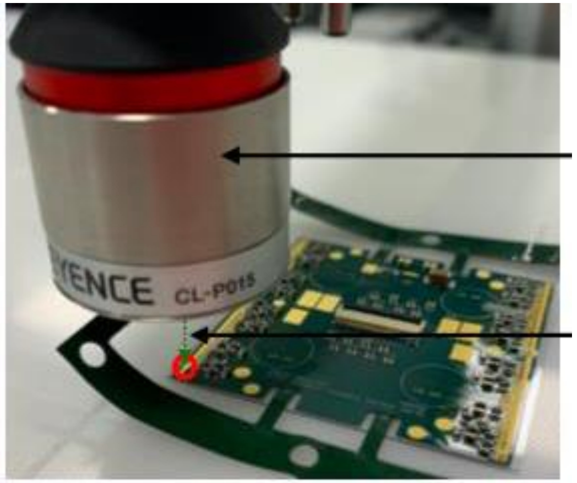
Visual Inspection and Metrology



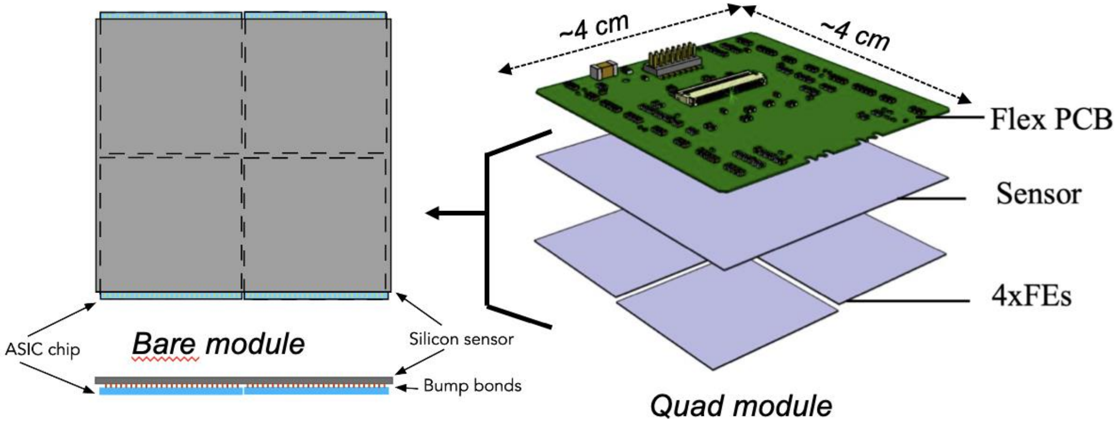


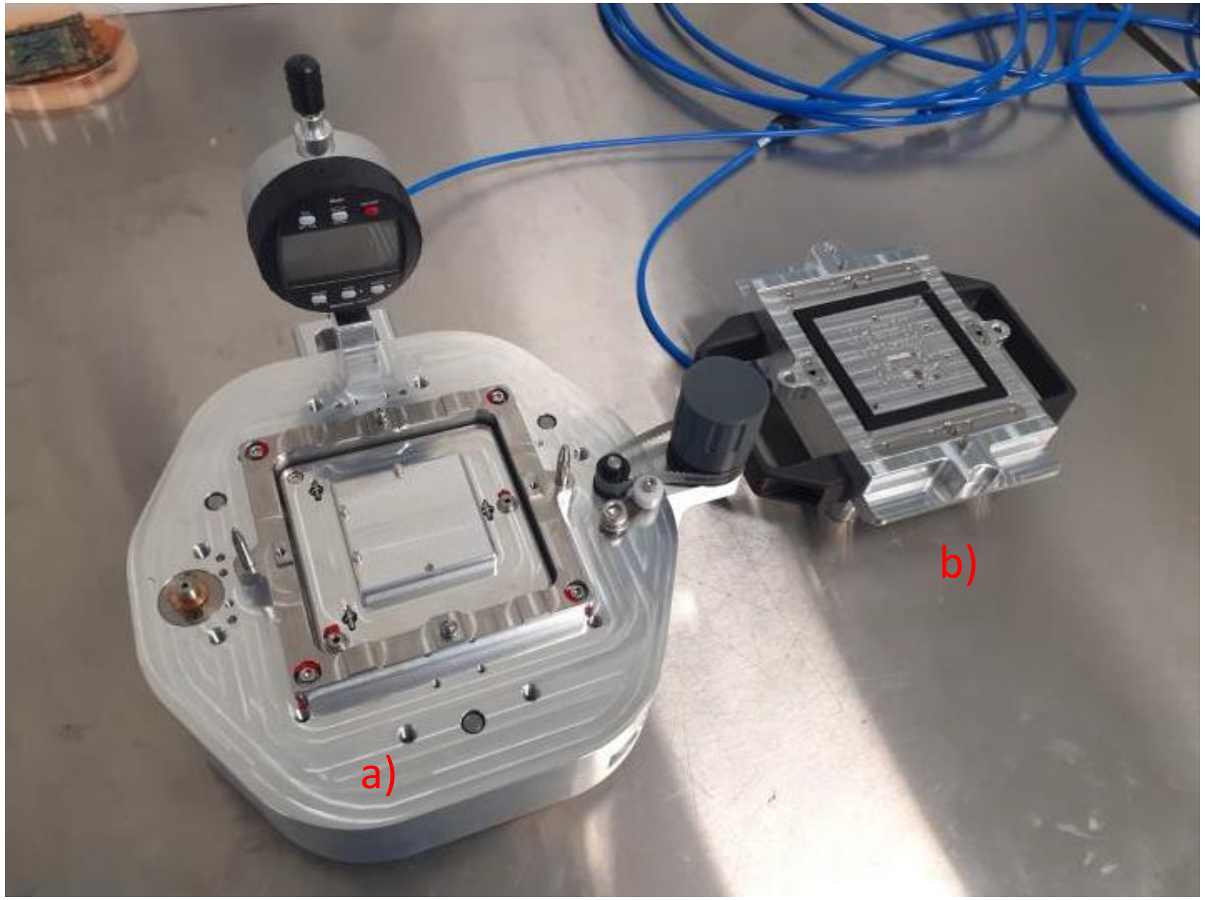
Chip thickness:
0.150 +0.025 -0.010 mm

Bare module thickness:
0.325 +0.090 -0.040 mm



Gluing

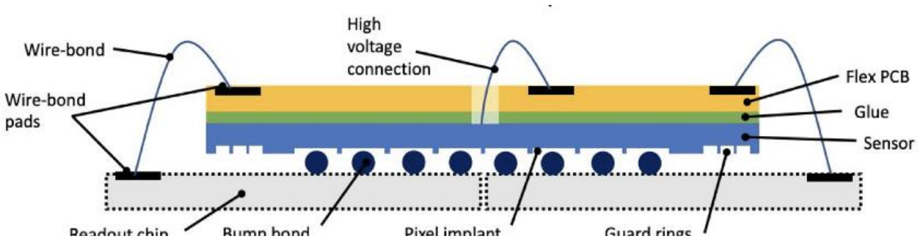


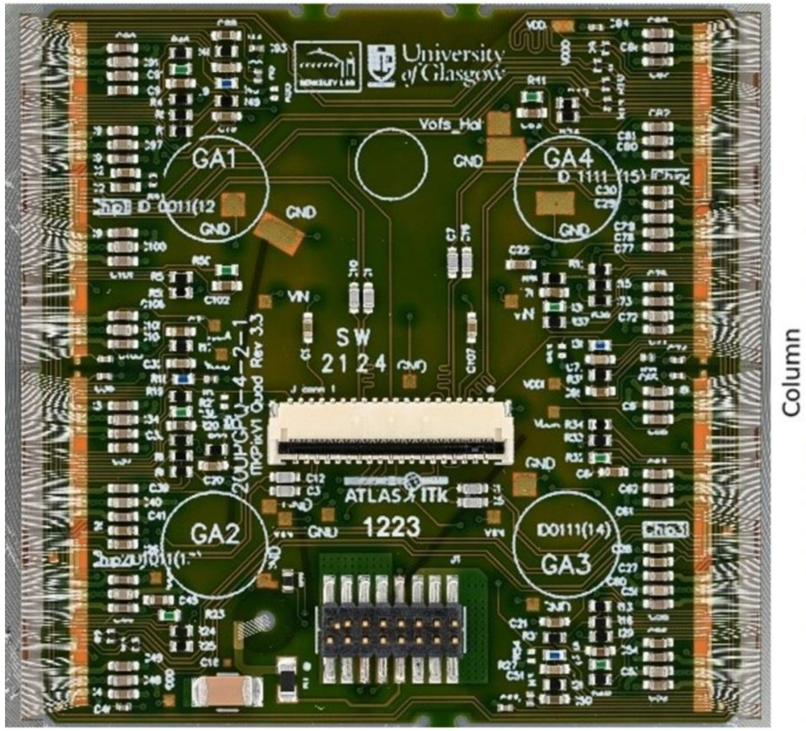


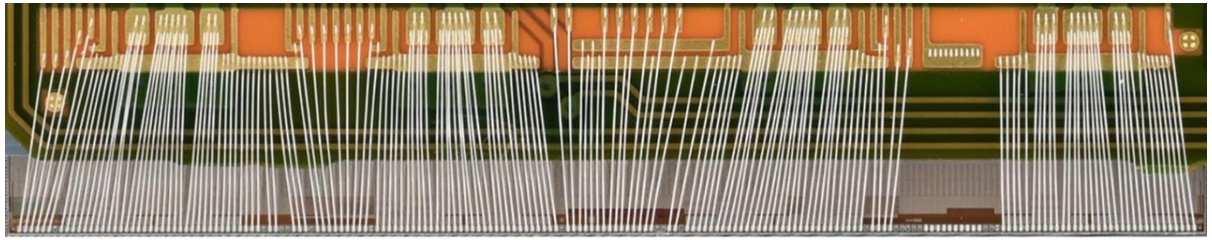
- Glue mixing method : Two components of Araldite;
- Temperature - 22°C, humidity - 45%;
- Two jigs: a) for the bare module; b) for the flex PCB;
- Components maintained in position with vacuum;
- The glue is deposited through a stencil and spread manually with a spatula;
- Aligned by dowel pins;
- The two jigs are then screwed on top of each other and left this way during the curing time of the glue (8 hours).

Wire-bonding

>> Pixel quad module







- Delicate operation depending a lot on cleanness of the bondable surfaces
- 700 wire bonds per quad module
- When/If everything works smoothly, this is about 1-2 hours for a fully automated WB machine

Module Testing

Thermal cycles setup

>> >> Thermal cycles aimed at selecting modules that survive this kind of stress tests

we use a Climate Chamber (CC) Weisstechnik LabEvent L T/150/70/3

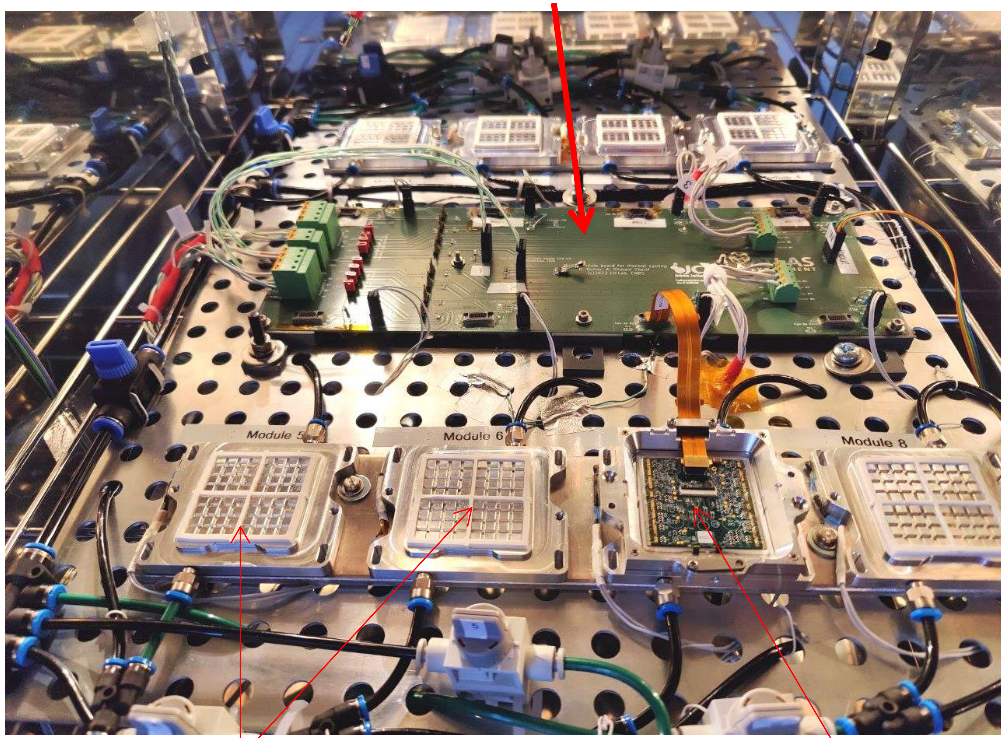
Features of the system:

- CC from - 70^0C to + 180^0C
- Test space of 500 x 490 x 610 mm^3
- Max rate cooling (heating) – 4 K/min (3,5 K/min)
- Dry air
- Pump and vacuum regulator
- DCS: Arduino Mega + LabRemote + Grafana

10 cycles	- 45° C -> + 40° C
1 extreme cycle	- 55° C -> + 60° C

The operating temperature of the ITk will be -35°C, but variations can be expected during the detector lifetime.

Multimodule PCB for NTC reading



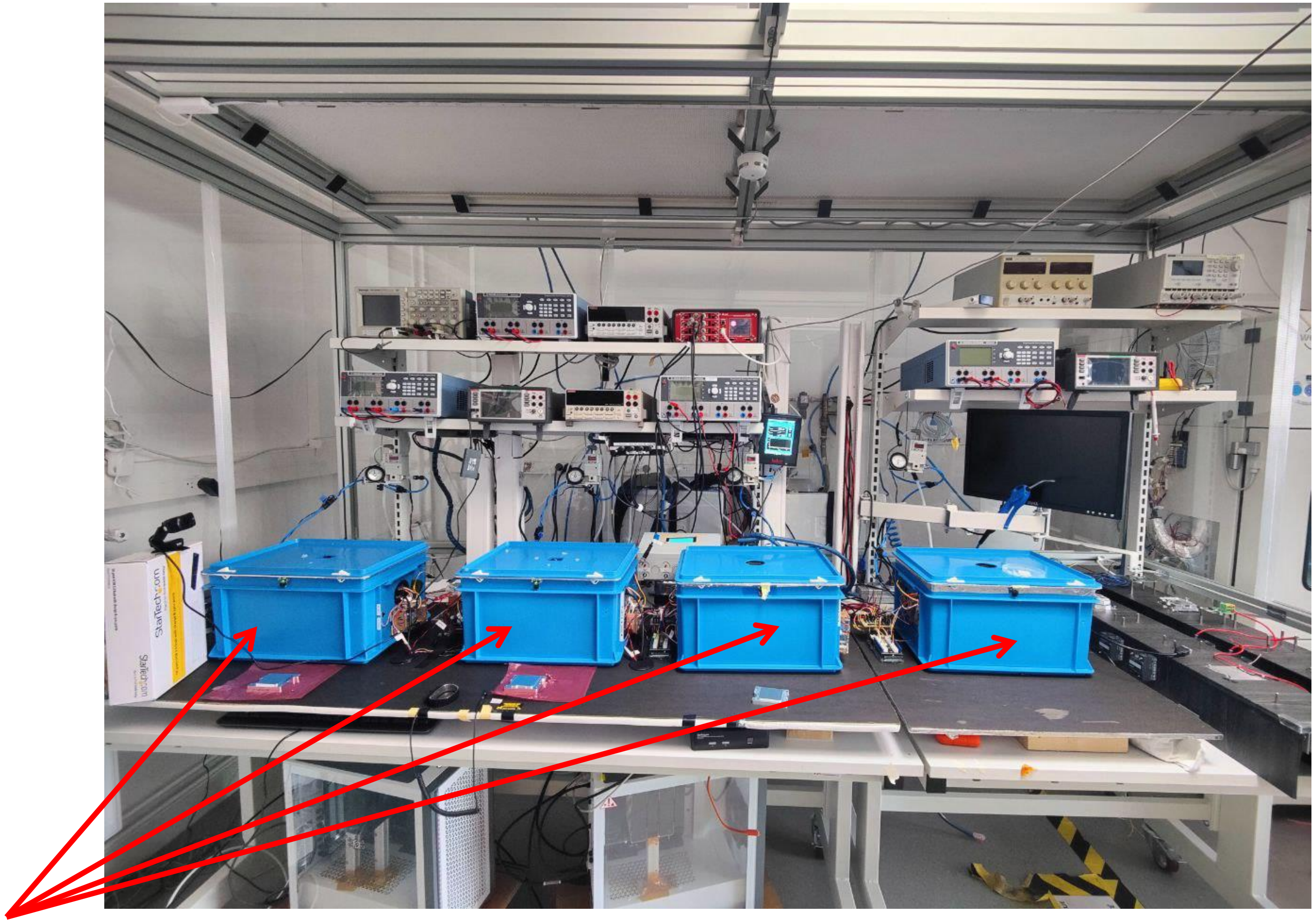
Vacuum chucks

Module

View inside the CC

Temperature controlled setup

- ➔ Temperature controlled by chiller (Huber) and Peltier.
- ➔ Dry air flow
- ➔ Vacuum regulators
- ➔ LV and HV power supplies
- ➔ 6 ½ digit multimeters
- ➔ Monitoring by Grafana of environmental sensors (Temperature, humidity, air-flow, pressure, dew point) and HV, LV, +Currents
- ➔ Software interlock
- ➔ Hardware interlock



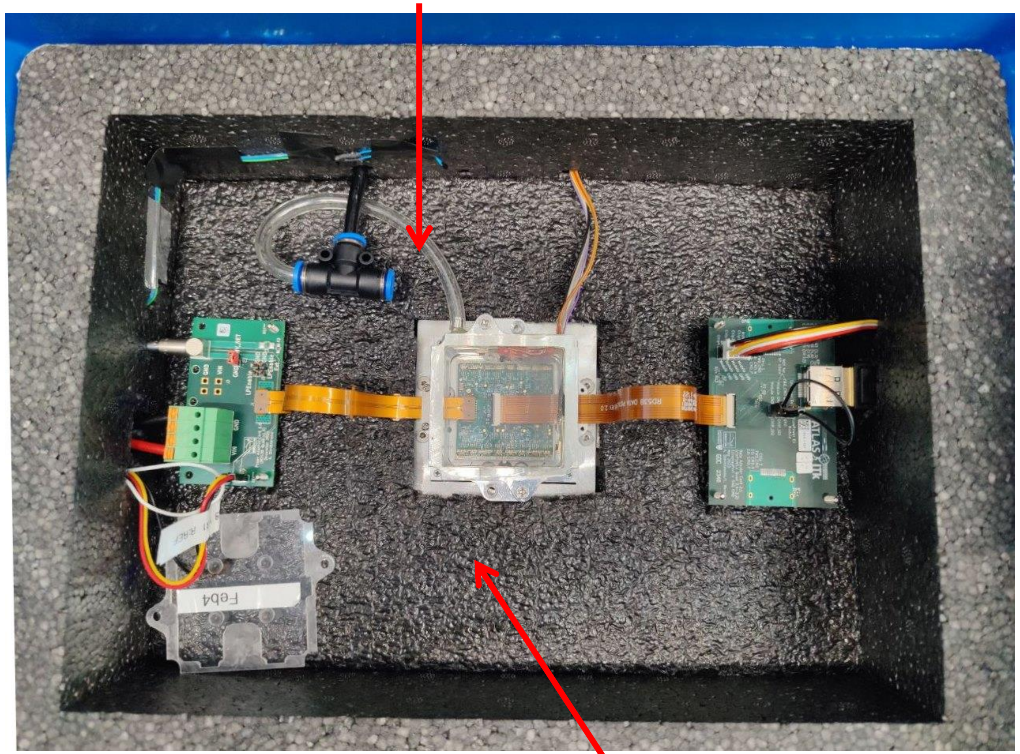
Cold boxes

Picture of the module testing setups (IJCLab)

Temperature controlled setup

>> The setup allows testing the quads at cold (-15ºC)

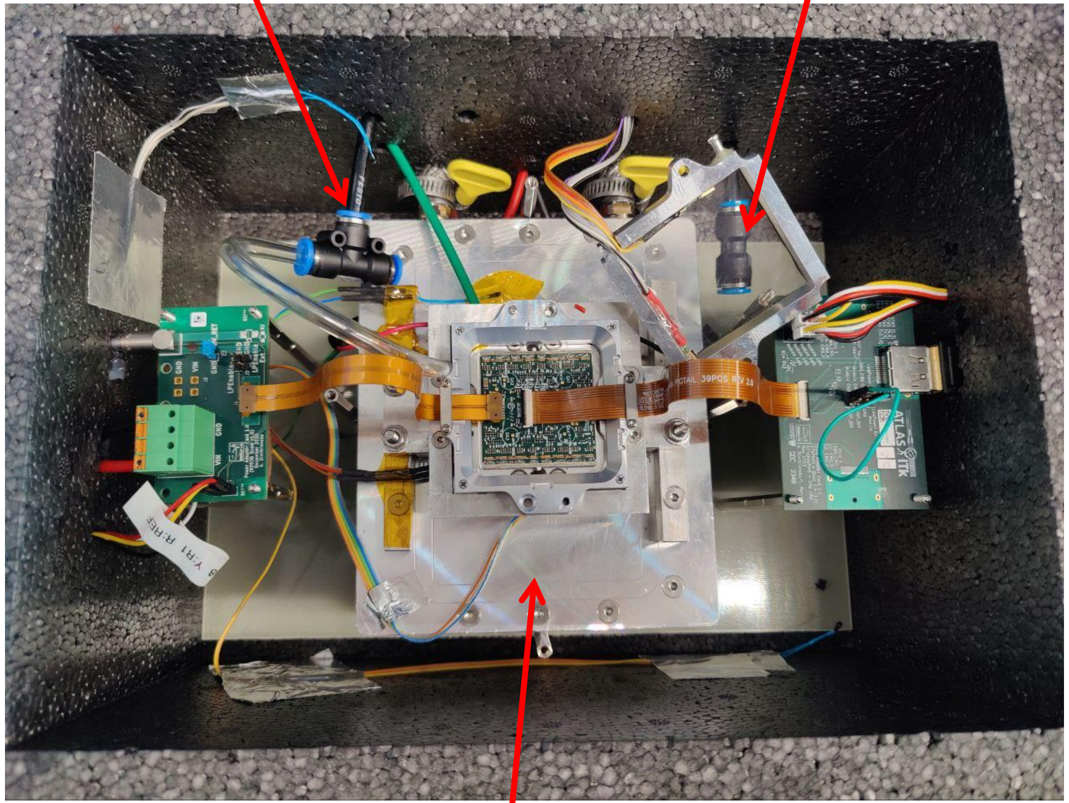
Dry air inside testing lid



Foam plate to split the box space on top and bottom part. It covers cooling unit, it allows changing modules without heating up the chiller.

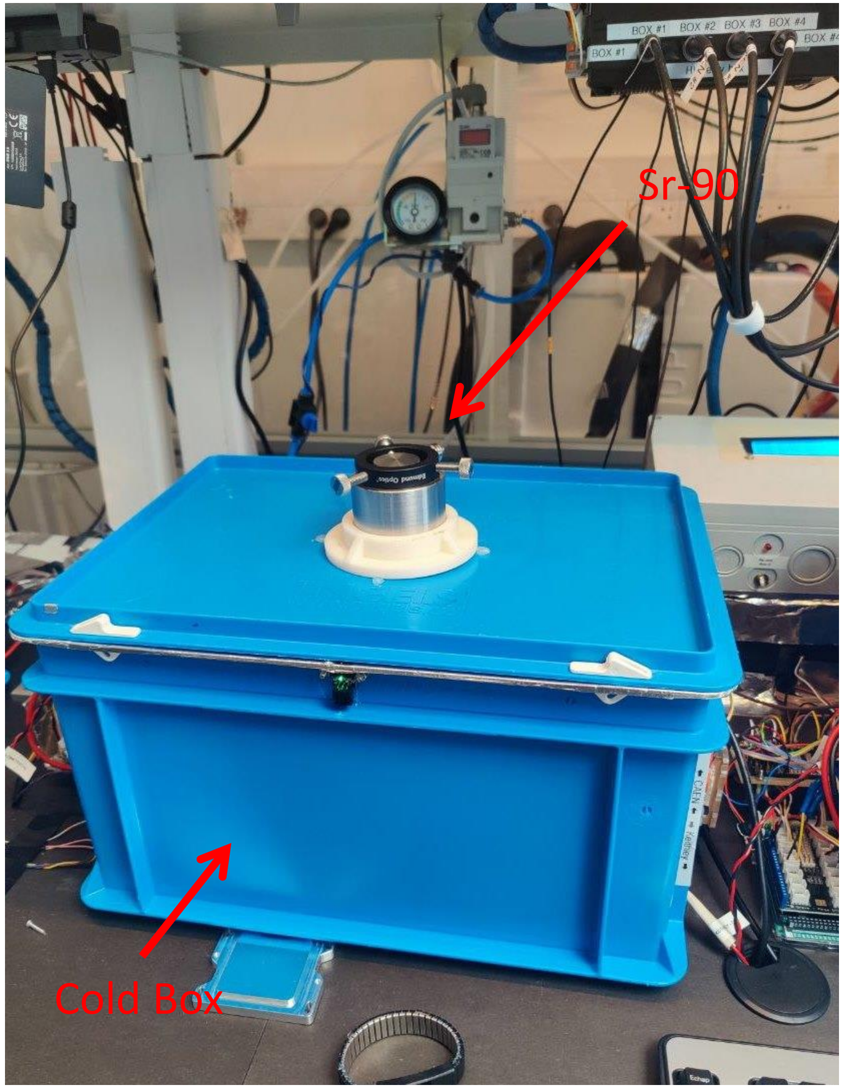
Dry air top part

Dry air bottom part



Cold plate

Temperature controlled setup

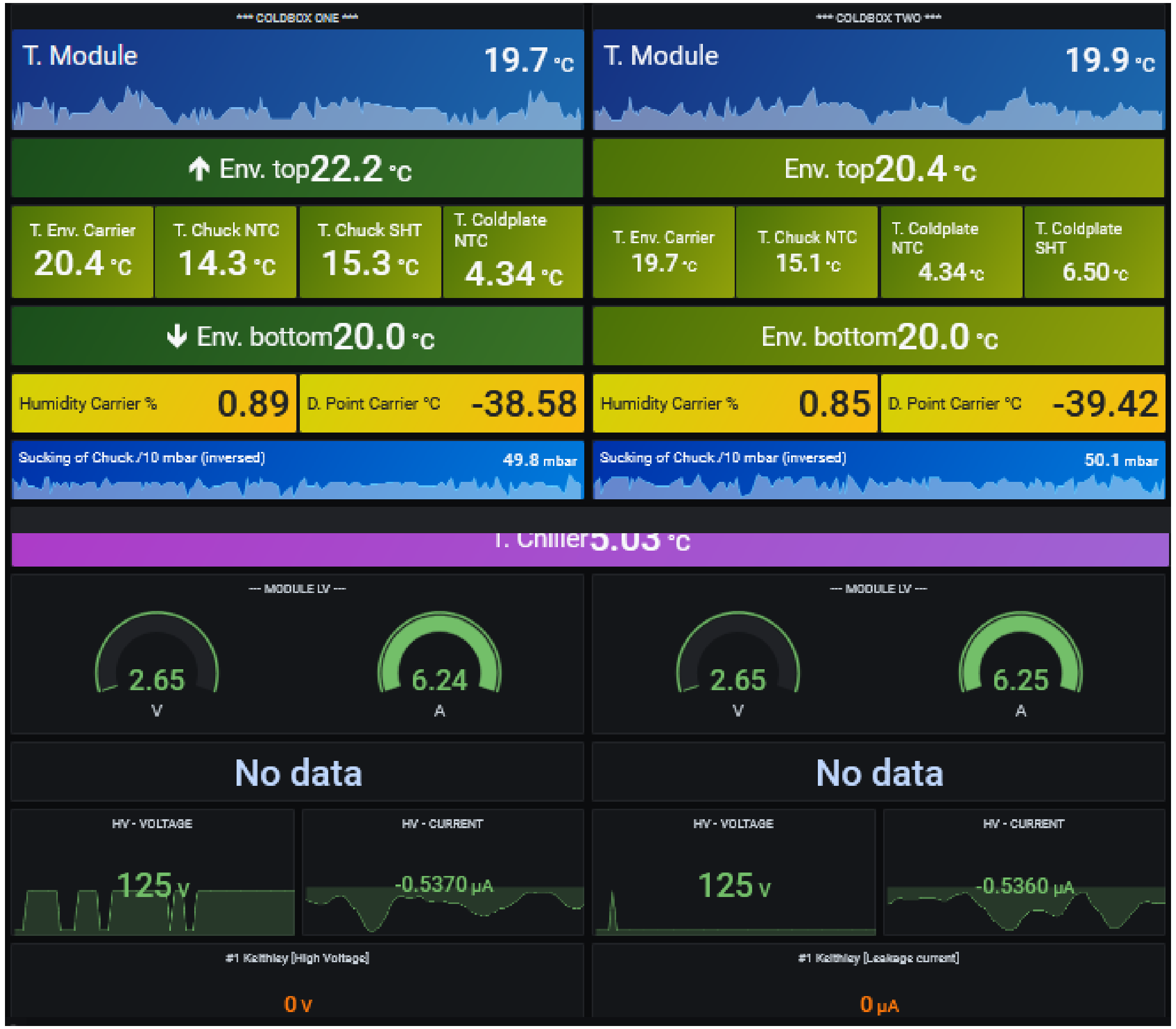


>> The source test setup needed for bump bonds checks is based on the temperature controlled setup

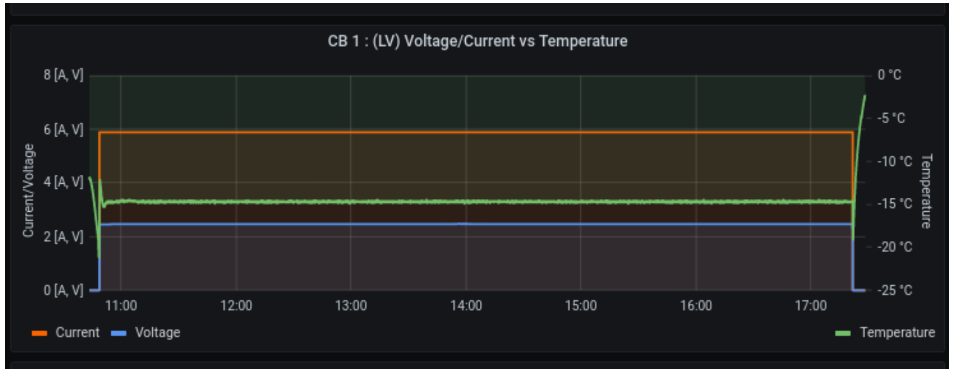
General info about the source setup:

- **Radioactive source Sr-90 (37Mbq)** (~ 10 y.o.) [one single source for the testing]
- **Minimum distance between** source and module carrier ~ **10 cm**
  - Opening in the lid (plastic lid), foam 1 cm and the Mylar thin lid on top of the testing carrier.

DCS system. Monitoring Software interlock.

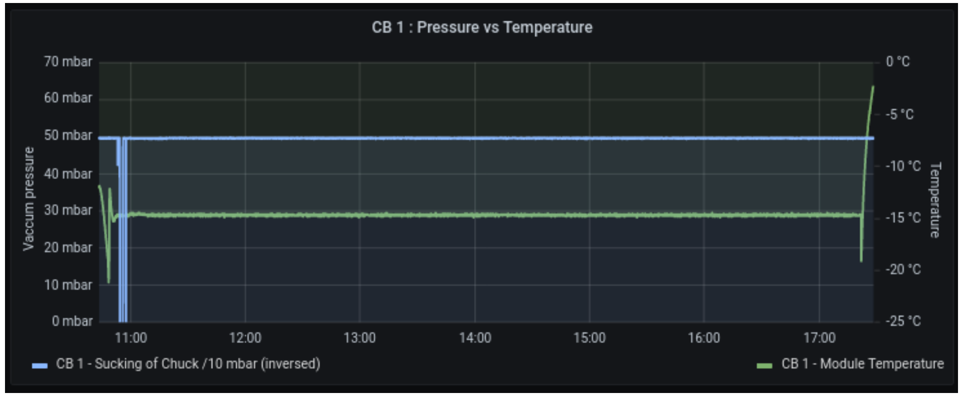


Screenshot from the Control PC



LV Current | LV Voltage | Module NTC

Plots showing LV, current and module NTC vs .time.

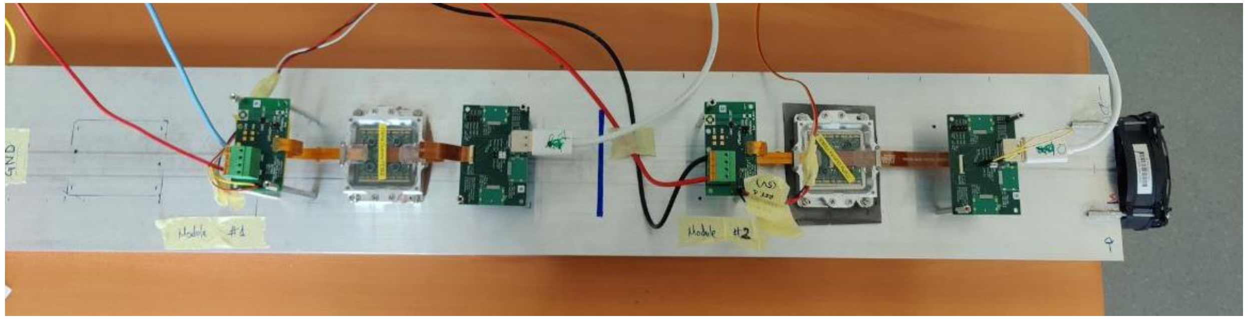


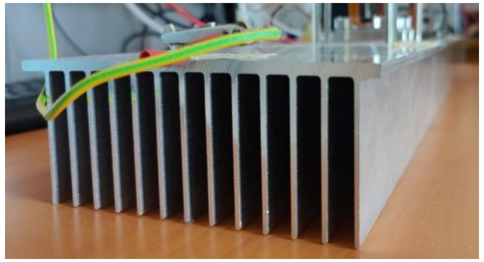
Vacuum | Module NTC

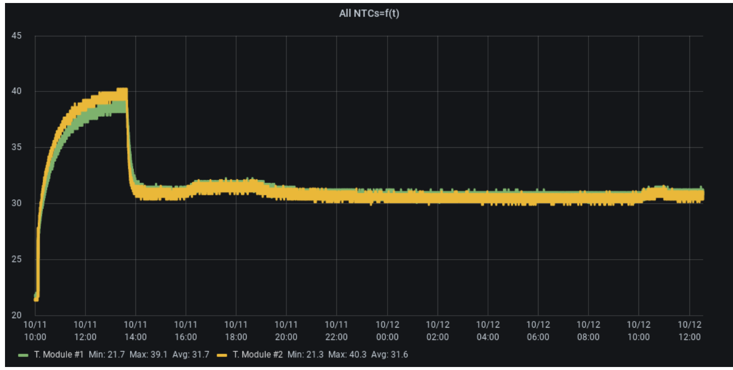
Plots showing the stability of the Vacuum (set to -500mbar) and the module NTC vs .time

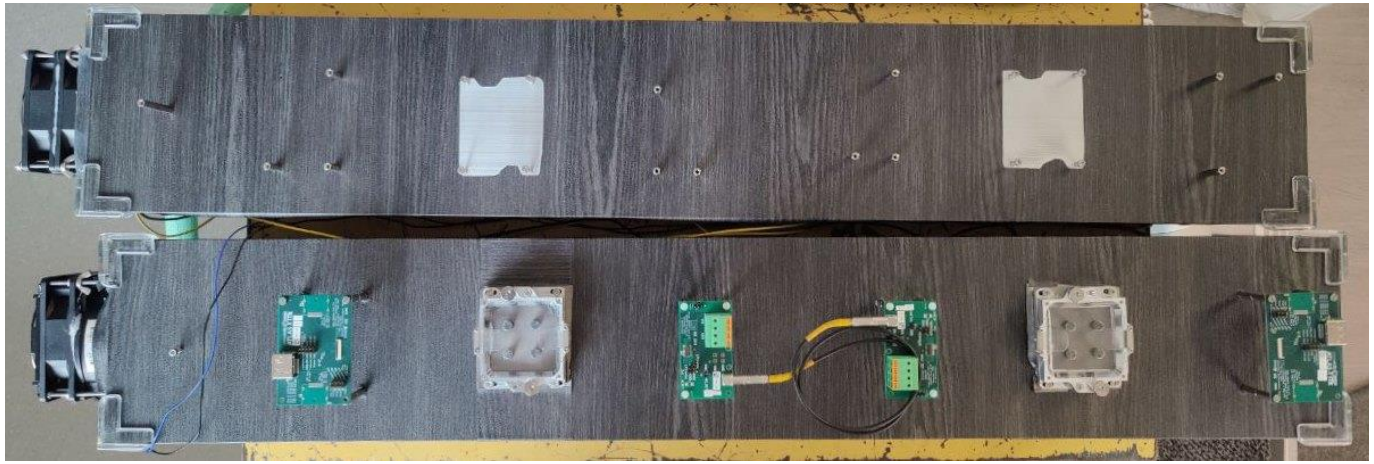
Stability test setup

>> The ITk pixel modules are tested at room temperature for stability









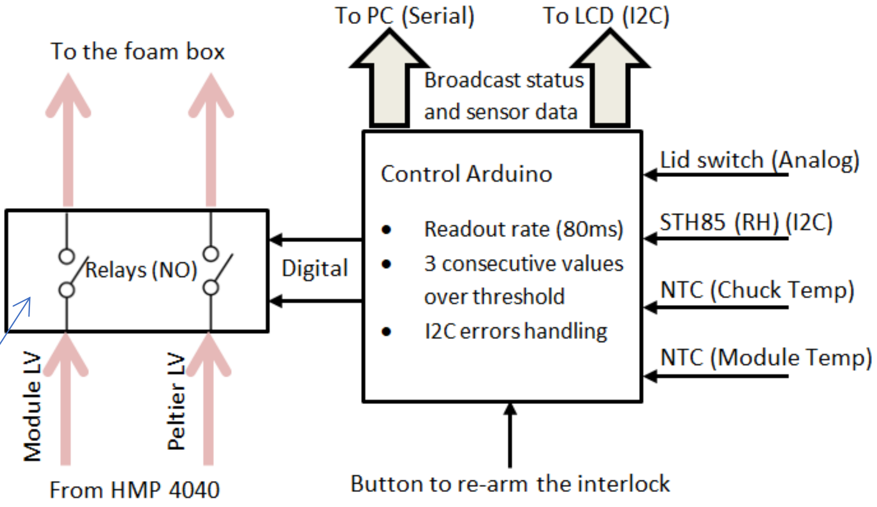
Pictures of the heatsinks prepared for the final production setup.
But this kind of test has been removed.

- The modules are powered and with HV on during the stability test duration.
- It is also required continuous readout by DAQ and HV current monitoring
- Test duration: from 36h to 48h
- Quad temperature range set point: from 25°C to 45°C

Hardware interlock

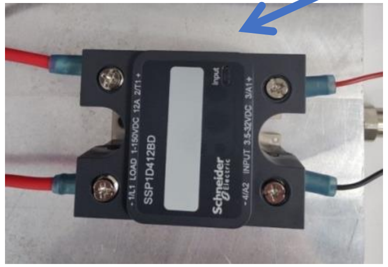
Conditions:

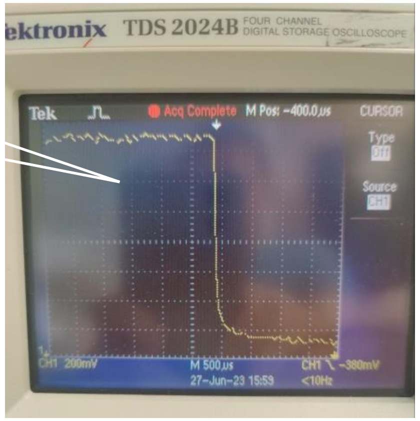
- Lid is open;
- Module NTC Temperature:
  - $T_{NTC} < 45\ ^oC$
  - $T_{NTC} < -60\ ^oC$
- Dew point >= T_{chuck}

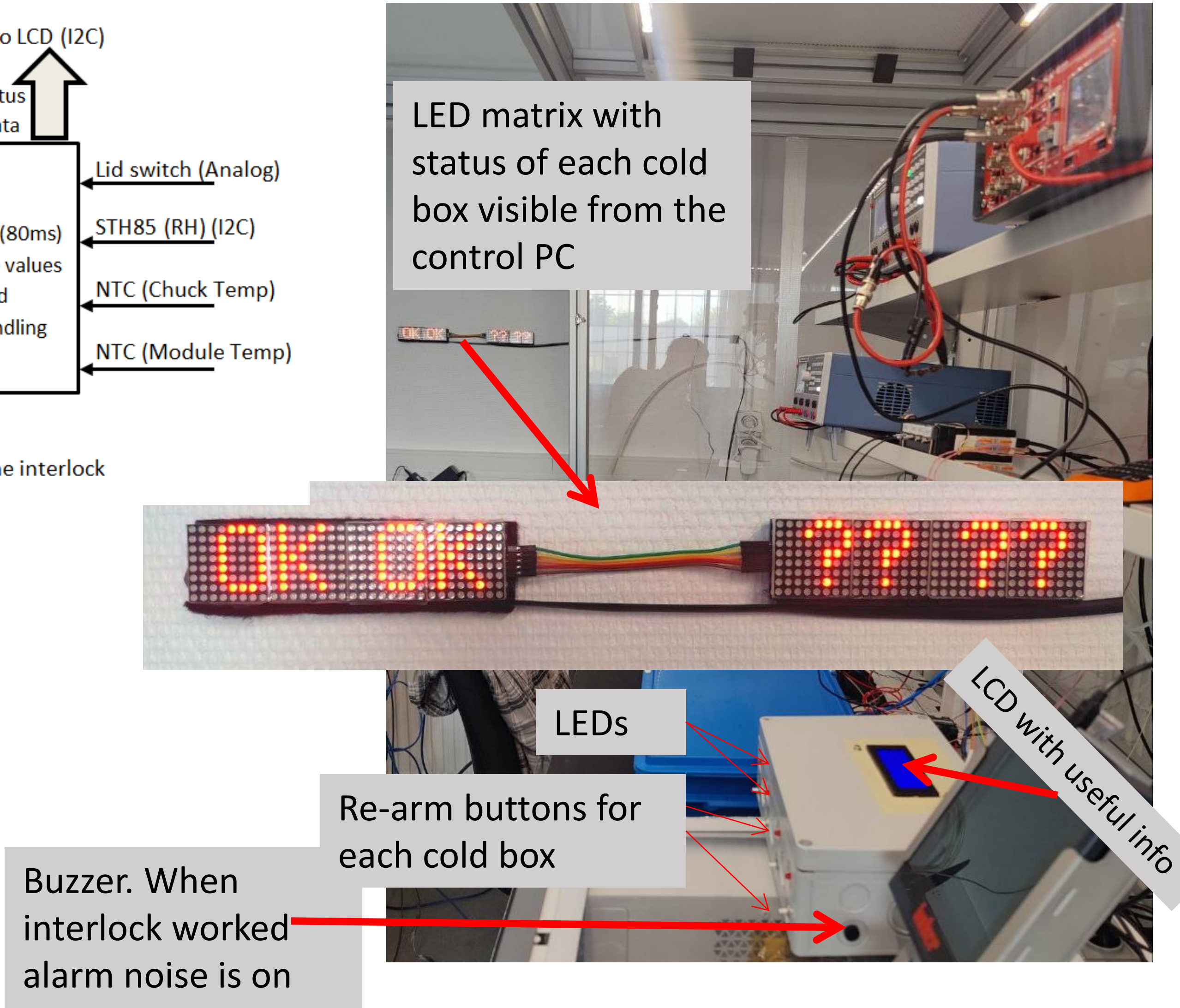


Peltier relay and HV – Reed relay

Module relay – **solid state relay**







Electrical QC stages

Initial module characterisation	*Initial module characterisation*	Parylene masking	Parylene coating	Parylene unmasking	Wirebond protection			Thermal cycling	*Burn-in*	*Module completed*	
Initial Warm	**Initial Cold**	**Parylene Masking**	**Parylene Coating**	**Parylene Unmasking (alt.)**	**Wirebond protection (alt)**	**Post Parylene Warm**	**Post Parylene Cold**	**Thermal cycles (at which T?)**	**Long term Stability Test**	**Final warm**	**Final cold**
INITIAL_WARM	INITIAL_COLD	PARYLENE_MASKING	PARYLENE_COATING	PARYLENE_UNMASKING	WIREBOND_PROTECTION			THERMAL_CYCLES	LONG_TERM_STABILITY_TEST	FINAL_WARM	FINAL_COLD
20 C	-15/-25 C (quads/triplets)			20 C	20 C	20 C	-15/-25 C (quads/triplets)	20 C		20 C	-15/-25 C (quads/triplets)
sensor IV	sensor IV			sensor IV *	sensor IV "	sensor IV	sensor IV	sensor IV^	sensor IV^	sensor IV	sensor IV
ADC Calibration	ADC Calibration					ADC Calibration	ADC Calibration			ADC Calibration	ADC Calibration
Analog readback	Analog readback					Analog readback	Analog readback			Analog readback	Analog readback
SLDO VI	SLDO VI					SLDO VI	SLDO VI			SLDO VI	SLDO VI
Vcal calibration	Vcal calibration					Vcal calibration	Vcal calibration			Vcal calibration	Vcal calibration
Injection capacitance	Injection capacitance					Injection capacitance	Injection capacitance			Injection capacitance	Injection capacitance
LP mode	LP mode					LP mode	LP mode			LP mode	
Data Transmission	Data Transmission					Data Transmission	Data Transmission			Data Transmission	Data Transmission
Min. health test	Min. health test			Min. health test	Min. health test	Min. health test	Min. health test	Min. health test	Min. health test	Min. health test	Min. health test
Tuning	Tuning			Tuning *	Tuning "	Tuning	Tuning	Tuning	Tuning	Tuning	Tuning
Pixel Failure Ana	Pixel Failure Ana			Pixel Failure Ana *	Pixel Failure Ana "	Pixel Failure Ana	Pixel Failure Ana	Pixel Failure Ana	Pixel Failure Ana	Pixel Failure Ana	Pixel Failure Ana (including source scan)

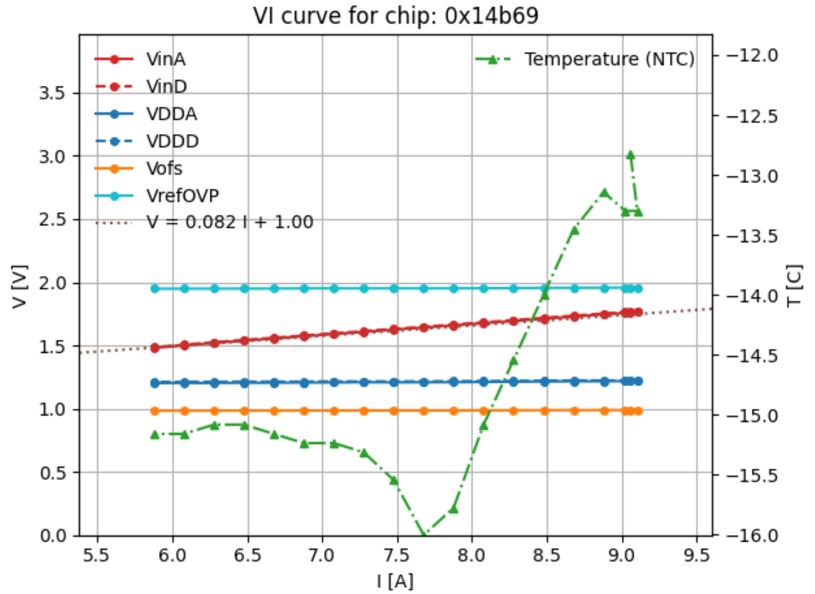
Electrical QC stages

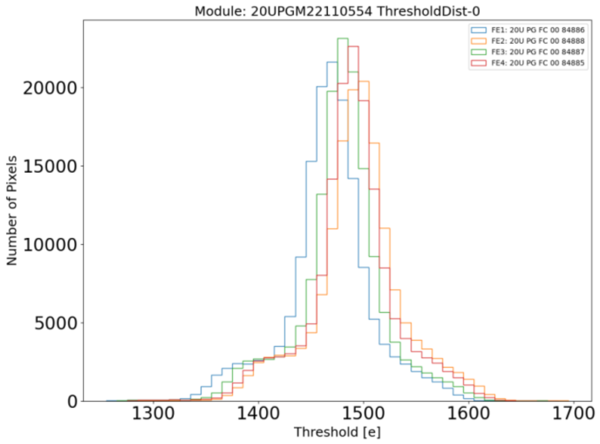
Initial module characterisation	*Initial module characterisation*	Parylene masking	Parylene coating	Parylene unmasking	Wirebond protection			Thermal cycling	*Burn-in*	*Module completed*	
Initial Warm	**Initial Cold**	**Parylene Masking**	**Parylene Coating**	**Parylene Unmasking (alt.)**	**Wirebond protection (alt)**	**Post Parylene Warm**	**Post Parylene Cold**	**Thermal cycles (at which T?)**	**Long term Stability Test**	**Final warm**	**Final cold**
INITIAL_WARM	INITIAL_COLD	PARYLENE_MASKING	PARYLENE_COATING	PARYLENE_UNMASKING	WIREBOND_PROTECTION			THERMAL_CYCLES	LONG_TERM_STABILITY_TEST	FINAL_WARM	FINAL_COLD
20 C										20 C	-15/-25 C (quads/triplets)
sensor IV										sensor IV	sensor IV
ADC Calibration										ADC Calibration	ADC Calibration
Analog readback										Analog readback	Analog readback
SLDO VI										SLDO VI	SLDO VI
Vcal calibration										Vcal calibration	Vcal calibration
Injection capacitance										Injection capacitance	Injection capacitance
LP mode										LP mode	
Data Transmission										Data Transmission	Data Transmission
Min. health test										Min. health test	Min. health test
Tuning										Tuning	Tuning
Pixel Failure Ana										Pixel Failure Ana	Pixel Failure Ana (including source scan)

After Production Advance review make decision on further testing reduction:
- based on data
- incorporate understanding on inputs needed for grading
- evaluate risks

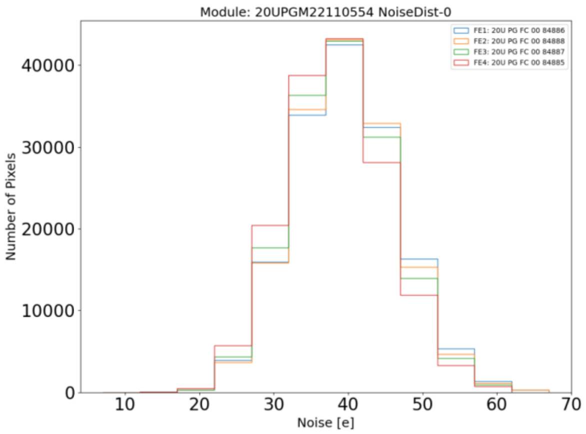
Module QC status and Results

Key	Data
MODULE_TEMPERATURE	20
ANALYSIS_VERSION	localdb-tools v2.2.39-rc7
QUAD-MODULE_ADC_CALIBRATION	1 2 3 4
QUAD-MODULE_SLDO	1 2 3 4
QUAD-MODULE_VCAL_CALIBRATION	1 2 3 4
QUAD-MODULE_ANALOG_READBACK	1 2 3 4
QUAD-MODULE_LP_MODE	1 2 3 4
QUAD-MODULE_OVERVOLTAGE_PROTECTION	1 2 3 4
QUAD-MODULE_INJECTION_CAPACITANCE	1 2 3 4
QUAD-MODULE_MIN_HEALTH_TEST	1 2 3 4
QUAD-MODULE_TUNING	1 2 3 4
QUAD-MODULE_PIXEL_FAILURE_ANALYSIS	1 2 3 4
MODULE_BAD_PIXEL_NUMBER	503
MODULE_ELECTRICALLY_BAD_PIXEL_NUMBER	499
MODULE_DISCONNECTED_PIXEL_NUMBER	4
MODULE_HIGHEST_NUMBER_BAD_PIXELS_CLUSTER	N/A
QUAD-MODULE_UNDERSHUNT_PROTECTION	1 2 3 4
QUAD-MODULE_DATA_TRANSMISSION	1 2 3 4





Threshold

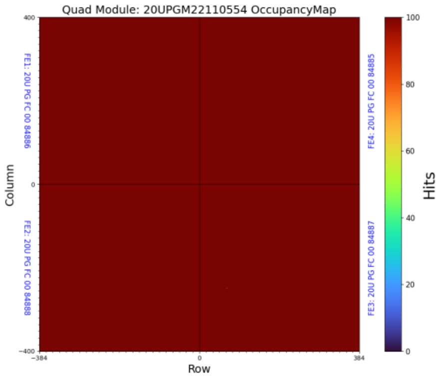


Noise

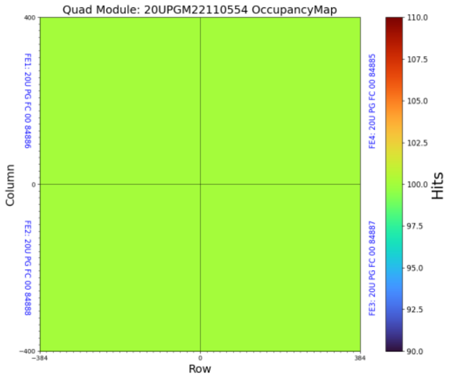
Module QC status and Results

>> Pixel Failure Analysis

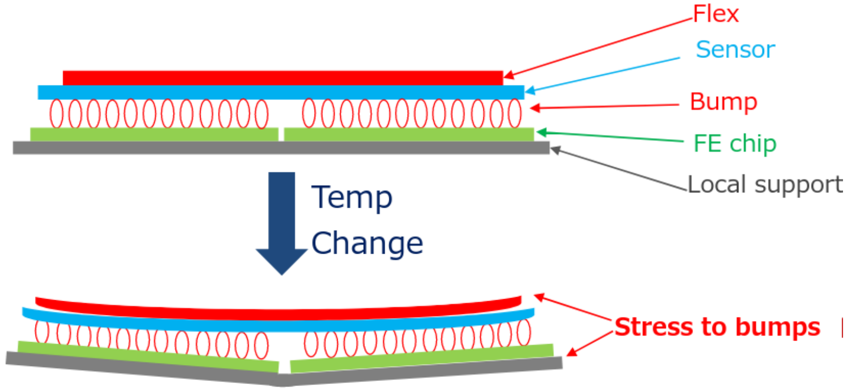
Digital scan

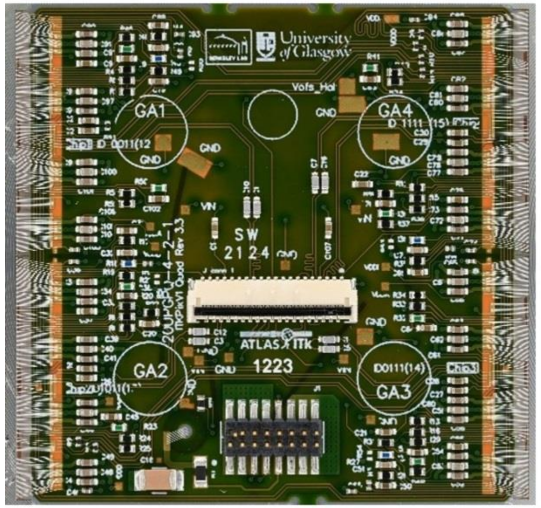


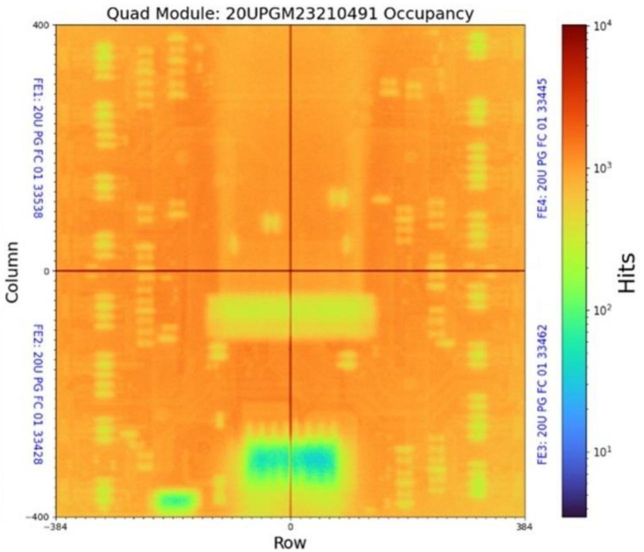
Analog scan

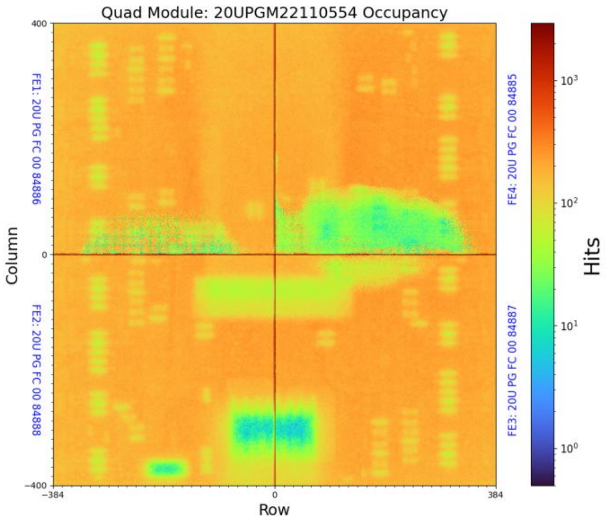


The deformations of a module under thermal stress

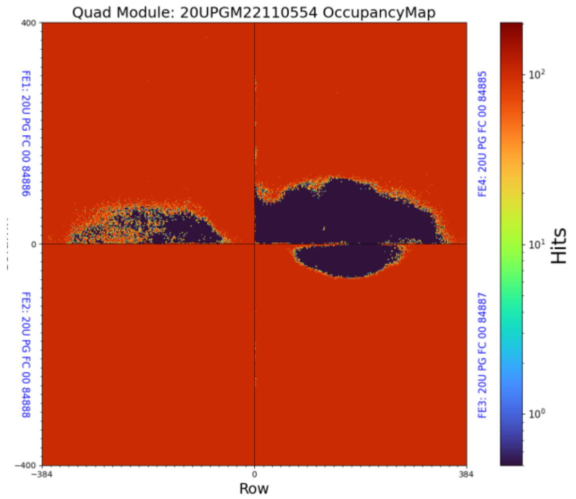




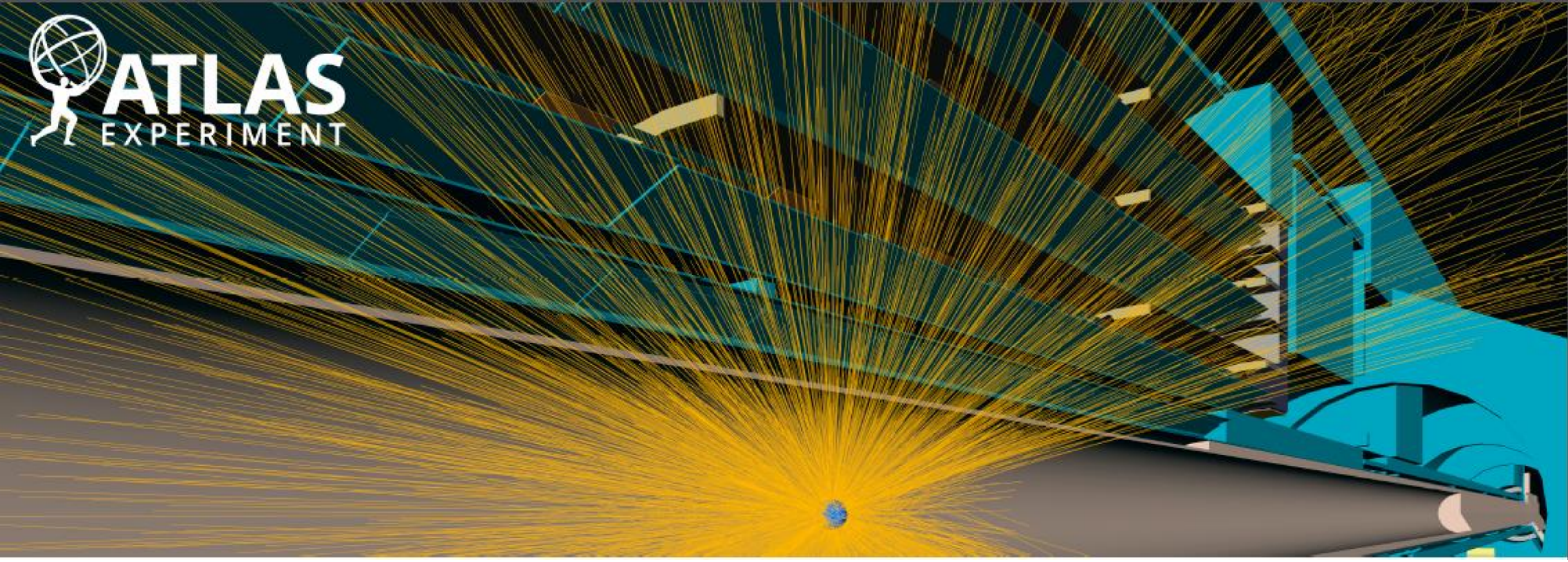




Source scan



Disconnected bumps



Thank you for your attention!!!