Updates on EICROC0 characterization at BNL: Digital Data Analysis

Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

B1 Board

Alex Jentsch (BNL)

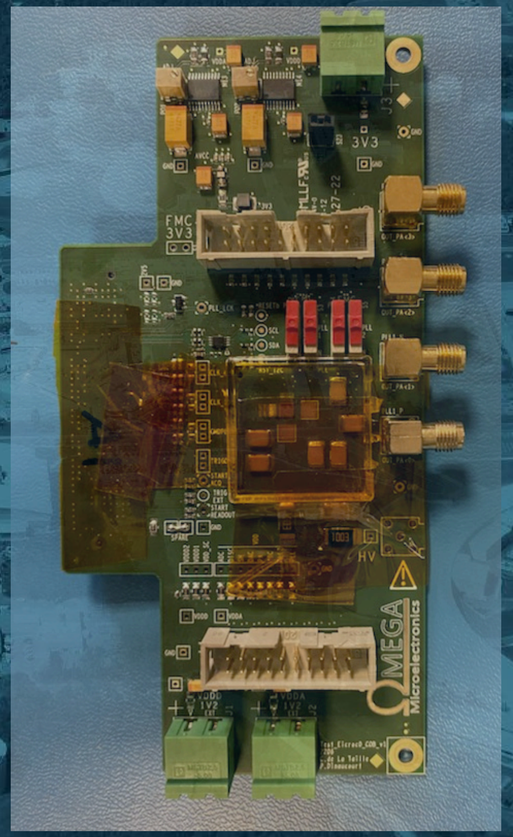
Ashik Ikbal (KSU)

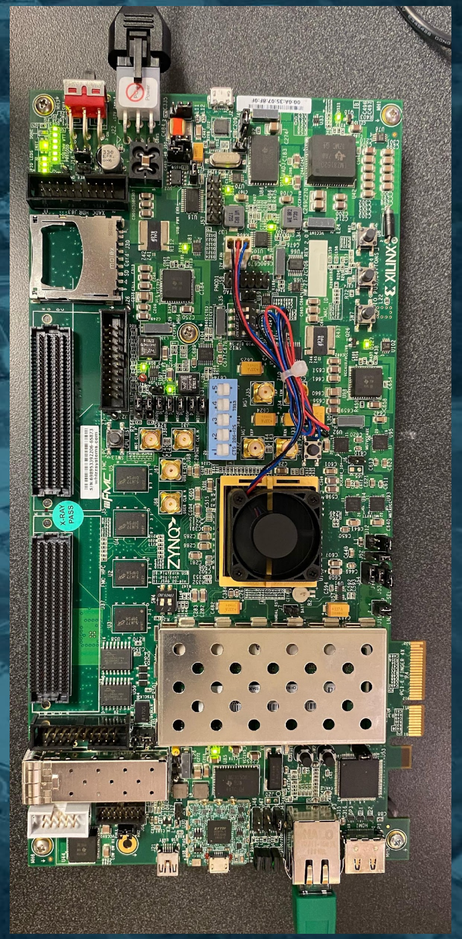
Souvik Paul (SBU)

Prashanth Sanmuganathan (BNL)

Prithwish Tribedy (BNL)

Alessandro Tricoli (BNL)





EICROC0 Meeting
Jun 23, 2025

BNL Test Bench Setup

LV Voltage = 3.3 V

LV Current Limit = 0.2 A

LV Current Consumption = 0.156 A

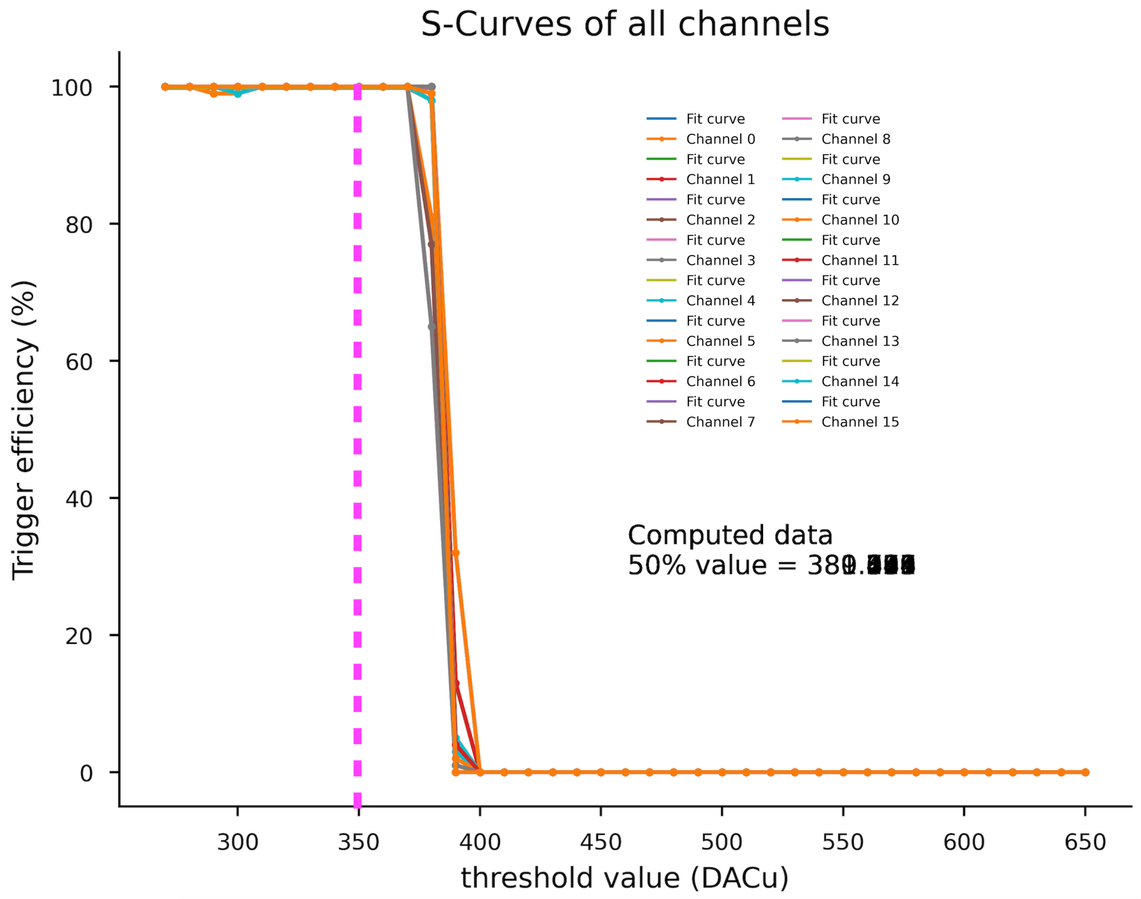
J5 Connector	Ideal (V)	BNL (V)
Vddd	~1.2	1.261
Vdda	~1.2	1.258
V_vbg_1V	~1	1.035

Sensor Bias Voltage: -100 V

Mode: Charge Injection
Board: B1 (ASIC+Sensor)

Threshold Scan @ Charge = 40 DAQu
Safe Threshold = 350 DAQu

40 MHz and 160 MHz clock: **OFF**

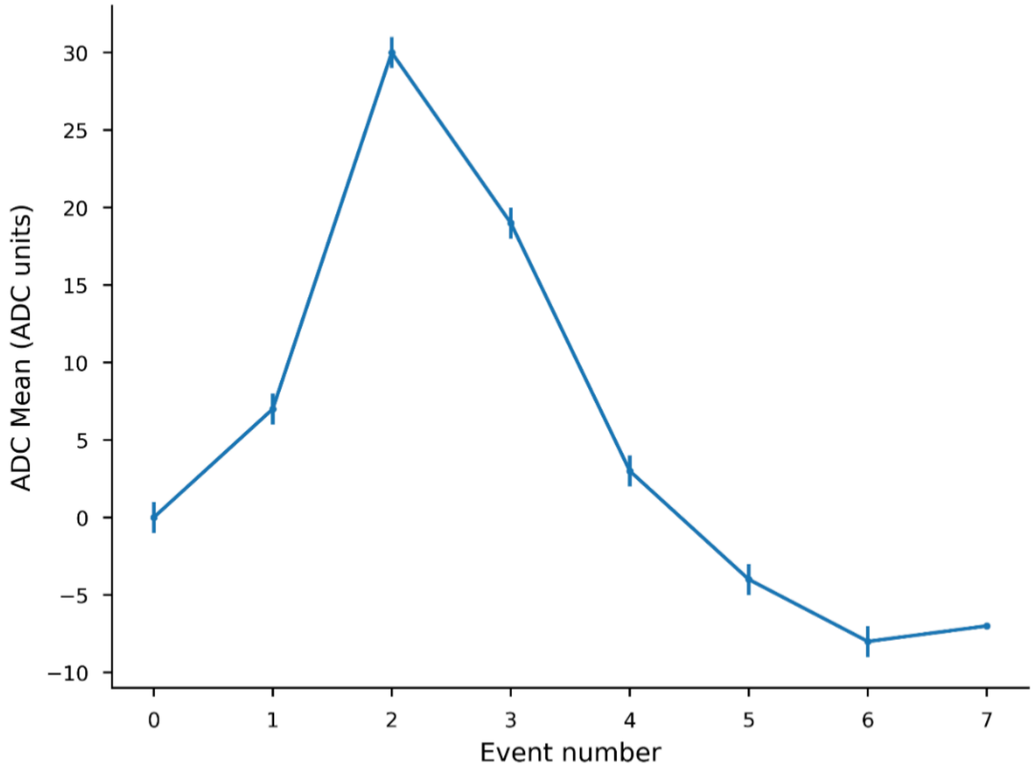


Q1: What is the optimal threshold value for all charges?

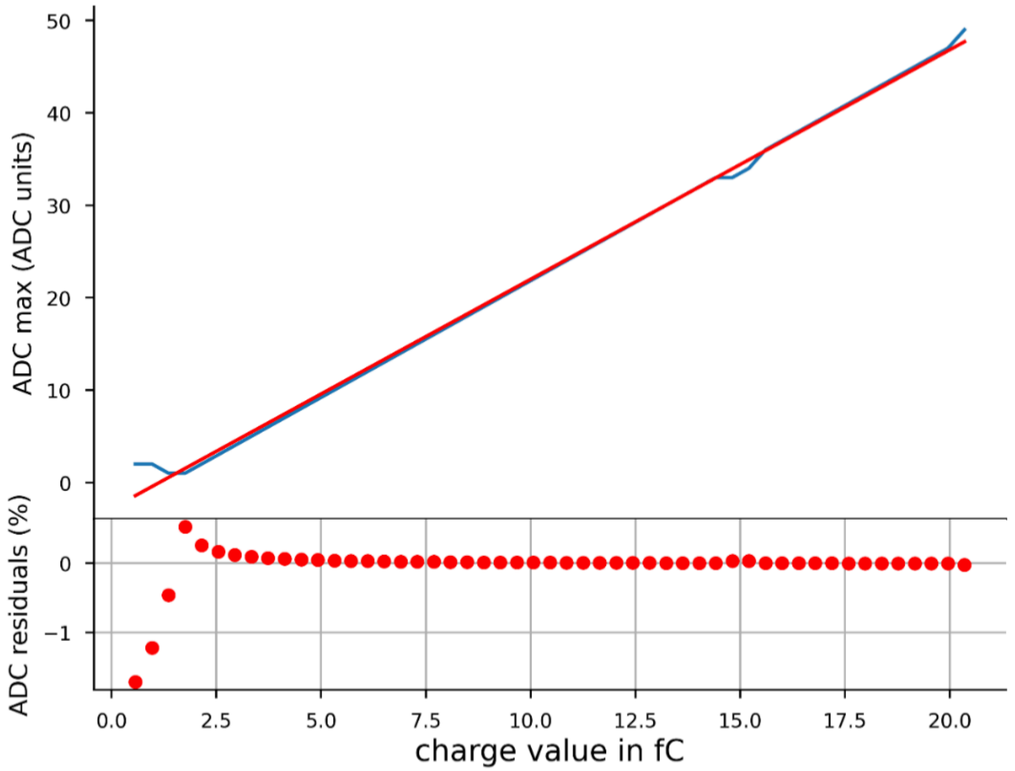
Q2: What's the effect of the clock on the S-curve?

Comparing ADC Results with Adrien

ADC : Channel 0 – ASIC with sensor



ADC Pulse reconstruction
(obtained with correction)

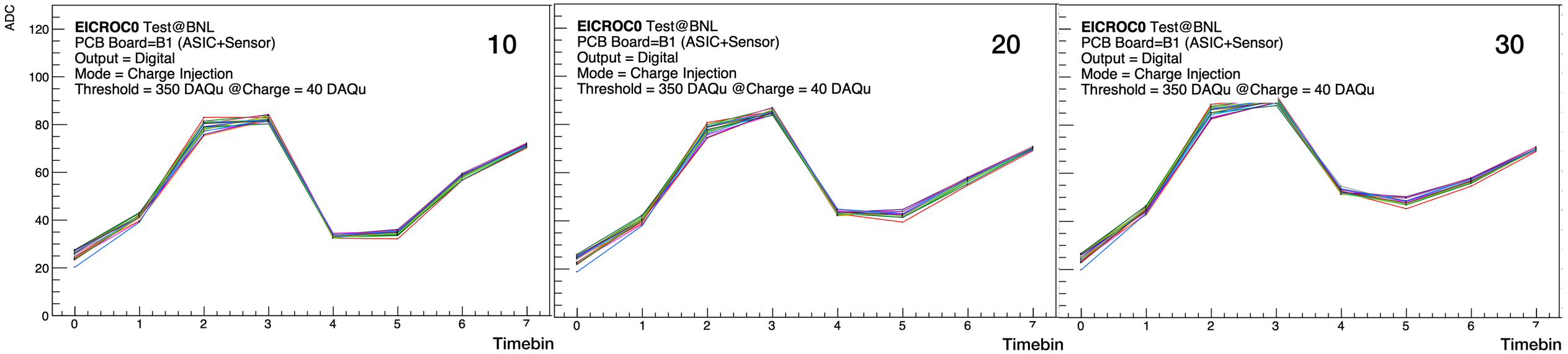


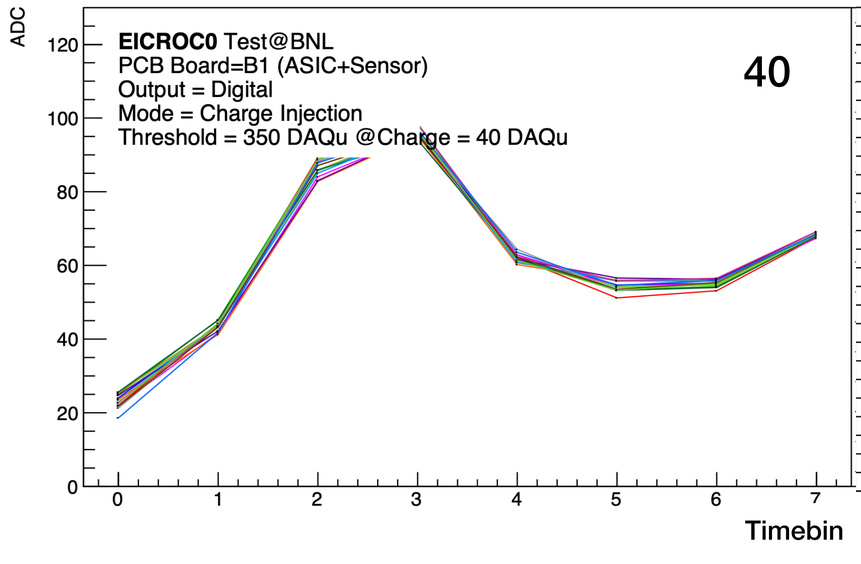
ADC max vs charge sweep

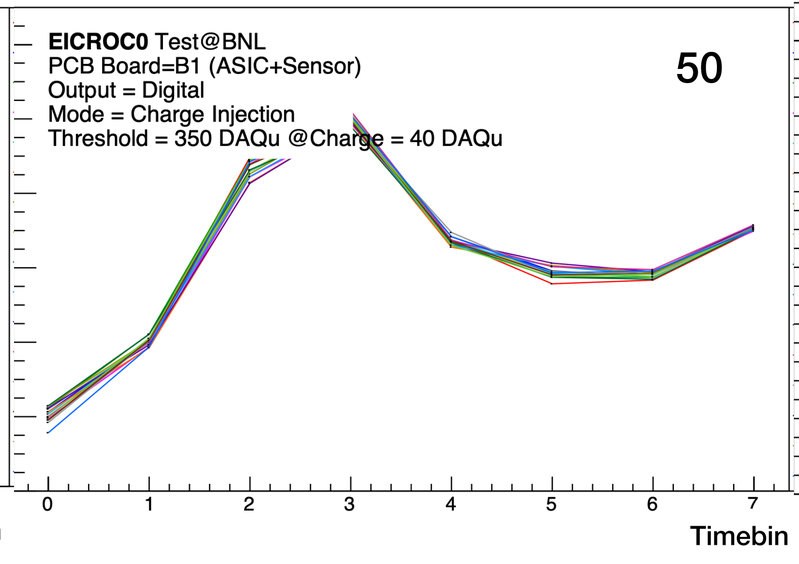
Elaborate?

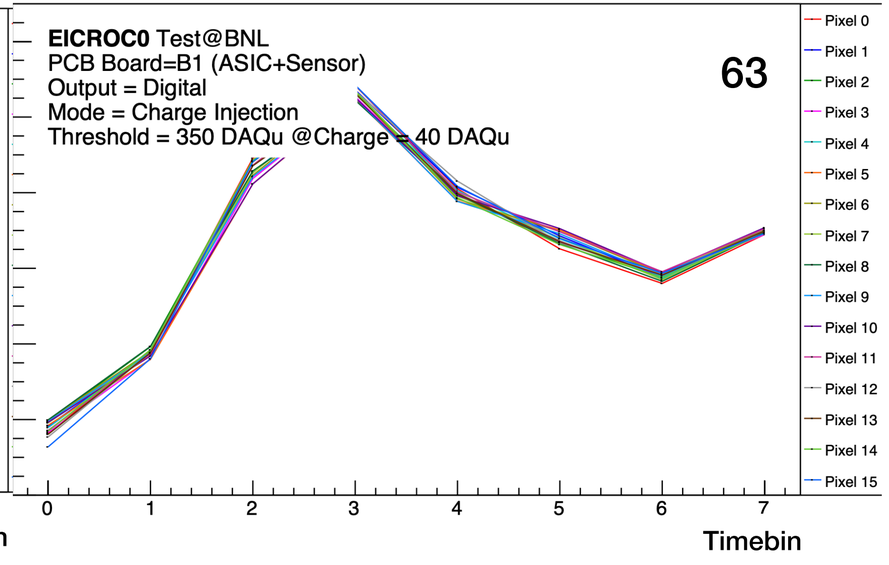
Charge Sweep: ADC Mean vs Timebin

- Similar amplitude and trend across different charges using threshold set @ 40 DAQu

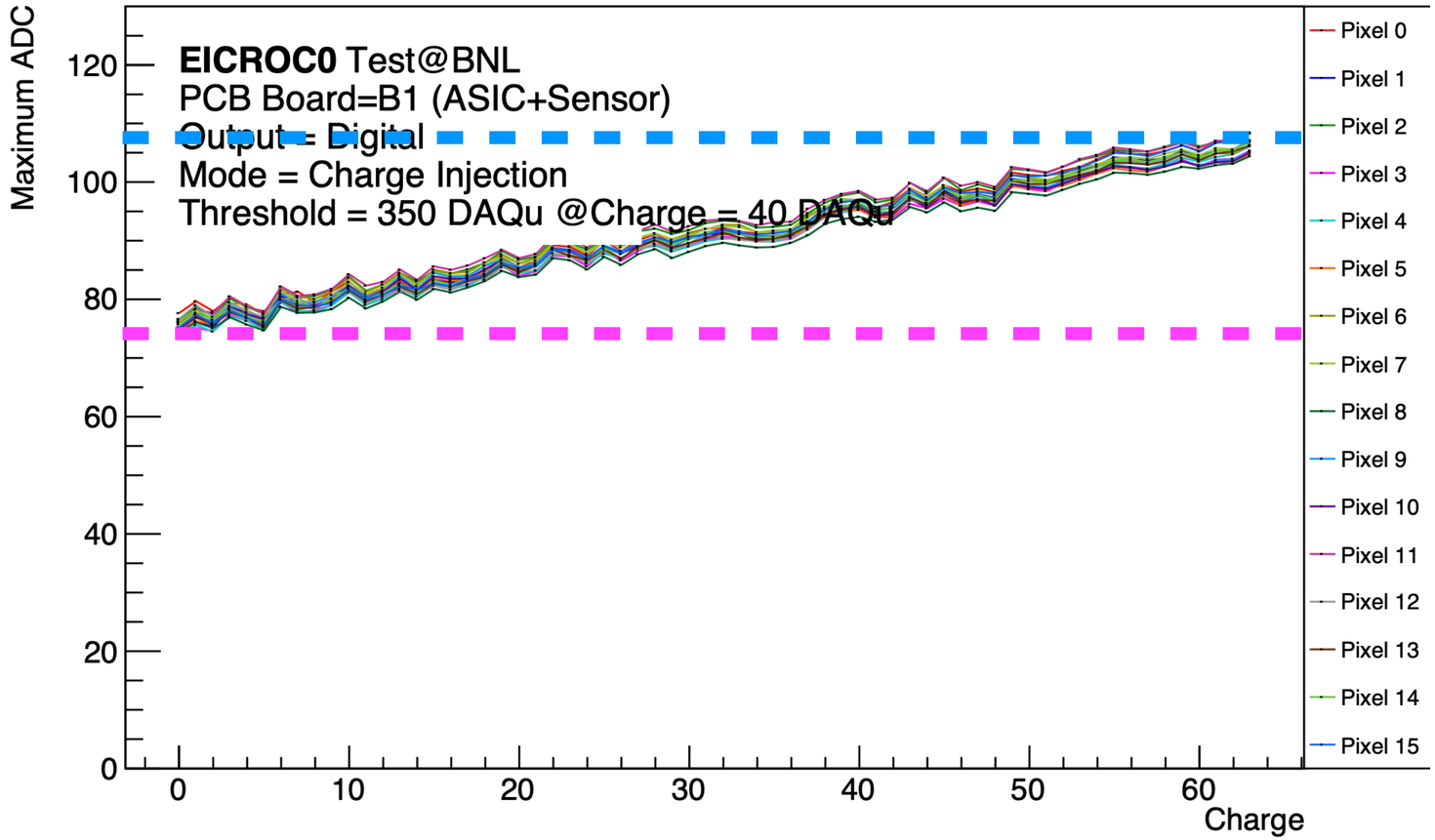








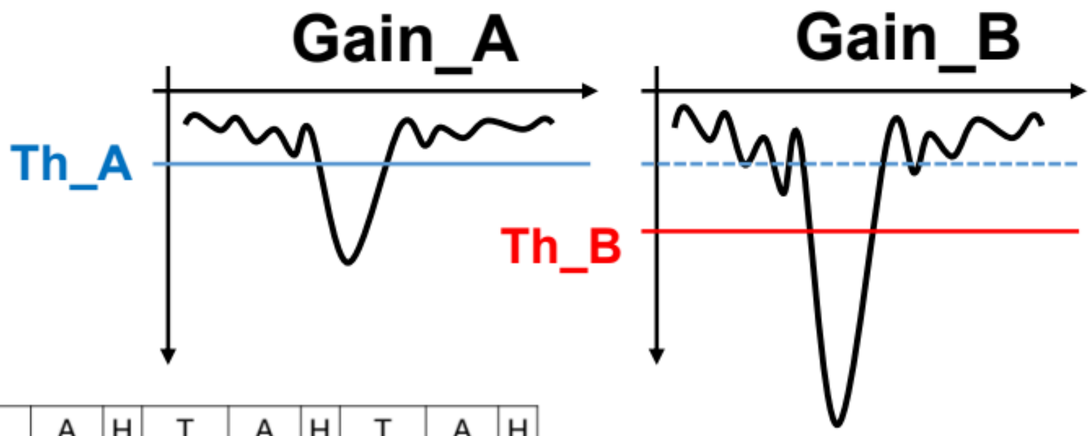
Charge Sweep: Max ADC vs Charge



- Presence of pedestal in ADC data. **Pedestal subtraction: Online or Offline?**
- Difference between lowest and highest Max ADC = 32 DAQu.
  Larger consequence of increasing charge on digital data?
- Fluctuations are less when thresholds are set using higher charge values

Charge Sweep: TDC Data Construction

Every channel has a unique gain
→ Unique threshold for every channel



Data Format: {TDC, ADC, HB} x 8

Th=70 DAC **Low threshold**

Event #	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H
43125864692	525	88	1	469	88	1	526	88	1	0	88	0	516	88	1	0	88	0	0	88	1	1024	88	0

Th=160 DAC **Optimal threshold**

Event #	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H
52838449618	0	88	0	0	88	0	0	88	0	157	88	0	0	88	0	0	88	1	0	88	0	0	88	0

Th=220 DAC **High threshold**

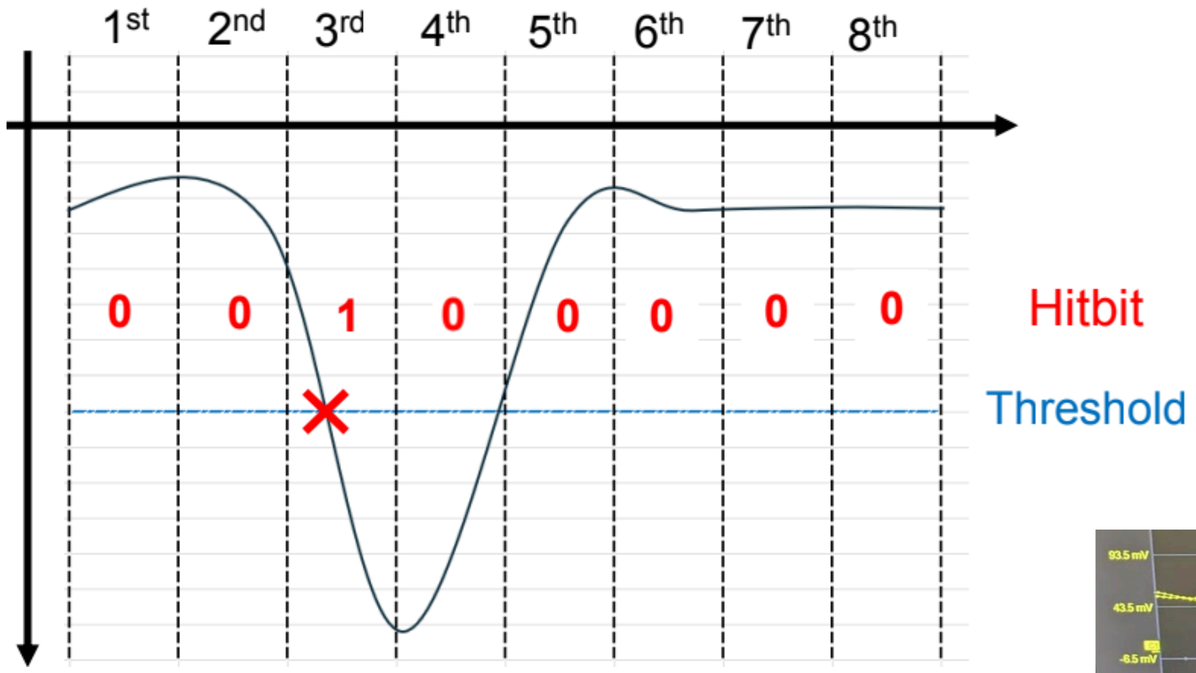
Event #	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H
62320292269	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0

Charge Sweep: TDC Data Construction

Timebin: 8th ... 1st

Event #	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H	T	A	H
16386365889	0	68	0	0	34	0	0	18	0	0	54	0	472	121	0	0	112	1	0	58	0	0	72	0

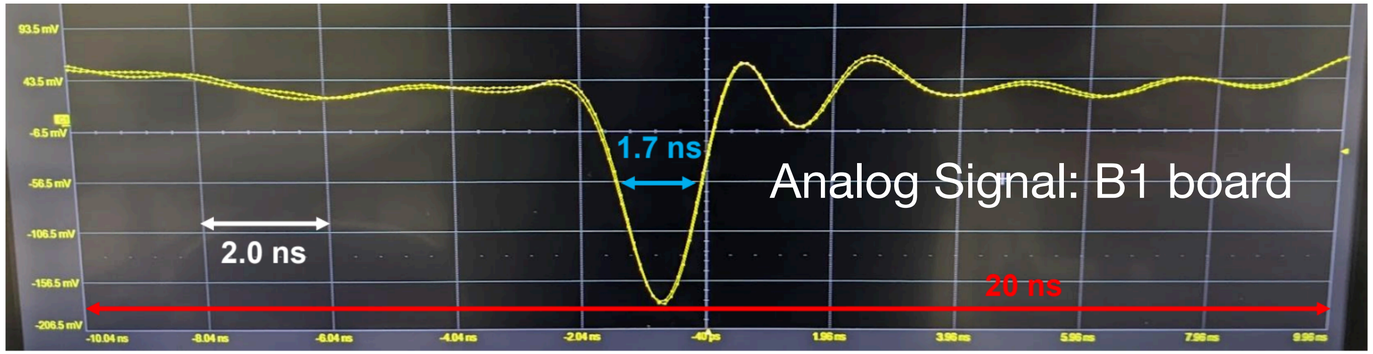
25 ns



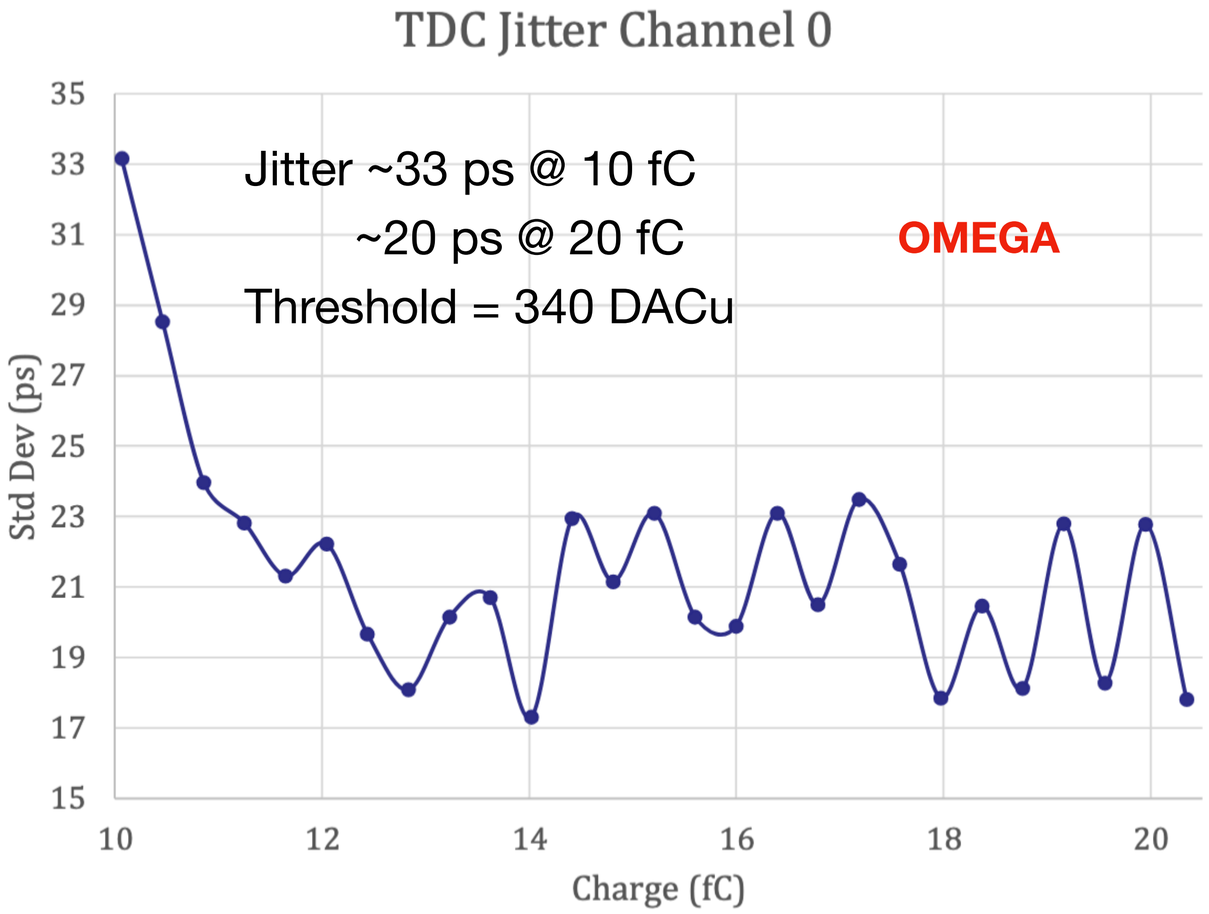
Q3: Characteristics of Timebin?

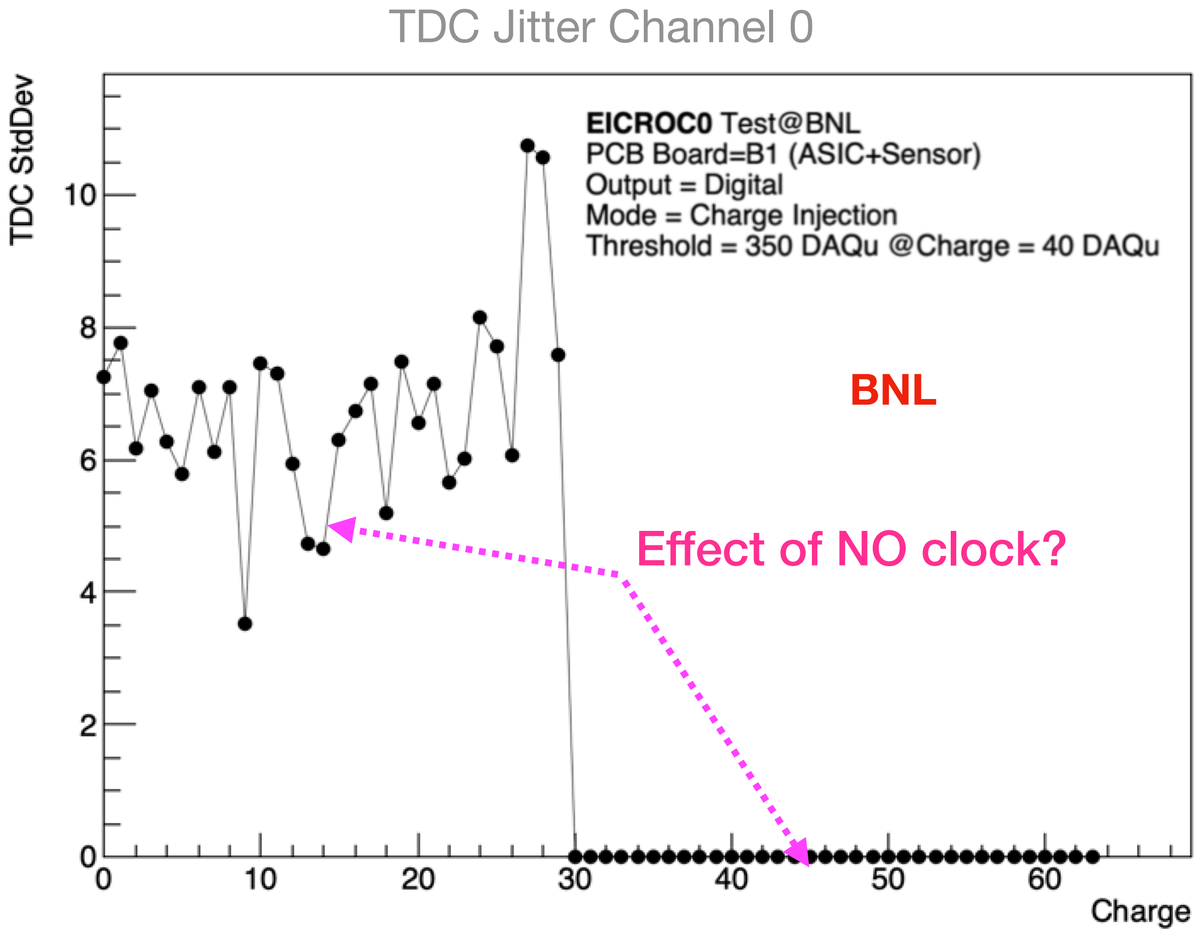
- TDC = 10 bit (0 – 1023) , 1 unit = 25 / 1024 ns
- 1 event = 8 time-samples
  = 25 ns
  = 10 bit

Q4: When is a HitBit registered?



Comparing TDC Jitter Results with Adrien





- TDC Jitter: Decreasing behaviour with increasing charge

- TDC Jitter
  - Random behaviour @ Charge < 30 DAQu
  - 0 @ Charge > 30 DAQu
- No TDC/HitBit for Charge > 30 DAQu

Summary

Conclusions

- Digital data with B1 board (ASIC+Sensor)
  - Understanding the data structure
  - Max ADC increases monotonously with increasing charge
  - Pedestal Subtraction & effect of clock on pedestal
  - TDC Jitter shows random behaviour for charge < 30 DAQu
  - TDC Jitter = 0 for charge > 30 DAQu

Future Work

- Take digital data with 40 MHz clock ON

Q5: Sync laser trigger and CMD pulse to make sense of digital data using TCT Scan?