



Update on EICROC0 testing effort at IJCLab



➤ Measurements with ^{90}Sr β source

- First analysis based on digital (ADC & TDC) data

Arzoo's talk

➤ Update on IR laser test bench development

Ana's talk

➤ Update on EICROC0 PCBs

➤ Update on firmware porting associated to ZCU106 FPGA board

➤ Update on next EICROC iterations

OMEGA team

➤ Discussion

Dominique Marchand on behalf of
Olivier Brand-Foissac, Vincent Chaumat, Thomas Cornet, Mathurin Grossetête,
Beng-Yun Ky, Arzoo Sharma, Laurent Serin, Ana-Sofia Torrentó

06/16/2025 - EICROC0 meeting

➤ 8 PCBs partially cabled at IJCLab (finalization end of May)

- 5 at BNL
 - 3 to be kept at BNL for testing needs
 - 2 to be shipped back to IJCLab after wire-bonding a flip chip (HPK sensor with metalization removed + EICROC0) *To be exploited with the IR Laser test bench (Summer '25)*
- 3 at IJCLab for next EICROC0 iterations



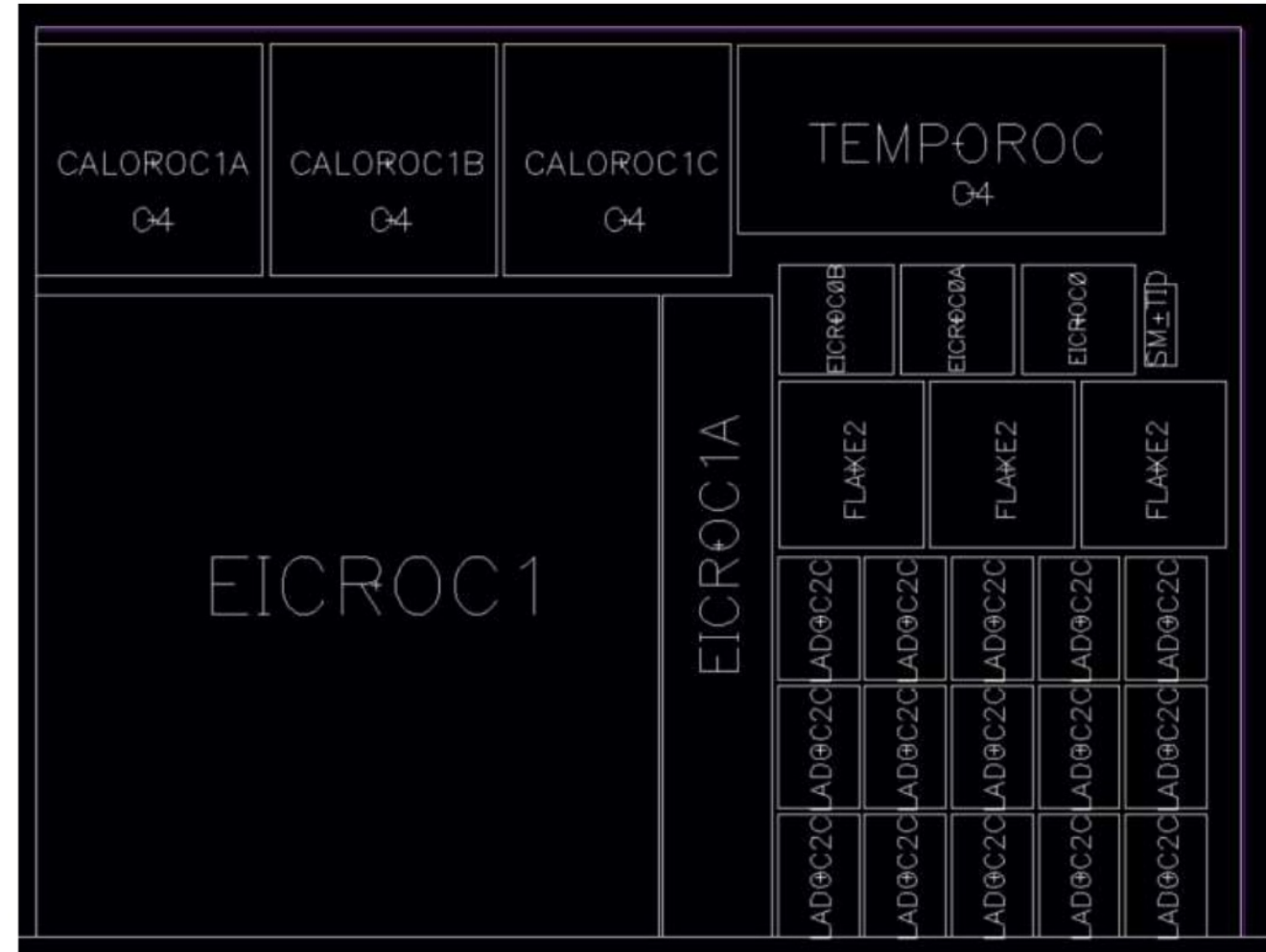
Update on firmware development concerning updated FPGA board

AMD Zynq™ UltraScale+™ MPSoC ZCU106

Still under development

- Firmware porting **DONE**
- For **I2C full compatibility** reasons: requires replacement of some « pull-up » resistor values on the PCB
 - Optimized resistor values still to be determined: **work on progress** with a PCB holding an EICROCO ASIC (only)
- Once successful resistor values determined, further tests will be performed at IJCLab before sharing with you the firmware/software suite.
We'll keep you informed

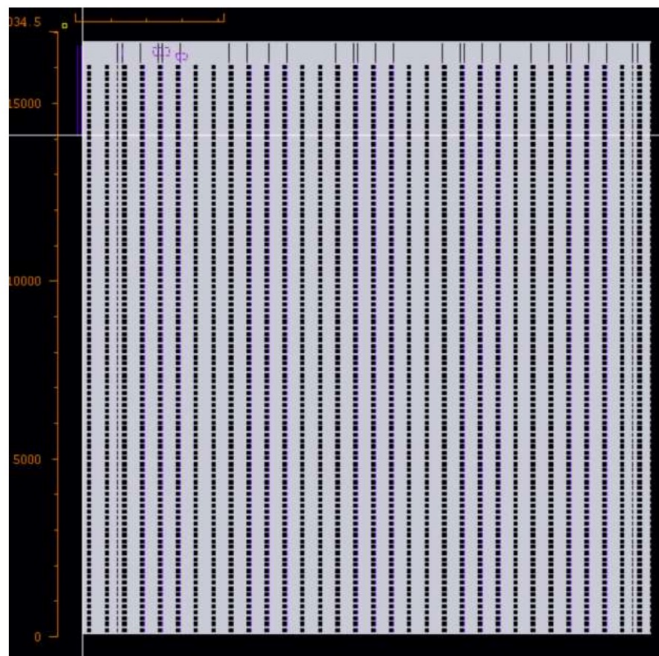
- TSMC now requires to fully populate the reticle
 - Cost ~300 k€
- For EIC we have
 - 1 EICROC1 32x32
 - 1 EICROC1A 4x32
 - 3 EICROC0/A/B 4x4
 - 3 CALOROC1A/B/C
 - ~70% of reticle area
 - EICROC1 is 40% of reticle area
 - gds files loaded end of may
- Still administrative issues delaying the start of fabrication



- **EICROC0A** same as EICROC0 with more testability
 - Each pixel can be by-passed by SC (clock is then turned off)
 - Buffers in SC to allow extension to 4x32
 - Larger dynamic range in pulse injection
- **EICROC0B**
 - Same preamp/discriminator/TDC/integrator
 - ADC and driver replaced by peak sensing and Wilkinson ADC
 - Currently ADC path ~ 1 mW/ch becomes 200 μ W/ch
- Will be fabricated with EICROC1 below

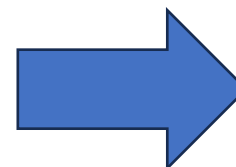
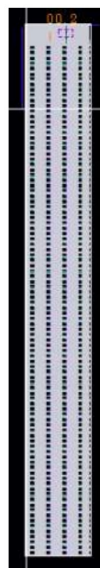


- 32x32 chip : final dimensions
- Goal :
 - test full-scale chip analog performance (IR drops)
 - Allow final sensor characterization
 - Test interface with DAQ : fast commands and 320 Mb/s data output
 - Progress on module/front-end boards
- Caveats ;
 - Not (yet) zero-suppressed data
 - Still 2mW/ch
 - Still analog-on-top



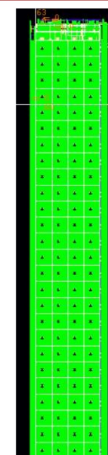
- Designed as 8 blocks of 4x32
 - Read out sequentially, like EICROC0
 - Pixel similar to EICROC0A
 - 8 CLPS outputs at 40 MHz
 - Clock tree for isochronous calib_pulse distribution

- Common balcony (End of column)
 - Biases and slow control
 - New : fast command decoder (clock, calib_pulse, enable_acquisition, start_readout)
 - Backup clock and cmd_pulse inputs available
 - New : 320 MHz serializer for 1 CLPS output



EICROC1A variant

- Full block of 4x32 of EICROC1 with old EICROC0 pinout
 - Same balcony as EICROC0A (same slow control parameters)
 - Same testboard and DAQ as EICROC0
 - Allows to test columns specific effects (IR drops)



Discussion

- **ePIC ASIC review meeting** (EICROC, CALOROC, CFDROC, SALSA, ALCOR): **June 2-3, 2025, Paris region**
Gathered ASIC designer teams, Dave Abbott, Elke Aschenauer, Fernando Barbosa, Rolf Ent, Jeff Landgraf



<https://indico.bnl.gov/event/28161/>

Very fruitful discussions

- Monday June 2nd and Tuesday morning at OMEGA
- Tuesday afternoon at CEA Saclay

Jointly organized by OMEGA, LLR, IJCLab and CEA/Irfu



- **ePIC meeting** (July 14-19, 2025, JLab): **we'll attend remotely**

- **Seeking for a postdoctoral researcher working at IJCLab: characterization of pixelated AC-LGAD with EICROC & simulation activities (i.e. exclusive process including far-forward detectors)**

(2,5 years, starting Oct. 2025)

Arzoo's contract is extended until January 9th, 2026. [original end: July 9th, 2025]