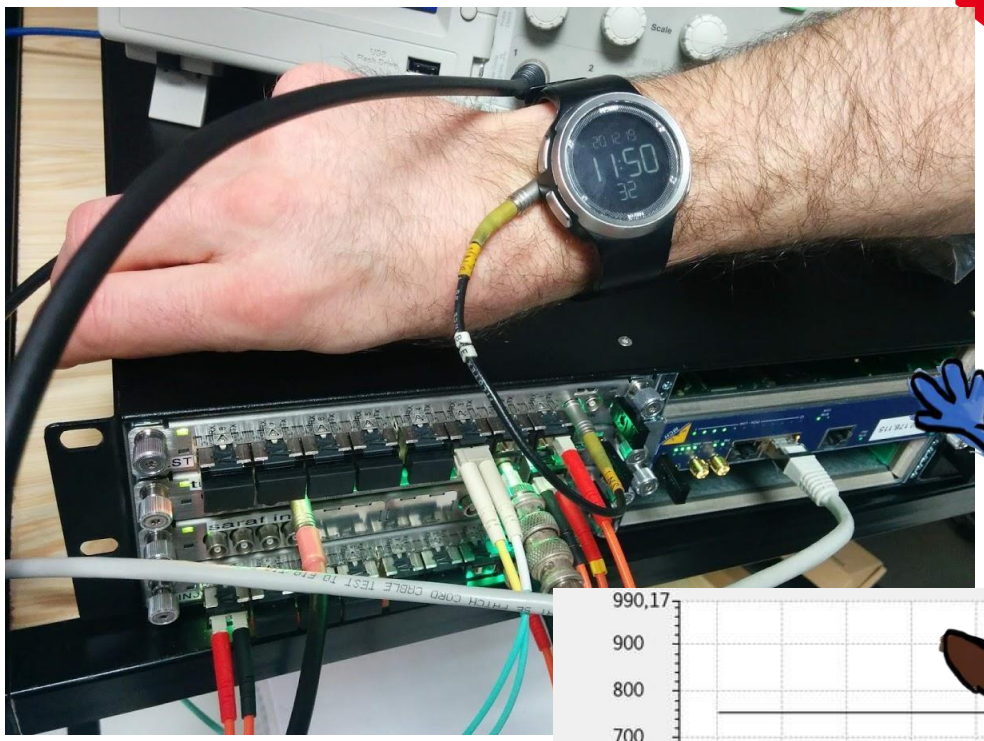
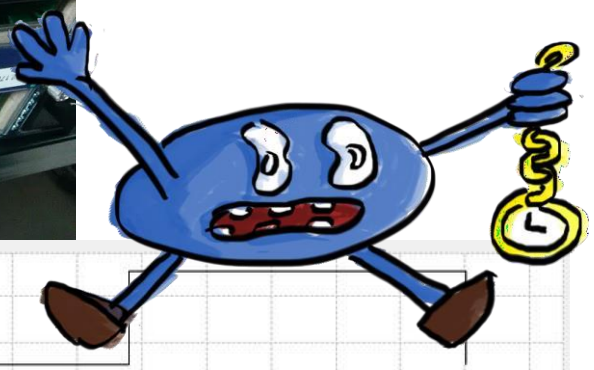
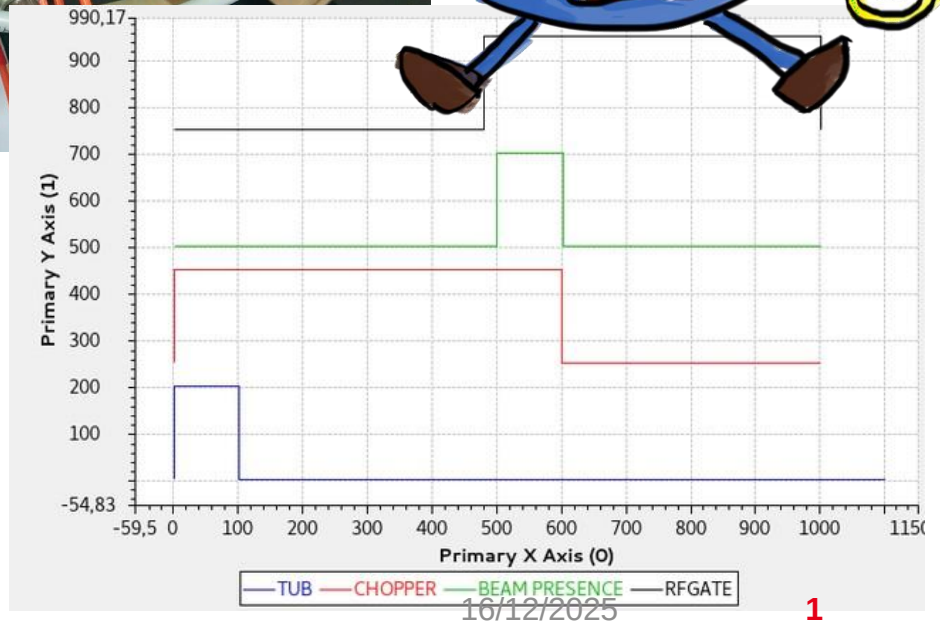
MRF Timing system appliqué à la synchronisation et à la protection machine de SARAF

Alexis Gaget IRFU / DIS /LDiSC







1. What is MRF timing system?

What is MRF Timing system ?

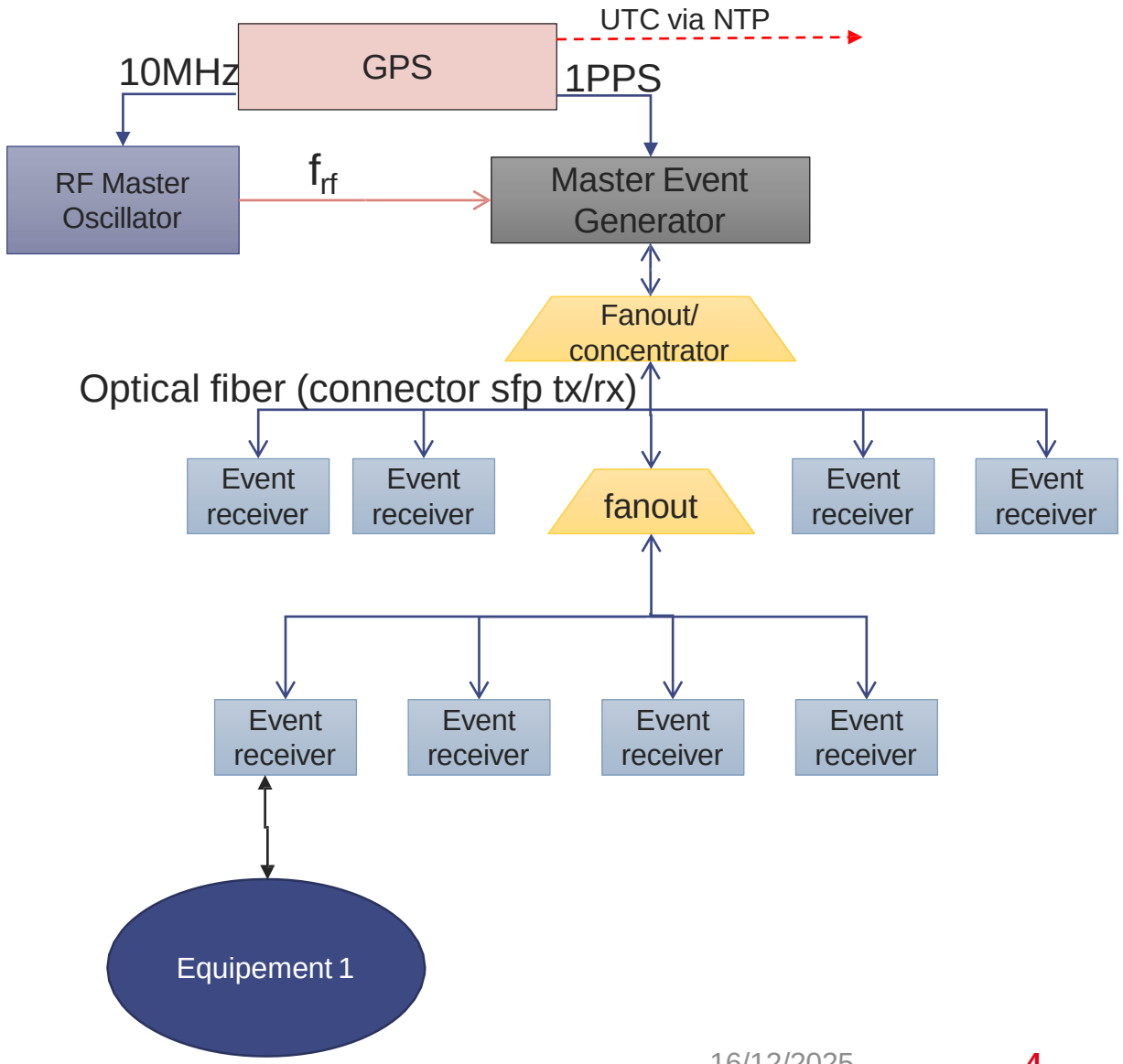
- Micro-Research Finland Oy
  - Founded in 1985
  - Timing System development initiated in 1999 by the design of the timing system for SLS (Swiss Light Source)
  - References:
    - **SLS, Paul-Scherrer Institute**, Switzerland
    - Diamond Light Source Ltd., U.K.
    - ASP, Australia
    - BEPCII, Insitute for High Energy Physics, Beijing, China
    - LCLS, Stanford Linear Accelerator Center, USA
    - SNS, Oak Ridge National Laboratory, USA
    - SSRF, Shanghai, China
    - Elettra, Trieste, Italy
    - ESS, Sweden
    - ALBA, Spain
    - And others...

Documentation : https://mrftiming.readthedocs.io/en/latest/hardware/mrfEventRef.html

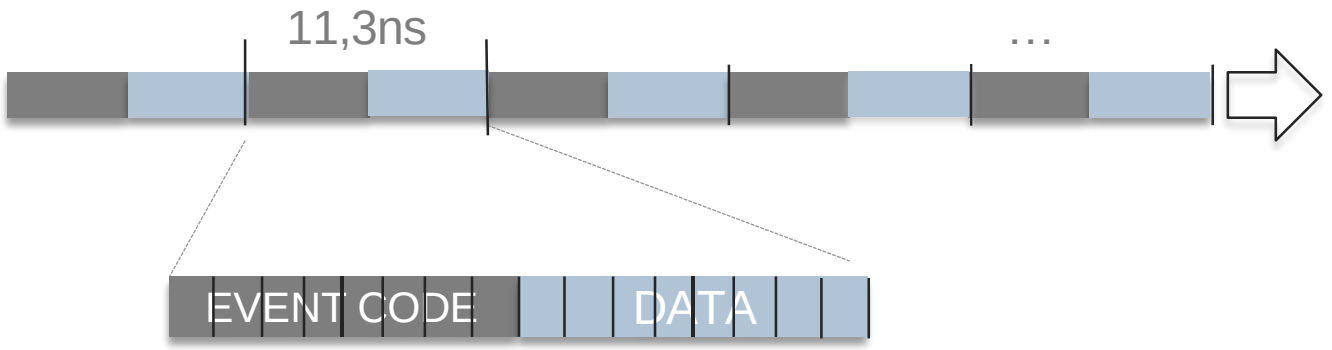
Official website : https://www.mrf.fi

Standard architecture

- Master Event Generator (EVG) generates a continuous data stream
- The (accelerator) synchronization frequency will be fed into the master event generator and used as the system clock.
- Event receivers synchronize to that clock and receive the data stream
- Fanout system distributes the signal downstream (and concentrates signals upstream)

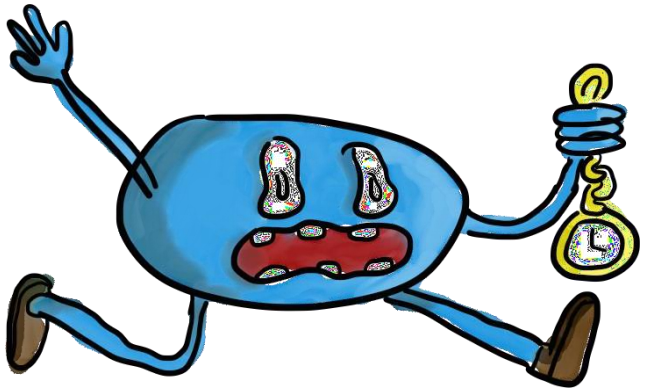


In (optical) wire protocol



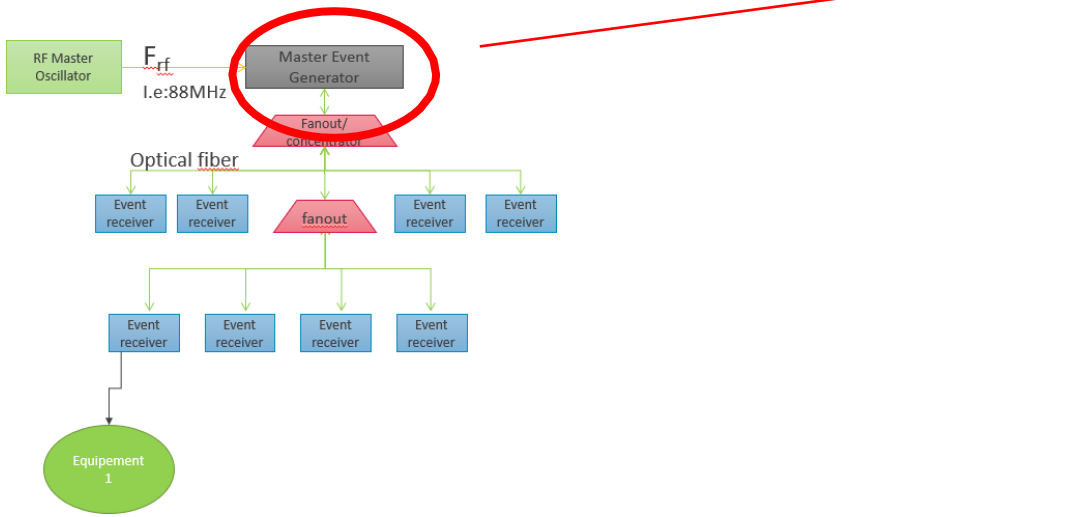
0-255
(some are reserved, check on MRF Documentation)

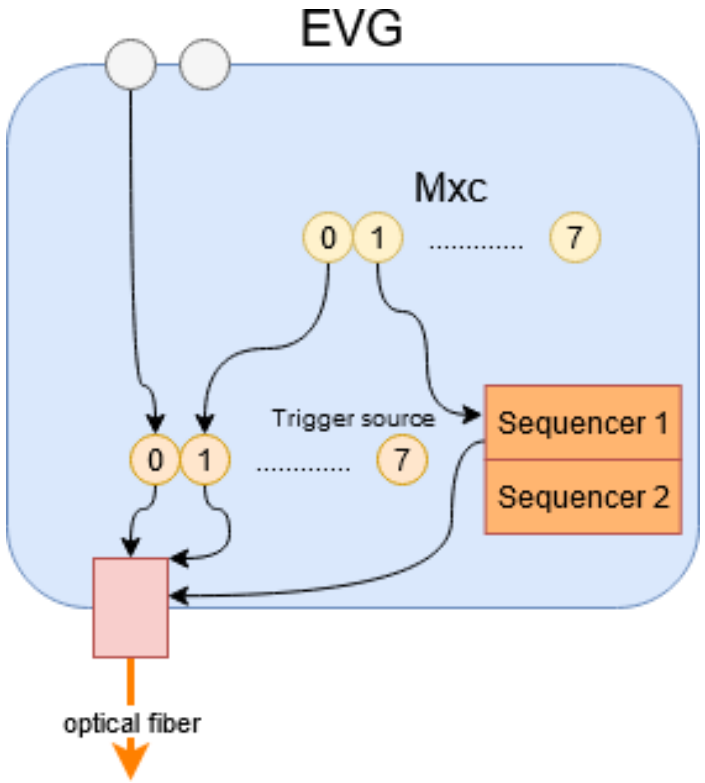
- 16-bit “frame” repeating at event clock frequency, e.g., 88 MHz
- Each frame contains an 8-bit event code and 8 bits for datas.



Understand the Event Generator (EVG)

- Event Generator (EVG) is responsible of creating and sending out timing events to an array of Event Receivers.
- 3 different ways
  - Software events (triggered by the software)
  - Trigger events x8 (trig one event)
  - Sequencer x2 (sequence of events)

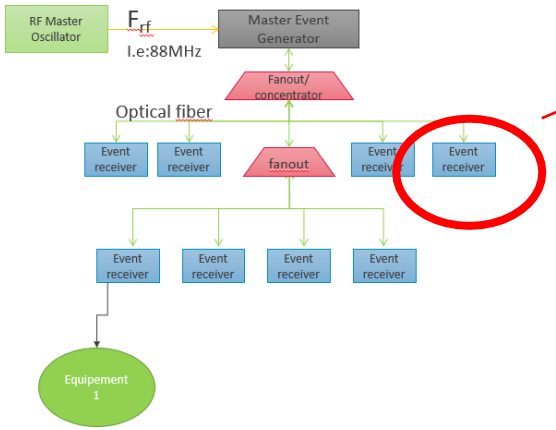


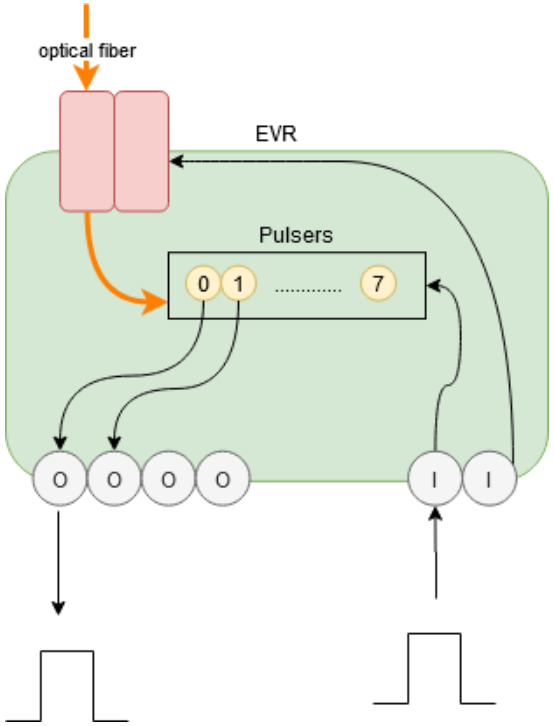


Mxc : Programmable Multiplexed counter

Understand the Event Receiver (EVR)

- “Decode timing events and signals from an optical event stream transmitted by an Event Generator.”
- Since generation “300”, EVRs can generate events itself :
  - Sequencer
  - software
- Output can be configured to react to a reception of a specific event code :
  - Trigger (pulse of a specified width and delay)
  - Set High or Low
- At the opposite Input can be configured to sent event upstream or locally



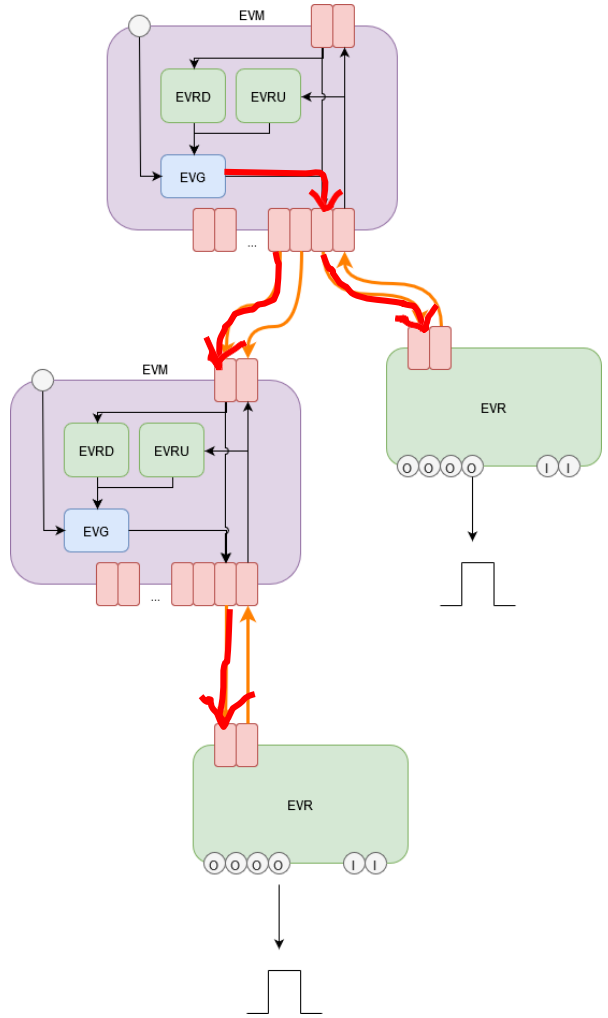


Timestamping

- EVG produces event 125 (reserved) at 1Hz
- Configured to have the timestamps from the « Sys Clk » meaning the date of the CPU executing the IOC.
- Internally the Clock provider of the EVR IOC is defined by the the mrf driver.
- EVRs update their PV « $(EVR):Time-I » that can be used as reference for other PVs
  - E.g :

```
record(ai, "$(P):myPV") {
  field(DESC, "Some timestamped PV")
  field(TSEL, "$(EVR)Time-I.TIME")
}
```

- Individual events counter can also be used as time reference for those events.
- EVRs can be use as NTP Server. For less critical PVs for example.

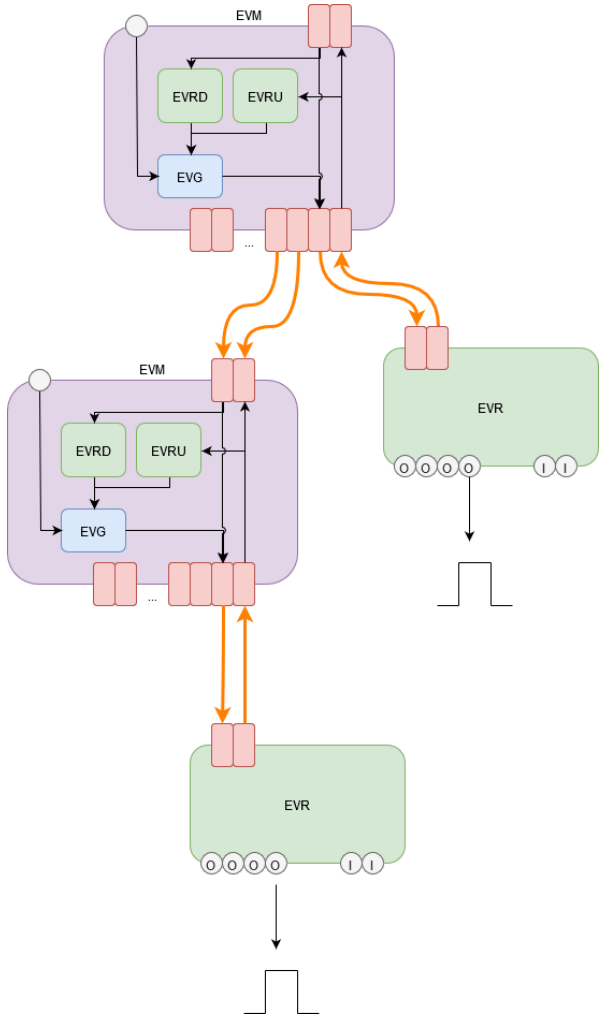


Delay compensation

“Delay compensation is achieved in measuring the propagation delay of events from the delay compensation master EVM through the distribution network up to the Event Receivers. At the last stage the EVR is aware of the delay through the network and adjusts an internal FIFO depth to match a programmed target delay value.”

- EVM Fanout have to be well configured as fanout
- 15 minutes to stabilize

WARNING : delay compensation impacts upstream propagation time.



3. MRF Hardware

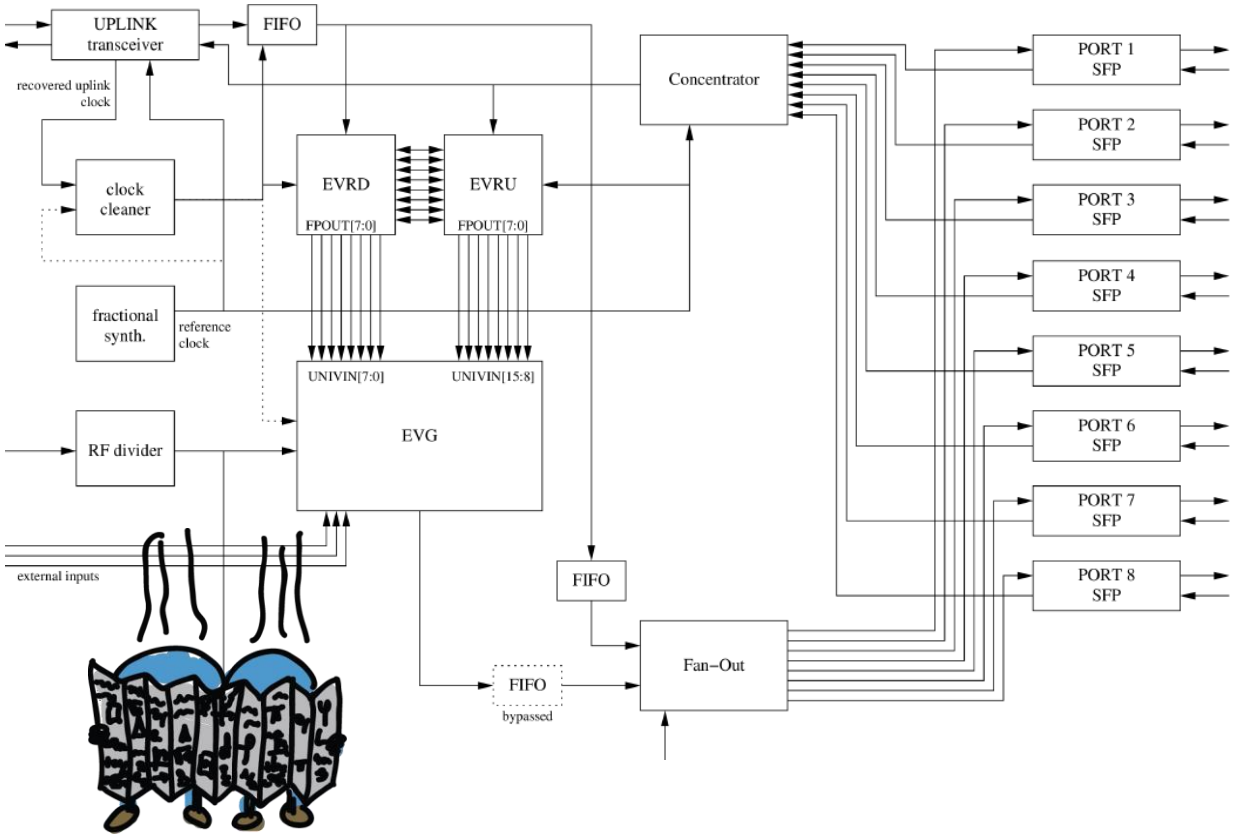
Different types

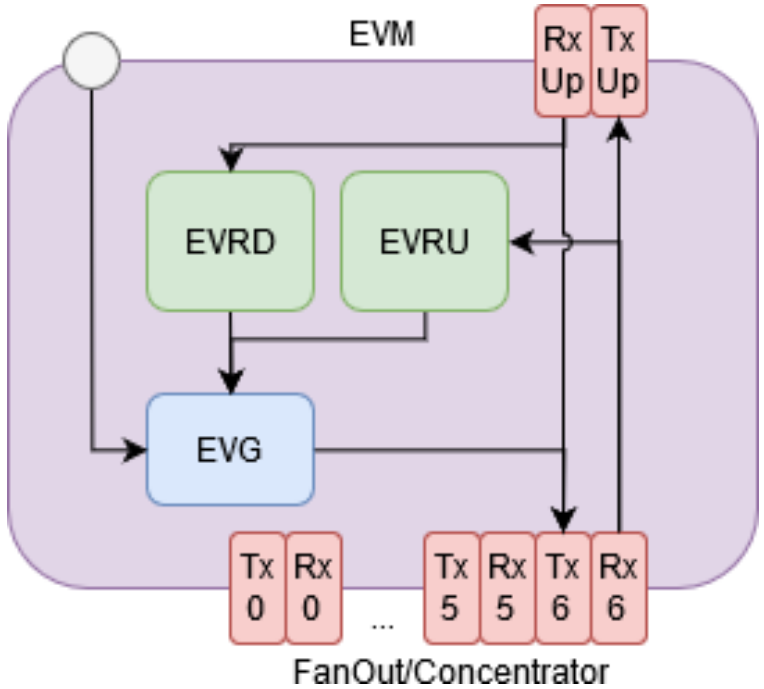
- cPCi
- VME
- MTCA

See other accelerators build their own EVR.

MTCA EVM 300

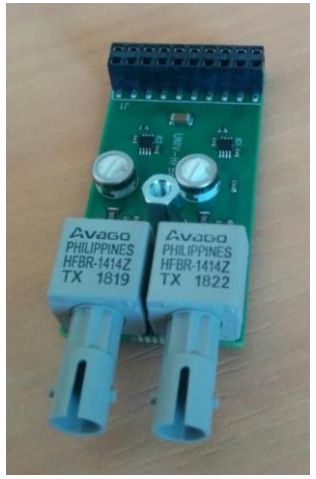

TLIN
RFIN
EVM-300


UPLINK transceiver
FIFO
recovered uplink clock
clock cleaner
EVRD
FPOUT[7:0]
EVRU
FPOUT[7:0]
Concentrator
PORT 1 SFP
PORT 2 SFP
PORT 3 SFP
PORT 4 SFP
PORT 5 SFP
PORT 6 SFP
PORT 7 SFP
PORT 8 SFP
fractional synth.
reference clock
UNIVIN[7:0]
UNIVIN[15:8]
EVG
RF divider
external inputs
FIFO
FIFO
bypassed
Fan–Out

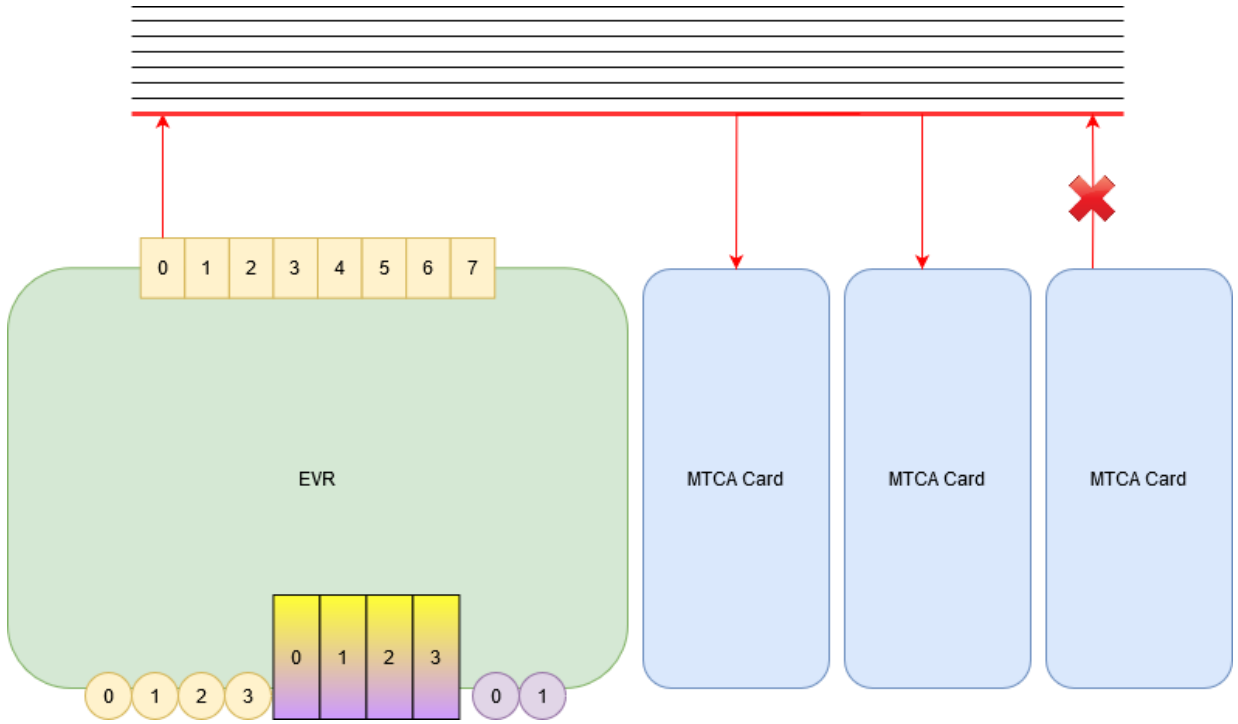

EVM
Rx Up
Tx Up
EVRD
EVRU
EVG
Tx 0
Rx 0
...
Tx 5
Rx 5
Tx 6
Rx 6
FanOut/Concentrator

MTCA EVR 300U

- MTCA authorized 8 backplane inputs/outputs (Every client card can “subscribe” to a trigger, only one can
  write to the channel)
- Front end
  - 4 outputs
  - 2 inputs
  - 4 Univ Input/Output (TTL, optical fiber..)



Universal output

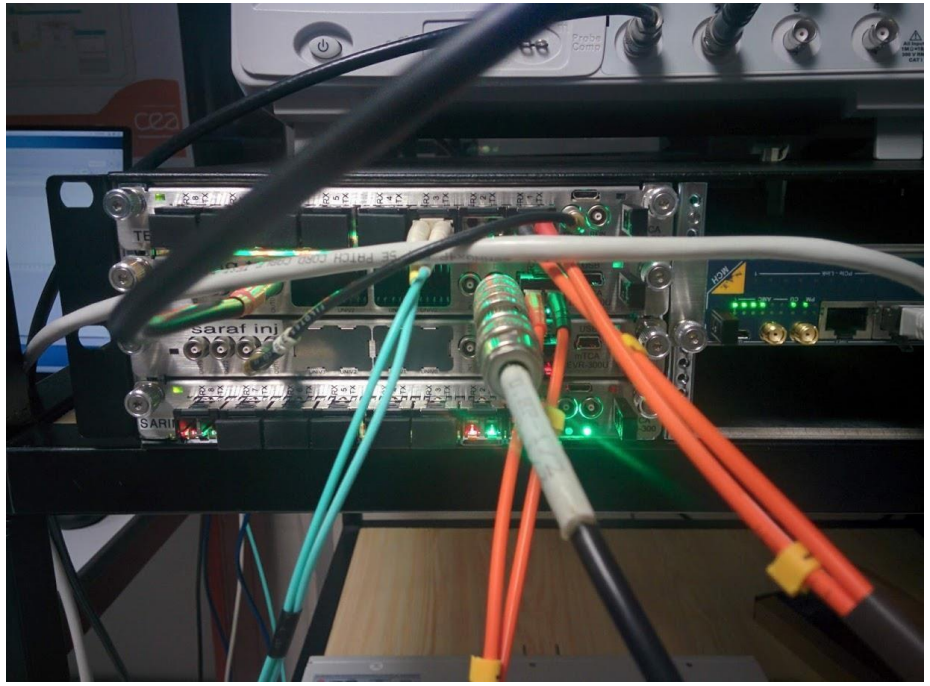


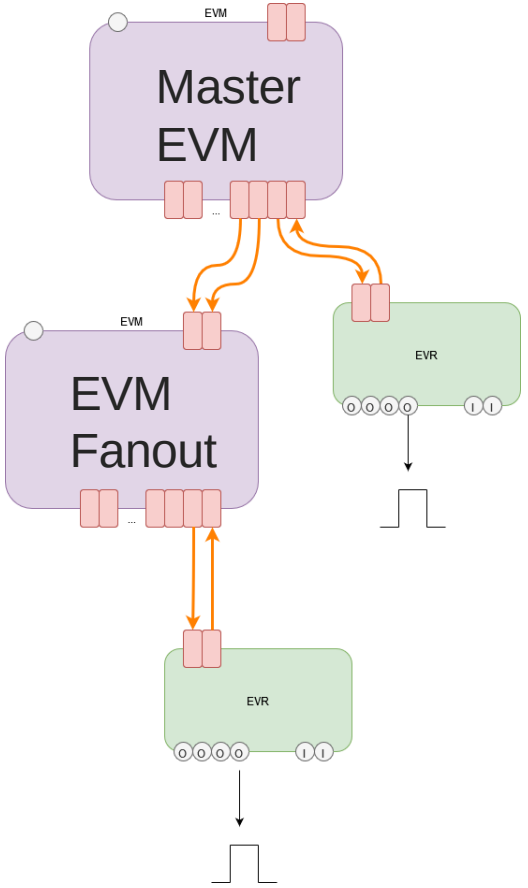
4. Various cases

Standard installation

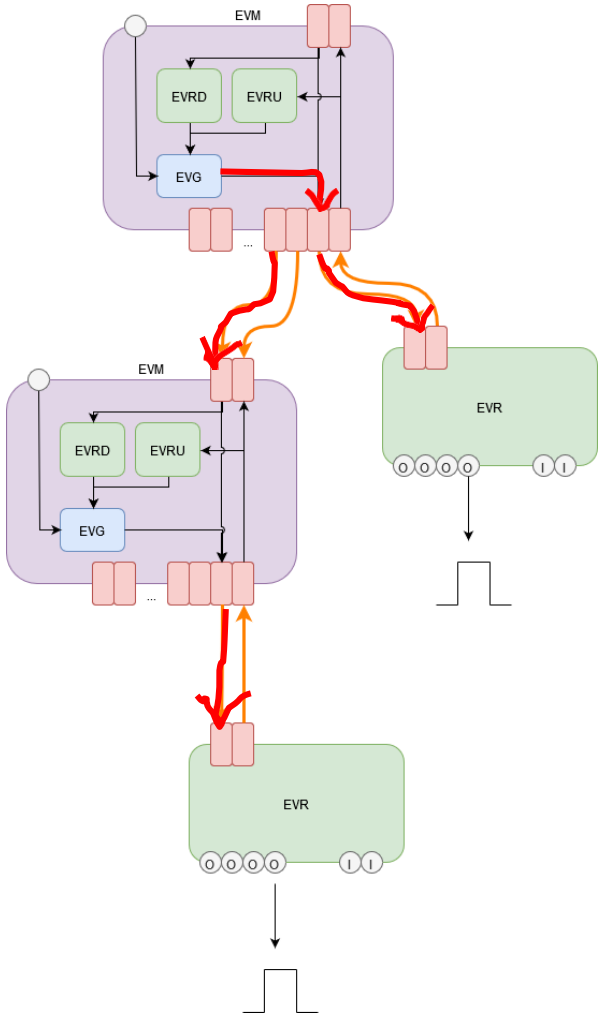
Imagine a test stand with the following installation :

- MTCA EVM 300 x2 : One master to rull them all, the other to be a simple fanout
- MTCA EVR 300U x2

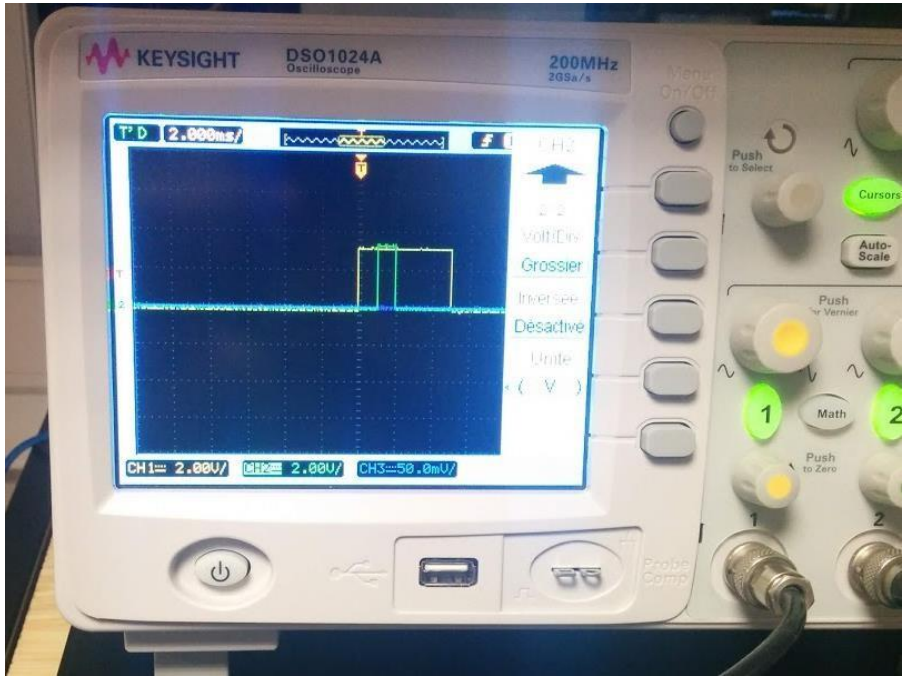




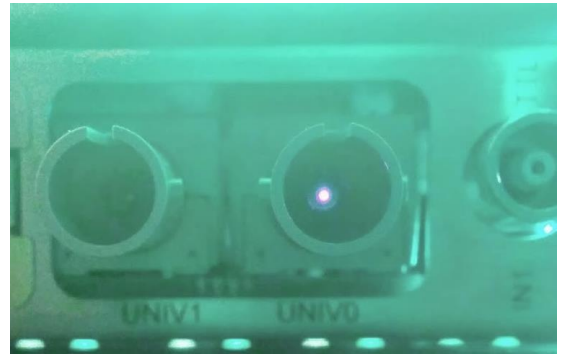
Standard case



- EVG produce Event #14 at 1Hz from internal clock.
- EVM Fanout transmit Event #14 to the following EVR
- EVRs receive Event #14 and produced the associated pulse to the defined front panel output

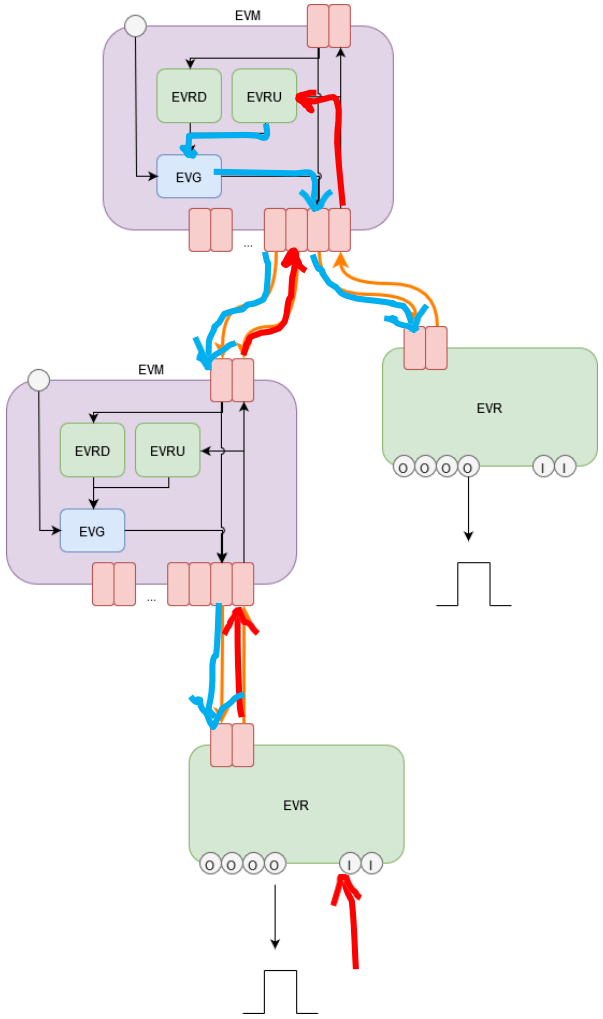


Front Panel TTL



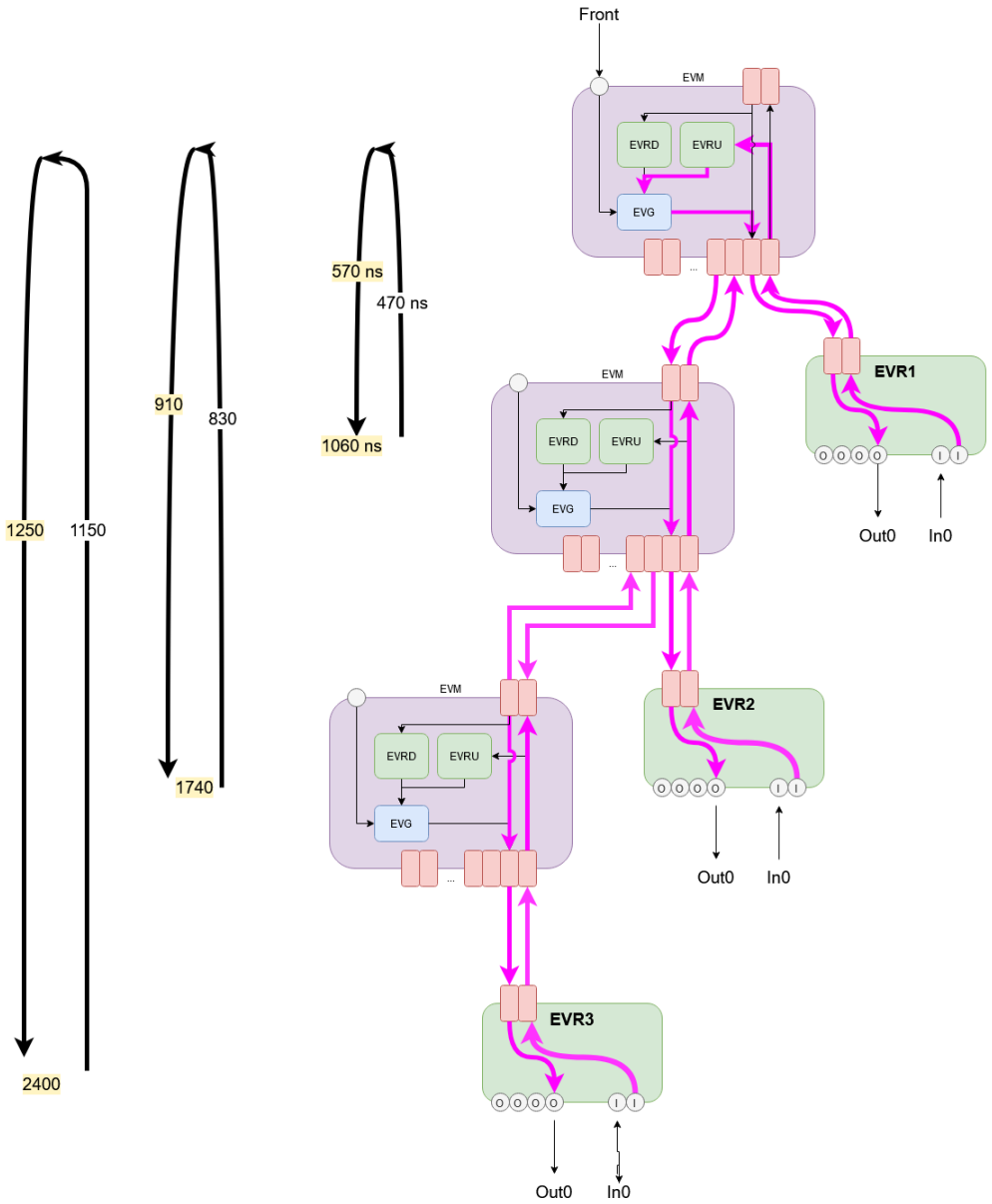
Front Panel Universe Optical Fiber (i.e Magnetron)

Upstream case



- A signal is received on input of an EVR
- The signal is configured to send and event upstream.
- The EVRU (for Upstream) received the event, and like any other EVR it is configured through its pulser to send a signal.
- The signal is received by the EVG that send an event downstream

Propagation delay



Specification : propagation time < 2,350µs

Test Bench

3 EVM, 3 EVR

Limitation of MRF Reference Frequency 145MHz so 88Mhz used. So the trame resolution is 11,3ns

The measures have been made by an oscilloscope. We measured the pulse at the input of the EVR and measured the pulse at the output. All the possible « path » that can take the event have been measured. (i.e from the input IN0 of the EVR1 to the Out0 of the EVR3)

Trig	Out0 EVR1	Out0 EVR2	Out0 EVR3
In0 EVR1	1060ns	1380ns	1720ns
In0 EVR2	1400ns	1740ns	2080ns
In0 EVR3	1720ns	2080ns	2400ns
Front EVM	570ns	910ns	1250ns

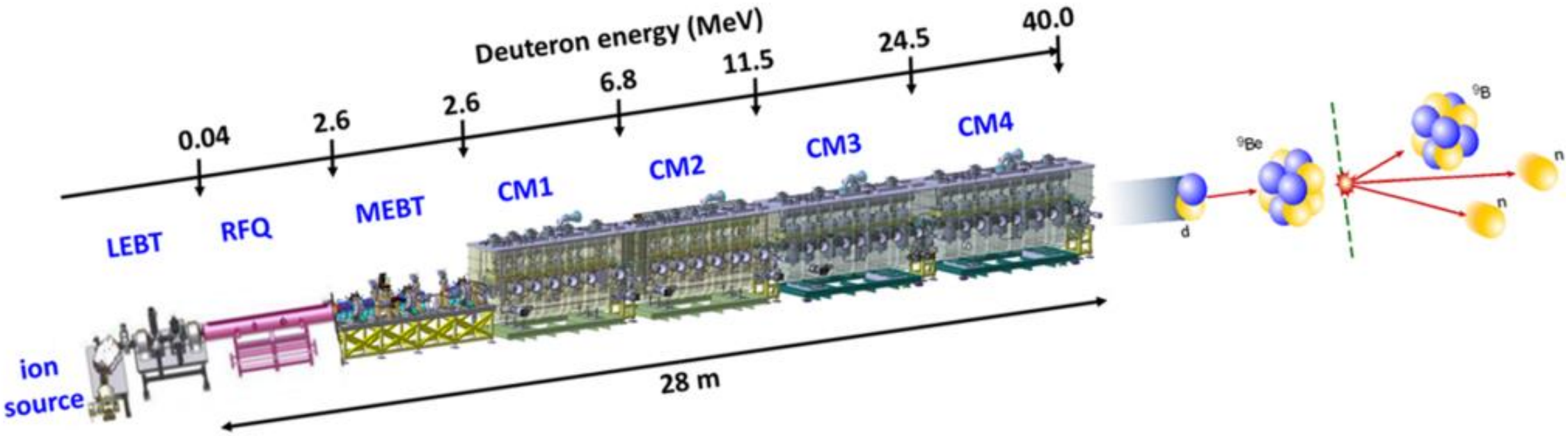
Propagation time measured at 88Mhz

Result not respecting the specification

It's not counting the time from the counter to the oscilloscope, so probably it's ok finally.

5. SARAF

SARAF Accelerator



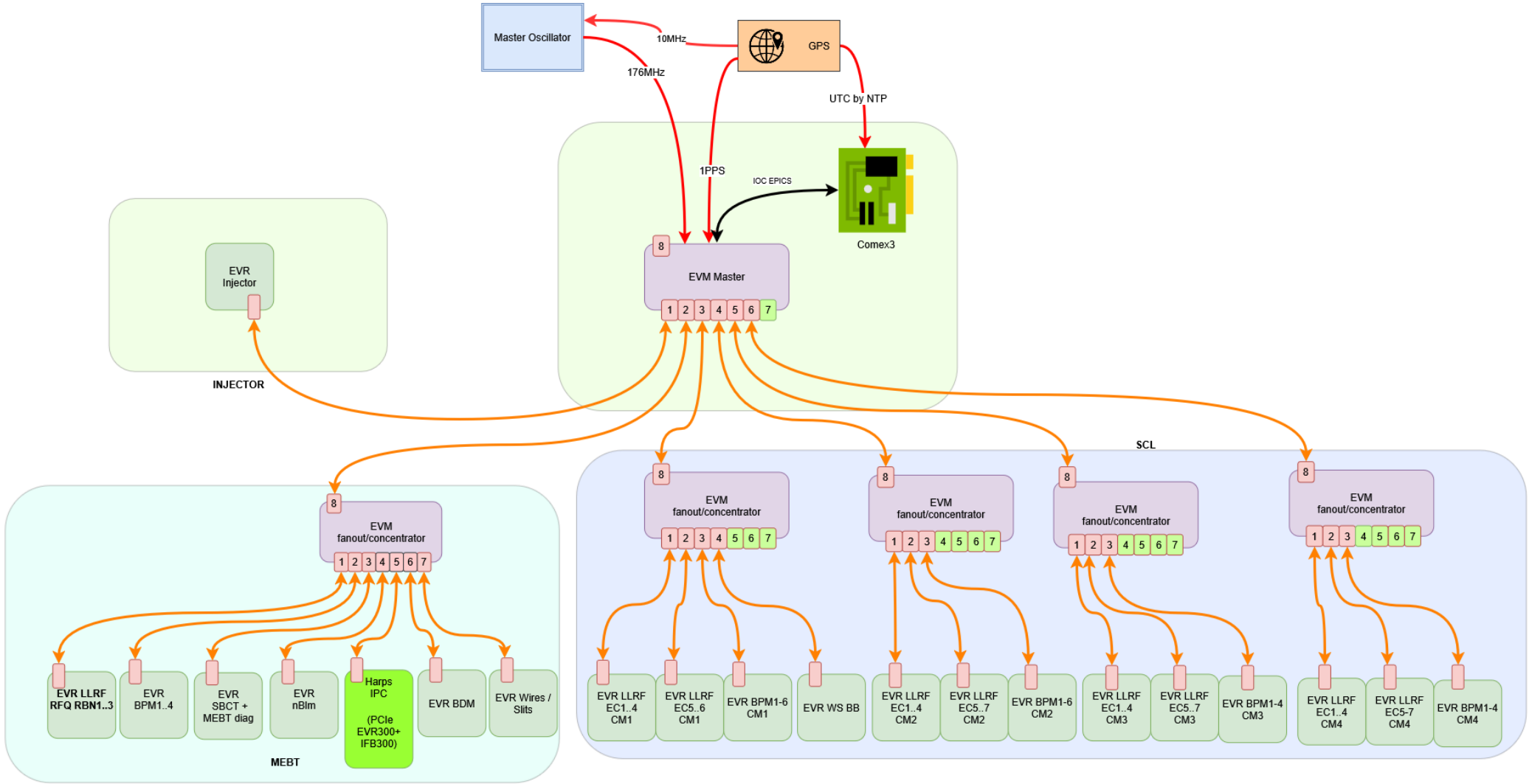
- Ref Freq : 176MHz
- CW (more or less)
- Period: 0,1Hz to 400Hz

- Plus d'info ?

-> Nicolas Pichoff

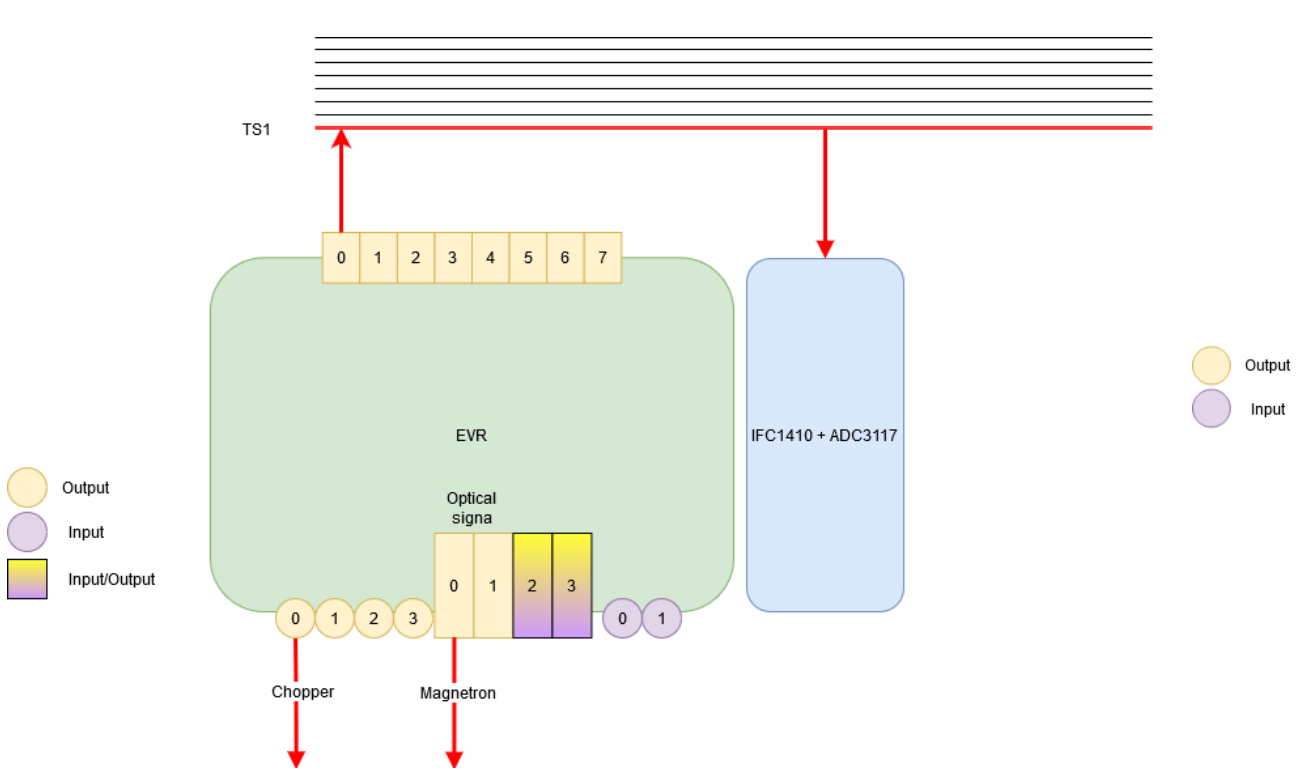
-> Antoine Chancé (dans la salle)

Topology

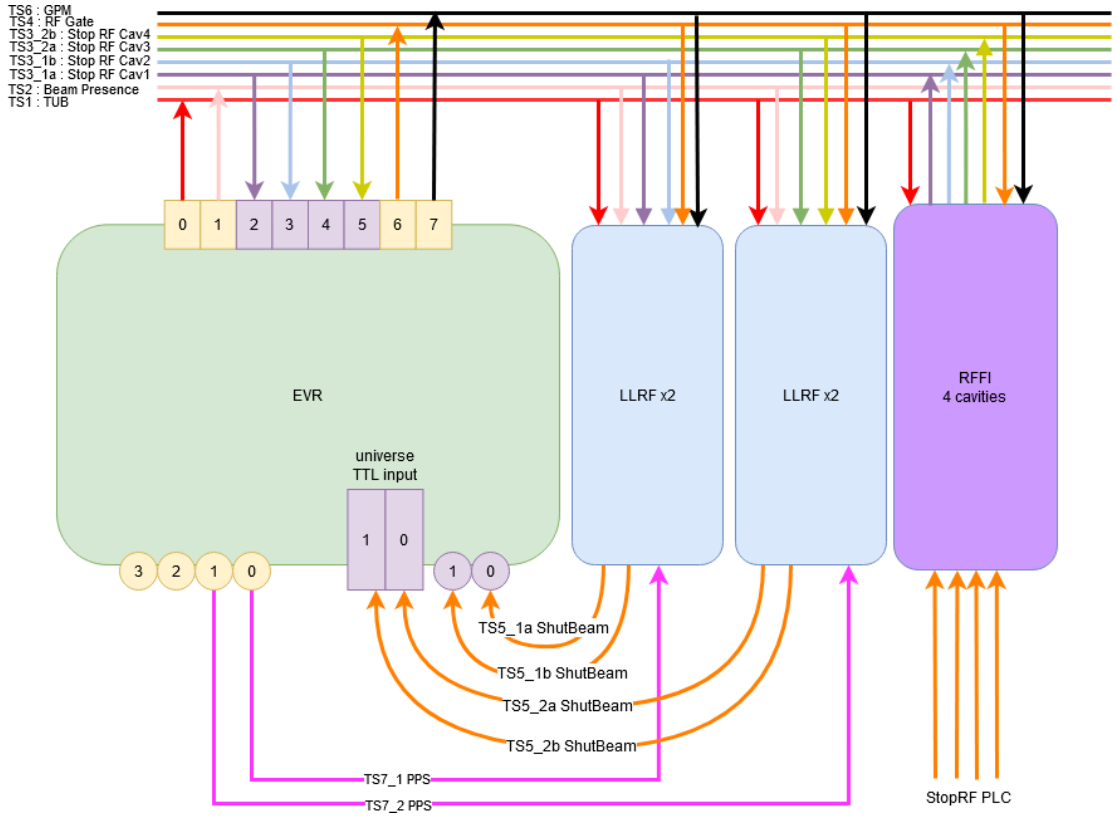

Master Oscillator
10MHz
176MHz
GPS
UTC by NTP
1PPS
IOC EPICS
Comex3
EVR Injector
INJECTOR
8
EVM Master
1 2 3 4 5 6 7
SCL
EVM fanout/concentrator
EVR LLRF RFQ RBN1..3
EVR BPM1..4
EVR SBCT + MEBT diag
EVR nBlm
Harps IPC
(PCIe EVR300+ IFB300)
EVR BDM
EVR Wires / Slits
MEBT
EVR LLRF EC1..4 CM1
EVR LLRF EC5..6 CM1
EVR BPM1-6 CM1
EVR WS BB
EVR LLRF EC1..4 CM2
EVR LLRF EC5..7 CM2
EVR BPM1-6 CM2
EVR LLRF EC1..4 CM3
EVR LLRF EC5..7 CM3
EVR BPM1-4 CM3
EVR LLRF EC1..4 CM4
EVR LLRF EC5-7 CM4
EVR BPM1-4 CM4

Some EVR examples

Example from SARAF for 2 LLRF cards (4 LLRF) and for the injector

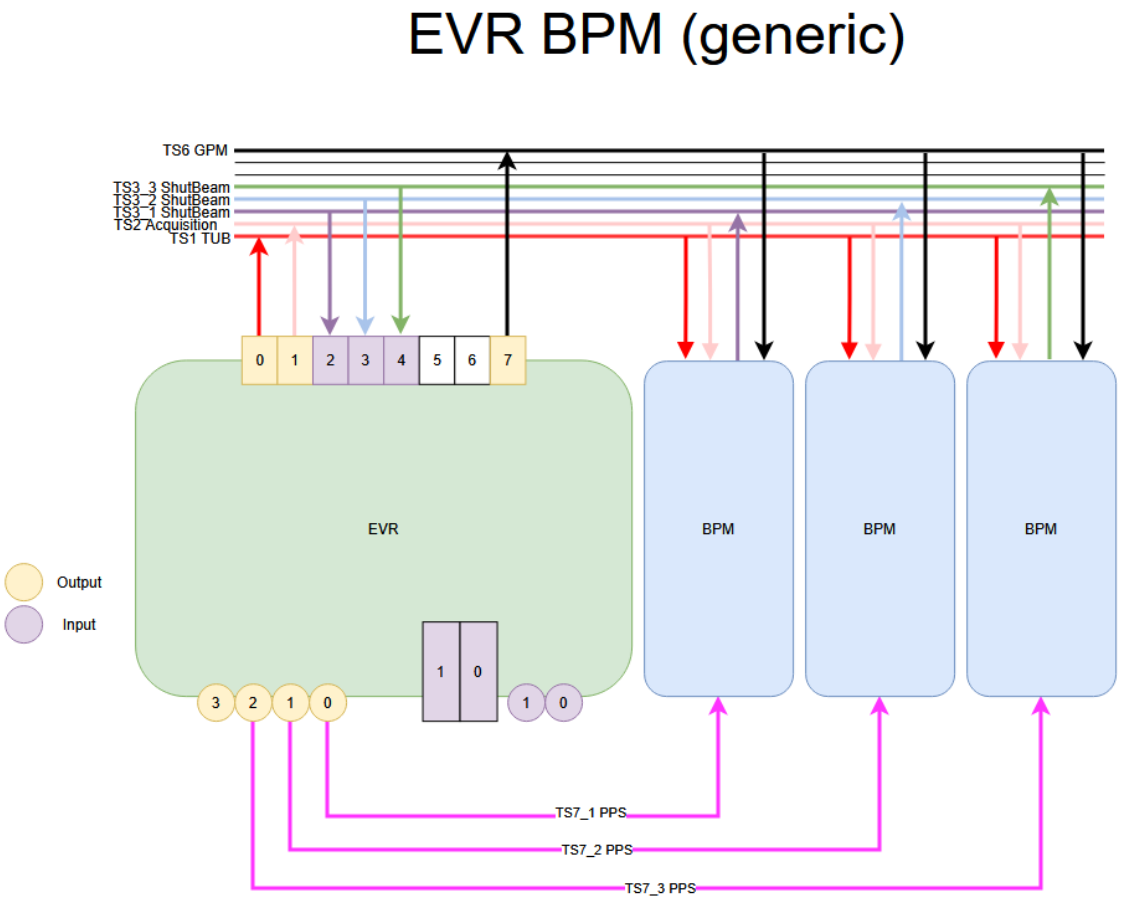


EVR Injector



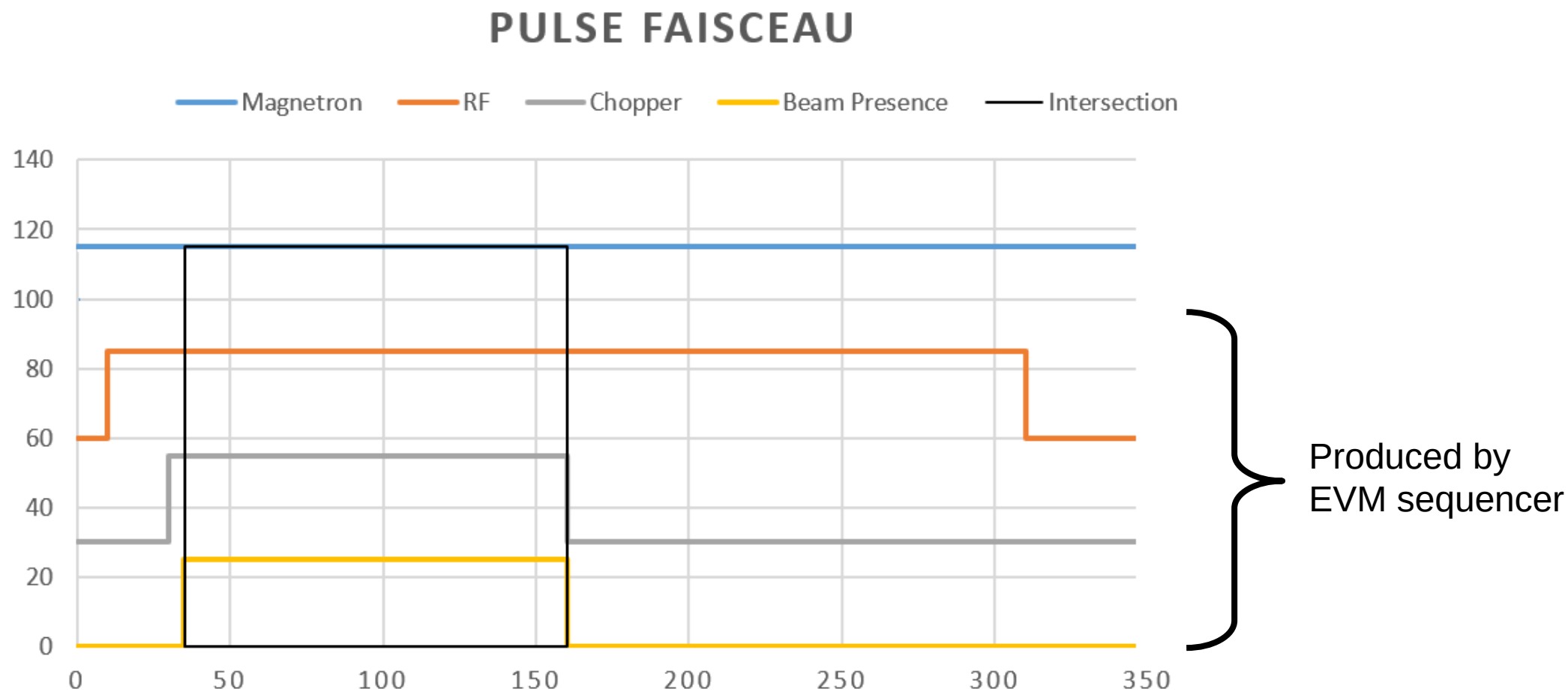
EVR LLRF

Some EVR examples

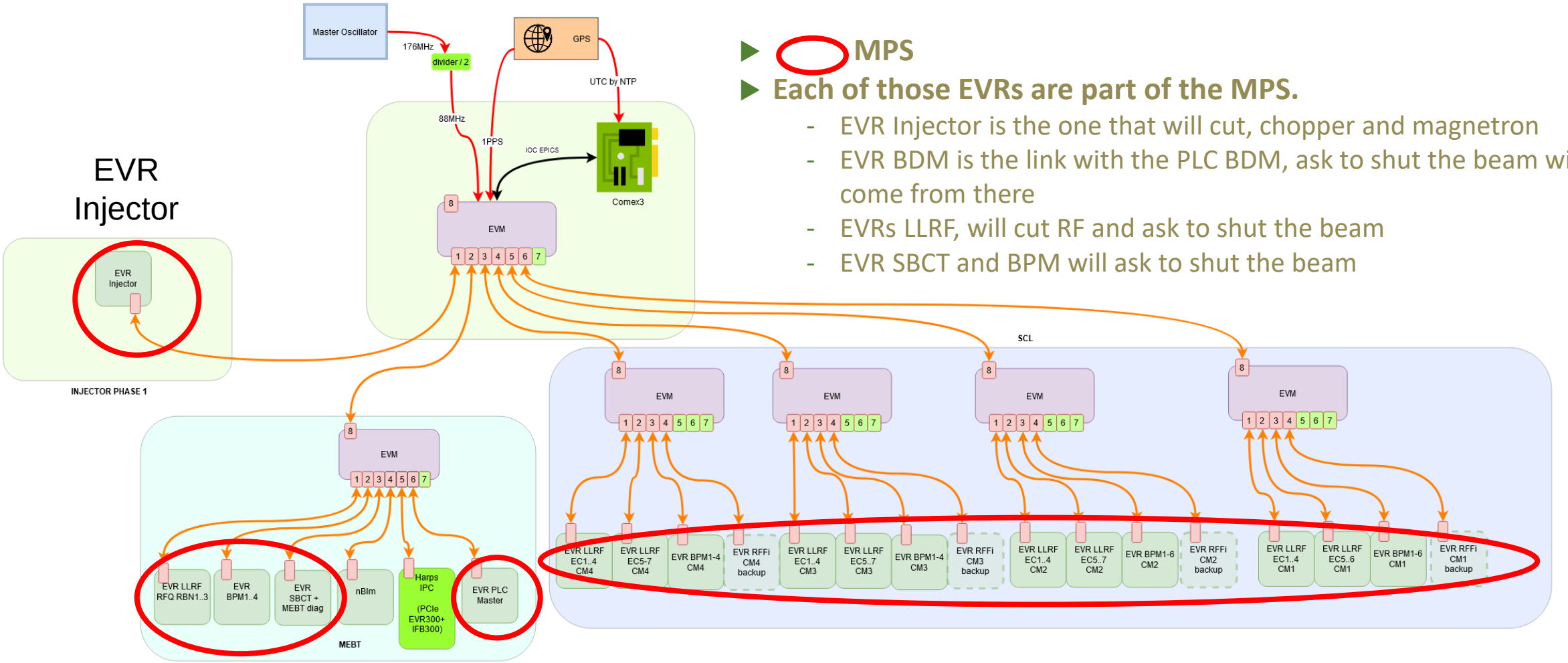


EVR BPM

Pulse Generation



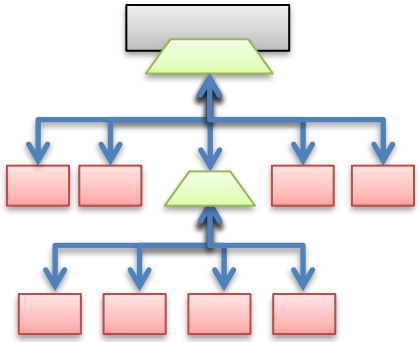
Machine Protection System

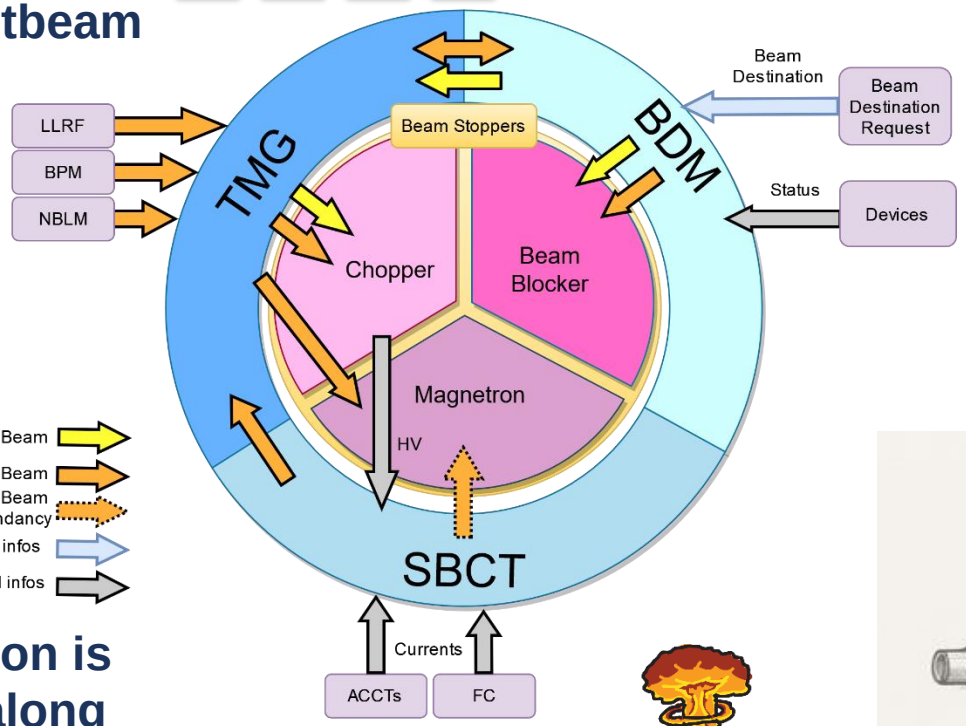


- MPS
- Each of those EVRs are part of the MPS.
  - EVR Injector is the one that will cut, chopper and magnetron
  - EVR BDM is the link with the PLC BDM, ask to shut the beam will come from there
  - EVRs LLRF, will cut RF and ask to shut the beam
  - EVR SBCT and BPM will ask to shut the beam

Machine Protection System

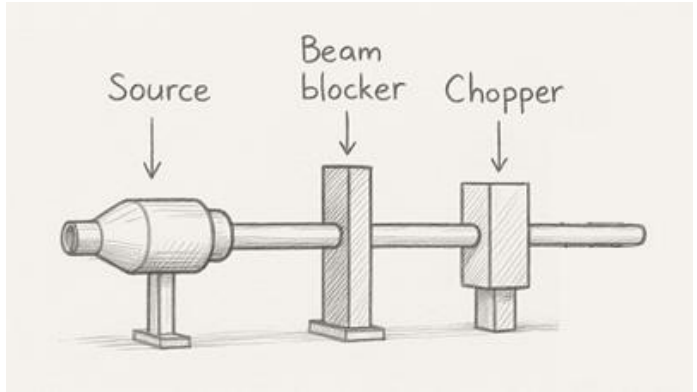
Timing (TMG) is the heart of the MPS creating or shutting the beam pulse through chopper and magnetron and being the messenger of the shutbeam event





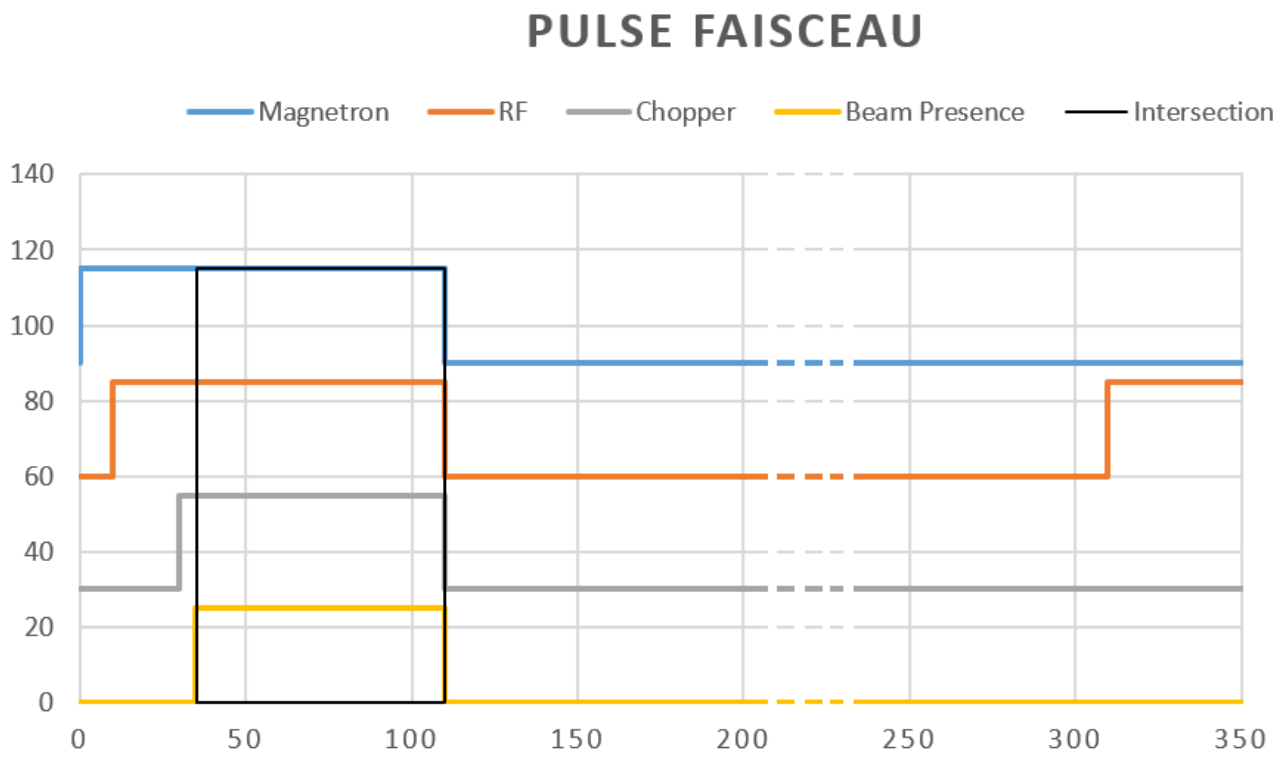
Section Beam Current Transmission is checking current of the beam all along the accelerator and compare them.

Beam destination master (BDM) controls that conditions to get the beam to a destination are checked. Linked to all PLC all along the accelerator through Profinet



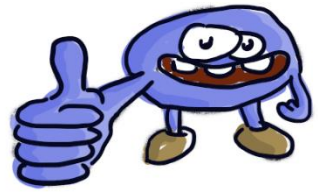
Machine Protection System

- During a shutbeam
  - All the pulses are immediatly interrupted
  - Sequence continue, but Beam Presence and Chopper pulses are masked

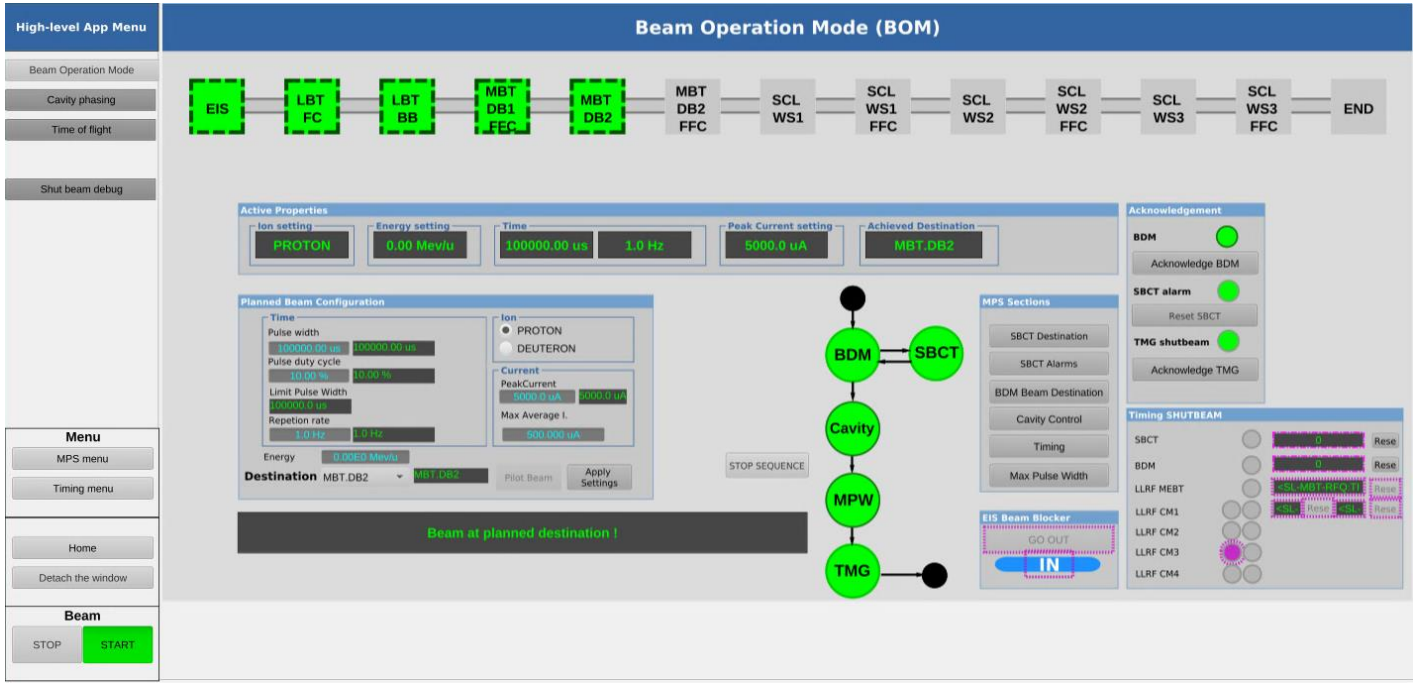


Conclusion

- MRF in MPS mode give great satisfaction for the commissioning of the MEBT of SARAF for now.
- Soon tested for the first cryomodule.



- Perspective
  - MRF will be used for Titan accelerator in Saclay (MPS not included this time)
  - MRF + MPS architecture proposed for pre-project for ICONE accelerator (introduced by Nicolas Pichoff yesterday).



Merci

CEA SACLAY

alexis.gaget@cea.fr

Why MRF choice at CEA

01 **EPICS DRIVER**
Developped by Michael Davidsaver SNS, Maintained by community (ESS team, PSI etc …)

02 **HARDWARE COMPATIBLE (MTCA, VME …)**
Pushed by ESS

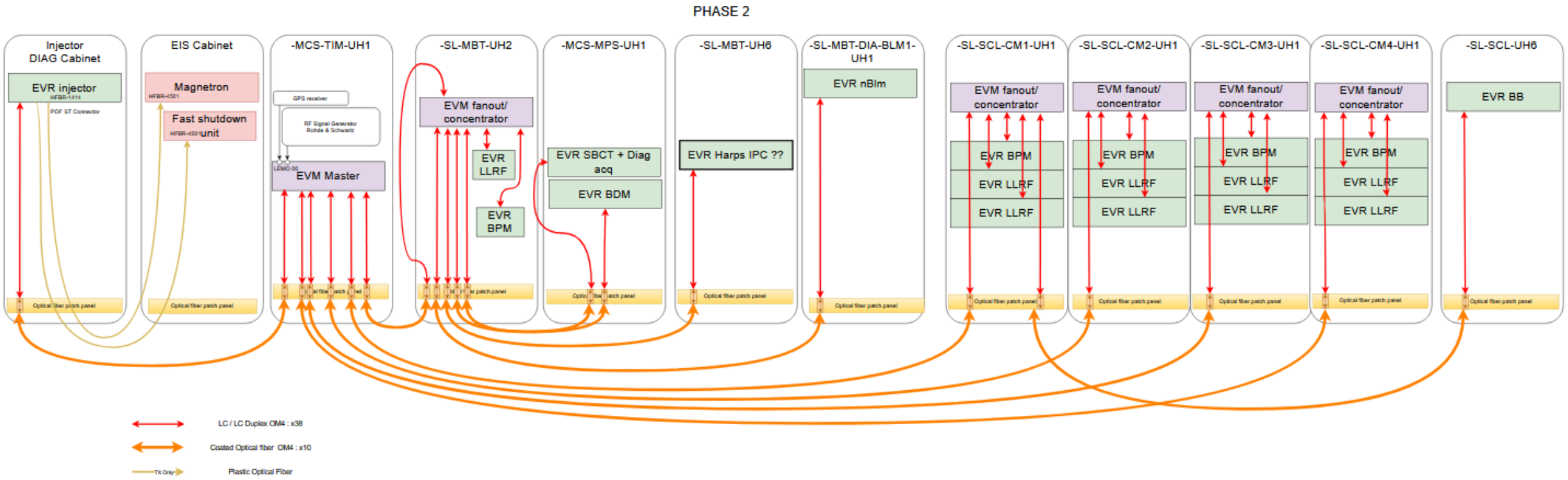
03 **USED IN A LOT OF ACCELERATOR**
ESS, SNS, PSI …

04 **OPEN SOURCE**
C library and VHDL

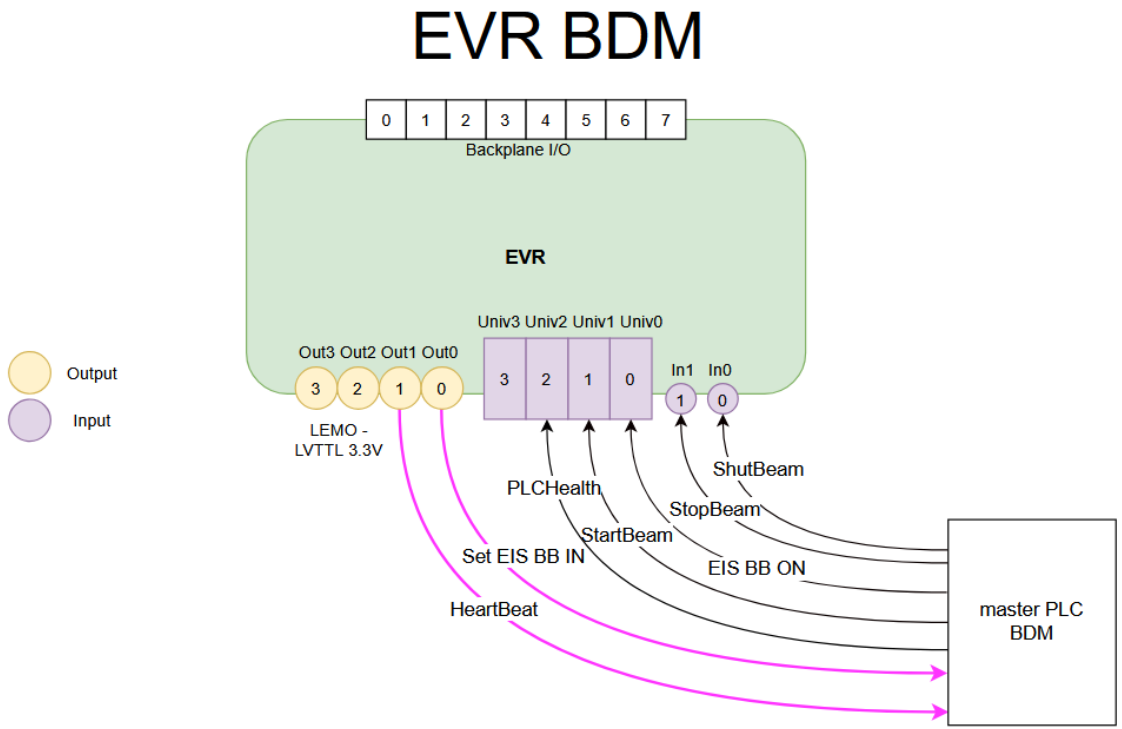
Why no White Rabbit ?

- At the time, not real industrial solution with EPICS driver.
- Precision similar

Annex


PHASE 2
Injector DIAG Cabinet
EVR injector
EIS Cabinet
Magnetron
Fast shutdown unit
-MCS-TIM-UH1
GPS receiver
RF Signal Generator Rohde & Schwarz
EVM Master
-SL-MBT-UH2
EVM fanout/ concentrator
EVR LLRF
EVR BPM
-MCS-MPS-UH1
EVR SBCT + Diag acq
EVR BDM
-SL-MBT-UH6
EVR Harps IPC ??
-SL-MBT-DIA-BLM1-UH1
EVR nBlm
-SL-SCL-CM1-UH1
EVM fanout/ concentrator
EVR BPM
EVR LLRF
EVR LLRF
-SL-SCL-CM2-UH1
EVM fanout/ concentrator
EVR BPM
EVR LLRF
EVR LLRF
-SL-SCL-CM3-UH1
EVM fanout/ concentrator
EVR BPM
EVR LLRF
EVR LLRF
-SL-SCL-CM4-UH1
EVM fanout/ concentrator
EVR BPM
EVR LLRF
EVR LLRF
-SL-SCL-UH6
EVR BB
LC / LC Duplex OM4 : x38
Coated Optical fiber OM4 : x10
Plastic Optical Fiber

Annex


EVR BDM
0 1 2 3 4 5 6 7
Backplane I/O
EVR
Univ3 Univ2 Univ1 Univ0
Out3 Out2 Out1 Out0
3 2 1 0
3 2 1 0
In1 In0
1 0
LEMO -
LVTTL 3.3V
Output
Input
PLCHealth
StartBeam
Set EIS BB IN
HeartBeat
StopBeam
EIS BB ON
ShutBeam
master PLC
BDM