EICROC « France » Meeting

18/09/2025

- Welcome to our colleagues from LPC Clermont Auvergne [indico…]
- Update on test bench development @ IJCLab: Firmware, setting, …
- Status on measurements with ^{90}Sr β source (Arzoo, EuNPC2025)
- Update on infrared laser test bench at IJClab
- Current issues: ADC pedestal, subtraction
- Update on EICROC0 testing at OMEGA and current developments
- On-going developments at LPC Clermont & CEA/Irfu/DEDIP
- Summary of EICROC0 testing meeting with BNL (08/09/25
- General information - Discussion

Update on firmware development at IJCLab (by Beng-Yun Ky]

❖ For measurements with the Beta source and and the infrared laser

- Acquisition of digital data (ADC, TDC) when at least 1 channel (among the 16) sees a signal with an amplitude passing the discriminator threshold [1 Hit Bit], before Summer 2025

- To take long Beta source run [~10 hours to largely increase the statistics]: « Time duration » and « multiple files setting a maximum event number for each file to ease the analysis [End of July 2025]

❖ For measurements with the infrared laser

- Acquisition driven by the laser TrigOut signal [TTL 2V5]: requires to weld a cable on the PCB [Spare 1 & grounded], mid-August 2025 – ceic_en_in_exttrig(1)

- « Resetb » before each event: Begining of Sept. 2025 – *ceic_resetb_before_acq*(1)

- Synchronization between the laser TrigOut signal and the 40 MHz clock? To be discussed

Caveat: with frimware/sofware update, we cannot use anymore Adrien's code to align the S-Curves – need previous versions

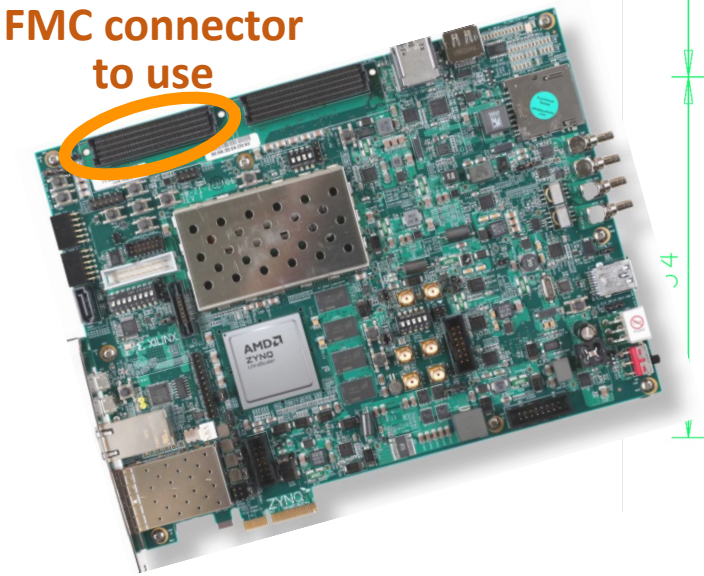
Update on firmware development concerning updated FPGA board

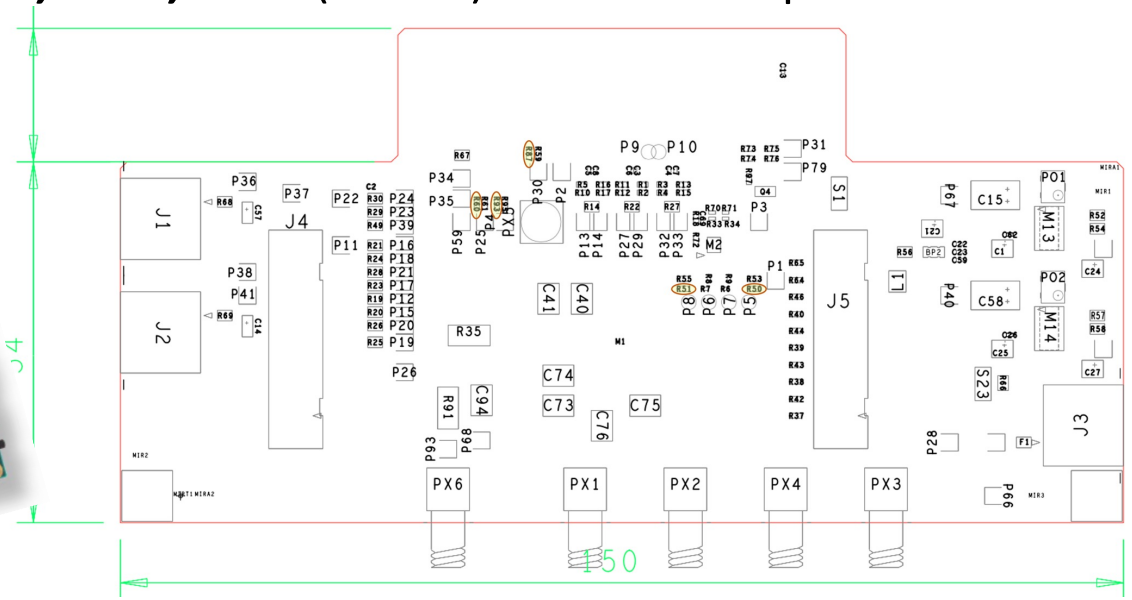
AMD Zynq™ UltraScale+™ MPSoC ZCU106

- Firmware porting **DONE**
  - For **I2C full Ios compatibility** reasons (**ZCU106: 1.8V** // ZC706: 2.5V): physical replacement of some « pull-up » resistor values on the PCB is mandatory

    R50, R51, R60, R87, R93 (2.8 kΩ) each to be replaced with **6.04 kΩ** (size 603)

FMC connector to use





@ IJCLab: modified PCBs
- **1 (1st version) w/ EICROC0**
- **2 bare_partially cabled (without EICROC0)**

- **ZCU106 Firmware/Software**: https://box.in2p3.fr/s/d92NYXC6BJ6koe8
- **ZCU106 Ubuntu Rootfs for armhf** : https://box.in2p3.fr/s/mbKpKBLbBqGLJsG
- **Guidelines to create SD card (from Arzoo):** https://box.in2p3.fr/s/f3oJw5NcWdYmHJb

Status of EICROC0 test boards

❖ With an AC-LGAD sensor:

- ➢ 1 Flip Chip: provided by BNL
- ➢ 1 HPK wire-bonded by Koji Nakamura @ KEK
- ➢ 1 BNL sensor wire-bonded by Koji Nakamura @ KEK
- ➢ 1 BNL sensor wire-bonded @ BNL: no more functionnal…

Concern: Wire-Bonding as we do have EICROC0 ASIC & BNL sensors

❖ Bare PCBs partially cabled:ithout an EICROC0 ASIC nor an AC-LGAD sensor

- ➢ 2
- ➢ 2 modified to run with ZCU106 FPGA board
- ➢ 3 shipped to BNL [June 2025] for their needs
- ➢ 2 shipped to BN [June 2025] to be shipped back to IJCLab with:
  - 1) Flip Chip (HPK etched]
  - 2) 1 HPK OR 1 BNL wire-bonded (? To be decided among us)

❖ Status of next PCB iteration with design optimized to IR laser testbench + trabslator for IO's compatibility with ZC706 & ZCU106, number of outputs to be increased – To be designed in close collaboration with Beng-Yun Ky

Slow parameter settings: Bias_PA

- **Investigating issues, discovered that « tuning » Bias_PA allowed us to see 4 probe PA simultanously on scope with 160 MHz clock ON, whatever sensor configuration we have**
  - Set the 7 bits to 45 (overall) checking that 600 < K_analog_probe [mV] < 750 [610]
    Didn’t know at that time that Bias_PA <6:0> = vbc_PA <6:2> « + » vbi_PA «<1:0>…
    Need to further investigate

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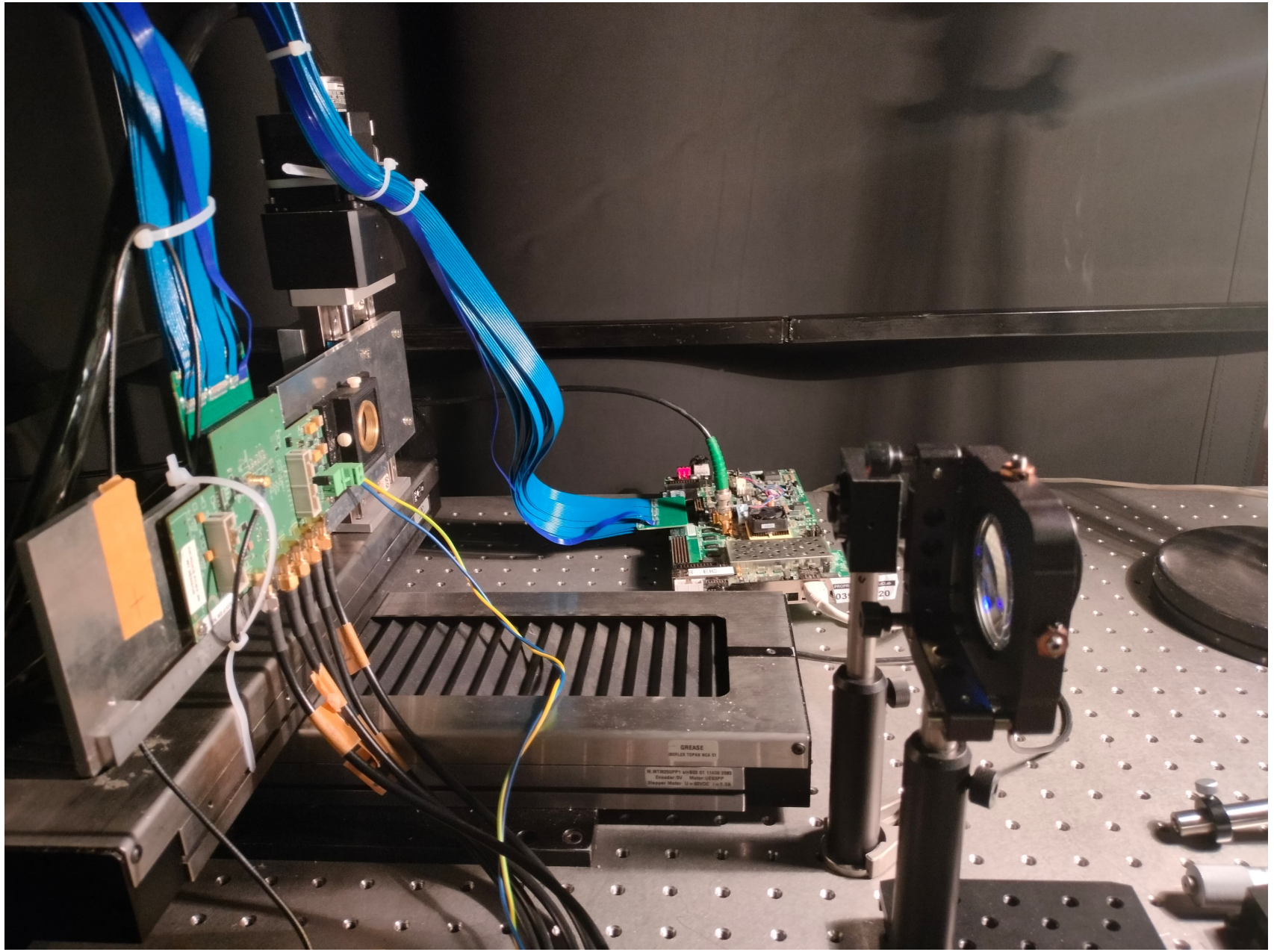
EICROC0 IR Laser Testbench @ IJCLab

Team: IJClab:

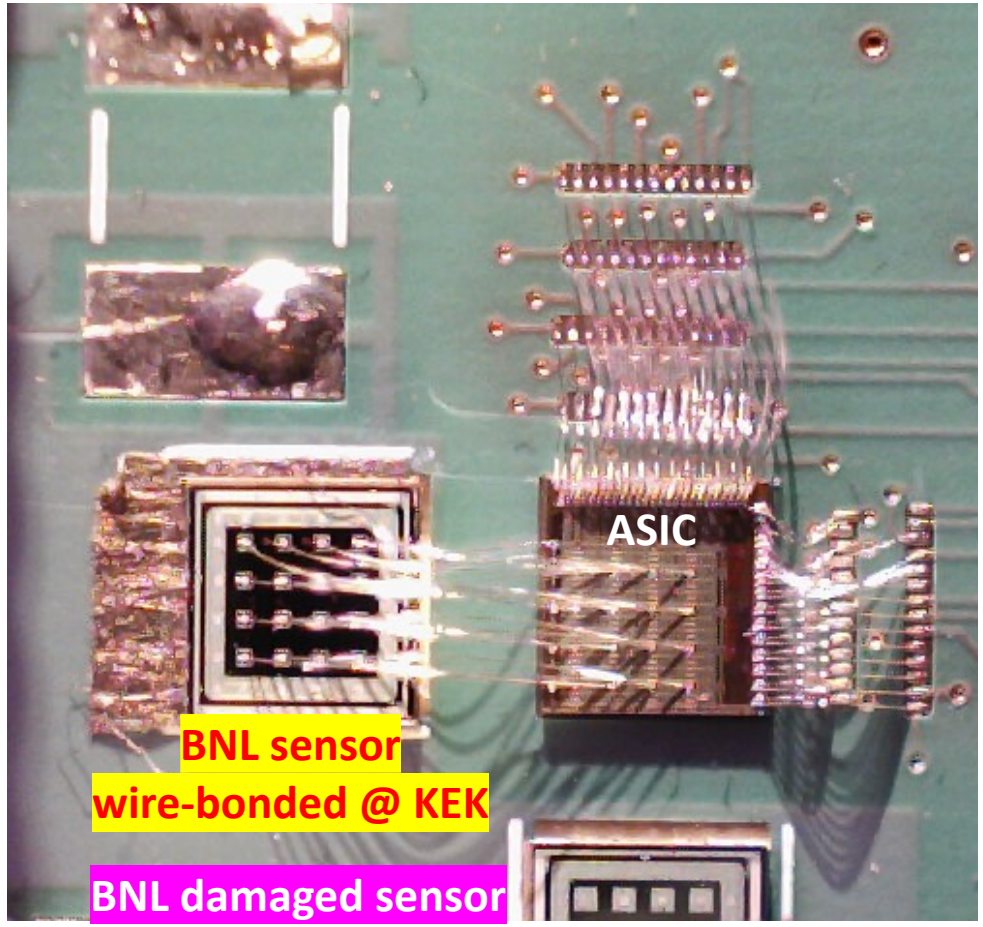
- A.-S. Torrento (coordinator)
- O. Brand-Foissac
- V. Chaumat
- T. Cornet

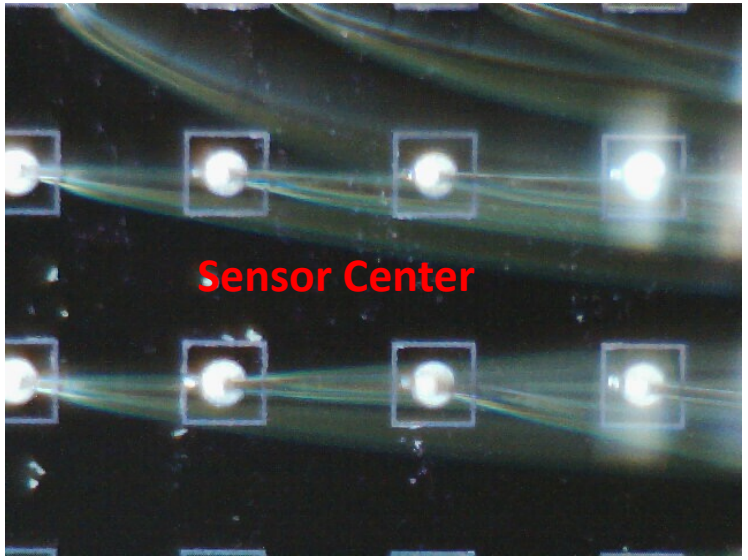


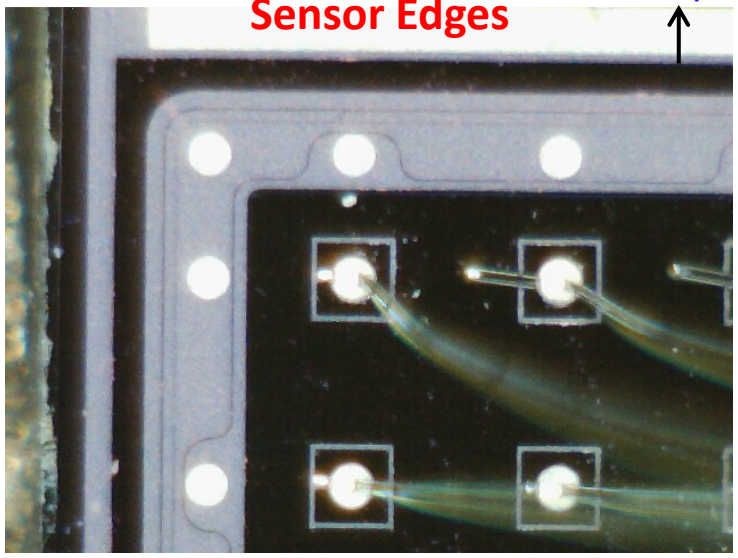
AC-LGAD and ASIC images with microscope

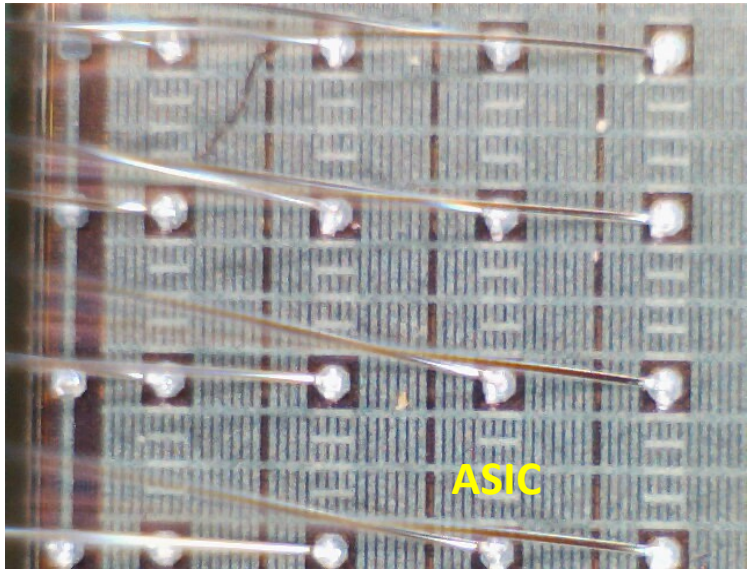
BNL WB sensor WB @ KEK

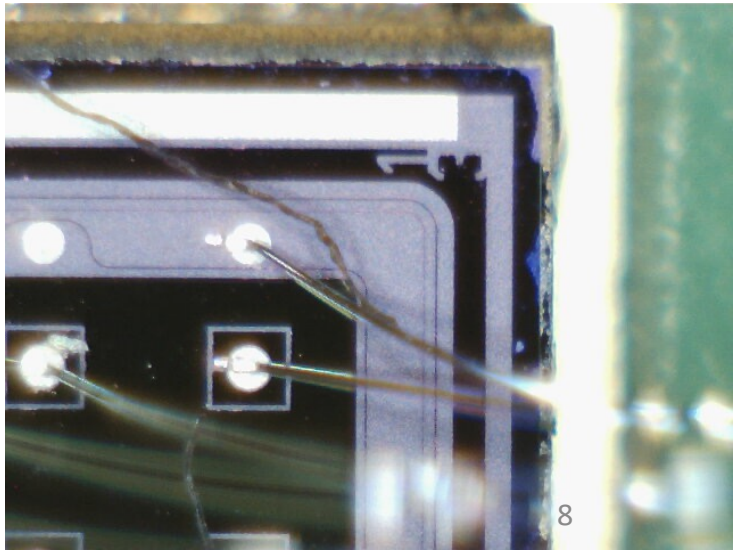
X = 11.99, Y = 0.98, Z = 241 mm)

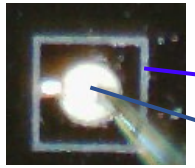












Terminology used:

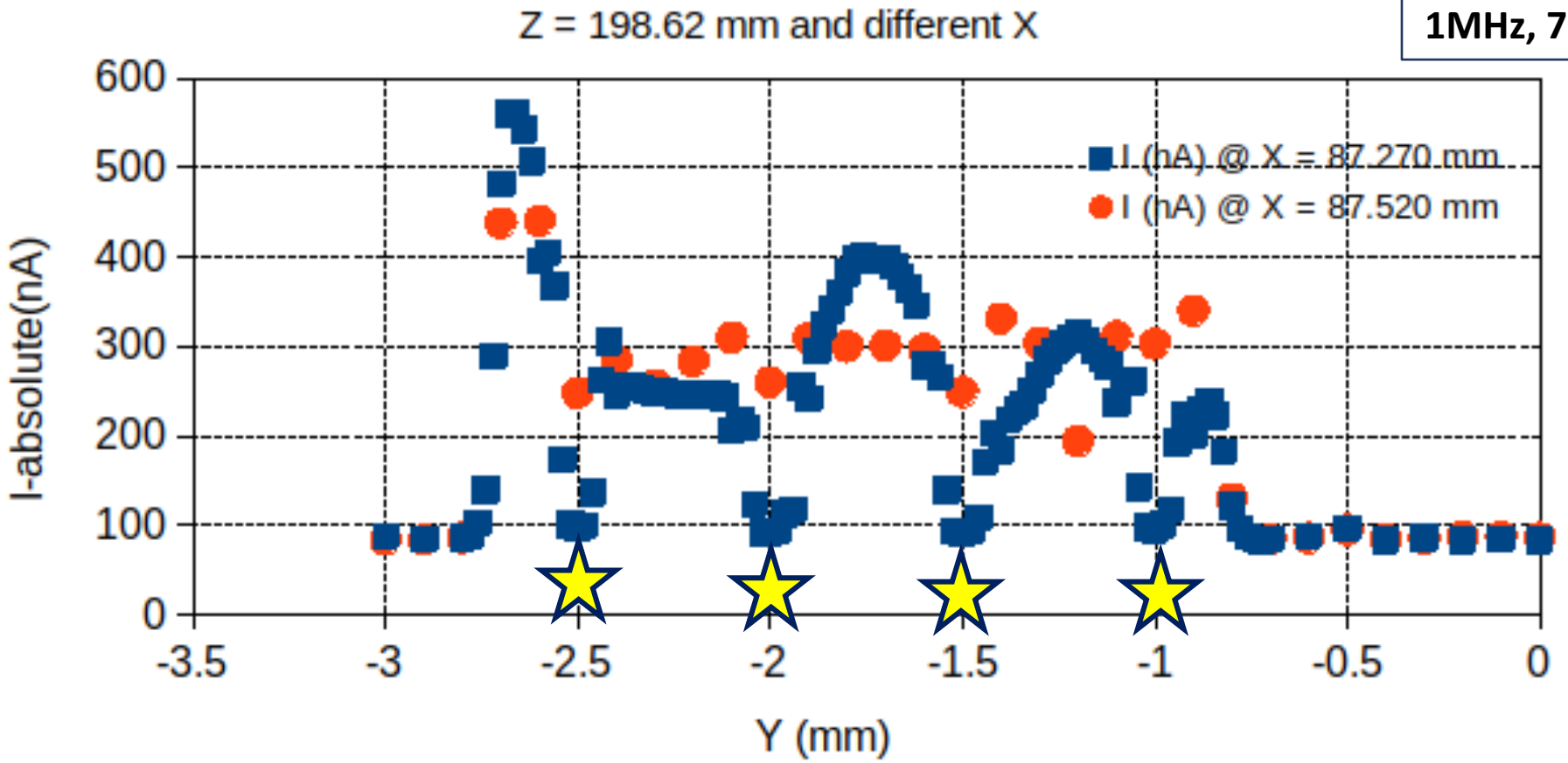
Aluminium Patch

Pickup Electrode

BNL AC-LGAD wire-bonded at KEK
Biased at – 190 V

Y scan with LASER

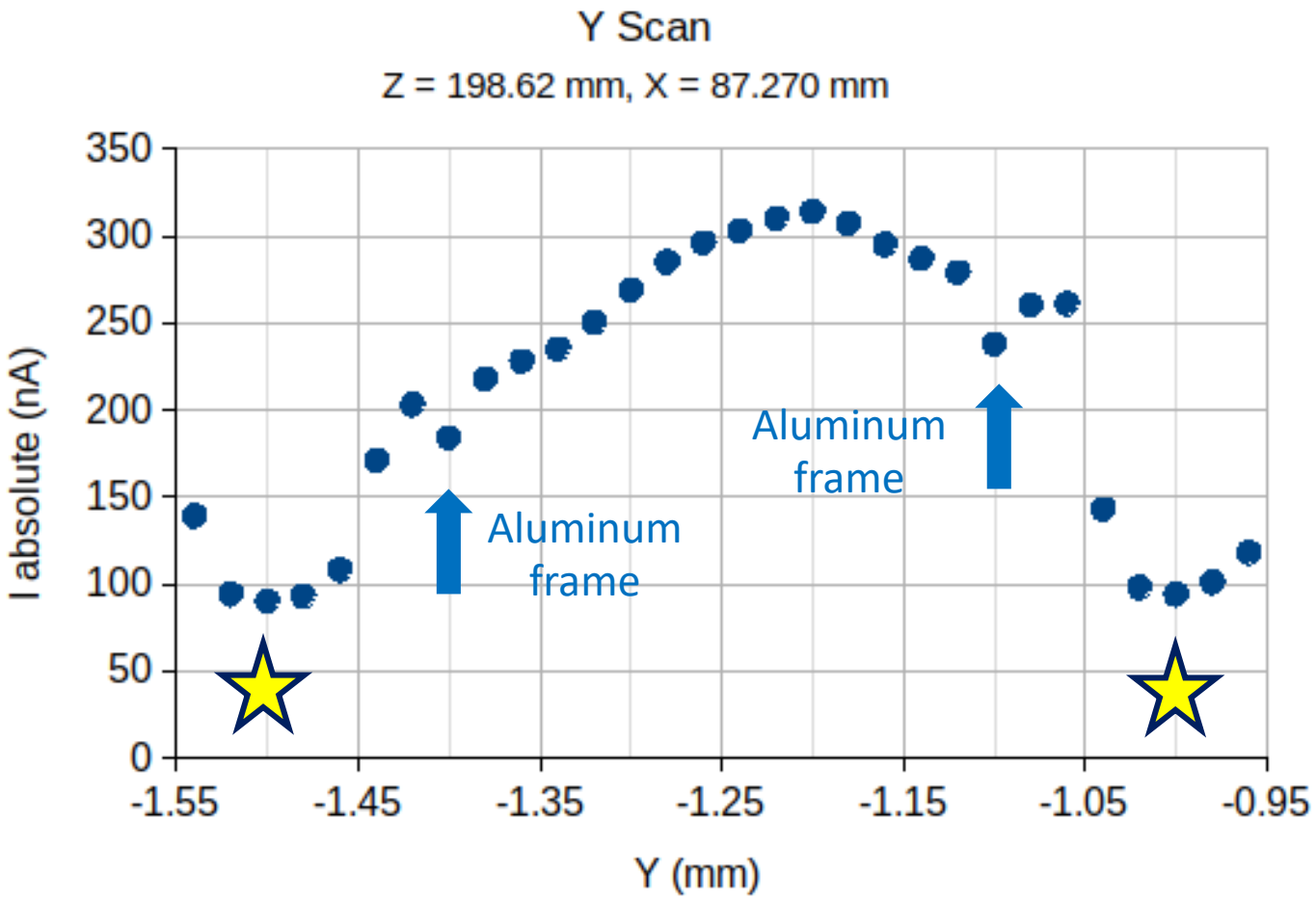
Laser Settings:
1MHz, 78.50 (attenuation)



electrode

- The aim was to observe the difference between the current, once when we are scanning the column with electrodes (X = 87.270 mm / blue data range) and moving it by 250 um to be between the two columns and/or inter-pixel (X = 87.520 mm / orange data range).
- Full analysis will be performed with digital data -> Next Steps.

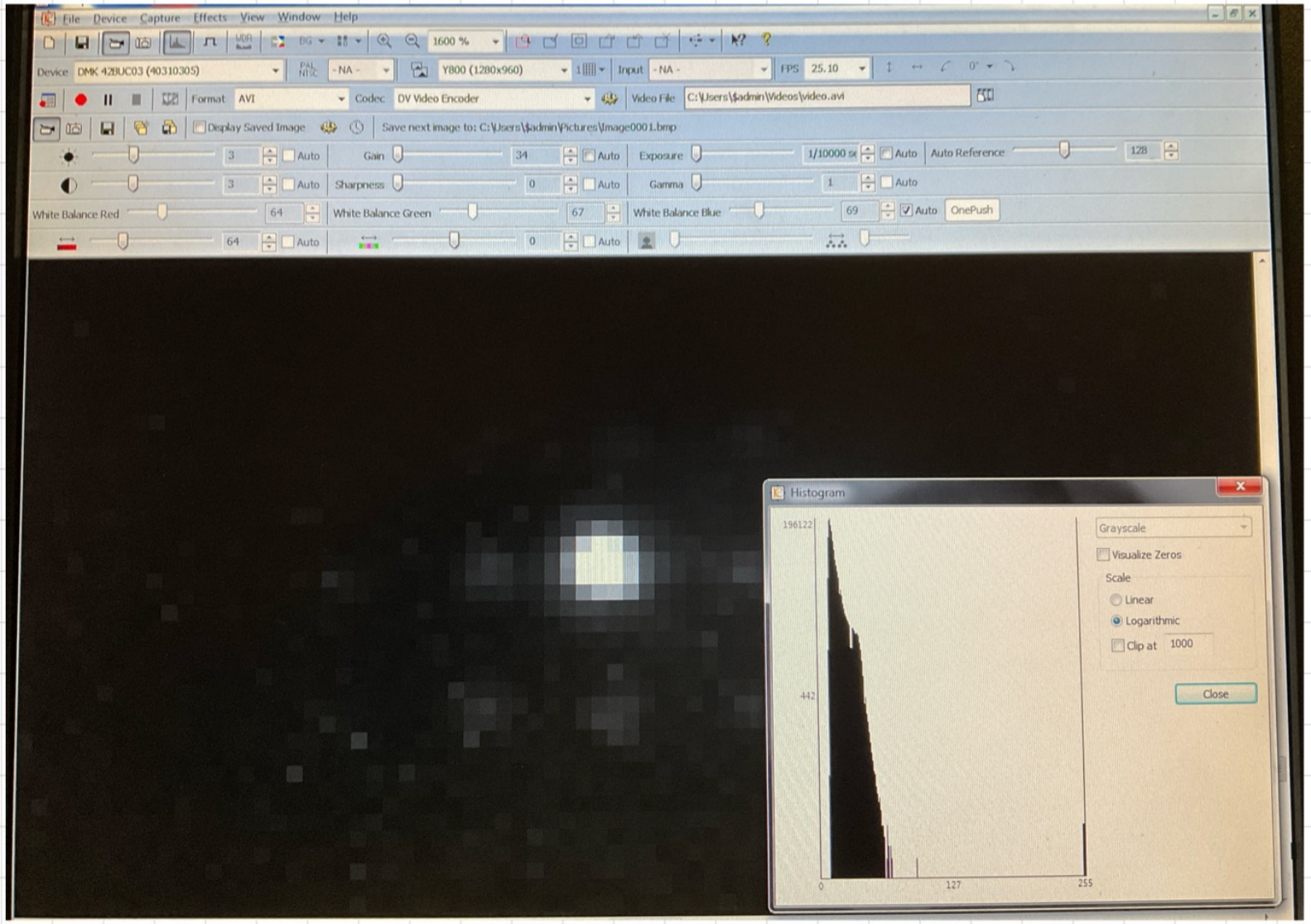
Image Zoomed: Effect of Al patch (outside the pickup electrode) on current



- The distance between the 2 electrodes is observed ~ 500 um.
- The current reduces while passing through Aluminum frame because of reflections.
- As, we can clearly observe the effect of Al frame (10 um thick) on the current, implies laser spot in Y is less than **10 um width**.

✓ **Ready to acquire data with oscilloscope**

CMOS images with LASER centered

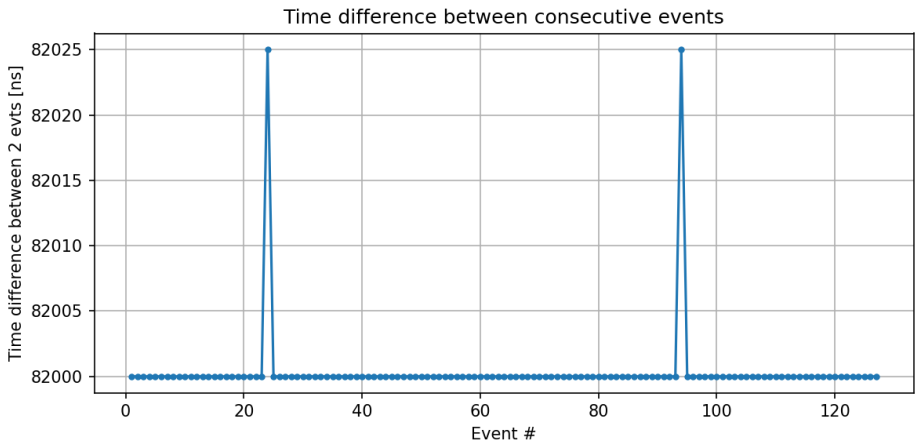


Laser Settings:
1MHz, 86 % (attenuation)

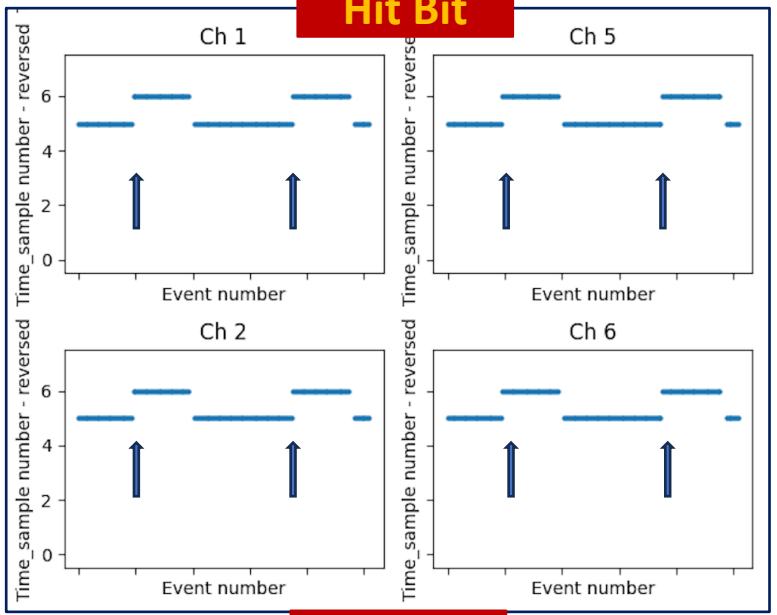
✓ **Diffraction effect now removed**

ADC pedestal subtraction

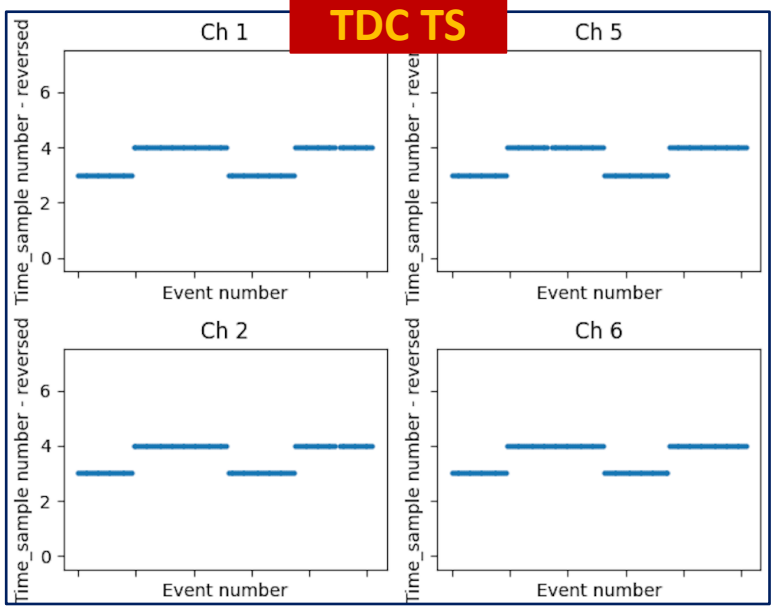
❖ Observation of shifts of Time Sample for TDC data & Hit Bit which coindide with Time Stamp shift



Hit Bit



TDC TS



ADC pedestal subtraction

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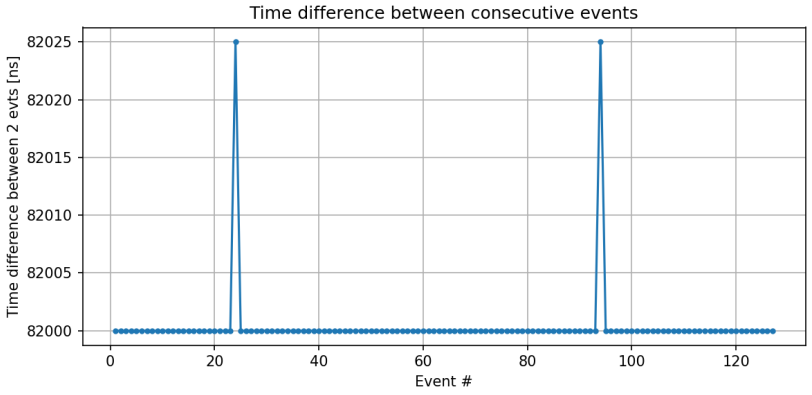
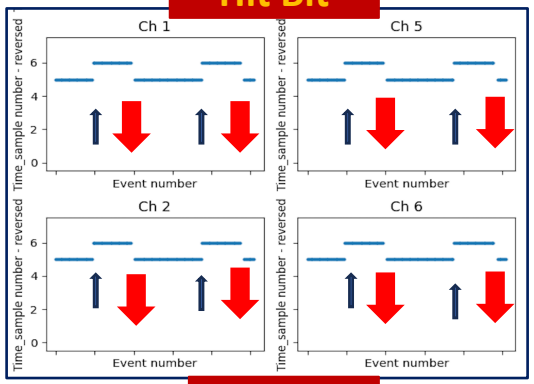
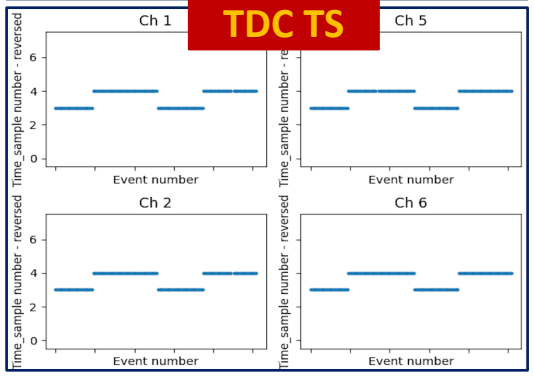
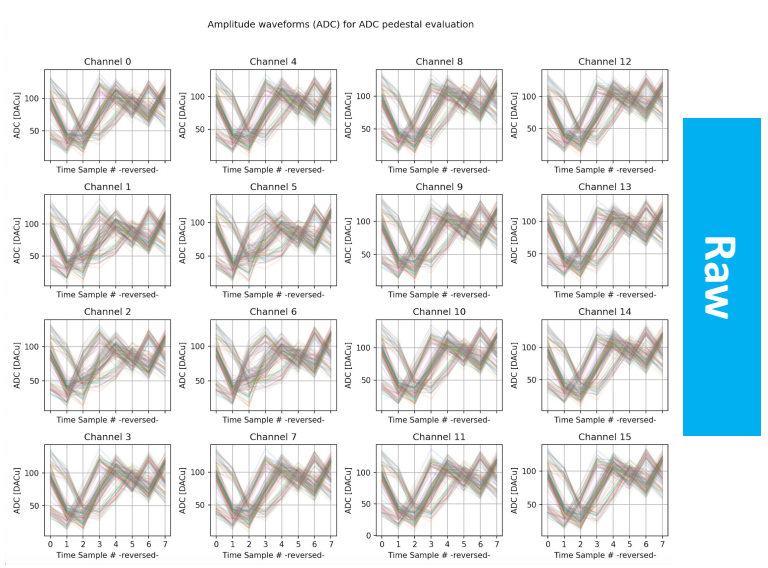
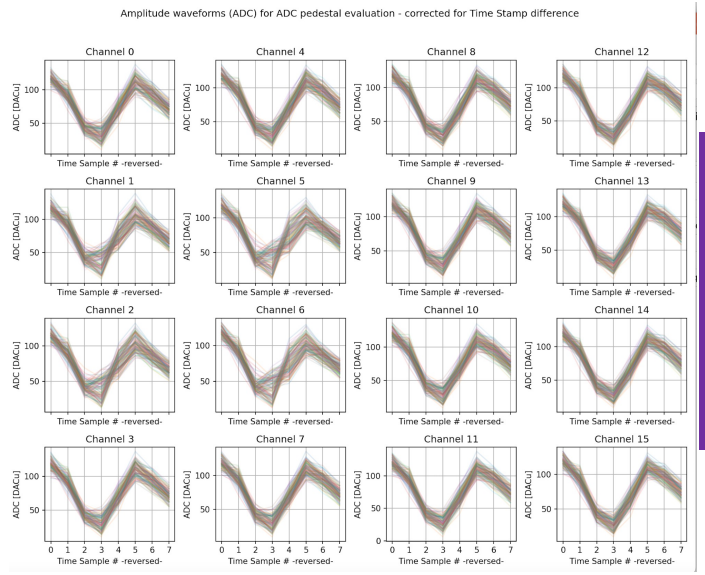
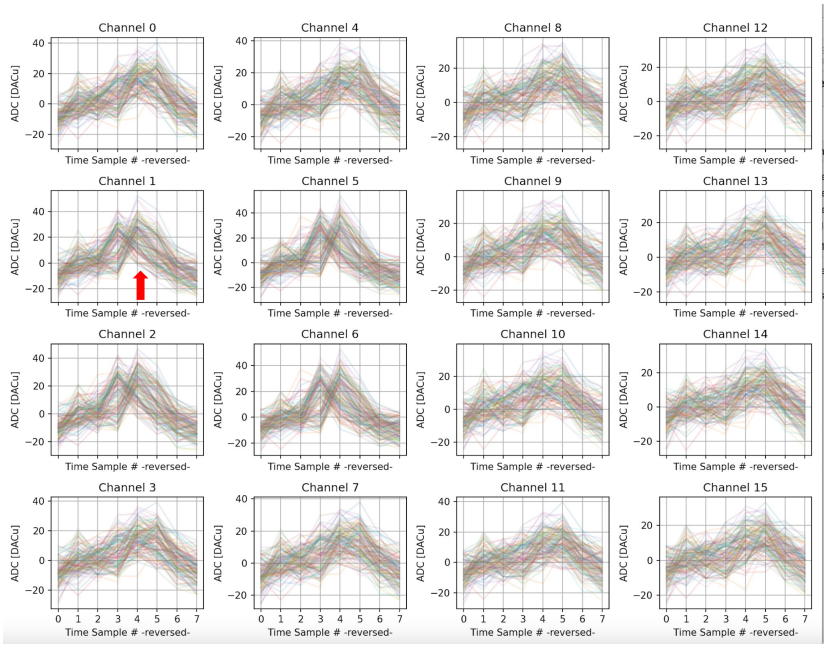












TDC jitter from Beta source & preliminary laser meaurements

AGENDA

- EuNPC2025: Sept. 21-26, 2025, Caen – Arzoo's talk (20')
- EAP EIC (Marcella Grasso) : Sept. 26th, 2025, IJCLab – 9:30 am
  IJCLab, LLR, LPC Clermont, OMEGA are concerned – EICROC contribution to the next engineering run
- Mathieu Benoît's visit at OMEGA & IJCLab: Sept. 29-30, 2025 => To be organized among us
- CPAD2025: Oct. 06-10, 2025, Philadelphia – Dominique's talk (20') [abstract accepted late August]
- Dominique at BNL: Oct. 11-17, 2025 – Registration being processed
- Bi-National INFN-IN2P3 workshop: November 21-25, LPNHE, Paris Arzoo submitted an abstract
- « New » EIC « France » meeting: December 01-03, 2025, IJLab (organized by GDR QCD)
- ePIC Collaboration meeting: mid-January, 2026, Triumph, Vancouver [To be announce]
- TIPP2026: Feb. 02-06, 2026, Mumbaï – abstract submitted late August, no update yet

Information - Discussion

- **Currently, main concern/effort: ADC pedestal subtraction**

- **Need closer collaboration OMEGA – IJCLab – CEA/Irfu/DEDIP to foster EICROC0 testing & to drive next EICROC iterations including LPC Clermont team**

- **Seeking for a postdoctoral researcher working at IJCLab: characterization of pixelated AC-LGAD with EICROC & simulation activities (i.e. exclusive process including far-forward detectors)**
  (2,5 years, starting Feb. 2026)
  Arzoo's contract is extended until January 9th, 2026.

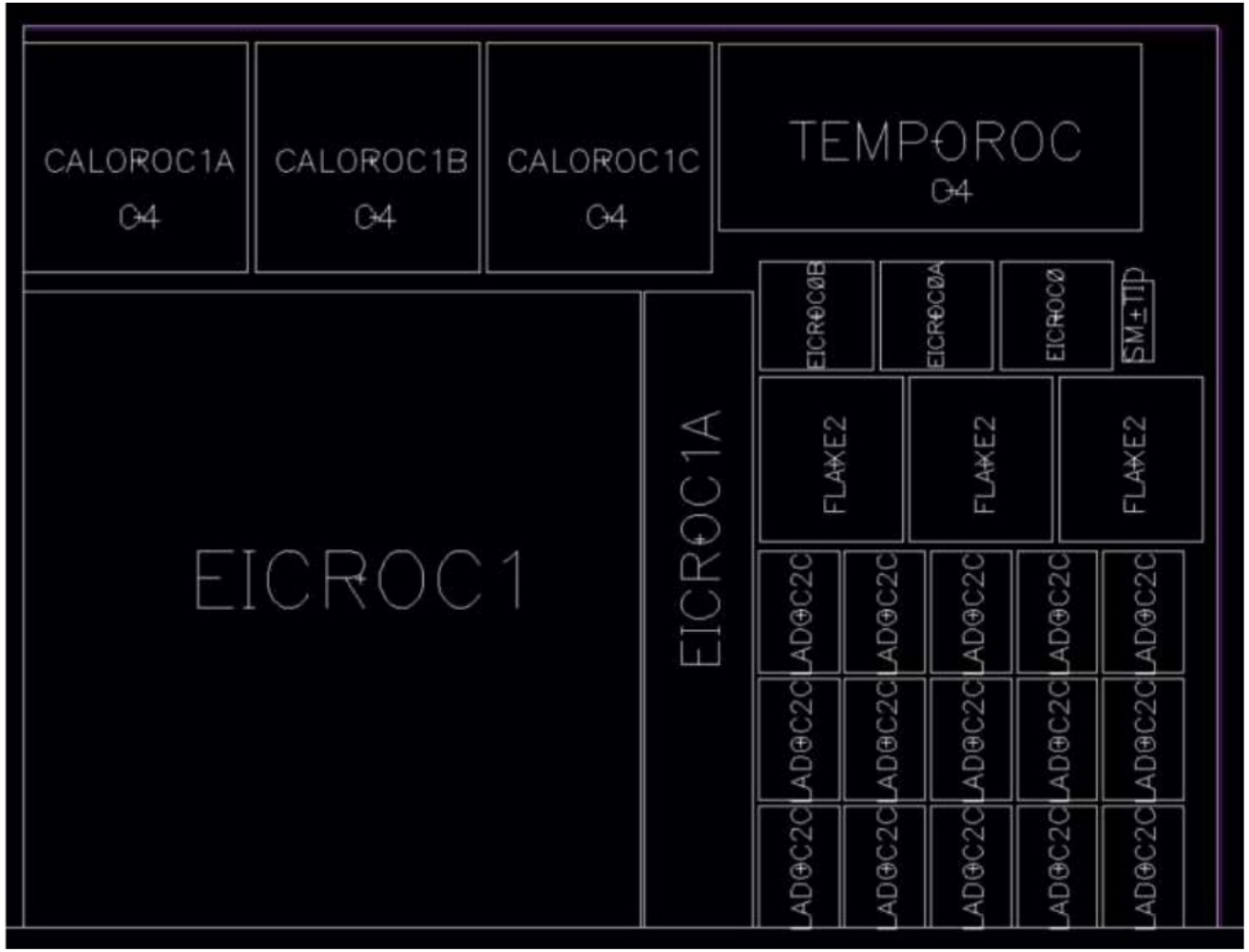
Back-up

EICROC reticle 2025

- TSMC now requires to fully populate the reticle
  - Cost ~300 k€

- For EIC we have
  - 1 EICROC1 32x32
  - 1 EICROC1A 4x32
  - 3 EICROC0/A/B 4x4
  - 3 CALOROC1A/B/C
  - ~70% of reticle area
  - EICROC1 is 40% of reticle area
  - gds files loaded end of may

- Still administrative issues delaying the start of fabrication



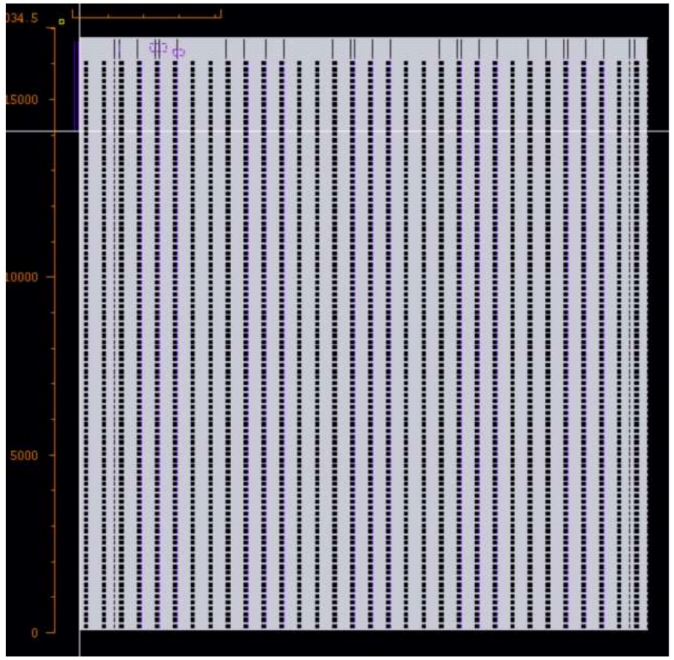
EICROC0 variants

- EICROC0A same as EICROC0 with more testability
  - Each pixel can be by-passed by SC (clock is then turned off)
  - Buffers in SC to allow extension to 4x32
  - Larger dynamic range in pulse injection

- EICROC0B
  - Same preamp/discri/TDC/integrator
  - ADC and driver replaced by peak sensing and Wilkinson ADC
  - Currently ADC path ~1 mW/ch becomes 200 uW/ch

- Will be fabricated with EICROC1 below

- 32x32 chip : final dimensions

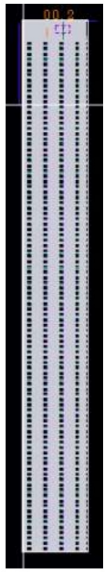


- Goal :
  - test full-scale chip analog performance (IR drops)
  - Allow final sensor characterization
  - Test interface with DAQ : fast commands and 320 Mb/s data output
  - Progress on module/front-end boards

- Caveats ;
  - Not (yet) zero-suppressed data
  - Still 2mW/ch
  - Still analog-on-top

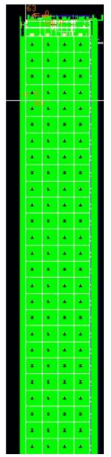
- Designed as 8 blocks of 4x32
  - Read out sequentially, like EICROC0
  - Pixel similar to EICROC0A
  - 8 CLPS outputs at 40 MHz
  - Clock tree for isochronous calib_pulse distribution

- Common balcony (End of column)
  - Biases and slow control
  - New : fast command decoder (clock, calib_pulse, enable_acquisition, start_readout)
  - Backup clock and cmd_pulse inputs available
  - New : 320 MHz serializer for 1 CLPS output



EICROC1A variant

- Full block of 4x32 of EICROC1 with old EICROC0 pinout
  - Same balcony as EICROC0A (same slow control parameters)
  - Same testboard and DAQ as EICROC0
  - Allows to test colums specific effects (IR drops)



Pixelated AC-LGAD Read Out with EICROC0: on-going characterization activities at IJCLab

❖ **Infrared laser test bench development:**

- Olivier Brand-Foissac
- Vincent Chaumat
- Thomas Cornet
- D. M.
- Arzoo Sharma
- Ana-Sofia Torrento

❖ **Beta source (^{90}Sr) test bench:**

- D. M.
- Laurent Serin
- Arzoo Sharma
- Beng-Yun Ky

Other ePIC Roman Pots activities at IJCLab: cooling studies & associated mechanics

- Raphaël Dupré
- Christine Le Galliard