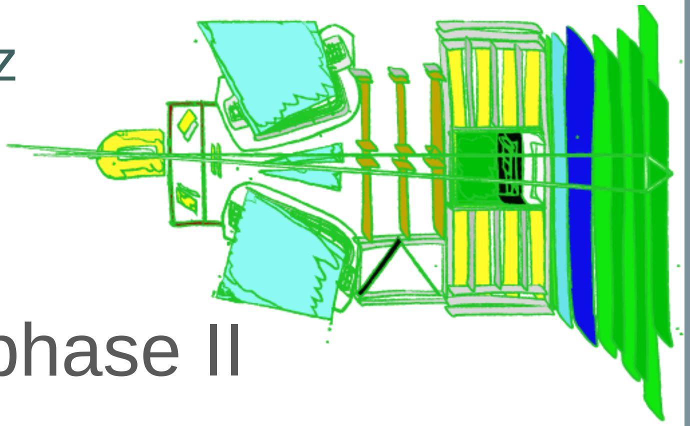
The need of Timing

Orateur: Zulal Kiraz

CNRS – IJCLab



LHCb Calo Upgrade phase II

2026, Orsay
April 2026

OUTLOOK

Irène Joliot-Curie
Laboratoire de Physique des 2 Infinis

LS4

- Why an Upgrade?
- Timing Requirement
- Electronics architecture
- SPIDER
- Where we are & what's next

Why an Upgrade?

The Challenge

- After Run 3, radiation damage degrades the existing ECAL
- Run 5 will bring much higher densities, especially in the central region
- Current electronics cannot measure time; only energy
- Multiple interactions pile up in the same beam crossing, making them impossible to separate

The Solution — PicoCal

- Full redesign of the calorimeter during Long Shutdown 4 (LS4)
- New detector modules: SpaCal and Shashlik, with dual-sided readout
- New Front-End Board (FEB) electronics
- Key addition: picosecond-level timing per detector cell

The timing requirement
Why do we need picosecond timing?

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25 ns

Time between two consecutive LHC beam crossings

30 Interactions

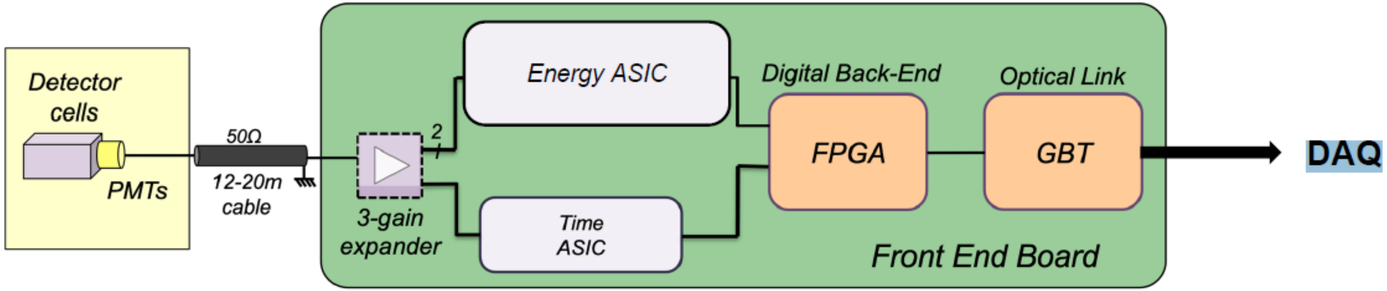
Average pile-up: collisions overlapping in the same bunch crossing

<15 ps rms

Target timing resolution to distinguish which interaction produced which particle

Timing lets us tag each photon to its collision of origin.

Electronics architecture
The new readout chain



On the Front-End Board
* 8 ICECAL + 8 SPIDER blocks per FEB
* MICROCHIP PolarFire MPF200 FPGA for signal processing
* LpGBT transceivers for high-speed optical readout
* 12V supply via DC/DC (bPOL)

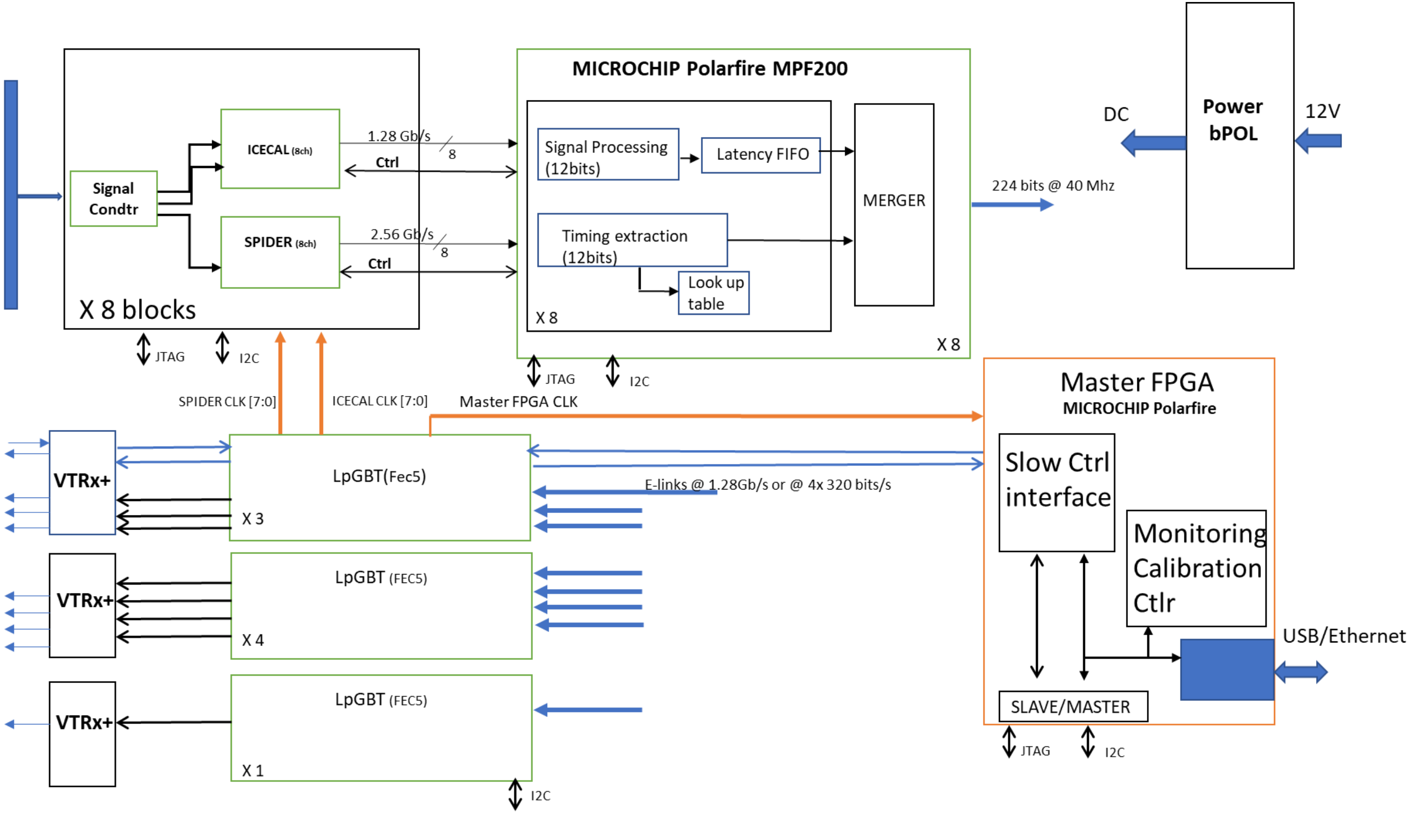
Key data rates
SPIDER → FPGA: 2.56 Gb/s per block

ICECAL → FPGA: 1.28 Gb/s per block

Output to DAQ: 224 bits @ 40 MHz

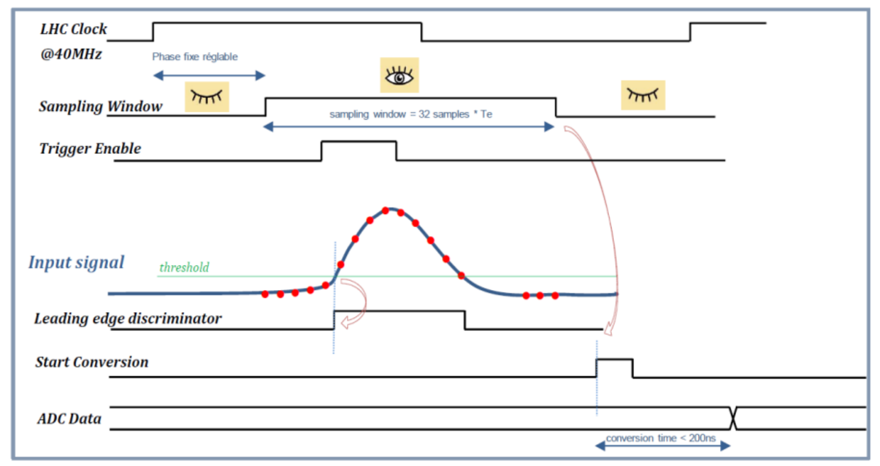
All clocked on the 40 MHz LHC clock

Electronics architecture The new readout chain



Meet SPIDER

- A Waveform TDC — it doesn't just detect a signal crossing a threshold; it digitizes the full waveform shape, then reconstructs the exact crossing time by interpolation.
- Fabricated in TSMC CMOS 65 nm
- Locked to the 40 MHz LHC clock — records a 32-sample window per beam crossing
- 8 banks per channel → handles up to 50% channel occupancy
- Parallel Wilkinson ADC — 10-bit, conversion in <200 ns



- FIRST PROTOTYPE
- **7.1 ps rms**

Time Difference Resolution (2-channel, same chip, no calibration)

- **SINGLE CHANNEL**

5 ps rms

Already exceeds the 15 ps target — without any time calibration yet

- **POWER**
- 64 mW digital · 4 mW analog — remarkably low

Test bench @ Orsay

Where we are & what's next

DONE

- SPIDER V0 taped out Feb 2025, received Jun 2025, packaged in CQFP128
- All main functionalities validated: both DLLs lock, self-trigger, multi-bank readout
- ADC characterised: **850 mV dynamic range**, linearity ±0.2%
- First timing result: <10 ps rms without calibration
- Two independent test benches operational (IJCLab & LPCA)

NEXT

- Fix known issues (PLL frequency lock, layout crosstalk on ADC ramp bus)
- Tape out SPIDER V0+ — corrected version of the 2-channel prototype
- Beam test with 4 channels at IJCLab module
- Design 8-channel version (V1) once V0+ validated — the PicoCal production target
- Evaluate possibility of 16-channel scaling

Thanks for your time and listening!

Questions & Discussion

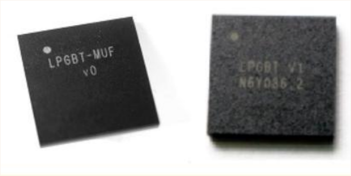
Backup Slides

VLDB+ : lpGBT and VTRx+

- lpGBT (Low-Power Gigabit Transceiver) and VTRx+ (Versatile Transceiver) form the core of the high-speed optical link between front-end electronics and DAQ.

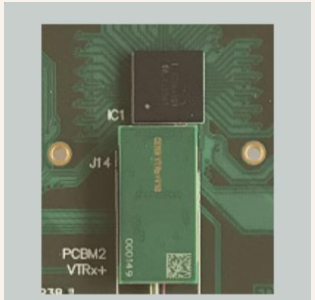
- The lpGBT ASIC handles data serialization, clock distribution, and slow-control communication, and the VTRx+ optical module converts into optical signals for transmission over fiber.

- This combination, hosted on the VLDB for radiation-tolerant, deterministic-latency communication from front-ends to the DAQ system.

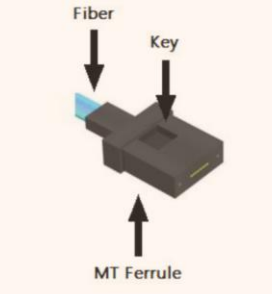


lpGBT V0 (left) and lpGBT V1 (right)

We've ordered: 3 VTRX+ / FEB (i.e. 11 up-links , i.e. ~100 Gbps / FEB)

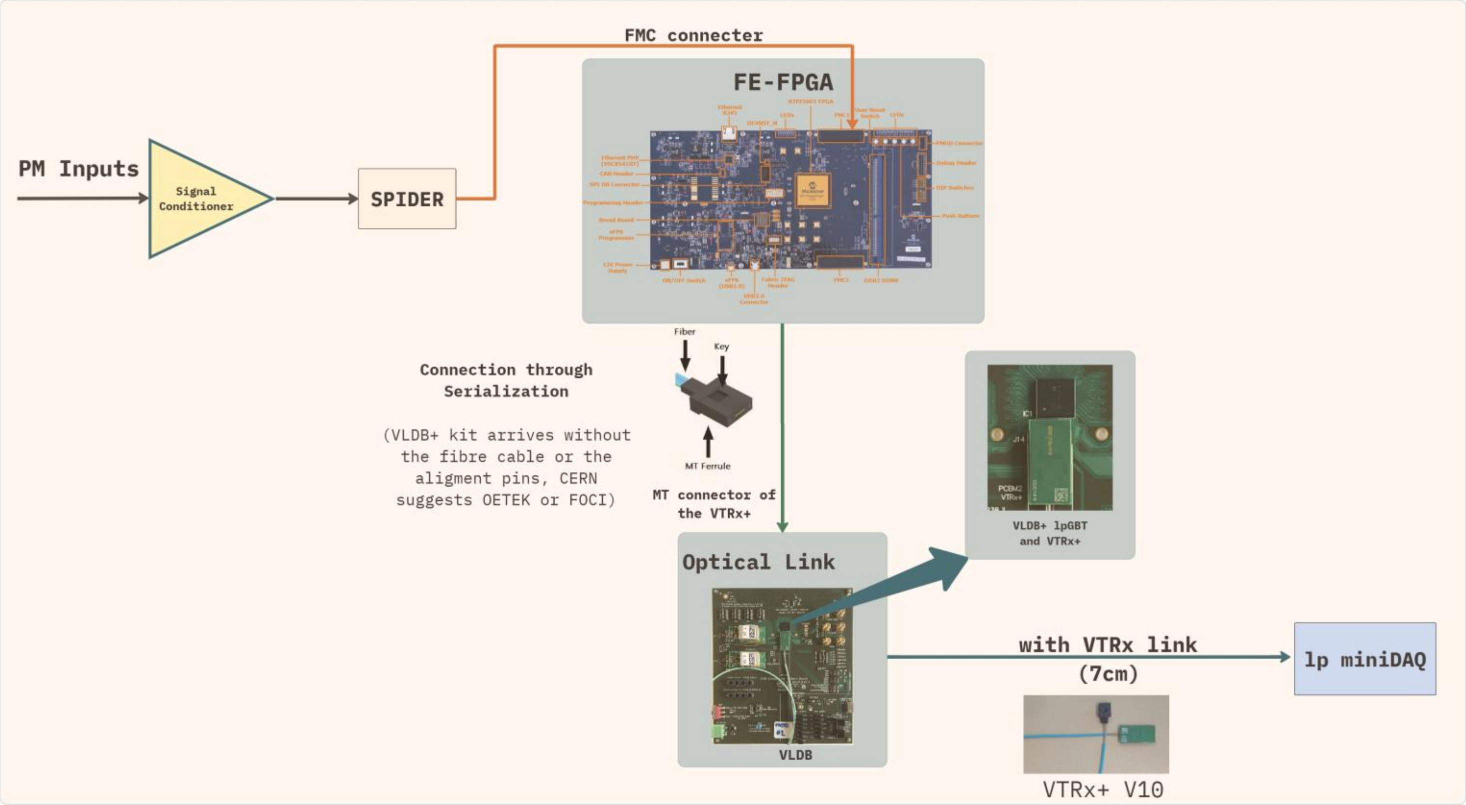


VLDB+ lpGBT and VTRx+

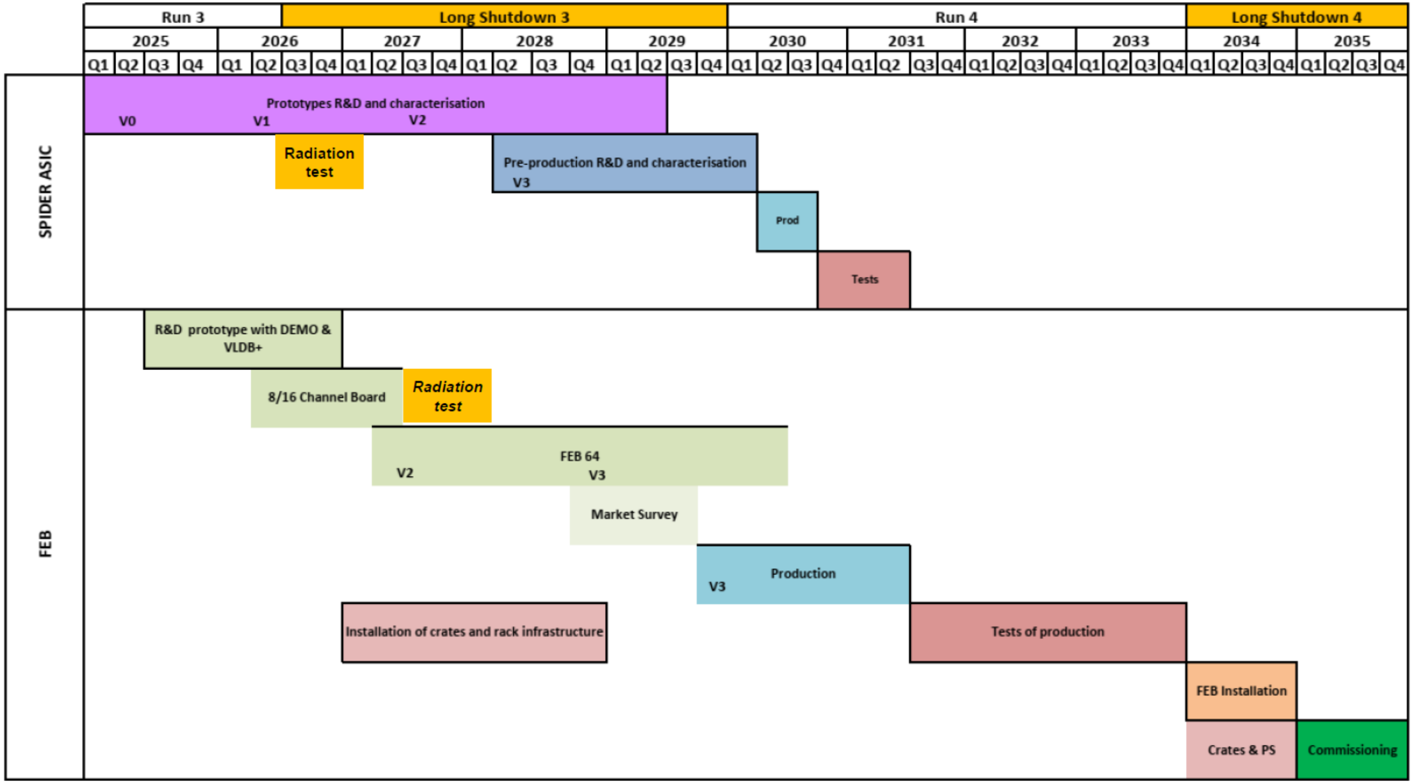


MT connector of the VTRx+

VLDB+ lpGBT and VTRx+ Connections



Timeline for LS4



Note: Syracuse is interested in helping with the radiation tests and will explore available facilities in the US