EICROC0A

Current state
Preliminary measurements

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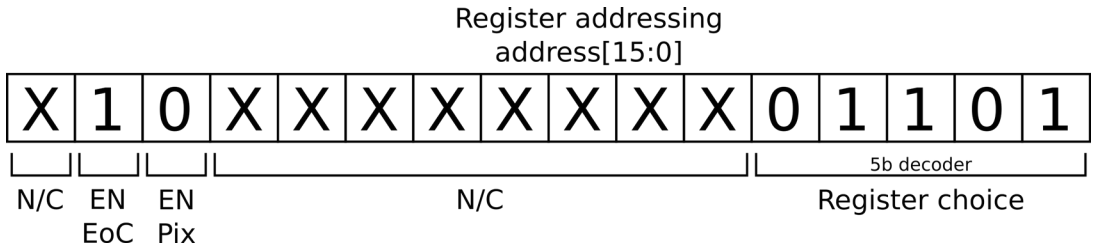
Summary

- EICROC0A/B and EICROC1 addressing issue
- EICROC0A workaround
- Preliminary measurements
- Next steps

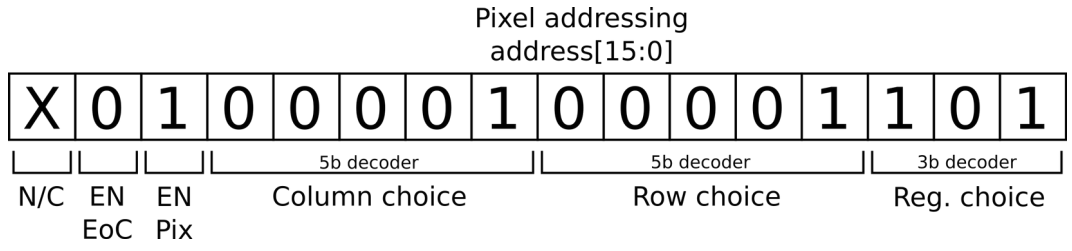
How are registers addressed in EICROC0A/B & EICROC1?

- Register addressing in new ASICs is derived from EICROC1
- The EICROC0 register addressing scheme would not have worked with 32x32 pixels

EICROC1 addressing logic :



End of Column (EoC) is properly addressed



Pixels should be enabled with :
EN_pix → col_choice → row_choice
BUT
The 3b_decoder for reg_choice has an enable which is always on

Default behavior in ASICs is to **disable** a single pixel at once, rest the addressed simultaneously.

EICROC0A addressing workaround

- Current workaround is to use the parallel writing behavior to load a default config in pixels that we are not directly testing

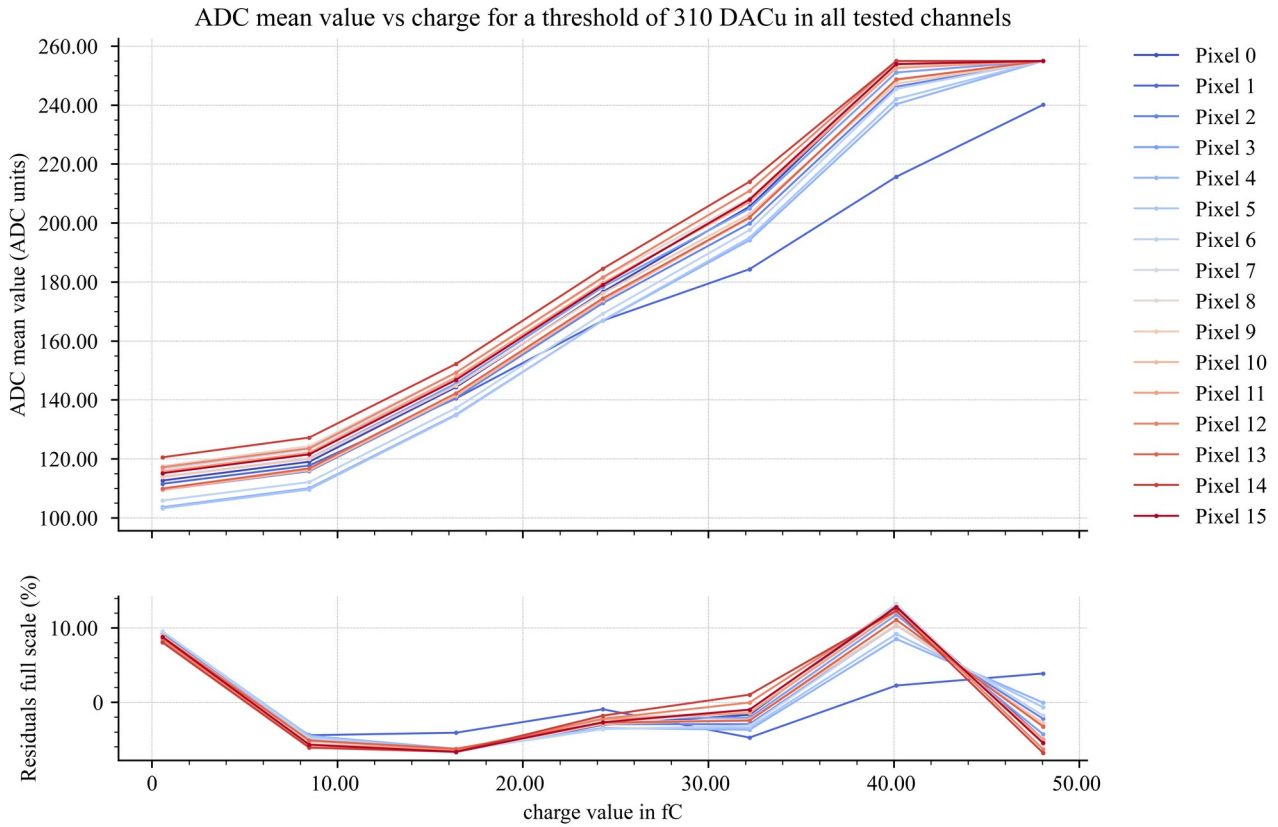
1) Load EoC configuration (this step also overwrites all pixels)

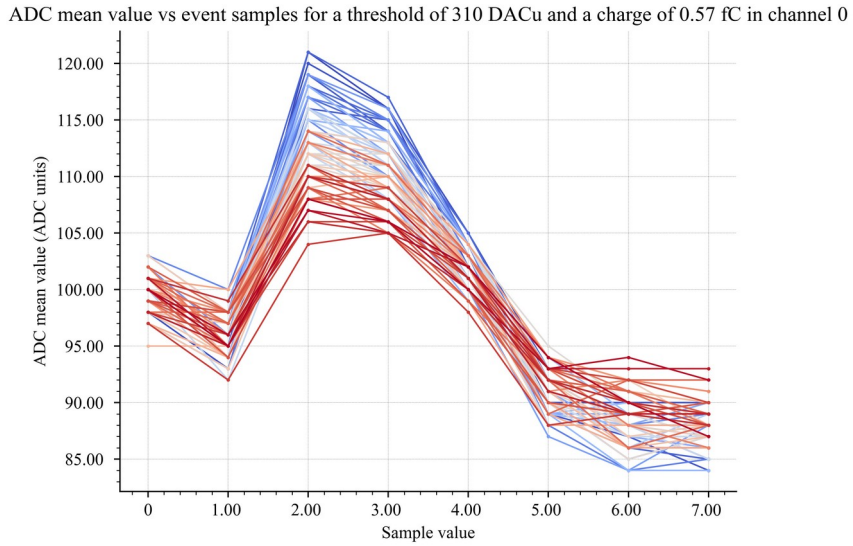
2) Load test configuration in all pixel matrix

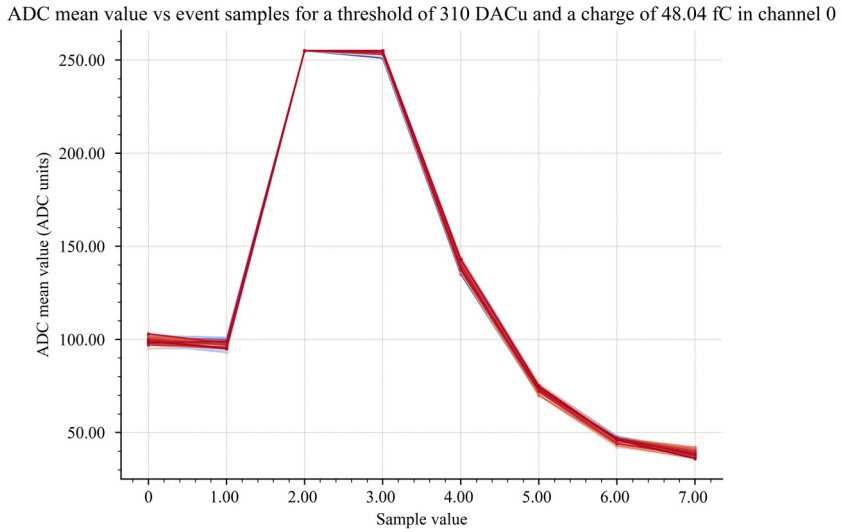
3) “Mask” the pixel under test and load “default” configuration in the rest of the matrix

- Problem lies with EoC writing after these steps :
  - EoC writing uses addr[4:0] (ex 0x400B = 0b0100000000001011 – loads global discriminator threshold)
  - Pix writing uses addr[2:0] (ex 0x210B = 0b0010000100001011 – loads local preamp & probe config…)

EICROC0A preliminary measurements : ADC

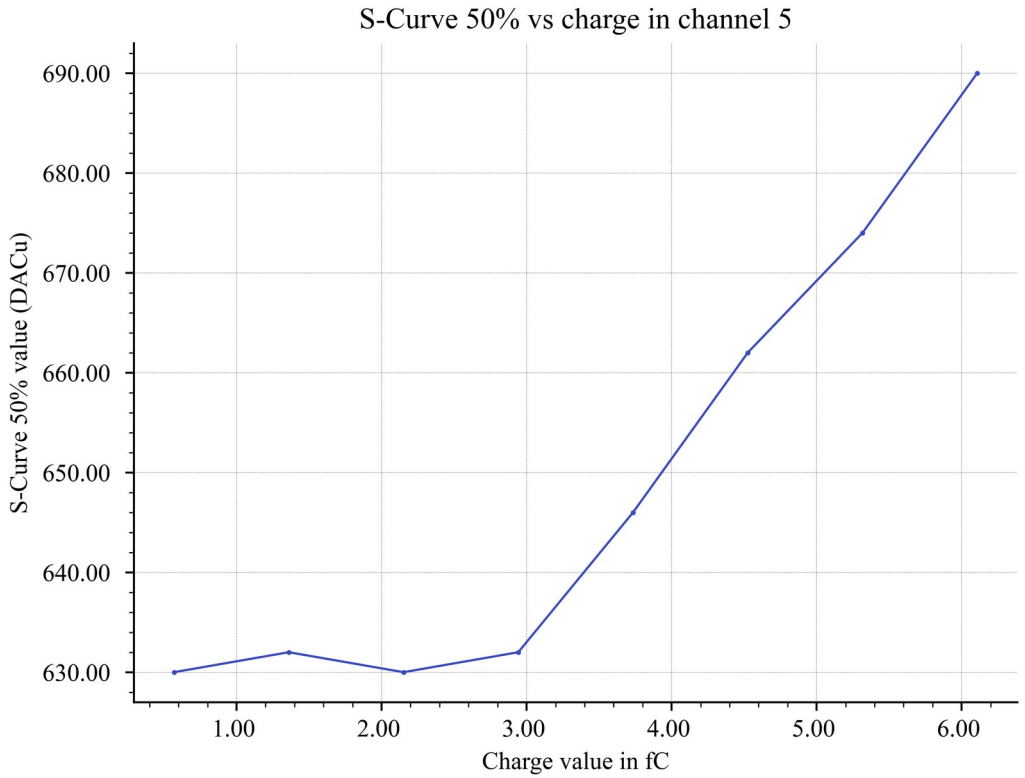


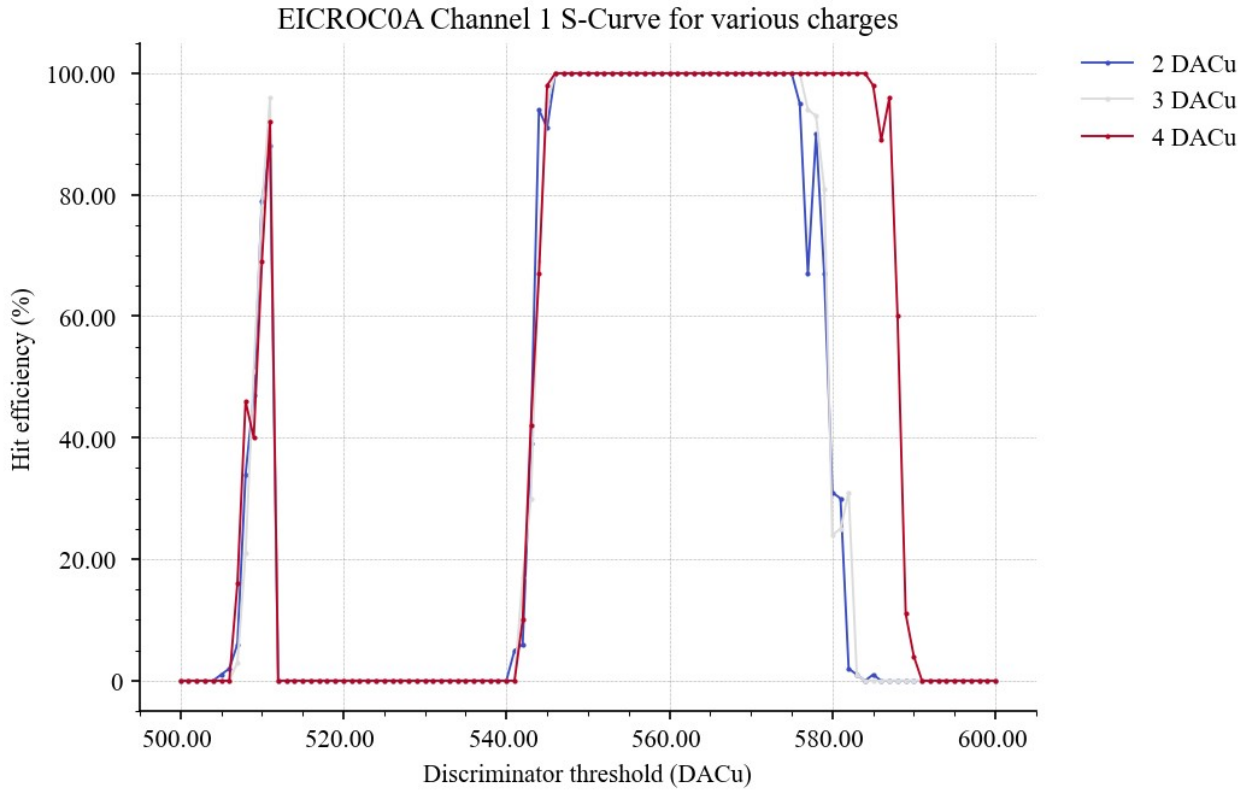




Can see data from all pixels
Plots show **raw data**, no pixel correction or post correction
ADC is in saturation for the highest charge as local correction is not used

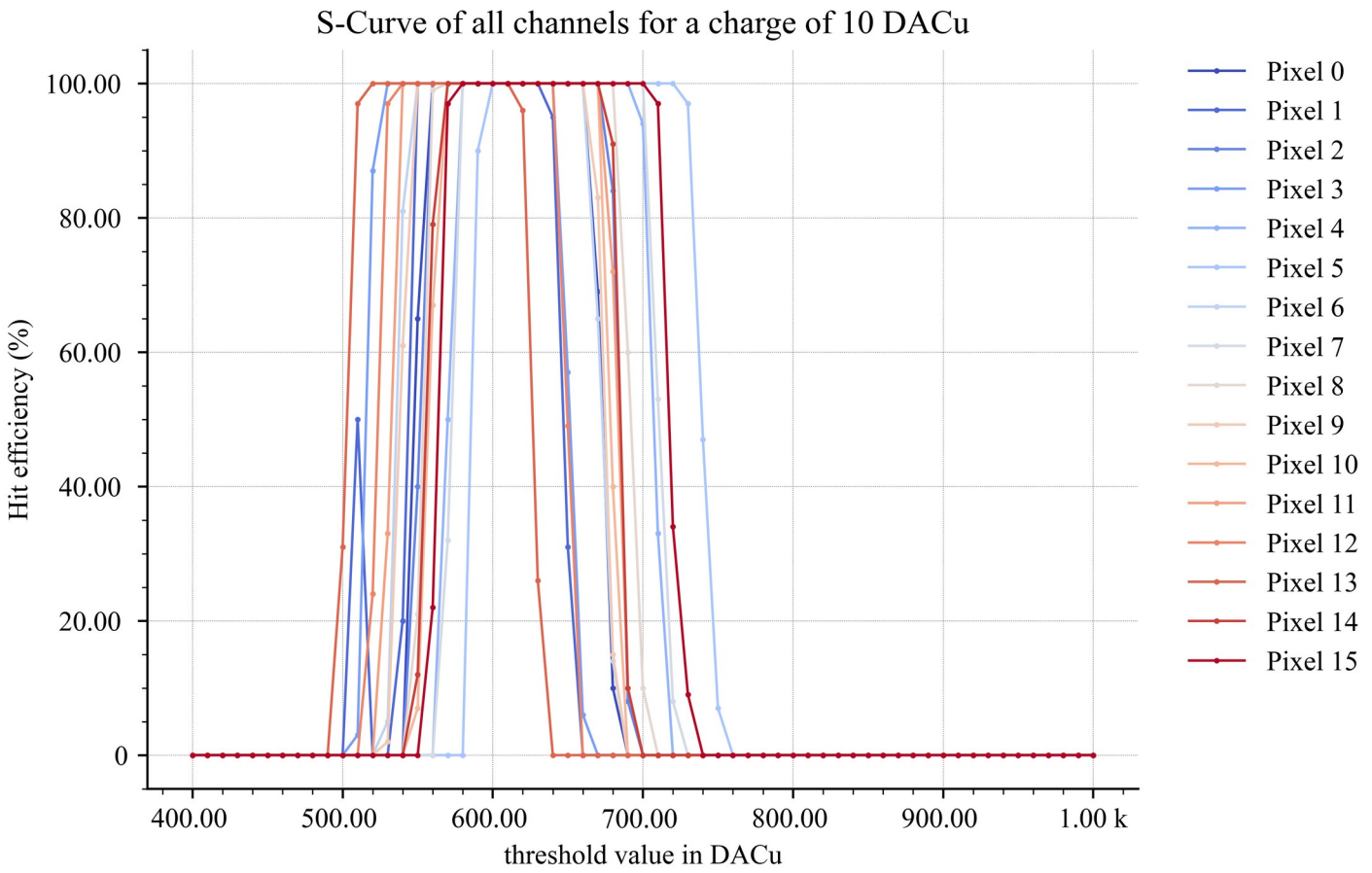
EICROC0A preliminary measurements : Discriminator





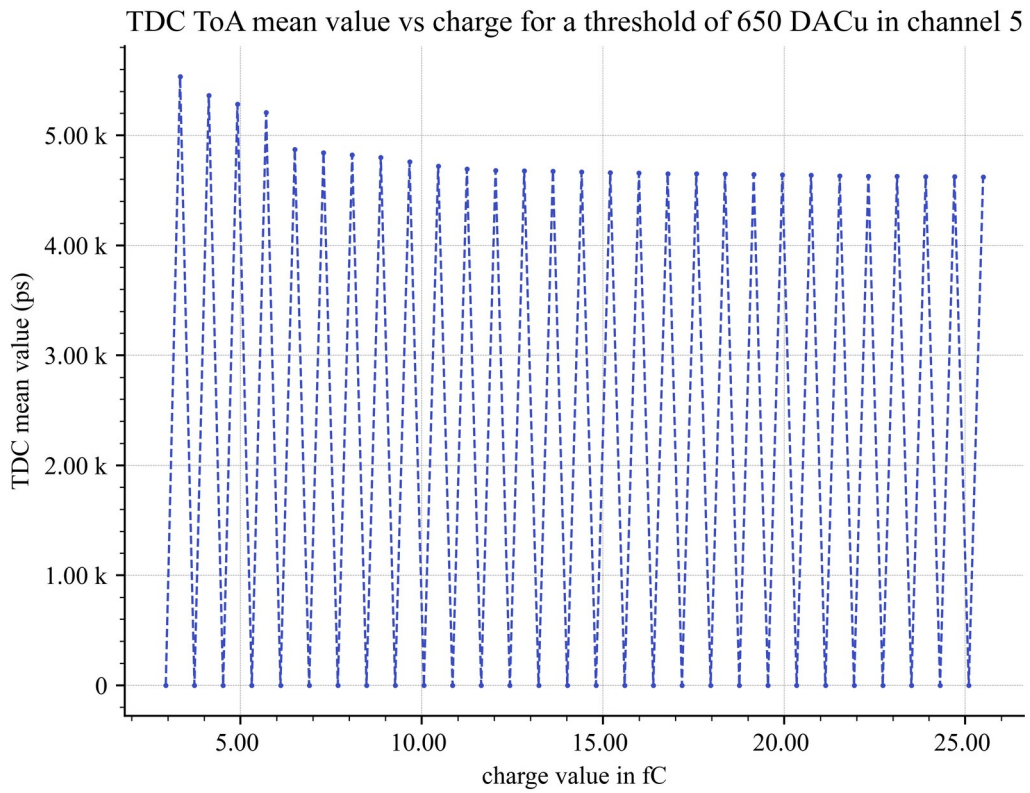
Lowest charge detected is currently between 3 and 4 fC
No pixel correction or optimization possible at the time

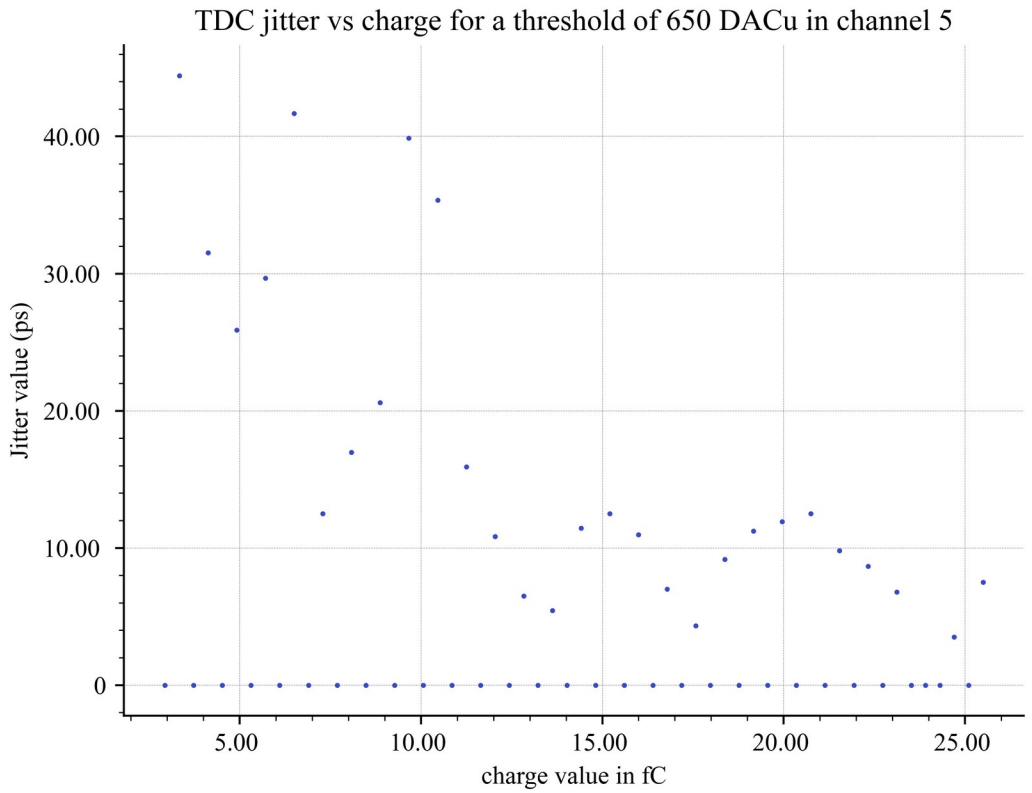
EICROC0A preliminary measurements : Discriminator



All channels can be measured with S-Curves
No local correction means the threshold is around 700 DACu : local correction in EICROC0 lowered it around 350 DACu.

EICROC0A preliminary measurements : TDC





New TDC parameters used, need to continue working on TDC to obtain “clean” plots

Promising results at the moment

Next steps

- Continue measurements to better understand ASICs
  - Fix TDC issues
  - Improve testing software (reg. Addressing, value masking, …)
  - EICROC0A and EICROC1 testing for metal fix
- Prepare metal fix