Single Event Effects

Actel AX FPGA

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Abstract

ACTEL and NASA performed irradiation tests at Brookhaven National Laboratory on the AX1000 component of the new ACTEL FPGA family "Axcelerator". The characteristics of these FPGAs are attractive and make them good candidates for the Front-End of the LHCb Calorimeters. The results of the measurements done at BNL are used to determine the resistance of the AX in the environment of the Calorimeter electronics. If mitigation techniques are used (triple voting or horizontal and vertical parity), no major worry is expected in spite of the safety factors applied in the evaluation. In this case and at maximum, a few bit errors could be observed per year on the full Calorimeter system.

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I - Introduction

Some intensive irradiation measurements have been performed by Actel and NASA at Brookhaven National Laboratory ([4]) on the new Actel FPGA AX1000. This component or the other Antifuse FPGA of the AX family are good candidates for the Front-End of the Calorimeter electronics. They associate a high number of combinatorial and register cells with a large memory. Moreover, the carry-logic implementation increases the efficiency for arithmetic calculations. Table 1 shows the main characteristics of the AX family FPGAs.

Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in Equivalent System Gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Modules					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Flip-Flops (Maximum)	1,344	2,816	5,376	12,096	21,504
Embedded RAM/FIFO					
Core RAM Blocks	4	12	16	36	64
Core RAM Bits	18,432	55,296	73,728	165,888	294,912
PerPin FIFOs	172	256	336	516	684
PerPin FIFO Bits	11,008	16,384	21,504	33,024	43,776
Total Embedded RAM Bits	29,440	71,680	95,232	198,912	338,688
Clocks (Segmentable)					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
PLLs	8	8	8	8	8
I/Os					
I/O Banks	8	8	8	8	8
I/O Cluster Blocks	8	16	16	24	32
User I/Os (Maximum)	172	256	336	516	684
I/O Registers	516	768	1,008	1,548	2,052
Package					
CSP	180				
BGA				729	
FBGA	256	256, 484	484, 676	676, 896	896, 1152

Table 1 The characteristics of the Actel AX family FPGAs. Extracted from the ACTEL AX datasheet [3].

Their resistance with respect to single event effects is studied in this note.

II - Particle flux in the LHCb cavern

The particle flux in the region of the electronics of the calorimeter has been estimated on a $b\overline{b}$ Monte Carlo sample (see [2] and figure 1 (left)). Neutrons are the main contribution to the flux of incoming particles.

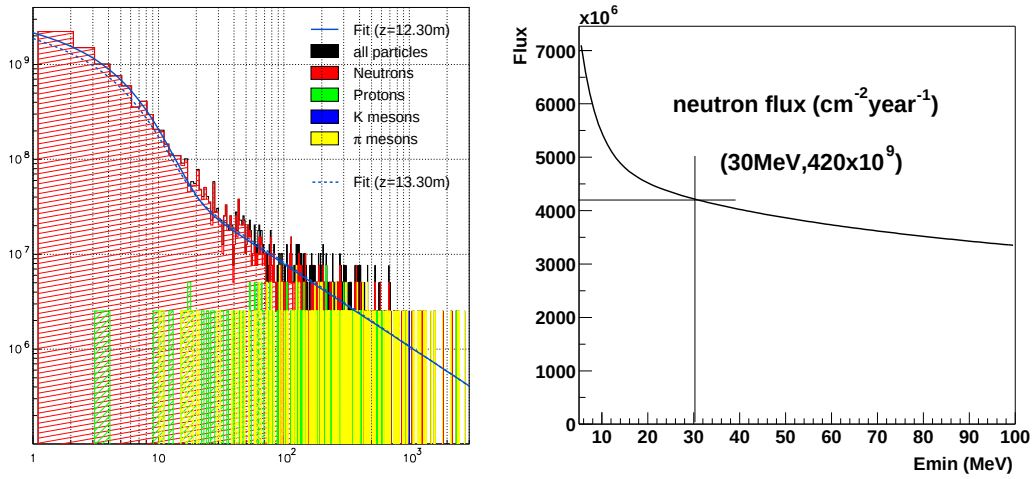

Figure 1

Left: Particle spectrum ($cm^{-2}.year^{-1}.MeV^{-1}$) in the Calorimeter Front-End electronics region at z=12.3m from the interaction point.

Right: Integrated spectrum in the region of the electronics of the Calorimeter (see left plot legend). The integral is performed on the fitted function (II 1) from x MeV up to 3 GeV. Above 10 MeV, the flux decrease is slow.

$$f(x) = Ae^{-Bx} + Cx^{D} \qquad \text{(II 1)}$$

Z position	***A***	***B***	***C***	***D***
12.30 meters (ECAL)	$2.2\text{x}10^9$	0.27	$0.43\text{x}10^9$	-0.87
13.32 meters (HCAL)	$A.8\text{x}10^9$	0.28	$0.49\text{x}10^9$	-0.89

Table 2 Result of the fits of function (II 1) to the flux simulations in the region of the electronics of the calorimeter[2].

Function (II 1) was fitted to the Monte Carlo data sample produced. The values of the parameters extracted at two different z positions along the detector and corresponding to the ECAL and the HCAL electronics locations are listed in table 2. In the following, we require an estimation of the total flux of neutrons capable of triggering an upset in the electronics of the detectors. In this purpose, the flux derived from equation (II 1) is integrated above a threshold of 30 MeV. Indeed, we can suppose that below that energy threshold the incoming neutrons cannot break the silicon nucleus and produce energetic enough fragments. Figure 1 (right) shows the running integral of the neutron spectrum from *x* MeV up to 3 GeV. From this plot, it is obvious that the evaluated flux doesn't depend rapidly on the threshold minimum energy, at least if this threshold is above 10 MeV.

III - Fragments produced by neutron-Si interaction

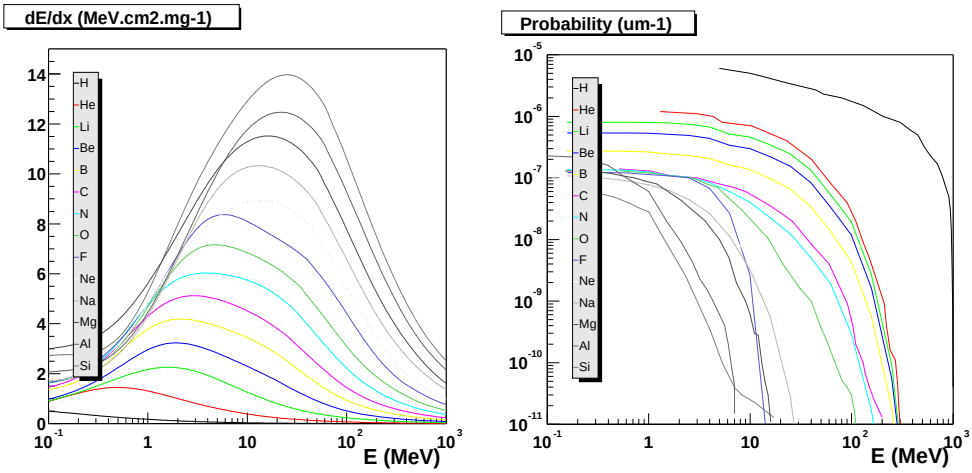

Figure 2:

Left: dE/dx (MeV.cm^2.mg^{-1}) of the various types of fragments produced by neutron-Silicon interaction according to the kinetic energy of the fragment.

Right: Probability (μm^{-1}) to produce a type of fragment at an energy greater than x MeV.

In a neutron-Silicon interaction, the fragments produced have an atomic mass ranging from Hydrogen up to Silicon. Any of the associated isotopes may appear. We used the program SRIM [5] to determine the *de/dx* of those ions in Silicon. The results are shown on figure 2 (left). The probability to produce any of those elements has been extracted from [6] where it was calculated for 1 GeV kinetic energy neutrons interacting with Silicon. In the region of the electronics of the calorimeter, most of the neutrons will have a lower energy. Nevertheless, in the following the values of figure 2 (right) are used whatever the incident neutron energy.

IV - Dose, Single Event Latchup and Single Event Dielectric Rupture

The Actel AX has been irradiated up to 200 krad (accumulated) at a dose rate of 33 rad/sec with γ particles. No change in the propagation delay or the I_{ccA} current has been observed. An increase of the I_{ccI} from 1.2mA to 8mA was seen. The dose expected at LHCb in the electronics area is of the order of 200 rad per year.

Apart from the cumulated dose, two other effects can permanently destroy a component, the Single Event Latchup (SEL, a "short-circuit" is triggered and caused by a ionising particle crossing the medium of the component) and Dielectric Rupture (SEDR, rupture of an antifuse connection due to a local ionisation). The SEL and SEDR immunity has been checked at BNL with several types of ions (I-127, Br-81, Cl-35, F-19, C-12) at Linear Energy Transfer (LET in the following) up to 120 MeV.cm^2.mg^{-1}. No SEL or SEDR was recorded confirming the resistance of the chip in the LHCb environment. We can expect that neutron-Silicon interactions produce debris whose maximum LET is 15 MeV.cm2.mg-1 (see part III), i.e. far below the values tested at BNL.

In order to estimate the resistance of the chip, the same method as the one applied in [2] is used and is recalled here. A SEL/SEDR sensitive area of the component s is defined together with the area affected by an incoming ion s_{ion}. These areas are expressed in proportion of the total surface of the active area of the component and the probability that an incoming ion doesn't hit a sensitive zone is $1-s-s_{ion}$. From the number of SEL/SEDR, or from the fact that no SEL/SEDR was recorded, 95% confidence level exclusion contours can be drawn in the $[s,\ s_{ion}]$ plane.

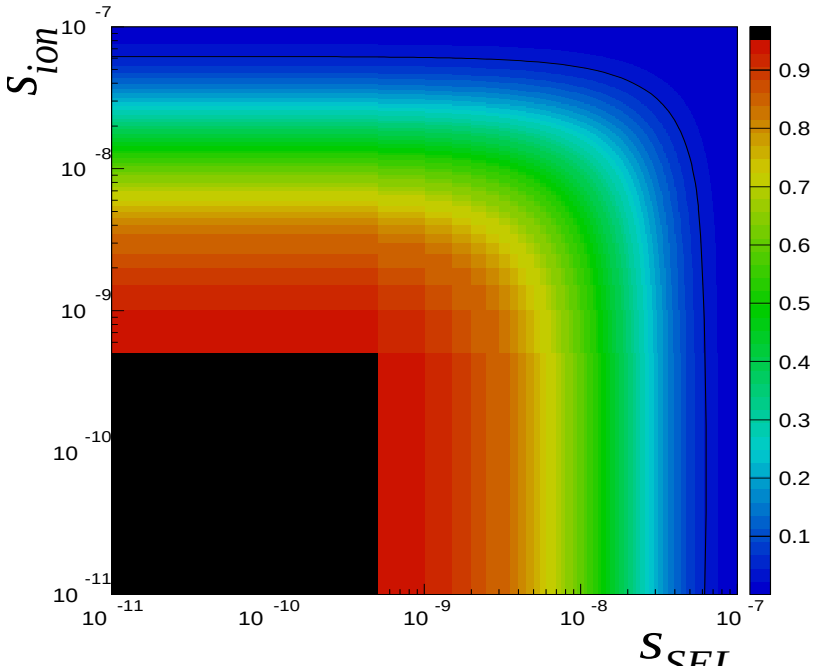

Figure 3 Probability not to have any SEL/SEDR with the AX1000 component in five runs of fluence 10^7 ions each. The black curve is the 95% CL contour in the $[s, s_{ion}]$ plane.

Such a contour has been calculated for SEL/SEDR on the AX1000 component. We supposed that 5 runs of 10^7 ions each (this is the typical fluence used for BNL tests but we have no confirmation that it was the real fluence for those runs[1]) had been performed to extract the plot of figure 3. Two regimes are identified:

- $s_{ion} > 6.2x10^{-8}$: the component has been fully scanned by the ions of the beam. There exist no sensitive zone at LET tested in the part.
- $s_{ion} < 6.2x10^{-8}$: the component has not been fully scanned, but a limit can be extracted on the size of the sensitive area, $s_{limit} = 6.2x10^{-8}$, which may have escaped the ions of the incoming beam.

Whatever the *true* regime, the safest and most pessimistic assumption consists of supposing that the sensitive area is smaller than $6.2x10^{-6}$ % of the surface of the active area of the component. The probability to produce an ion with a LET greater than 6 MeV.cm^2.mg^{-1} was estimated[2] to $2x10^{-6}$. We conclude that the resistance is greater than 1920 years per chip at 95% Conf. Level. A neutron flux of $4.2x10^9$ year^{-1}.cm^{-2} was assumed as described in section II of this note.

V - Single Event Upset and Clock Upset cross-sections

Unlike the SEL or the SEDR, the Single Event Upset or the Clock Upset are not destructive. The user loses the functionalities of the component until a power reset is done. The SEU is due to an ionising particle that changes a(several) bit value(s) in the RAM or in registers. The clock upset is a glitch on a clock line distributed in the component that desynchronises (part of) the component. The AX components include 4 hardwired clocks and 4 clocks that can be routed by the user (as shown on figure 4).

1 A fluence of 10^7 ions is consistent with the cross-section limits obtained in [1].
2 We suppose that below a LET=6 MeV.cm^2.mg^{-1}, it is not possible to trigger a SEL (see [2]).

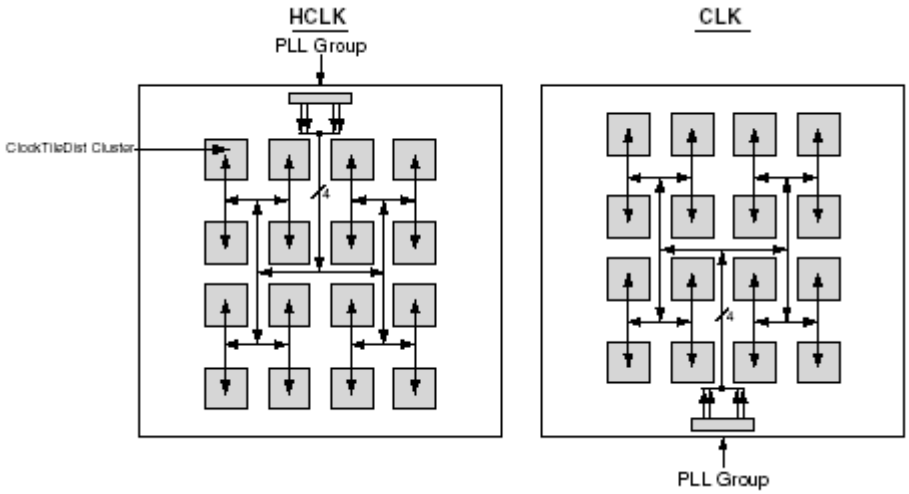

Figure 4 The 4 hardwired clocks (left) and the 4 user routed clocks (right). A glitch on a line can fake a clock beat and desynchronize (part of) the component.

In this section, some of the measurements performed at BNL are shown ([4], [7]). The Single Event Upset cross-sections are given for the SRAM and the registers, respectively. The last curves concern the problem of clock upset. All these measurements and the figures of this section are extracted from [1].

a.SRAM

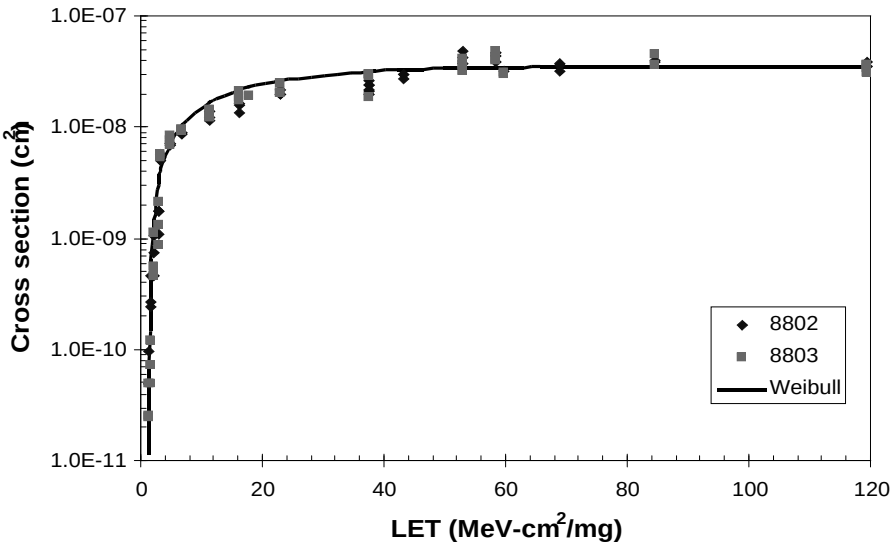

Figure 5: AX1000 SRAM SEU cross-section (cm^2) and Weibull curve.

b.R-Cell

"Zero" and "One" patterns

"0" and "1" patterns have been used for test purpose, as shown on figure 6. "0" pattern seems to be more sensitive than "1" pattern at least for large LET which are far above the LET values reached in

our environment. In the following, the measurements obtained with the "0" configuration, which correspond to the largest set of data, will be used only.

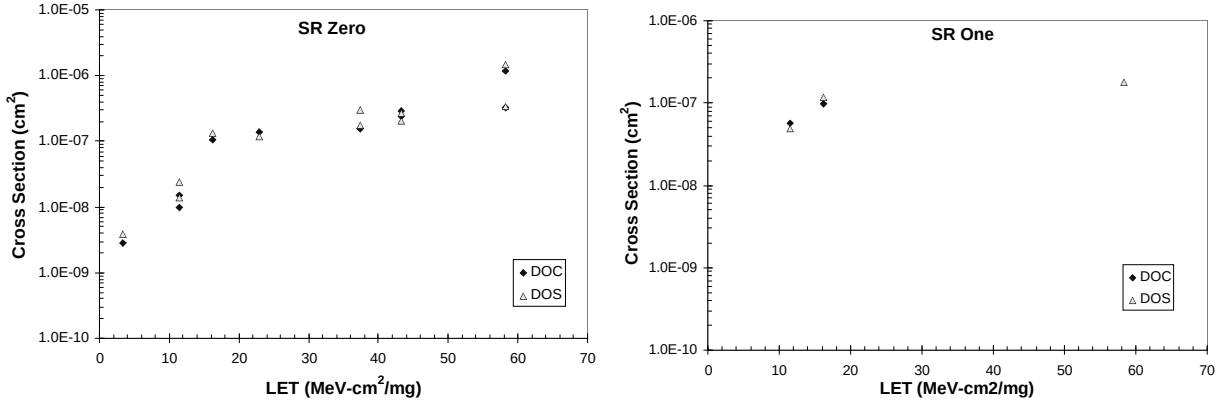

Figure 6 AX1000 R-Cell SEU cross-section (cm^2) for "0" (left) and "1" (right) patterns.

c.Single Event Upset Weibull curves

The cross-section curves have been used to extract the parameters of the corresponding Weibull functions defined by

$$f(E_{LET}) = \sigma_0 \left(1 - e^{\left(\frac{(E_{LET} - E_{L_0})}{W}\right)^s}\right) \qquad \text{(V 1)}$$

The results of the fits is given in table 3.

	σ_0	L_0	*Width*	*Shape*
S-RAM	$3.5 \times 10^{-8} cm^2$	1.44 MeV.cm^2/mg	15 MeV.cm^2/mg	1
R-Cell("0" pattern)	$1.x10^{-6} cm^2$	3.0 MeV.cm^2/mg	30 MeV.cm^2/mg	2

Table 3 Weibull curve (defined by equation V 1) parameters used in the following for SRAM and R-Cells.

d.Clock Upset

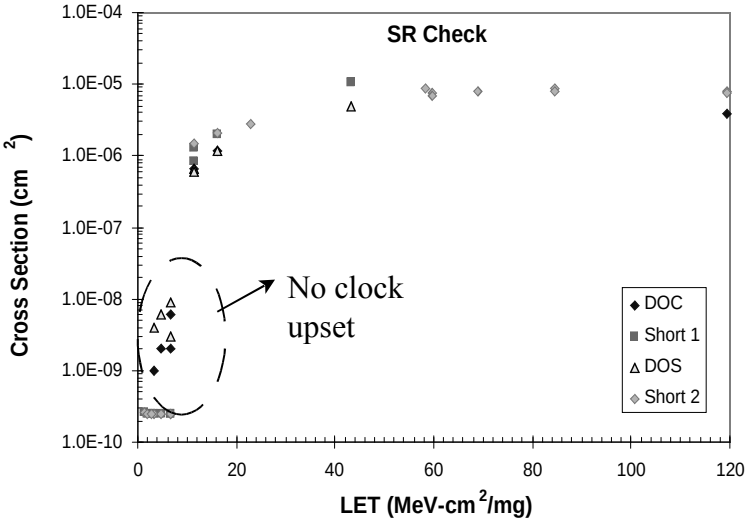

Figure 7 AX1000 Clock Upset cross-section (cm^2) measurements and limits.

VI - SEU and Clock Upset rate estimations

a.Method

In the previous sections, the necessary information has been gathered in order to evaluate the sensitivity of the Calorimeter electronics with respect to SEU and Clock Upset.

The simplest technique to calculate the SEU and Clock Upset rates consists of integrating the neutron flux multiplied by the upset cross-section expressed in term of the neutron kinetic energy :

$$\int_0^\infty \phi_{neutron}(E) \times \sigma(E)\, dE$$

In our case, the cross-section is given with respect to the LET of the ions and the previous method cannot be applied. The neutron flux defined by equation (II 1) allows to derive the flux of ions of type *i* and of energy E MeV produced by neutron-Silicon interaction in a thickness of Silicon *t*,

$$\phi_i(E) = \int_0^\infty \phi_{neutron}(E')\, p_i(E, E')\, t\, dE'$$

where $p_i(E, E')$ is the probability to produce a fragment of energy E MeV per µm from an incoming neutron of energy E'. As we suppose that this probability is independent of E', the term $p_i(E, E')$ can be extracted from the integral and the total neutron flux enters the $\phi_i(E)$ evaluation. Moreover, we suppose in the following that the active thickness of the components is of the order of *t*=20 µm. The range of the ions that can potentially trigger a SEU is lower than this value (see reference [6]). Hence, the flux $\phi_i(E)$ evaluated this way is rather pessimistic. The correspondence of the LET of the ions versus their energy can be read from figure 2.

At this point, the complication comes from the fact that along its way in the Silicon of the component, the ion will lose energy. If the initial energy of the fragment *i* is below the energy for

which the LET is max (LET_i^{max}), we assume that the LET keeps its initial value in matter. This is a safe assumption that will lead to pessimistic estimations. On the contrary, if the energy of the debris is high, its LET will first increase while crossing the component. In this case, the LET taken all the way through the thickness *t* is LET_i^{max} . Once again, this is a safe (and pessimistic) statement. The total SEU rate is calculated by integrating over the full LET range the product of the cross-section (expressed in terms of the LET) by the ion flux (in LET) and summing over the ion species at reach :

$$\sum_{ions} \int_0^{\infty} \phi_i(E_{LET}) \times \sigma(E_{LET})\, dE_{LET} \qquad \text{(VI 1)}$$

Finally a factor 5 is applied on all the rate estimations to take into account the isotopes of the ion species.

This method has been used to evaluate SEU for SRAM, R-Cell ("0" pattern) and Clock Upset.

In the rest of this section, the calculated upset rates per incoming neutron ($s^{-1}.cm^{-2}$) are given. The *total* upset rate is determined by multiplying this rate by the total incident neutron flux[3], which was obtained in section II.

b.SRAM

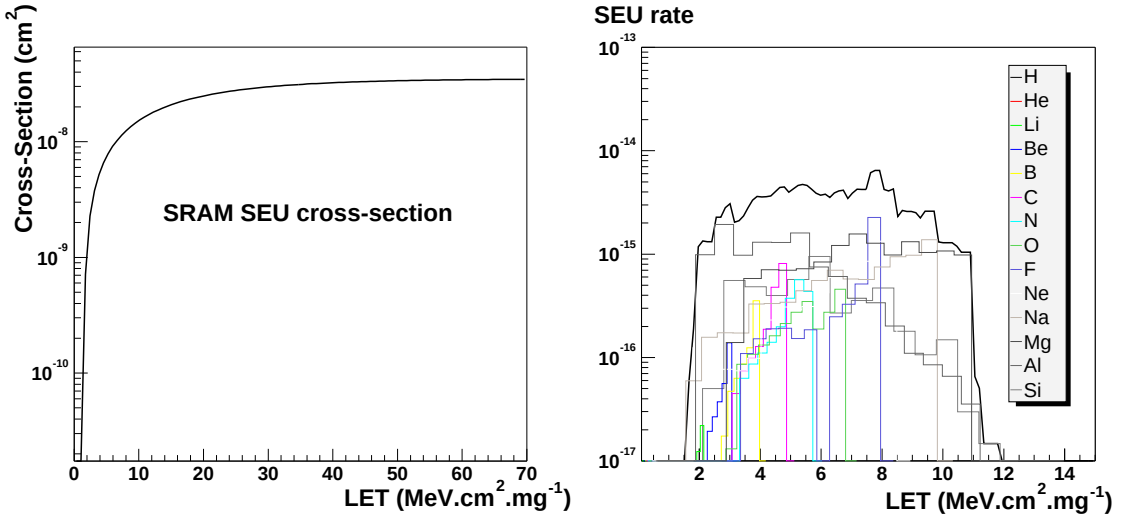

Figure 8 On the left, the cross-section used in the integration of formula (VI 1) for SRAM is given. The right plot is the cross-section multiplied by the flux of the possible ions in LET bins. The black curve is the sum over the various ion species. The integration of this curve leads to a SEU rate per incoming neutron ($s^{-1}.cm^{-2}$) for SRAM of $6.5x10^{-13} bit^{-1}.s^{-1}$

3 This is possible because the probability to produce an ion at a certain energy is supposed to be independent of the energy of the incoming neutron. Moreover, we assumed that the neutron energy had to exceed 30 MeV to be able to produce any type of fragment (see section II).

c.R-Cell

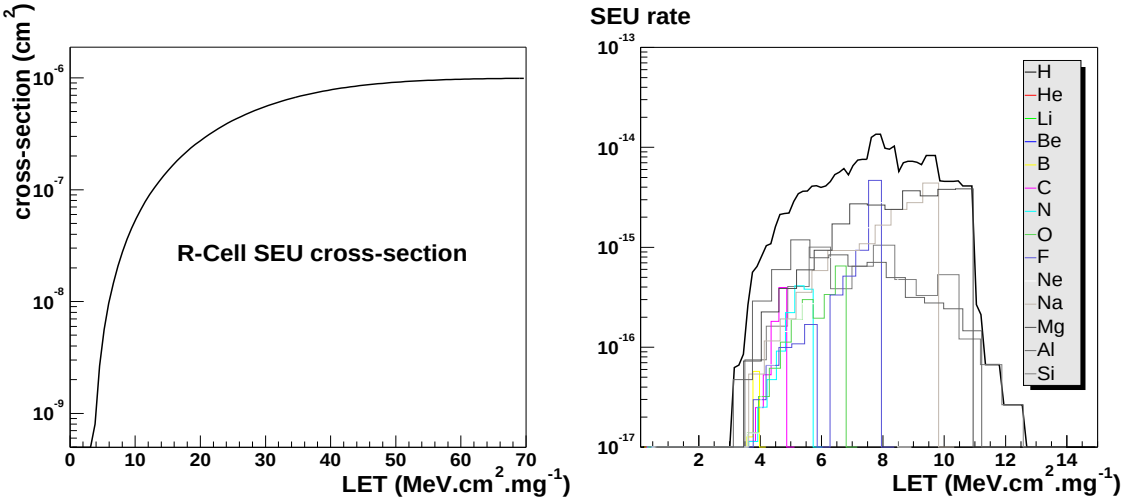

Figure 9 On the left, the cross-section used in the integration of formula (VI 1) for R-Cell is given. The right plot is the cross-section multiplied by the flux of the possible ions in LET bins. The black curve is the sum over the various ion species. The integration of this curve leads to a SEU rate per incoming neutron ($s^{-1}.cm^{-2}$) for R-Cell of $5.5x10^{-13} bit^{-1}.s^{-1}$.

The SEU rate per incoming neutron is slightly higher for SRAM than for register-cell. This could seem paradoxical regarding the asymptotes of the cross-section curves, $3.5x10^{-8}$ and 10^{-6} cm^2 respectively. The reason is in the shape of the two curves. In the SRAM case, the fragments leading to a low LET can still trigger a SEU when registers need an a larger ionisation. Fewer ions species can contribute to SEU in R-Cells and a larger neutron energy is necessary, as can be seen from picture 10.

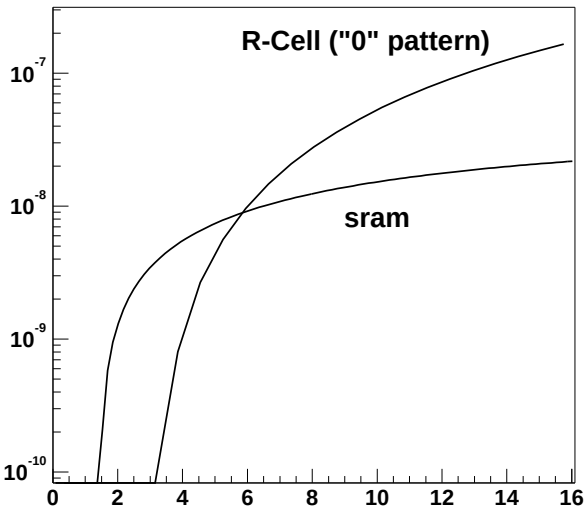

Figure 10: Comparison of the SEU cross-section Weibull curves for RAM and R-Cell.

d.Clock Upset

No Clock Upset Weibull function was given in reference [1] and we estimated ourself the corresponding parameters. The values of the cross-section have been extracted directly from figure

5. Below LET=11.4 MeV.cm^2.mg^{-1} the points of this figure are limits on the cross-section due to the lack of statistics. We used these limits as measured quantities to perform the fit (the cross-section used are listed in table 4).

LET (MeV.cm^2.mg^{-1})	***Cross-section (cm^2)***
5	10^{-9}
6	$5x10^{-8}$
11	10^{-6}
20	$3x10^{-6}$
40	10^{-5}
100	10^{-5}

Table 4 Clock Upset cross-section (cm^2) values extracted from figure 7 ([1]) and used for the Weibull curve parameter estimation.

The parameters obtained from the fit are in table 5:

	σ_0	***L_0***	***Width***	***Shape***
Clock Upset	10^{-5}cm^2	5.0 MeV.cm^2/mg	20 MeV.cm^2/mg	2

Table 5 Weibull curve parameters obtained for the AX1000 Clock Upset cross-section (cm^2).

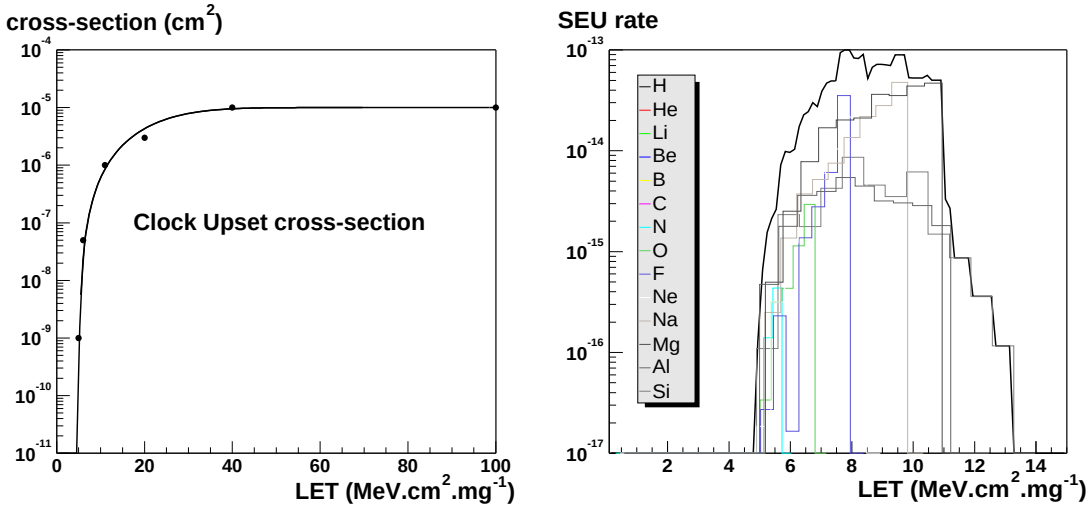

Figure 11 On the left, the cross-section used in the integration of formula VI 1 for Clock Upset is given. The right plot is the cross-section multiplied by the flux of the possible ions in LET bins. The black curve is the sum over the various ion species. The integration of this curve leads to a Clock Upset rate per incoming neutron (s^{-1}.cm^{-2}) of 35.0x10^{-13}bit^{-1}.s^{-1}.

VII - LHCb Front-end FPGA sensitivity

a.Protections foreseen

No protection is planned for the SRAM. The high frequency data related to the measured signals are stored in RAM and a SEU would affect a very limited set of information. The registers will keep critical data (calibration values, counters, ...) that will be reloaded typically once a day. Two

protections are foreseen for registers :

- Triple Voting Registers (TVR): the information is stored three times and a vote is done on the three bits.
- Horizontal and Vertical Parity (HVP) : the values are stored in a table and horizontal and vertical parities are calculated. When the values are needed the parities are checked. An error can be corrected. When two errors occur in the table, the problem is known.

The TVR mitigation is a stronger protection, but consums more registers (3N registers -TVR- versus $(\sqrt{N}+1)(\sqrt{N}+1)$ -HVP- to protect N bits). According to the number of values to store, TVR or HVP technique is chosen.

b.Calorimeter sensitivity

In the following, the LHCb Calorimeter (ECAL/HCAL and PRS/SPD) sensitivity is given after a recall of the requirements of the systems. The numbers are given for a AX1000 component based electronics with 512 FPGAs (2 x 256 boards, 16 channels per component) for the ECAL/HCAL and 300 FPGAs (3 x 100 boards) for the PRS/SPD (64 channels per board).

Registers:

Registers		
	TVR (N=1 bit)	HVP (N=4x48=192 bits)
SEU Probability	5.5×10^{-13}	
Flux	420 $s^{-1}.cm^{-2}$	
Reload	1 day	
SEU/Reload/N bits	1.2×10^{-9}	7.3×10^{-6}

Table 6 The SEU rate for registers is given for the two mitigations, TVR and HVP. The TVR rate is evaluated per bit. The HVP rate is given for a 4x48=192 bit table.

ECAL/HCAL

There are two types of registers protected by triple voting:

- constants refreshed on the every day basis:
    - clock front inversion (1 bit / channel)
    - subtraction control switch (1 bit / FPGA)
    - second subtraction scheme value (2 bits / FPGA)
    - No subtraction selector (1 bit / FPGA)
    - L0-latency address (8 bits / FPGA)

The error frequency for those bits is 1.7×10^{-5} per day (see table 6), i.e. once every 484 years[4].

- values updated at 40MHz:
    - counter for the write address in the RAM (8 bits / FPGA)

4 Here, a year is 10^7 seconds and equivalently 120 days.

- L0-Yes position in de-randomiser (4 bits / FPGA)

The numbers of table 6 have to be evaluated for high reload frequency. The error rate obtained is $2.5x10^{-16}$ errors per year. Of course, the reason for such a small number is the constraint that two errors have be in coincidence.

PRS/SPD

The list of necessary registers per half-channel (two parallel integrators) is :

- pedestal (10 bits)
- alpha constant (6 bits)
- threshold trigger (8 bits)

A total of 24 bits per half-channel, so that 48 bits are required per channel and 192 constants are necessary for 4 channels. This is a large number of bits and the HVP technique will most probably be chosen. The error rate evaluation is of 1.3 bit wrong per year (or one every 91 consecutive days).

In this part that concerned register cells, we assumed that the constants were loaded once a day and that no correction was applied on the bits stored. With the mitigation techniques foreseen two bit flips must happen on the same set of data and before any reload to have an impact on the electronics. But, the components may be coded so that when one error bit occurs, it is detected and corrected automatically after 25 or 50ns. Of course, such a system would require more combinatorial cells but the probability to have a second bit error on the same data set and before the correction of the first bit flip is negligible. With the estimated particle flux and coding the AX components this way, our constants would be safely stored at the cost of the use of extra combinatorial cells.

RAM:

SRAM	
SEU Probability	$6.5x10^{-13}$
Flux	420 $s^{-1}.cm^{-2}$
Reload	16μs
SEU/Reload/bit	$4.4x10^{-15}$

Table 7 SRAM SEU rate for a typical reload of the L0 de-randomiser events of 16 μs.

The Calorimeter (ECAL/HCAL and PRS/SPD) will produce $2.9x10^{5}$ bits per event. The error frequency in the L0 de-randomiser will be $1.3x10^{-9}$ at the L1 input, i.e. one event out of $7.7x10^{8}$.

Clock

Clock	
SEU Probability	$3.5x10^{-12}$
Flux	420 $s^{-1}.cm^{-2}$
Clock Upset / Clock	$1.47x10^{-9}$

Table 8 Clock Upset rate per incoming particle and for the LHCb cavern expected particle flux.

With 512 FPGAs, the estimated frequency of clock upset is 2.5 per year (48.5 consecutive days) for the HCAL/ECAL and 1.4 per year (82.8 consecutive days) for the SPD/PRS.

VIII - Control Logic Upset

Finally, the Control Logic Upset is the occurrence of an unwanted power reset that would initialise the registers of the FPGA. We do not have any estimation of the rate of such an upset for AX components, but according to the tests performed at Brookhaven their frequency is lower than the clock upset rate. Moreover, we may think of various ways of detecting them. We could for example spy two registers (protected by TVR) in each chip that would be loaded by a “0” and “1” respectively. A reset and their initialisation would lead to two equal stored values in the registers that could be interpreted as a chip failure. This technique is efficient if the power reset initialises the full FPGA but doesn't permit to identify a power reset that affects only part of the component.

IX - Conclusion

The Actel AX FPGAs are good candidates for the Calorimeter Front-End electronics of the LHCb detector. In this note, studies performed on radiation tolerance in the environment of the cavern, and more precisely in the region of the electronics are shown. No measurement has been done and the results given are extracted from test beams performed both by NASA and Actel. From the cross-section curves they obtained, the resistance of our electronics with respect to Single Event Effects is evaluated.

No major problem is foreseen. We applied safety factor in the evaluation at various stage of the calculation. Nevertheless, only few problems are expected for the whole Calorimeter system (SPD, PRS, ECAL and HCAL). What is called a problem is at most a bit failure in the data stored or in the calibration constants that should be reloaded either every 25ns or every day.

The results obtained in this note lie fully on the measurements done at Brookhaven National Laboratory. The group that performed those tests used ion beams and it would probably be very difficult to extract more data on the AX components than those they obtained. We could simply think of checking that the SEE frequency rate is lower than the one we evaluated here.

References

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