LHCb Calorimeter Front-End Electronics Radiation Dose and Single Event Effects

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Abstract

The LHCb calorimeter front-end electronics will be located above the ECAL / HCAL, i.e. in a region which is not protected from radiations. We present here an estimation of the radiation effect for the electronics and the solutions we investigate to reduce it. Two irradiation tests of the calorimeter front-end shaper have been performed, in June 2001 at the Centre de Proton Thérapie (Orsay) and in December 2001 at GANIL (Caen). The results of the tests clearly show the satisfying resistance of the shaper to SEL.

Contents

1 Introduction

Two types of radiation effects could potentially affect the LHCb calorimeter front-end electronics : cumulative and single event effects (SEE). The former has two contributions:

- Total ionizing dose: the creation of electron-hole pairs in the component degrades its behavior.
- Displacement damage: atoms are displaced from their initial position because of non-ionizing energy losses. The characteristics of the component are progressively degraded.

The SEEs are due to a single incident particle interacting with the component medium. The main manifestations of SEEs are the following:

- Single Event Upset (SEU): the medium energy incident particle breaks a Silicon nucleus and produces a highly ionizing nuclear recoil. The consequences for the component may be bit flips (RAM-FPGA) and modifications of the configurations (FPGA). This problem is solved by a reload of the corrupted bits.
- Single Event Latch-up (SEL): the incident particle breaks a Silicon nucleus. The debris of the reaction trigger a short-circuit in the chip which may be destroyed. The SEL could potentially affect both commercial parts and the calorimeter front-end shaper.
- Single Event Transient (SET): likewise, the incident particle indirectly causes the ionization of a region of the component. Then, charge collection leads to the production of a fake signal in the part.

Section 2 on the following page of this note will be devoted on the evaluation of the flux of particles in the electronics zone. Then, the SEE risks is evaluated for commercial parts, considering the original design (which is not SEE protected) and the available information. In the last section, the results of the front-end shaper irradiation tests performed at CPO (Centre de Proton Thérapie d'Orsay) and at GANIL (Grand Accélérateur National d'Ions Lourds) are given.

2 LHCb environment

2.1 Radiation dose

Radiation doses at the position of the calorimeter crates have already been estimated (see references [1, 11]). The predicted level reaches 100 rad per year and no serious cumulative radiation damage of electronics are expected.

2.2 Particle flux

The only serious problem of concern for the calorimeter electronics is the one of Single Event Effects (SEEs) . The estimation of the SEE risk requires the determination of the particle flux and energy spectra in the region of the front-end electronics. The corresponding curves have been calculated from a Monte Carlo pp interaction sample of 5000 events[1]. The processes selected for the production were QCD processes, as defined by PYTHIA (MSEL=2). They are listed in table 1 together with the cross-sections, as calculated during the generation. The flux has been normalized to a luminosity $L = 5 \times 10^{32}\text{cm}^{-2}\text{s}^{-1}$.

Subprocesses	Cross-Section (mb)
All included subprocesses	101.5
$f + f\prime \rightarrow f + f\prime$	11.12
$f + f \rightarrow f\prime + f\prime$	0.0
$f + f \rightarrow g + g$	0.0
$f + g \rightarrow f + g$	10.74
$g + g \rightarrow f + f$	0.5752
$g + g \rightarrow g + g$	32.79
Elastic scattering	22.21
Single diffractive (XB)	7.151
Single diffractive (AX)	7.151
Double diffractive	9.779
low p_t scattering	0.0

Table 1: Processes generated by PYTHIA (MSEL=2) to evaluate the particle flux in the electronics area of the calorimeter[6].

This value is rather large as the peak luminosity (e.g. at the beginning of a fill) is currently expected to be $2 \times 10^{32}\text{cm}^{-2}\text{s}^{-1}$. Figure 1 shows the particle (π and K mesons, protons and neutrons) flux ($\text{cm}^{-2}.\text{year}^{-1}$) at two depth values along the z direction: 12.30 meters (at the level of the front of the SPD/PS) and 13.32 meters (at the level of the back of the ECAL). The red box gives a rough indication of the crate position ; the black box shows the area (1 meter high and 4 meter wide) located 3.5 m above the proton beam on which the particle flux is averaged to determine the energy spectrum. This last area is

[1]The Monte Carlo sample has been produced by Ivan Korolko who used SICBMC v245r1[6] .

not the rack zone, but it is a region around the point of the electronics where the flux is expected to be the largest (i.e. at the bottom center). Figure 2 shows the obtained energy

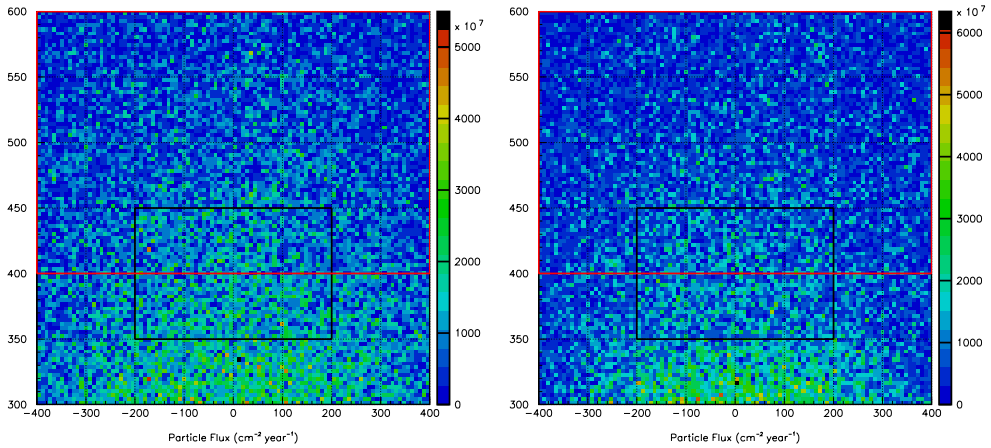

Figure 1: Particle flux ($\mathrm{cm}^{-2} \times \mathrm{year}^{-1}$) in two rectangular areas (left plot at $z = 12.30$ m, right plot at $z = 13.32$ m) above the proton beam (x and y axis in cm). The red box roughly indicates the position of the electronics ; the black one shows the area where the flux has been averaged to produce figure 2.

spectrum for π and K mesons, protons, neutrons at $z = 12.30$ meters. Among the various contributions, neutron's is by far the dominant one below 100 MeV.

A fit has been performed on the total energy spectrum at the two different z depths. The function

$$f(x) = Ae^{-Bx} + Cx^D \tag{1}$$

was used, where the exponential describes the low energy part and the power law corresponds to higher momentum particles. The parameter values are given in table 2 and the curves are showed on figure 2.

parameter	$z = 12.30$ m	$z = 13.32$ m
A	2.2×10^9	1.8×10^9
B	0.27	0.28
C	0.43×10^9	0.49×10^9
D	-0.87	-0.89

Table 2: Fitted parameters for the total energy spectrum evaluated at the two z positions, 12.30 and 13.32 meters. The function used is (1).

Two populations are observed in the electronics region. Low energy particles are isotropic neutrons produced in the matter of the detector. A second population consists of higher energy particles moving forward and produced close to the interaction region.

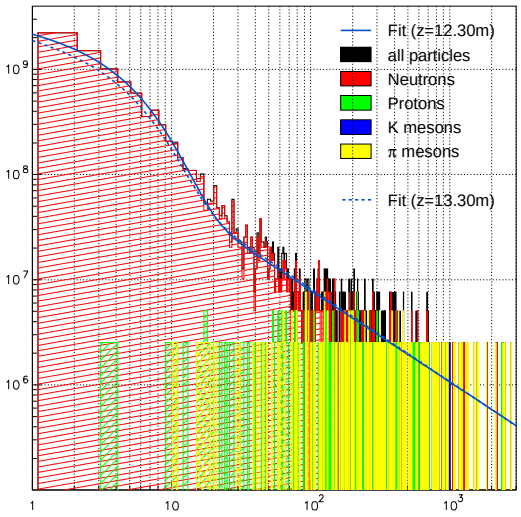

Figure 2: The figures show the particle spectrum ($\mathrm{cm}^{-2}.\mathrm{year}^{-1}.\mathrm{MeV}^{-1}$) in the rectangular region defined on plot 1 (empty black box) and in the text. The histograms have been calculated at $z = 12.30$ meters. The two fits have been performed on the total particle spectra.

3 Estimation of the Single Event Effect risk for commercial parts

The estimation of the SEE rate is a difficult task. Apart from LHC developments, spatial and military research are the only fields that require details about component sensitivity. Some web pages and articles, usually connected with spatial industry provide accessible information on the mostly used components, or describe the results of irradiation tests. We used them to estimate what we can expect at LHCb and to determine the test procedure.

3.1 Single Event Upset rate

3.1.1 High energy neutrons

SEU sensitivity of a component can be described by a cross-section that depends on the energy of the incoming particle, $\sigma_{SEU}(E)$, expressed in $\mathrm{cm}^2.\mathrm{bit}^{-1}$. Both FPGAs and RAMs, can be affected, but the sensitivity of the latter is usually from ten to hundred times larger. Figure 3 gives some examples of SRAM SEU cross-sections (extracted from [4]).

The number of SEU per bit can then be estimated by integrating over the energy the particle energy spectrum times the cross-section

$$N_{SEU} = \int_0^\infty \phi(E)\sigma(E)dE \tag{2}$$

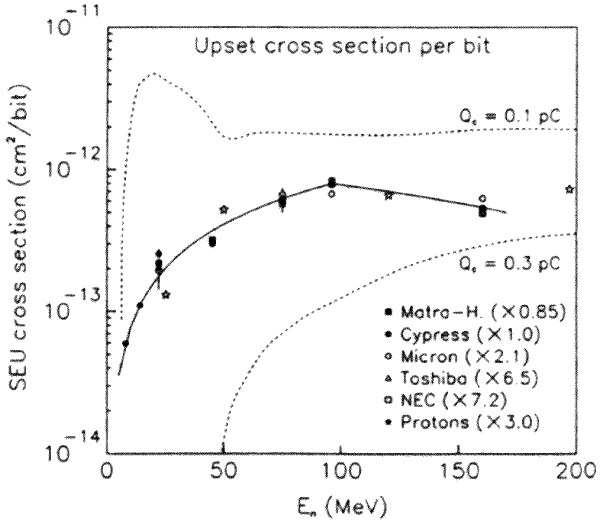

Figure 3: Single Event Upset cross-section ($cm^2 \times bit^{-1}$) for several RAM types and constructors [4].

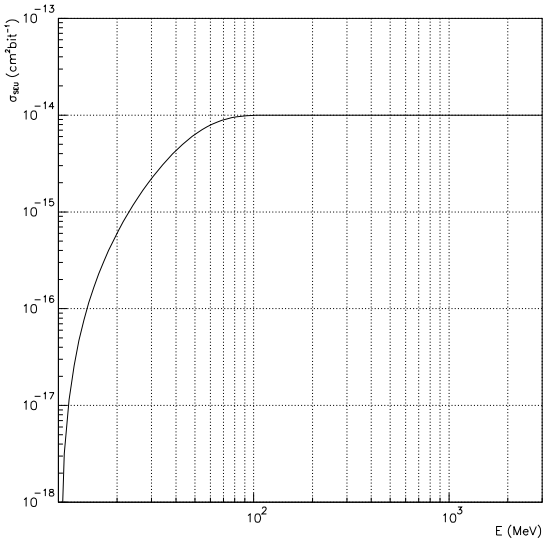

Figure 4: Typical FPGA SEU cross-section variation with respect to the energy of the incoming particle (MeV).

We will use the cross-section function of figure 4 for a typical FPGA and multiply the result by 50 for a RAM. To evaluate the SEU frequency, it is also necessary to evaluate the number of bits for the RAMs and the FPGAs used in front-end board. With the initial design (no SEU immunity):

- FPGA: on average 500 kbits of code per FPGA, 1 FPGA per channel, 32 channels

component	SEU rate ($\text{bit}^{-1}\text{year}^{-1}$)
FPGA	0.40×10^{-4}
RAM	0.20×10^{-2}

Table 3: SEU rate calculated from the flux estimation at $z = 12.30$ m and using the cross-section function from plot 4. The rate is the same at $z = 13.32$ m.

per board.

- RAM(trigger): 4096 values (8 bits) per channel.
- RAM(L0 latency): 160 depth buffer (12 bits) per channel.
- RAM(de-randomizer + L1 latency): 16+1024 depth buffer (14 bits) per channel

which makes a total of 16 Mbit (FPGA), 1 Mbit (RAM trigger), 62 kbit (RAM L0 latency) and 0.5 Mbit (RAM L1 latency). Taking into account the data flow in the L0 and L1 latencies (100 MHz and up to 100 kHz) and the SEU frequency estimated (0.2 $\text{bits}^{-1}\text{year}^{-1}$), the proportion of bits corrupted out of the total amount of bits transported is very close to zero. It is important to keep in mind that the data stored every 25 ns in the latencies are used for one unique event. On the contrary, trigger RAM are LUT and any SEU corrupts all the events until reload. Thus, the latencies can be neglected in the evaluation of the SEU rate. In the same spirit, the effect of an error on a bit will depend on the corrupted bit: a low weight error won't change any measurement. In this note, whatever the bit weight, an error means corruption of the full information.

The total SEU rate per board would reach 640(FPGA)+2000(RAM)=2640 SEU per board per year[2], which means one every 4 minutes per crate or every 15 seconds for the whole ECAL/HCAL front-end electronics.

To reduce SEU effects several methods are possible:

- FPGA configuration: the use of standard FPGA (Altera, Xilinx, ...) seems a hard task in an environment like ours. Xilinx provides a series of products that can be (partly) reloaded while in use. Still, the interval between the occurrence of the SEU and the reloading of the configuration should be considered as a dead-time. The foreseen solution consist of using Actel Anti-fuse FPGA. The characteristics of this component is that the routing is burned in the chip and can't be modified neither by the user (no flexibility) nor by a SEU (SEU immunity). However, it contains flip-flops that must be protected (probably by a triple voting technique) and we can expect *a priori* both SET and SEL (see section 3.2) to occur with this type of component.
- RAM: could be protected by parity bits which are stored with the original information so that one error is detected and corrected, and two errors are detected (the corresponding data being automatically rejected).

These solutions will be tested in the future during irradiation tests.

[2]Taking into account the LHC running expectations, an effective year is defined as 10^7 seconds.

3.1.2 Low Energy neutrons

Recent studies showed that thermal and fast neutrons can trigger SEU with a relatively high rate [3]. The ionizing fragment is produced by the reaction of neutrons on boron B^{10}. Natural Boron is present as a dopant in the semi-conductors and is made of 80% B^{11} and 20% B^{10}. The fragments of the reaction are alpha particles and Li^7 leading to a LET of 1 or 2 MeV/mg.cm^2. These values are high enough to produce SEU in SRAMs.

3.2 Single Event Latch-up and Single event Transient

It is not possible to get SET or SEL rates from the available information. But it is possible to be helped by heavy ion beam data[7].

The Actel SX32A 'Anti-Fuse' that is the SEU immune FPGA solution foreseen in the previous section has been tested in various situations and with Linear Energy Transfer (LET) from 11.4 to 74.7 MeV.cm^2.mg^{-1}[8, 9]. Four types of configurations were defined:

1. Chain of 100 flip-flops (SEU sensitive).
2. Chain of 100 flip-flops (SEU sensitive) with buffers (SET sensitive) in between two consecutive flip-flops.
3. Chain of 300 flip-flops programmed as a chain of 100 triple voting protected blocks.
4. Chain of 100 triple voting protected blocks with buffers (SET sensitive) in between two consecutive blocks.

Two technologies have been used for tests: 0.22 and 0.25 μm.

The following conclusions can be extracted from the obtained measurements:

- Whatever the configuration, no SEL was recorded during the irradiation periods whose total fluence was 1.7×10^8 particles at LET ranging from 11.4 to 74.7 MeV.cm^2.mg^{-1} (800 flip-flops).
- SEU have been seen with the four configurations and in comparable amount (figure 5 shows the total error cross-section for the two first configurations and for two technologies, 0.22 and 0.25 μm).
- The triple voting technique proved to be fully efficient. Although SEU occurred with the last two setups, they have been identified and corrected by the triple voting method successfully. No SEU remained after correction.
- Configurations 2 and 4 detect SET, but the sensitivity of the last one is even enhanced. In setup 2, a SET can be triggered by a glitch during a clock beat. In setup 4, a sufficient transient can be caught by a flip-flop independently of the clock[3]. After

[3]In setup 2, the output of the buffer is connected to the data flip-flop input which is written and read at clock beat. In setup 4, the buffer output is connected to the presets and clears of the flip-flops.

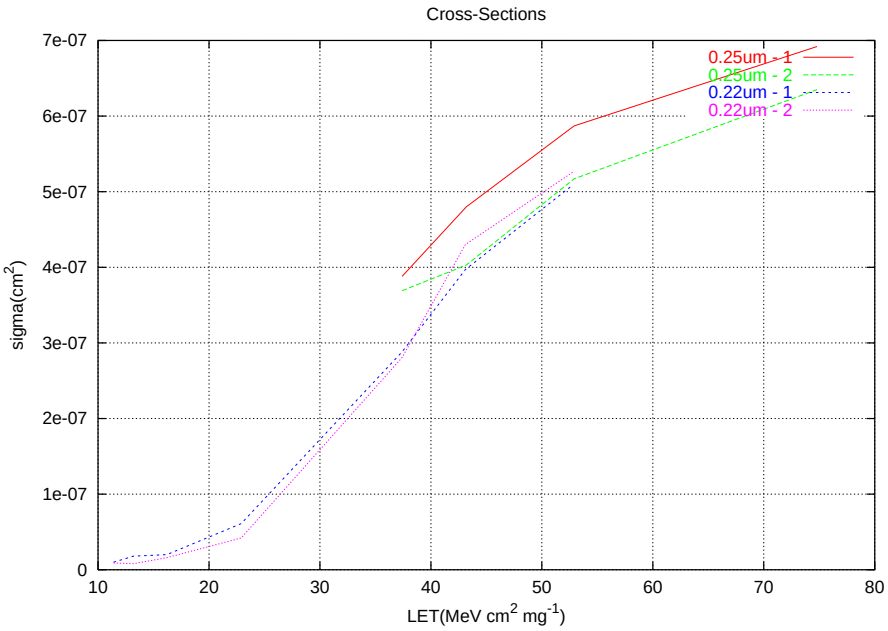

Figure 5: Error (SEU+SET) cross-sections measured with the configurations 1 and 2 defined in the text. Two technologies (0.22 and 0.25 μm) have been used (compilation of results from [8, 9]).

triple voting correction of the SEU, no SET have been identified with configuration 4.

- A small increase of the number of errors is noticeable between configurations 1 and 2 in technology 0.25 μm. This difference vanishes for technology 0.22 μm and it is difficult to associate it to a SET induced increase of the errors.

Other irradiation tests have been performed with SX-AS Space Application Actel FPGA and showed a small SET cross-section for these types of components. However, if we want to compare the LHCb environment with these irradiation tests, we need to know the LET we can expect at LHCb, i.e. what is the dE/dx of the neutron-Si^{28} interaction nuclear recoil capable of producing a SEU. Simulations [5] suggest that we can expect the fragments to have an energy rarely exceeding 10 MeV, with atomic numbers Z greater than 10 and a limited range below 10 μm (see figures 8 and 10).

The corresponding dE/dx, scaling as Z^2 is roughly of 30 GeV $\times$ cm^{-1} and leads to a LET of 15 MeV $\times$ cm^2 $\times$ mg^{-1}. Let's recall that no SEL and anti-fuse rupture was detected below 74.7 MeV$\times$cm^2$\times$mg^{-1} in the tests described above and performed on Actel SX32A components. For completeness, we mention that during recent experiments done at Brookhaven, SEL were detected on Actel anti-fuse SX16A components[10]. Moreover, whatever the component considered we cannot reject the possibility of SET. There exists some ways of limiting their occurrence and an electronics board based on Actel anti-fuse component will be designed to estimate more precisely their frequency.

4 Irradiations of the Calorimeter front-end shaper

In the previous section the SEE risks was presented for commercial components. Although they are not concerned by SEU, analogic chips can potentially be affected by SEL. Two irradiation tests have been performed in June 2001 at CPO and in December 2001 at GANIL on the Calorimeter front-end shaper to evaluate the sensitivity of the chip.

4.1 Irradiation at the Centre de Proton Thérapie

The Centre de Proton Thérapie at Orsay is an institute for the treatment of patients suffering from cancer. The cells located in the brain or in the eye are killed by an intense proton beam. This type of treatment has the advantage of making the most of the Bragg peak of the particles : the energy deposition is limited to the tumor region and avoids irradiation of healthy tissues.

The conditions of the test were a flux of $10^8 \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and a kinetic energy of 200 MeV. The diameter of the beam was 4 cm. Assuming that a 200 MeV proton deposits 4 $\mathrm{MeV.mg}^{-1}.\mathrm{cm}^2$, the dose accumulated reaches 6.5 $\mathrm{rad.s}^{-1}$. The setup is shown on figure 6 with a description of the system. The measurements performed during the irradiation were :

- pedestal runs (no input signal),
- calibration runs : a signal is generated on the board and injected at the signal input,
- front-end shaper current measurements.

A SEL should manifest itself by a large increase of the current of a chip. In the same time, a malfunction should be detected from pedestal and/or calibration runs. During the irradiation and in spite of the duration of the test, we observed

- no variation of the supply currents of the chips,
- no variation of the signal noise,
- no variation of the recorded calibration signal.

If we suppose that the SEL cross-section has the same shape as the SEU cross-section showed on figure 3, a year of data taking with LHCb is roughly equivalent to 40s of test at CPO. This equivalence is extracted from the integration of the LHCb neutron flux spectra. A summary of the irradiations for the four tested chips is given in table 4.

The dose accumulated (from 10.7 to 22.6 krad) was by far larger than what we can expect in 10 years of functioning of the detector. A total of 220 years[4] has been tested without any SEL.

The four chips have since been thoroughly tested on the LAL test bench. The following points have been looked at :

[4] A year is 10^7s.

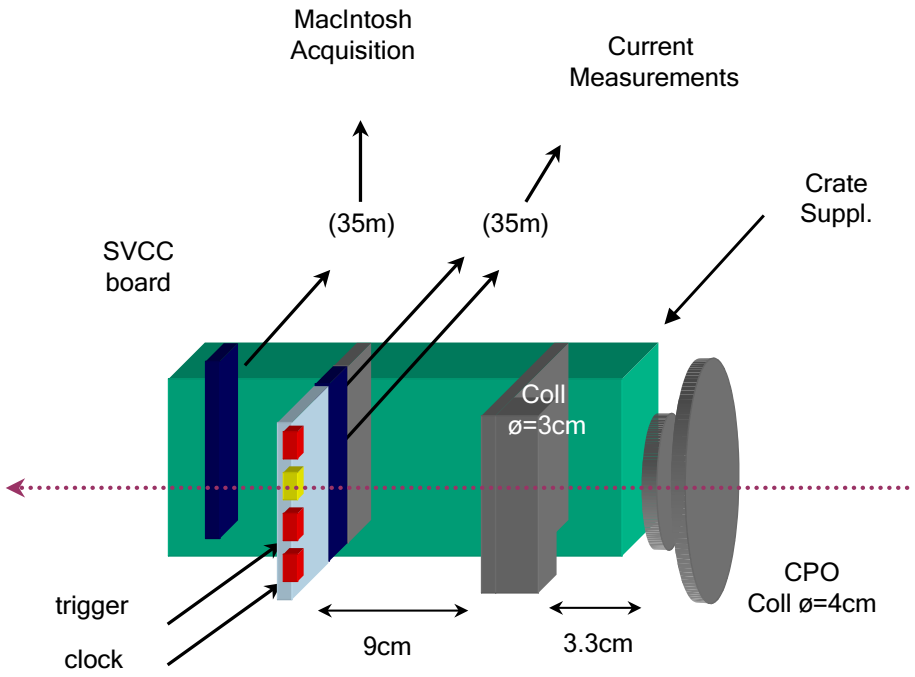

Figure 6: Schematics of the shaper irradiation test at CPO. The color code chosen is the following : the crate is in green, the inactive parts (collimators, extension board) are in gray, the tested electronics is in red and yellow (yellow for the chip presently showed in the beam) and the sensitive electronics for the acquisition is in dark blue. The dotted magenta line is the proton beam. The height of the crate was adjustable so that the four chips could be presented to the beam. Two signals (40MHz clock and trigger) were brought to the board. The acquisition was performed by the front-end board itself and by a SVCC board located in the same crate. To move the acquisition electronics away from the beam the front-end board was plugged on an extension.

Component	Duration (s)	Dose (krad)	SEL equivalent (year)
1	3479 (~ 1h)	22.6	87
2	1643 (~ 1/2h)	10.7	41
3	1896 (~ 1/2h)	12.3	47
4	1800(~ 1/2h)	11.7	45

Table 4: Irradiation duration, dose accumulated and SEL equivalent (a year is supposed to be 10^7s) for the four tested front-end shapers.

- output buffer/integrator tensions,
- rise/fall time of the integrator,
- output signal plateau,
- linearity,

- crosstalk,
- noise.

The four chips have the same characteristics after the test as before the irradiation and are still used.

In spite of the good results obtained, it is important to notice that the sample is very limited. 2500 chips will be functioning on the calorimeters, and 220 years for one chip is roughly 10 days for the electromagnetic and hadronic calorimeters. Although the result was very encouraging, this limitation was the motivation for an irradiation at GANIL.

4.2 Irradiation at GANIL

GANIL (Grand Accélérateur National d'Ions Lourds) is an accelerator located at Caen in Normandie, whose purpose is to provide heavy ion beams reaching energies up to 90 MeV/A for nuclear physics experiments. At CPO, the incident particles interact with the Silicon nucleus and produce a ionizing fragment capable of triggering a SEL. At GANIL, the incident particle is the ionizing fragment which explains the efficiency of the test. The conditions of the last run of year 2001, Krypton at 58 MeV/A, were particularly well-adapted to our requirements which was to deposit in the chip a LET equivalent or slightly larger than what we could indirectly get with neutrons at LHCb, i.e. roughly 15 MeV.mg^{-1}.cm^2. We had three hours at our disposal for the test and we divided that time interval in two periods. During each period two chips were simultaneously irradiated, each period being divided into four runs corresponding to four different deposited LET. Between two consecutive runs, the LET was modified by introducing different layers of Aluminium between the vacuum pipe aperture and the irradiated chips. Four chips have been used during the test: two during the first period and two during the second one. The run conditions of the two periods and the accumulated fluences are given in table 5.

Run	Al Thickness (μm)	LET (MeV.mg^{-1}.cm^2)	Fluence (cm^{-2})	
			Period 1	Period 2
1	0.	11.4	2.4×10^7	2.4×10^7
2	250	13	2.4×10^7	3.0×10^7
3	500	15	2.4×10^7	2.3×10^7
4	750	20	2.4×10^7	2.4×10^7

Table 5: The run conditions for the two periods with the corresponding fluences and LET.

The tension and the current of the power supply were monitored continuously in order to detect any SEL. No variation of these parameters has been noticed except for a slow and even increase from 43 mA to 52 mA of the current of the supply during the run 4 of the second period. After shutdown of the ion beam, the current slowly returned to a nominal value. This phenomenon doesn't appear to be the consequence of a SEL, but is more

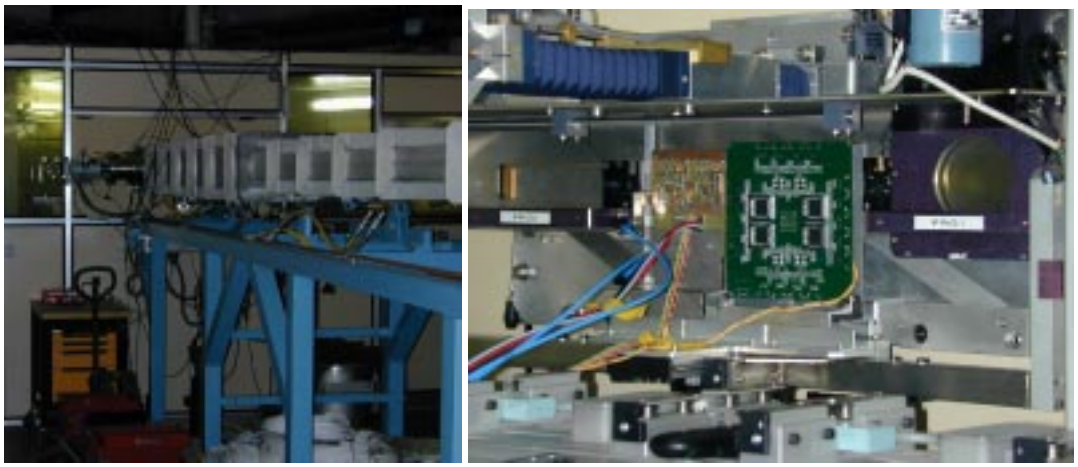

Figure 7: The picture on the left shows the vacuum pipe in the experiment hall. The pipe ends in the room in the background and is closed by an inox window. The picture on the right is taken from in the inside the room and shows the tested boards facing the inox window. Two boards are visible : the one on the left supports two front-end shapers for the ECAL and the HCAL. The one on the right (large green board) is the PRS front-end board (LPC, Clermont-Ferrand).

certainly due to the accumulated dose which reached 23 and 24 krad for the chips of the period 1 and 2 respectively (see table 6). As for the CPO test, the irradiated components

Run	Accumulated Dose (krad)	
	Period 1	Period 2
1	4.4	4.4
2	9.4	10.7
3	15.2	16.2
4	22.9	23.9

Table 6: Accumulated dose (krad) at the end of each run of the two periods.

characteristics have been carefully measured on a test-bench at Orsay and still fulfil the specifications.

We now interpret the results obtained at GANIL in terms of the sensitivity of the shaper to SEL. To produce a latch-up, we assume first that the ionizing particle should at least deposit 6 MeV.mg^{-1}cm^2 ($\sim$ 1.5 MeV.μm^{-1}), value that is slightly above the LET threshold to trigger a SEU in a standard commercial part. Only fragments heavier than nitrogen can reach such a LET, moreover their kinetic energy should be greater than 1 or 2 MeV (see picture 8,[2]). The probability to produce such an ion from neutron-Silicon collisions is below 10^{-7} μm^{-1} (see picture 9). Taking into account the SEL sensitive thickness of the component that is evaluated to 10 μm and summing up over the various ion species that can be obtained by collisions, the total probability to get a ion capable of triggering a SEL

reaches 2×10^{-6}. If the active thickness is smaller than 10 μm, then the limiting factor that must enter the total probability evaluation is the range of the ion which is of the order of 10 μm or below (see picture 10). Thus, the previous estimation is rather conservative. Out of the incident neutrons only a small proportion have the potential to produce a SEL.

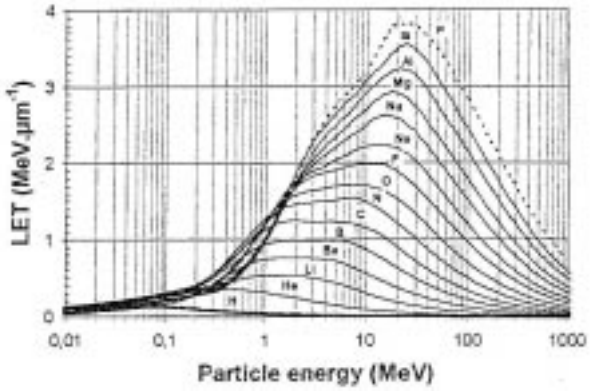

Figure 8: LET of several ions which can be produced by neutron-Si collisions with respect to their kinetic energy. Only ions heavier than nitrogen can have a LET greater than 6 MeV.mg^{-1}.cm^2 (1.5 MeV.μm^{-1}). The maximum LET that can be reached with Silicon fragments is 15 MeV.mg^{-1}.cm^2[2].

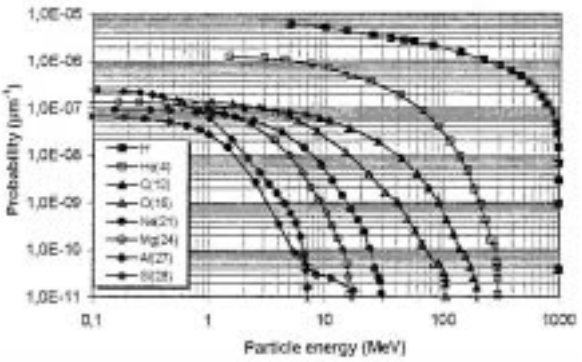

Figure 9: Probability (μm^{-1}) to produce a fragment with a energy greater than x MeV from neutron-Si collisions. Here, the incident neutron energy is 1 GeV[2].

Let's define the total *sensitive* area s_{SEL} of the component and the area s_{Kr} affected on average by an incoming krypton ion. If these areas are expressed in proportion of the total active surface of the chip, the probability that an incoming ion doesn't hit a sensitive zone is $1 - s_{SEL} - s_{Kr}$. From the actual number of SEL detected, 95%CL exclusions contours can be drawn in the $[s_{SEL}, s_{Kr}]$ plane (see picture 11).

At GANIL, no SEL was detected and two regimes are identified :

- $s_{Kr} > 10^{-8}$ regime : the component has been completely scanned by Krypton and no SEL sensitive zone (at $LET \leq 15$ MeV.mg^{-1}.cm^2) exists.

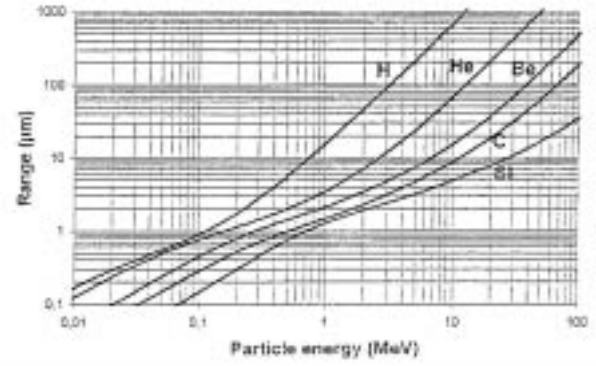

Figure 10: Ranges (μm) of several types of ions with respect to their kinetic energy[2].

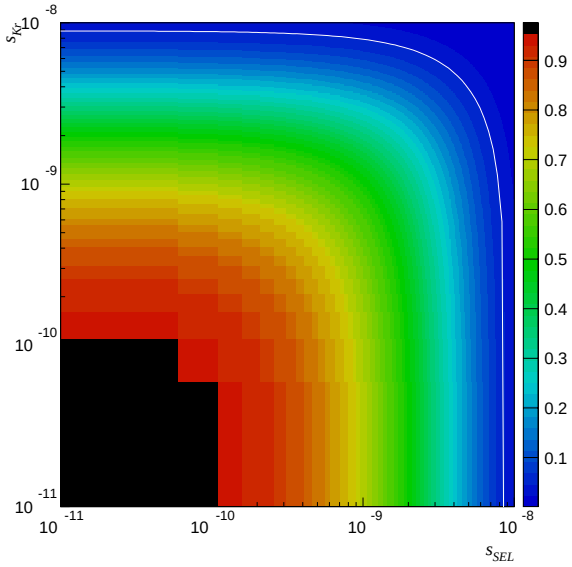

Figure 11: The $[s_{SEL}, s_{Kr}]$ plane is shown with the corresponding probability not to have seen any SEL with the front-end shaper. The white line is the 95%CL Exclusion contour in the $[s_{SEL}, s_{Kr}]$ plane.

- $s_{Kr} < 10^{-8}$ regime : only part of the component has been scanned and if the sensitive area is smaller than s_{Limit} it may have escaped scanning. From picture 11, $s_{Limit} = 8.9 \times 10^{-9}$ at 95%CL.

Whatever the *true* regime, the most conservative is the second one and we keep the pessimistic statement that the SEL sensitive zone of the shaper is less than 8.9×10^{-7}% of its active surface. Hence, the probability to trigger a SEL with a Krypton ion is below 8.9×10^{-9}. The probability to produce an ion with a LET greater than 6 MeV.mg^{-1}.cm^2 was estimated to 2×10^{-6}. Thus, the probability to trigger a SEL with neutrons reaches a

maximum limit of 1.8×10^{-14}. The flux of neutrons above 30 MeV[5] is 4×10^9 years^{-1}.cm^{-2} and is calculated by integrating the spectrum of picture 2. If we assume that the probability to produce a heavy and energetic enough ion is the same at 1 GeV (value at which it was initially evaluated) and at lower incident neutron energies, the equivalent resistance of the chip is greater than 14 thousand years per chip (see table 7).

Component	# SEL	Cumul. time (s)	s_{Limit} 95% CL	s_{min} 95% CL	SEL resistance ($year.chip^{-1}$)
Shaper	0	16000	8.9×10^{-9}	-	>14000
RAM	0	4000	3.9×10^{-8}	-	>3205
Serialiseur 215	2	2521	1.3×10^{-7}	4.0×10^{-8}	>961
Serialiseur 216 (drv)	9	1682	5.0×10^{-7}	1.3×10^{-7}	>250
Serialiseur 483	7	2254	3.1×10^{-7}	5.7×10^{-8}	>403
Serialiseur 484 (drv)	13 (?)	13 (?)	8.1×10^{-5}	2.7×10^{-5}	>1.5 (?)

Table 7: Results of SEL resistance obtained from GANIL measurements. s_{Limit} is explained in the text. s_{min} is the minimum size of the sensitive area compared to the total silicon surface of the component. This last parameter can be extracted only when SEL really occured. The assumed probability to produce a sufficiently ionising ion from Silicon-neutron interacton is 2×10^{-6} and the value taken for the neutron flux is $4.0 \times^9 \text{cm}^{-2}.\text{year}^{-1}$. The last component tested (last row) suffered almost instantaneous SEL when in the beam, so that the resistance time interval was difficult to estimate. This is emphasized by the question marks added for this row.

This second test is by far more powerful than the CPO test and clearly proves the SEL resistance of the ECAL/HCAL front-end shaper.

Several digital components, that are good candidates to be used on the front-end board of the LHCb calorimeters, have also been tested at GANIL in the same conditions as for the front-end shaper. These components (RAM, Serialiseur) will suffer a CPO radiation test in 2002. Then, a note will synthesize both GANIL and CPO measurements. However, the SEL resistance already extracted at GANIL for digital parts is given in table 7 together with the results obtained for the front-end shaper.

[5]We make the assumption that a neutron must have at least 30 MeV to produce a sufficiently ionizing ion. This is motivated by the fact that only a small fraction of the energy of the neutron is given to the heaviest fragment of the collision neutron-Si. The same threshold for SEU is estimated to be around 20 MeV.

5 Conclusion

The front-end electronics of the LHCb electromagnetic and hadronic calorimeters will be located in a region where the dose will be limited and no serious cumulative radiation damage is expected in 10 years. However, the flux of particles and especially of neutrons in this area will be high enough to trigger Single Event Effects. The use of mitigation techniques such as triple voting and of special anti-fuse digital components is necessary to prevent frequent corruption of data by Single Event Upsets and Transients and temporary or permanent malfunction by Single Event Latch-up. The analogic front-end shaper developed at LAL could also be sensitive to latch-up. Two successful radiation tests have been performed, at the Centre de Proton Thérapie (Orsay) and at GANIL (Grand Accélérateur National d'Ions Lourds, Caen), and proved the ability of the component to resist the flux of particles expected in the LHCb cavern.

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