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Coordinator's name		ARNAUD Nicolas			
Acronym		SUPERB-PID			
Titre de la proposition de projet		Identification de particules chargées avec un détecteur Cherenkov innovant pour l'expérience SuperB			
Proposal title		Charged particle identification with an innovative Cerenkov detector for the SuperB experiment			
Evaluation committee		SIMI 4 – Physique			
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DOCUMENT SCIENTIFIQUE

 Pro 	PPOSAL ABSTRACT	3
	NTEXT, POSITIONNING AND OBJECTIVES OF THE PROPOSAL	
2.1.	Context of the proposal	
2.2.	State of the art and positionning of the proposal	
2.3.	Objectives, originality and/ or novelty of the proposal	
3. Scii	ENTIFIC AND TECHNICAL PROGRAMME, PROPOSAL ORGANISATION	
3.1.	Scientific programme, proposal structure	10
3.2.	Description by task	
3.2.1	Task 1 : Management	11
3.2.2	2 Task 2 : CRT tests	11
3.2.3	B Task 3 : Electronics design	13
3.2.4		17
3.2.5		18
3.2.6		19
3.2.7		19
3.2.8		20
3.3.	Tasks schedule, deliverables and milestones	21
4. Dis	SEMINATION AND EXPLOITATION OF RESULTS, INTELLECTUAL PROPERTY \dots	23
5. Con	NSORTIUM DESCRIPTION	23
5.1.	Partners description and relevance, complementarity	23
5.2.	Qualification of the proposal coordinator	
5.3.	Qualification and contribution of each partner	
6. S CII	ENTIFIC JUSTIFICATION OF REQUESTED RESSOURCES	26
7. A NN	IEXES	29
7.1.	References	29
7.2.	CV, resume	
7.3.	Staff involvment in other contracts	



DOCUMENT SCIENTIFIQUE

1. Proposal abstract

This ANR proposal aims at contributing strongly to the **design of the 'Focusing Detector of Internally Reflected Cherenkov light'** (**FDIRC**), a key component of the SuperB detector dedicated to the identification of charged particles (PID). The SuperB experiment has recently been approved by the Italian government as a 'flagship project' within a multiannual funding plan.

The proposal is coordinated by a LAL-Orsay physicist and gathers participants (physicists, engineers and technicians) from CNRS-IN2P3 laboratories (the LAL and the LPNHE-Paris), from the SLAC National Accelerator Laboratory (DOE) and from the Maryland University. Its various tasks described in details in the following cover all the main aspects of the FDIRC design:

- tests of various detector components (including the FDIRC layout itself) in test benches and at the SLAC Cosmic Ray Telescope (CRT) facility
- design of the front-end electronics
- simulation and reconstruction of the data; study and mitigation of the background
- integration and finally installation of the FDIRC into the SuperB detector.

Various R&D activities are needed to fulfill the FDIRC requirements: this detector must be at least as powerful and reliable as the BaBar DIRC (both detectors are based on the same principle) while working in harder conditions as the SuperB instantaneous luminosity is expected to exceed the BaBar one by a factor of ~100. A key part of this proposal is the innovative design of the FDIRC front-end electronics which are expected to provide a very good timing resolution (around 70 ps) while bearing a 1 MHz rate per channel. These new boards will be extensively tested in test benches (where high background conditions can be simulated by using a laser as light source) and at the CRT where they will readout actual signals generated by energetic cosmic muons in a full-scale prototype of 1/12th of the FDIRC. Currently, electronics fulfilling these strict requirements do not exist.

Computing-related activities are another pillar of this ANR proposal. First, one will have to simulate the various CRT test layouts, in order to make sure that their data are understood and can be used to extrapolate the behavior of the final FDIRC. Then, that device needs to be simulated properly as a part of the SuperB detector operating in a very high luminosity ($10^{36} \, \mathrm{cm}^{-2} \, \mathrm{s}^{-1}$) environment where the background can potentially be very high. Backgrounds which could impact the data taking or lead to an accelerated ageing of the FDIRC will have to be mitigated.

Finally, the reconstruction code used to convert the FDIRC raw data into PID quantities useful for physics analysis is a fundamental aspect of this proposal. The final resolution of the FDIRC detector will depend on the way ambiguities in the photon paths or distortions of the Cherenkov rings (emitted by charged particles crossing the FDIRC quartz bars) are taken into account. State-of-the-art analysis methods (multivariate analysis, maximum likelihood, etc.) will be used in the FDIRC reconstruction code which will have to be written from scratch to fit optimally in the new SuperB computing framework.

With this ANR proposal, we request manpower (a postdoc for 4 years) and funds, mainly for the front-end electronics design and for frequent trips to the SLAC CRT and to the future SuperB experiment site. More than 3.5 FTEs of permanent staff will support the proposal and help the postdoc funded by the ANR to reach these ambitious goals.



DOCUMENT SCIENTIFIQUE

All the participants to this ANR proposal have been involved in the successful operations of the BaBar DIRC for years. They are used to work together which should ensure a fruitful collaboration during the four years of the proposal. Clear deliverables culminating with the successful installation of the FDIRC into the SuperB detector have been identified for each task and regular reports will be provided, in addition to the presentation of our results inside the SuperB experiment and to the particle physics community.

2. CONTEXT, POSITIONNING AND OBJECTIVES OF THE PROPOSAL

SuperB is a particle physics experiment which aims at collecting an unprecedented amount of data to test very accurately the Standard Model (SM) and probe various scenarii of New Physics (NP). This "precision physics" project, which has been recently approved by the Italian government within a multiannual funding program [1], will start taking data around 2016 and is complementary with the LHC "discovery" experiments whose results will certainly boost in the near future our knowledge of the elementary particles and of their interactions.

To reach these ambitious scientific goals, each component of the SuperB detector has to be properly designed, carefully built and optimized in order to keep a high level of performances during the 5+ years of operation of the facility. In addition to showing excellent vertexing, tracking and calorimetry capabilities, SuperB will need a very good charged particle identification (PID), in particular a powerful separation between kaons and pions with momenta up to a few GeV/c. This ANR proposal is focused on the innovative Cherenkov detector which is currently being designed within the SuperB PID group to fulfill this requirement: the 'Focusing Detector of Internally Reflected Cherenkov light' (FDIRC). **The duration of this ANR proposal (4 years) will allow us to follow the main aspects of the FDIRC development**: optimization of the design; tests of full-scale prototypes; design of the readout electronics; writing and optimization of the data taking and reconstruction algorithms; study of the FDIRC robustness against the backgrounds expected at a very high luminosity collider like SuperB.

Finally, we expect to be able to contribute to the FDIRC installation into the SuperB detector during the final year of this ANR proposal.

Physicists, engineers and technicians from four laboratories:

- the Laboratoire de l'Accélérateur Linéaire (CNRS/IN2P3 and Université Paris Sud XI, http://www.lal.in2p3.fr), home institution of the coordinator of this ANR proposal
- the Laboratoire de Physique Nucléaire et de Hautes Energies (CNRS/IN2P3 and Universités Paris VI and Paris VII, http://www-lpnhep.in2p3.fr)
- the SLAC National Accelerator Laboratory, http://www.slac.stanford.edu)
- the Maryland University SuperB group

will participate to this ANR proposal which should lead to a collaboration as fruitful as the one which has been existing among these groups for the BaBar DIRC for more than a decade.

Should this proposal be accepted by the ANR, we would like to start the work on July 1^{rst} 2011.

2.1. CONTEXT OF THE PROPOSAL

In the previous decade, the first generation B-factories (BaBar at the SLAC National Accelerator Laboratory in the USA and Belle at the KEK laboratory in Japan) have been very successful: very



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large amounts of data (about 500 fb⁻¹ for BaBar and in excess of 1 ab⁻¹ for Belle) have been recorded and these huge datasets have been extensively analyzed to produce important physics results. The BaBar+Belle scientific harvest includes the confirmation of the validity of the CKM mechanism – which describes the quark mixing and the CP violation in the SM – but is not limited to this achievement, which was the original goal of these two experiments. Among their various discoveries one can name the D⁰ mixing, the observation of direct CP violation, the discovery of new charmonium and bottomonium states, etc.

This new decade started with the promising startup of the LHC accelerator whose luminosity is increasing steadily and rapidly. The general purpose ATLAS and CMS experiments such as the flavor-physics-oriented LHCb experiment are scanning a new and wide energy range, testing the SM and looking for experimental signatures of NP. The second generation B-factories (of course SuperB but also the Belle-2 project in Japan) have similar goals but a very different approach. Running at a fixed low energy (most of the time around 10.6 GeV, the mass of the Y(4S) resonance), they plan to accumulate between 50 and 100 times more data than the first generation experiments and to use these huge datasets to make very precise measurements or to look for extremely rare decays. These measurements will be sensitive to NP through virtual loop corrections and will provide some information complementary to the LHC results.

Following its long and constant involvement in BaBar (from its design in the early 1990's until the analysis of the full dataset which are still ongoing), the BaBar group from the "Laboratoire de l'Accélérateur Linéaire" (LAL) has been part of the SuperB project since the idea of building a very high luminosity asymmetric e⁺e⁻ collider was first presented a few years ago. It was also involved in the upgrade of the DAFNE collider at Frascati in 2007-2009 during which a new design of the interaction region was tested. This "crab waist sextupole compensation scheme" was considered as a key part of the SuperB accelerator proposal whose ambitious goal is to reach an instantaneous luminosity of 10^{36} cm⁻² s⁻¹. Therefore, the success of its implementation at DAFNE (proven in particular by the luminosity measurements [2,3] made by the LUMI collaboration of which the LAL group was a member) certainly played a major role in the approval decision of SuperB by the Italian government.

Now that the SuperB project has been approved, the LAL group wants to increase its already important contribution to the PID group by taking various responsibilities on the FDIRC, the detector which will provide the main K/π separation in the SuperB barrel region – that is in the $[\sim 25^{\circ}; \sim 150^{\circ}]$ polar angle range. This ANR proposal is needed to support our involvement, in terms of manpower, money and material. As SuperB is still a relatively new project, the size of the collaboration is currently quite small. Therefore, there are several interesting challenges to be taken up – both from the technological and physical standpoints – and this is the time to tackle them, while increasing the size and impact of the LAL group and acquiring new skills. Moreover, increasing the size of the groups in charge of key aspects of the SuperB detector – among which the barrel PID – has been identified as a priority for the new collaboration in 2011.

To clarify our funding requests, we would like to stress out that Italy will provide money for the SuperB accelerator and all the related facilities and services. Money for the detector – and in particular for all detector R&D activities – should come from other sources. We are submitting this ANR proposal to get part of the money needed to turn the FDIRC into reality. Other groups and institutions will contribute to this effort; for instance, we will use computing resources provided by our institutions (in particular by SLAC where the CRT data will be located), by various (CC-IN2P3, GRIF and CNAF) grid infrastructures and by the SuperB collaboration.

2.2. STATE OF THE ART AND POSITIONNING OF THE PROPOSAL

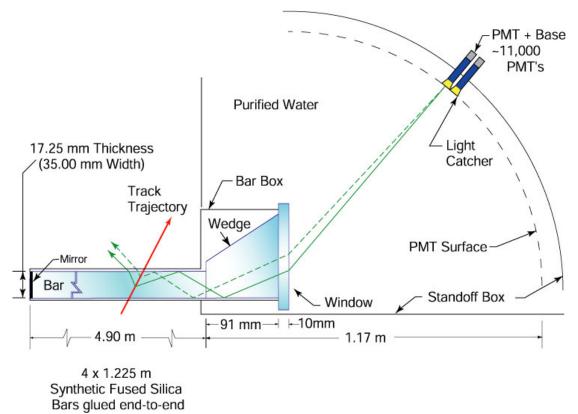


Fig.1: schematic of the BaBar DIRC.

When charged particles coming from the interaction point or produced by the decays of the e⁺e⁻ collision products reach the radius at which the DIRC is located, they cross quartz bars in which they produce Cherenkov light. Trapped by internal reflection, part of these photons propagate into the bar until its exit window where they enter a large volume of ultra-pure water. The inner surface of the tank is a huge array of photomultipliers (PMTs) which detect the photons. The time and position of the PMT hits are gathered with tracking information to separate signal and background photons and to compute the Cerenkov angle, finally allowing one to estimate the masses of the various particles – and hence their types.

The DIRC ("Detector of Internally Reflected Cherenkov light", see Fig.1) has been a very successful component of the BaBar detector [4]. During the whole data taking period (1999-2008), this innovative device showed a very high duty cycle and its high-quality performances were not impacted much by ageing nor by the background (which increased with the PEP-II collider luminosity, which finally exceeded its design value by a factor of 4). Therefore, it is obvious to foresee a similar detector for SuperB [5,6], all the more that the DIRC quartz bars, protected by the detector design and carefully monitored over the whole BaBar experiment are still in excellent shape¹.

ANR-GUI-AAP-04 – Doc Scientifique 2011

¹ No loss of performances attributed to the quartz bars has ever been observed in the BaBar data. Moreover, last Fall, the 144 quartz bars of the DIRC have been removed from the BaBar detector by a SLAC team, with contributions from the BaBar IRFU and LAL groups. A visual exam of their front faces has been very satisfactory and the bars are now safely stored in a closed container where Nitrogen is continuously circulating to prevent moisture.

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Yet, while the photon production and transport in the bars can be kept unchanged, the camera has to be modified for SuperB. Indeed, in BaBar, the optical coupling medium was ultra-pure water. A dedicated water plant had to be built and operated in order to purify the water running in closed circuit. Moreover, the experiment was always very concerned about possible leaks between the 6,000 liter tank and the rest of the detector. Moisture around the DIRC was carefully monitored and an automated dump system was designed to empty the big tank in a few minutes, should water be detected outside it. Finally, this large volume was a source of background for BaBar (for instance neutrons could interact with the H_20 molecules) and the situation would be much worse in SuperB as the luminosity is expected to be 100 times higher.

Therefore, the FDIRC camera is a block of solid fused silica, the FBLOCK. Two mirrors will guide the photons to a plane instrumented with multi-anode photomultipliers (MaPMTs). The reduced camera size (~1/10th of the DIRC one) and the fast MaPMTs will provide headroom for background and the goal is to achieve an overall Cherenkov angle resolution at the level of or better than what we had in BaBar. Fig. 2 shows the current schematic of the SuperB FBLOCK.

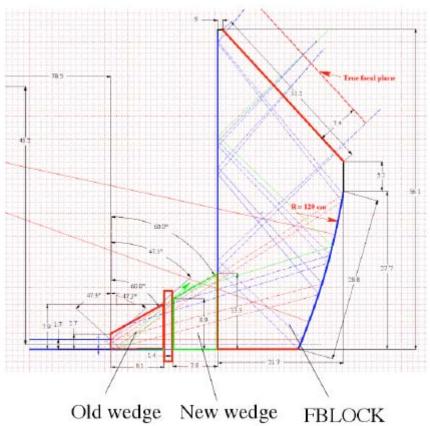


Fig.2: schematics of the FBLOCK, the camera of the SuperB FDIRC detector.

On the left part of this side view, one can see a quartz bar (in blue) glued to its BaBar wedge (in red). The green component is an additional wedge which may be added to the existing setup in order to help focusing the photons. The right part of the view shows the FBLOCK, its two mirrors (in blue) and the detection plane instrumented with MaPMTs (in red).

A R&D program on the focusing DIRC technology has been existing for years at SLAC which has been leading the field of DIRC-like detectors since the beginning of the BaBar project. The experience gained in designing and operating a focusing DIRC prototype helped for the design of the SuperB



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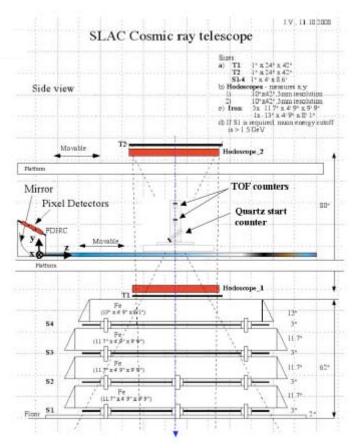


Fig. 3: schematic of the SLAC Cosmic Ray Telescope (CRT) facility.

In the lower part of the schematics the four absorber layers (iron stacks) are visible such as the four associated scintillation counters, labeled S1 to S4. Above them, one can see the two hodoscopes (in red) and the two scintillator trigger counters T1 and T2. An additional quartz counter (the tilted bar indicated by an arrow with the label 'Quartz start counter') allows a more accurate determination of the timing when needed (for instance to do chromatic corrections). A coincidence T1 && T2 && S1, selecting muons with an energy above ~1.5 GeV produces an event rate of about 5 kEvents / day.

FDIRC. SLAC is also providing a very convenient facility to build and test new Cherenkov detector: the **Cosmic Ray Telescope** [7] (**CRT**, see Fig. 3). A thick stack of iron and scintillator layers allows one to select hard cosmic muons with energies above 1.5 GeV while two hodoscopes provide a tracking precise at the 1-2 mrad level. Detectors can be installed in the space between the hodoscopes where they can take data for weeks, allowing to test their various components. The CRT has already been used by the SLAC focusing DIRC prototype and it currently hosts a SLAC-LAL joint experiment to validate a concept of time-of-flight (TOF) Cherenkov PID detector for the SuperB forward² side whose electronics need to make timing measurements at the few ps level. Now that SuperB has been approved, the CRT is expected to become the main facility to test PID detector prototypes. Participating actively to these future CRT tests is a key element of this ANR proposal.

ANR-GUI-AAP-04 – Doc Scientifique 2011

² Like the first generation B-factories, SuperB will be an asymmetric e⁺e⁻ collider. The energy imbalance between the two beams boosts the produced B mesons which fly on a short distance before decaying. These displaced vertices are detected by the SuperB detector, thus allowing B-mesons to be detected and physicists to perform time-dependent analysis. The "forward" side of the detector corresponds to the direction of the electron beam, more energetic than the positron one. The particle distribution as a function of the polar angle peaks in the forward direction.



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Real data (from BaBar, the focusing DIRC and FDIRC prototypes) will be used to validate and optimize the FDIRC. Moreover, an important simulation work will be needed to understand the behavior of this new apparatus and to define the algorithms reconstructing its data. Therefore, **this proposal covers most aspects of the FDIRC design, from the technical work in the CRT to the data analysis with computers**. The participants will benefit from their experience on BaBar and they will work in close contact with the other SuperB groups: the collaboration should be mutually beneficial.

To conclude this state-of-the-art overview, we would like to recall that DIRC-like detectors are well-recognized in the particle physics detector community. For instance, the Panda collaboration [8] will build its own 'DIRC' to study the products of anti-proton collisions on a fixed target.

2.3. OBJECTIVES, ORIGINALITY AND/OR NOVELTY OF THE PROPOSAL

A detector like the FDIRC has never been built for a 'big' particle physics experiment like SuperB; moreover, the associated accelerator is expected to deliver hundred times more luminosity than the current B-Factories PEP-II and KEK-B. This single sentence summarizes nicely the challenges that the FDIRC needs to tackle and which are addressed by the present ANR proposal. Its objectives are the following.

- To optimize the optical design of the FBLOCK.
- To design the readout electronics (required to be more than 10 times faster than for BaBar), to validate their performances and to make sure the final board is affordable and robust enough for the SuperB mass production. Currently, there is no solution available which would provide a time resolution at the 100-ps level while coping with a 1-MHz input rate per channel. The innovative design proposed by the ANR proposal participants aims at fulfilling both of these requirements for the first time.
- To finalize the design of the FDIRC and to integrate it within the whole SuperB detector.
- To define the reconstruction and data analysis algorithms. The ring pattern is distorted in the FDIRC as the photons can follow various optical paths to reach the MaPMTs; the complexity of the resulting picture depends on the parameters of the track which produces the cone of Cherenkov light in the quartz bars.
- To prove that this detector will cope with the accelerator backgrounds and that its performances will remain constant during the whole data taking period (5+ years).

The main deliverable for this ANR proposal is a global design for the FDIRC, the primary PID detector for the SuperB barrel. Well-defined deliverables associated with this global design are the readout electronics board and a set of C++ codes to simulate, decode and reconstruct the FDIRC data. These programs will be part of the SuperB computing framework and are expected to be used during the data taking and analysis phases of the experiment.

In addition, we expect to be able to take part in the detector assembly on the SuperB experiment site during the final year of this ANR proposal.

About 15 years ago the LAL was involved in the design of the BaBar DIRC. The SuperB FDIRC, based on a similar concept, has some unique features which require new studies to understand its behavior and to optimize its performances. Moreover, the LAL has not been involved in the study of Cherenkov detectors since the BaBar DIRC. Therefore, this ANR proposal will broaden the scope of the lab by adding new skills to the existing ones.

3. SCIENTIFIC AND TECHNICAL PROGRAMME, PROPOSAL ORGANISATION

3.1. SCIENTIFIC PROGRAMME, PROPOSAL STRUCTURE

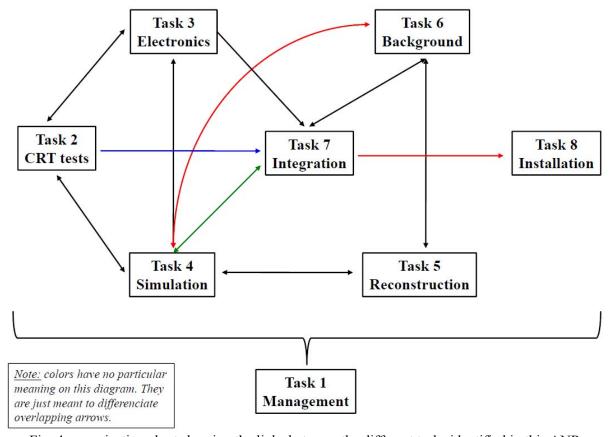


Fig. 4: organization chart showing the links between the different tasks identified in this ANR proposal – see text for details.

The structure of this ANR proposal follows closely the connections between the different tasks which need to be achieved in order to design the FDIRC detector for the SuperB experiment.

- Task 1: ANR proposal management
- Task 2: FDIRC tests at the SLAC CRT
- Task 3: Design of the FDIRC electronics
- Task 4: FDIRC simulation
- Task 5: Reconstruction of the FDIRC data
- Task 6: FDIRC background estimation and mitigation
- Task 7: FDIRC integration in the SuperB detector
- Task 8: FDIRC installation into the SuperB detector



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The coordination of the whole proposal will be ensured by regular meetings (in person, by phone or through video-conference tools like EVO) and trips to SLAC or to the locations of the SuperB general meetings, held every ~3 months. The interaction with the SuperB experiment will be easy as **the coordinator of this proposal is also the co-manager of the SuperB PID group** (such as of the **BaBar DIRC group**) and hence attends the monthly Technical Board meetings.

Fig. 4 displays the ANR proposal organization charts, with arrows showing the links between the different tasks. There will be a strong interplay between the CRT tests and the electronics design, with valuable inputs coming from the LAL test benches. Simulation software will be developed in close contact with the CRT tests, whose outcomes will be used by the integration task, which will be driven by simulation results as well. The simulation task will indeed be a core task of this proposal as it will interact a lot with the background and reconstruction tasks. Finally, the completion of the integration task should lead to a successful installation of the FDIRC into the SuperB detector.

3.2. DESCRIPTION BY TASK

3.2.1 TASK 1: MANAGEMENT

The ANR proposal manager ensures that the tasks progress smoothly, that the information circulates efficiently between the different participants and that the developments in the various areas are known and approved by the SuperB management. Internally, **biweekly meetings with slides archived on Indico webpages** will be organized with the following structure:

- first, a general overview of the FDIRC project followed by short status reports from the different ongoing tasks
- then, a detailed discussion focused on 1 or 2 "hot topics" (if applicable) or a technical presentation of one particular task
- finally, a review of the next important milestones (report to the SuperB collaboration or the management; new production of electronics chips or boards; release of a new version of some SuperB codes; massive production of simulated data; etc.) to make sure that everybody is aware of the project calendar.

Supporting documents (describing the work done, the results achieved and how other members of the SuperB collaboration could use them) will be produced regularly. The need for a clear, complete and up-to-date documentation will be enforced at each meeting as any failure to make these new developments available to all SuperB members will have to be paid for later. Progress reports will be shown at the SuperB collaboration meetings (at least 4 times a year), presented at international conferences (RICH detectors, IEEE, etc.) and published in peer-reviewed journals like NIM.

The deliverables for this task will be reports to the ANR, published every six months.

3.2.2 TASK 2 : CRT TESTS

Several tests will be organized in the CRT to test different aspects of the FDIRC detector. Their three main goals are:

- the validation of the FBLOCK design and of its optical coupling to the existing DIRC quartz bars
- the design of the FDIRC front-end electronics



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• The definition and coding of the data reconstruction algorithms.

We want to contribute to these tests at various levels:

- definition of the experimental setup
- assembly
- data taking
- monitoring
- analysis of the recorded data

This task will be covered by the ANR manager, the postdoc funded by the ANR and all the proposal participants involved in a given test (for instance the electronics engineers when the goal of the setup is to test the newly designed boards). Regular meetings with the SLAC group will be organized before a new test starts and while the data taking is ongoing to make sure everything proceeds as planned. People based in France will take part in software tasks (DAQ, monitoring as close to real-time and as automated as possible, analysis of the data available through the SLAC network) and in preparation tests at LAL, but several trips to SLAC are also foreseen to prepare and participate to the CRT experiments. It is not possible to understand and use optimally a device with which one is not familiar. This is the main reason why the travel budget included in this ANR proposal exceeds significantly the 3% number suggested in the ANR FAQ document — as SuperB is supported by the labs which participate to this proposal additional money will be provided by the home institutions, for instance to attend the SuperB collaboration meetings.

Reports (at least one every 3 months, synchronized with the SuperB collaboration meetings) will be written to describe the test setup, the evolution and state of the data acquisition system, the results achieved and, when applicable, their comparison to simulation. These reports will be used to define the following tests whose goals could be either completely different or closely related to the recent ones, depending on what the outcomes of the latter are. These reports will be among the deliverables for this task. The final deliverable of this task will be an almost final design (minor changes may occur before the actual installation into the SuperB detector starts) for the FBLOCK and the FDIRC structure.

The first CRT test is scheduled to start this Summer, with a full-scale prototype of a FBLOCK (1/12th of the FDIRC) connected to a full-length quartz bar. Electronics from the Hawaii University will be used initially until the first version of the LAL electronics becomes available in 2012. Other tests will follow based on a schedule which will evolve with time, depending on how the tests proceed and on the availability of the items to be tested (e.g. electronics boards). The advantage of using the CRT is that this facility belongs to the SLAC SuperB group. So we should be able to plan its operation according to our needs, without having to take into account planning constraints from other experiments.

Additional tests (e.g. the validation of the newly produced electronics boards or various MaPMT pixel by pixel performance scans) will be performed in other facilities, in particular at LAL where test benches are already in operation and will be upgraded in the coming months. These supporting tests will help optimizing the tests of the full FDIRC chain at the SLAC CRT facility.

The deliverables for this task will be three validations:

- of the FBLOCK design in Spring-Summer 2012
- of the final front-end electronics board (with the new front-end and TDC chips) end of 2014
- and of the FDIRC data reconstruction code, around the same date.



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3.2.3 TASK 3: ELECTRONICS DESIGN

Introduction

New electronics need to be designed to readout the FDIRC. The LAL and the Laboratoire de Physique Nucléaire et de Hautes Energies (LPNHE) groups are working on this project with the goal of having a first prototype board in 2012. Two chips need to be designed: a 16-channel front-end chip handling the PM output signals and a fast (70-ps resolution) 16-channel TDC chip, able to cope with a trigger rate of 150 kHz and a background level up to 1 MHz per channel. When available, these chips will be tested on the Orsay test bench and in the FDIRC prototype installed in the CRT. The process will iterate until a satisfactory design is achieved – 2-3 iterations are foreseen. The final deliverable for this task is a front-end board which will then be massively produced to readout the ~36 kChannels of the SuperB FDIRC.

As summarized in the above paragraph, the baseline design includes two chips embedded with a companion FPGA chip on a 64 to 128-channel front-end board – the final number of channels will depend on constraints coming from the FBLOCK integration. The 16-channel front-end chip provides both an output discriminator signal for the TDC and an integrated signal used to measure the charge thanks to a 12-bit ADC. The charge measurement will be used for electronics calibration, monitoring and survey purposes. Moreover, in case of a signal firing two neighboring pixels, the charge measurement will improve the spatial resolution – the 'charge sharing' method. The FPGA synchronizes the two chips, merges the time and charge information and finally packs them into a data frame which is sent to the acquisition system through a crate concentrator. The proposed architecture is non-triggered at the board level while the crate concentrator is in charge of packing the event when a trigger has been received from the DAQ system. A proposal for the DAQ architecture has been submitted by the Orsay group in 2010 and is considered as the baseline option in the SuperB TDR.

Technical information on the proposed design

The front-end board

We plan to develop three prototypes of the front-end board – see Fig. 5. Their production will follow the schedule of the front-end and TDC chips such as the mechanical studies of the FDIRC structure. The first prototype is foreseen to have only 16 channels in order to reduce its cost and simplify the initial design. The board will be connected by a short cable to a row of pixels from a Hamamatsu H-8500 MaPMT. The size and the acquisition interface of the board will be compatible with the SLAC CRT setup as the tests of the FDIRC prototype will start with the already existing but less efficient Hawaii electronics.

The second prototype board will be designed as close as possible to the current final design. The board requirements will follow the mechanical and thermal constraints coming from the design of the mechanical structure of the FBLOCK. In parallel, the design of the backplane and of the power supply will be under study, such as the integration of the whole system on the detector. These studies will provide additional inputs to the front-end board design. As was done for the LHCb calorimeter electronics, a third prototype will be designed as a pre-series. After the completion of the tests of these last boards, the SuperB experiment will provide funding to have a complete FBLOCK equipped. A combined test with the concentrator crate (developed outside the scope of this ANR proposal) will then be performed to fully test the whole electronics test. Finally, the mass production – paid by the SuperB detector collaboration – could be launched.

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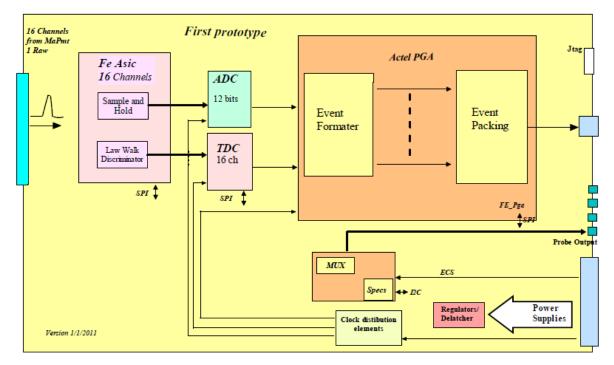


Fig. 5: current schematics of the FDIRC front-end board first prototype.

The TDC chip

A TDC chip (the 'SNATS') has been designed for the Super Nemo experiment. It provides a time measurement with both a high resolution (70 ps RMS) and a large dynamic range (53 bits). The architecture of this chip is based on the association of Delay Locked Loops (DLLs) with a digital counter, all of these components being synchronized to a 160 MHz external clock.

A 16-channel prototype chip was produced using the AMS 0.35 μ m CMOS technology. The chip contains 8 DLLs (each shared between 2 channels) and a common 48-bit counter. Each DLL houses 32 delay elements giving each a typical binning of 200 ps for fine time measurement. The 48-bit GRAY counter is used for coarse conversion and has a time range of about 20 days. The measured performances are as follows [9]: a differential non-linearity of about \pm 0.2 LSB; an integral non-linearity around \pm 1.3 LSB and a static power dissipation of 380 mW.

The SNATS architecture can be divided into two main blocks: one performing the timing measurement and the other the readout part. The SuperB chip – see Fig. 6 – will keep the same philosophy but the input rate requirement lead to a complete re-design of the readout part, in order to minimize the dead time per channel by increasing the data output speed. Instead of the registers and multiplexer which are the bottlenecks of the Super Nemo chip readout, we plan to use for SuperB an individual FIFO memory per channel in order to derandomize the high frequency bursts of input data. With this architecture, data from the DLLs and the coarse counters are transferred into the FIFO memory within two clock cycles. When the transfer is complete, the channel is automatically reset and ready for the next hit. A readout scrutation test performed by a state machine showed an output FIFO data rate of 80 MHz. Time ranges for the DLLs and the coarse counter can be easily customized by



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adjusting the output data format (from 16 to 64 bits). Thus, the chip is suitable for various applications with either high count rate and short integration time or low count rate and long integration time.

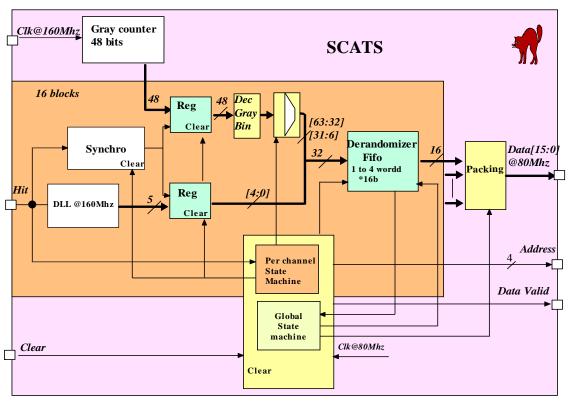


Fig. 6: current schematics of the SuperB FDIRC TDC chip – the 'SCATS'.

A FIFO depth of 8 words has been selected after simulation of the verilog code targeted in an Actel PGA with an exponential distribution model for the time difference between hits and a mean rate of \sim 1 MHz. To design this FIFO, a full custom RAM will be developed to reduce the size of the chip and consequently its cost. The chip will be designed using known and proved mitigation techniques to face single event upset (SEU) issues due to the low-level radiation environment.

The front-end chip

The proposed architecture for the front-end chip (called the 'PIF') is the following – see Fig. 7.

- A discriminator receiving the MaPMT output and sending a logic signal to the TDC which timing is independent of the amplitude of the MaPMT signal. This discriminator will be a pseudo Constant Fraction Discriminator (CFD), i.e. a 'classical' armed fast discriminator comparing the MaPMT signal and the output of an amplifier acting as a delay.
- A charge amplifier integrating the MaPMT signal and sending its output to an external 12-bit ADC.
- A 'Sample and Hold' circuit triggered by the output of the pseudo CFD.
- A 'State machine' aiming at synchronizing the charge information with the TDC timing.

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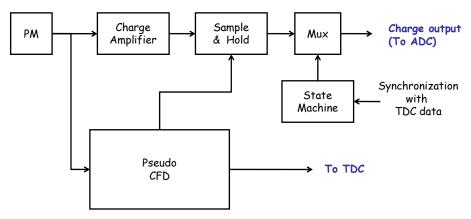


Fig. 7: Current schematics of the front-end chip.

The challenge is double:

- first, the time measurement requires a null time walk at the discriminator output, in order not to deteriorate the electronics resolution
- then, the high number of channels (about 36,000 for the DIRC) makes mandatory the design of a very-integrated circuit which would fit in a little space.

State-of-the-art solutions are based on the 'delay and fraction' principle with the discrimination performed by discrete components, especially inductances implemented on board. The solution we propose here is to integrate the whole design in a single chip, hence reducing its area and its cost and to investigate a very innovative 'gain and integrator' scheme to cope with the 'no time walk' requirement.

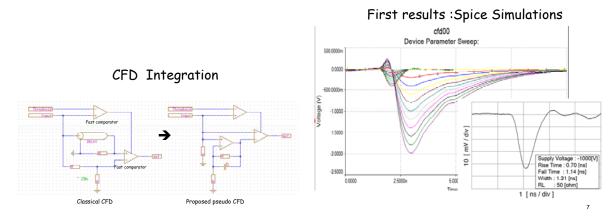


Fig. 8a: Delay + Fraction \rightarrow Gain + Integrators

Fig 8b: Spice simulation for time walk and output shape (preliminary results)

Testing the new electronics

As stated above, the new chips and boards will be tested in the SLAC CRT facility where they will receive real signals generated by high-energetic muons passing through a quartz bar – the produced photons will propagate through internal reflections until the detection plane of the FBLOCK prototype. Moreover, having a local test facility at LAL is a key part of the electronics development program. First, we will be able to test and debug the newly-designed components prior to shipping them to SLAC, which should ensure productive and efficient tests in the CRT. Then, a test



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bench where a controlled laser sends light pulses to a MaPMT at a frequency around 1 MHz will be essential to study the electronics in a high background (simulated) environment. Therefore, **the Orsay tests will complement those done at SLAC and positive results from both sets of tests will be required to validate the FDIRC electronics**.

This front-end electronics design task will be covered by the LAL and LPNHE electronics groups with the help of the physicists working on this project, among which the coordinator of the proposal and the postdoc funded by the ANR. More generally, all steps of the electronics design will be broadly discussed in the SuperB PID group, with a close interaction with the SuperB "Electronics, Trigger and Data Acquisition" group, in charge of the global design of the SuperB electronics.

Deliverables

The three cycles of development foreseen for the FDIRC front-end electronics will produce each three deliverables: a front-end chip, a TDC chip and a board based on these two components.

3.2.4 TASK 4 : SIMULATION

Various simulation studies are needed for the FDIRC.

First, **each test setup in the CRT will have to be simulated in order to make sure that its data are understood**. As we are learning from the TOF technology test currently ongoing at the CRT and briefly mentioned in Section 2.2, the choice of a particular experimental layout can have a significant impact on the data produced. The level of agreement between data and Monte-Carlo will tell us whether these simulations are accurate-enough or not. For each category of tests (corresponding only to minor modifications of the setup, such as a new version of the front-end electronics) there will be a deliverable: a simulation code, released while the tests will be ongoing and optimized by comparing its predictions to the real data.

In addition, **full Geant4-based simulations are mandatory to understand the patterns produced on the FDIRC detection plane** by the photons emitted by the charged tracks when they cross a quartz bar. These patterns are more complicated than in the BaBar case and strongly vary with the track parameters: rings can be distorted and/or split into different pieces. Deliverables associated with these simulations will be a set of Look-Up Tables (LUT) allowing a fast and accurate parameterization of the FDIRC response.

Another class of simulations will aim at estimating the background the FDIRC will be sensitive to when the luminosity reaches or exceeds 10^{36} cm⁻² s⁻¹. These simulations will be developed within the general SuperB framework as they require an accurate description of the interaction region and of the detector, such as realistic contributions from the different categories of background (Bhabha events, Touschek effect, losses all along the ring, thermal neutrons, etc.). More details are given in the description of Task 6 below. The deliverables for the background task will be background rates in the FDIRC such as the time and spatial distributions of these hits.

Finally, detailed simulations of the full FDIRC within the SuperB simulation framework will be needed to test and validate the algorithms used to reconstruct the data and hence to measure the performances of the FDIRC, both in terms of efficiency (what is the probability to positively identify a particle of a given type, say a kaon?) and mis-identification (which fraction of pions will be wrongly identified as kaons by the same procedure?). Depending on the type of data analysis, configurations maximizing either the purity of the sample of selected tracks or the efficiency of the identification



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procedure will be preferred. Therefore, various optimizations will be performed – see next task for details. These simulation codes will be the deliverables associated with this part of the simulation task.

This task will be covered by the proposal coordinator and the postdoc funded by the ANR with contributions from the other physicists involved in this project. The developments will be presented and discussed within the SuperB simulation groups, both to have them validated by experts and also to allow them to be used by a wider community of people.

3.2.5 TASK 5 : RECONSTRUCTION

As the FDIRC camera is different from the BaBar one, new reconstruction algorithms have to be developed. They need to be fast, at least as efficient as those used in BaBar and to fully use the potential of this new detector. For instance, the timing resolution of the MaPMTs and of the readout electronics will be good enough to make the measurements sensitive to the chromatic dispersion in the bars (the photon propagation speed depends on its wavelength). Taking properly this effect into account, the Cherenkov angle resolution can be improved.

Algorithms used to analyze the BaBar data or the SLAC focusing DIRC prototype will be studied to understand which parts can be directly transposed to the FDIRC reconstruction code and which procedures need to be modified. Yet, a complete rewriting of the FDIRC reconstruction code is foreseen for SuperB, first to fit within the global framework developed for this new experiment and also because the existing codes are old-fashioned, not maintained nor flexible enough. Converging on a proper design before starting the actual coding will be mandatory.

In DIRC-like detectors, part of the complexity of the analysis comes from the fact that the actual path of a given photon between the track and the MaPMT is unknown. Different optical paths are possible, each one corresponding to an "ambiguity" in the Cherenkov angle measurement. The final resolution of the device will strongly depend on the way these irreducible ambiguities are dealt with. In principle, the higher the number of photons taken into account for a measurement, the better the result. This may not be true when pathological photons with too many ambiguities are added. Therefore, the cuts to reject these photons and/or the procedures to weight their contributions in multivariate algorithms like the maximum likelihood method will have to be carefully tuned.

Although the initial developments of the reconstruction algorithm can be done with "signal" photons truly generated by particles crossing the CRT quartz bar, its proof of principle and final tuning require to include "background" photons as modeled by the Task 4. The FDIRC measurements will then be used as inputs for the PID selectors, a set of programs which gather data from various detectors (the FDIRC, the tracking devices, etc.) to identify the tracks. The quality of a selector is usually expressed in terms of two quantities: its efficiency, i.e. the probability to identify correctly a given particle, and the probability of mis-identification which tells how often a particle of a different nature is selected (e.g. a true pion being identified as a kaon).

The deliverables for this task are C++ algorithms which will be part of the SuperB global reconstruction framework, run identically in simulation and with real data. A set of monitoring data (stored as ROOT ntuples and displayed through an automated set of plots) will also be created to check the quality of the FDIRC data and to make sure that problems with the raw data or during the reconstruction phase are spotted out quickly. The quality of the FDIRC reconstructed data will be established by comparing various PID selector performance plots with and without the FDIRC inputs.



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This task will be covered by the postdoc funded by the ANR and by the proposal coordinator. This work will benefit from discussions among the SuperB PID & computing groups and with other PID & software experts, in particular from the BaBar experiment.

3.2.6 TASK 6: BACKGROUND ESTIMATION AND MITIGATION

Neglected backgrounds could completely modify the behavior of a detector and, in the worst case, turn a very promising device into a useless piece of material. That is why **it is mandatory to estimate the FDIRC backgrounds at the maximum SuperB luminosity** and to make sure that there is enough headroom in the detector design to avoid a sharp loss of performances if the actual level of background exceeds the prediction by a few percent – actually, the BaBar experience showed that the difference between the real background and the predictions could be at the level of one order of magnitude! That is why the FDIRC needs to be quite robust against backgrounds. So far, the maximum foreseen rate is 1 MHz per channel, a value which will be confirmed and/or refined by the studies to which this ANR proposal will take part.

Like for the other tasks (but this aspect will probably be more important in this case), a bibliographical research will be needed for this work: one needs to identify the potential sources of background, to estimate their rates and to compare these predictions with actual data seen by experiments with a similar setup. BaBar data will obviously be important but changes in the accelerator design make some of the background extrapolations unclear. Therefore, background reports from Belle should be useful as well. In addition, one will have to understand how background will affect the MaPMTs in order to set limits on the instantaneous and integrated levels of background. Finally, one will need to study the background impact on the electronics: integrated dose (not expected to be a major concern for the FDIRC electronics), SEUs and latchups. This last topic will require a close interaction between electronics engineers and physicists and will benefit from the experienced gained while designing electronics for the LHC experiments.

The simulation, already described in Task 4, will be a major part of these background studies. Should the computed background appear too high, appropriate shieldings would have to be designed or the detector/accelerator would have to be modified.

This task will be covered by the postdoc funded by the ANR and the proposal coordinator. Like for the other tasks, progresses will require frequent discussions with SuperB simulation experts. The background estimation task will be done in close connection with the SuperB "Machine-Detector-Interface" (MDI) group, whose work will be crucial to make sure that the detector can stand the very high luminosity delivered by the accelerator. Its deliverables will be a set of predictions for the background rates in the FDIRC, depending on the accelerator conditions. If mitigation is needed for a background component, the task will deliver advices on how to proceed.

<u>Note:</u> for the tasks 4 to 6, BaBar real and simulated data may be used as comparison or cross-check tools. Moreover, effects observed in the CRT data or predicted by the SuperB simulation could potentially be searched for in BaBar.

3.2.7 TASK 7: INTEGRATION IN THE SUPERB DETECTOR

As the FDIRC design becomes more concrete and closer to its final layout, one will have to focus on the integration of this device in the full SuperB detector – see Fig. 9. Not only should the

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FDIRC fit in its allowed space but people should access as easily as possible the components which may fail (mainly electronics boards and MaPMTs) during the data taking. Obviously its design should also guarantee a very high duty cycle and constant high performances.

Discussions about this topic already started inside the SuperB Technical Board and we would like to contribute to it through this ANR task. Inputs from all participants to this proposal (in particular from the postdoc funded by the ANR and from Christophe Beigbeder, the main engineer associated with this proposal) will be taken into account and brought to the SuperB PID group by the proposal coordinator. The deliverables for this task will be a final design for the FBLOCK and an installation procedure onto the SuperB detector.

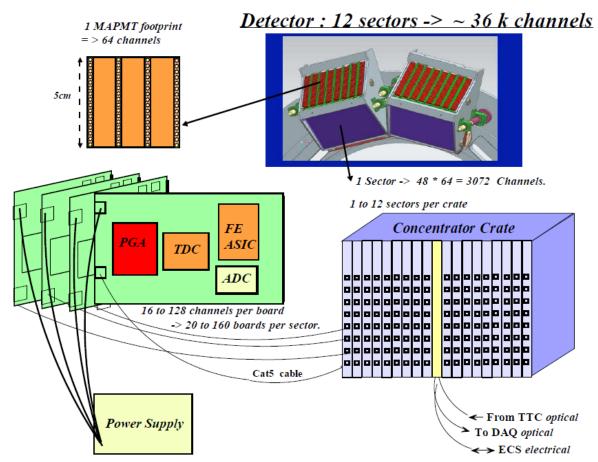


Fig. 9: FDIRC integration.

The top CAD drawing shows a possible preliminary design for the FBLOCK support structure and its associated components, among which the electronics front-end boards. Each board will read the data from several MaPMT pixels and send them via optical fibers to the SuperB DAQ system through a concentrator crate located outside of the detector.

3.2.8 TASK 8: INSTALLATION INTO THE SUPERB DETECTOR

The final task of this ANR proposal covers our participation to the installation of the FDIRC into the SuperB detector at the experiment site. The successful installation of our device (the obvious deliverable for this task) followed by its commissioning and the first collision beam data will be a nice conclusion to all the work done on the FDIRC and will prove that the above-described tasks have all



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been properly completed. Many people external to this ANR proposal will take part in this final task but most of – if not all – the participants to this ANR are expected to play a role in it.

3.3. TASKS SCHEDULE, DELIVERABLES AND MILESTONES

Fig. 10 below shows a Gantt diagram describing the schedule of this ANR proposal. **Most tasks span a large fraction of the ANR duration as they are complex and as their study will evolve as the work proceeds**. For instance, the simulation task will first focus on simulating the CRT tests. Then, it will be enriched as our understanding of the FDIRC improves and as the design of the detector and of its components (in particular the electronics boards) gets refined. Finally, the simulation will focus on the FDIRC as a component of the whole SuperB detector, operated in a very high luminosity environment where backgrounds are potential issues.

For the TDC chip design, the first two runs are scheduled for July 2011 and mid-2012. The chips should be delivered at LAL about three months later. A similar schedule is foreseen for the front-end chip, although the detailed planning will depend on the technology chosen for this chip (either AMS $0.35~\mu m$ or CMOS XFAB $0.18~\mu m$). The front-end boards will be assembled when the chips get available. The test of the second prototype board is expected to be long and extensive: as the next step will the pre-serial production, all features of the board will have to be studied extensively.

The reconstruction task will probably be delayed by a few months with respect to the start of this ANR proposal, in order to focus on the CRT tests first. Then, it will benefit from a constant interplay with the simulation and background tasks, in order to finally deliver a set of realistic and powerful reconstruction algorithms. This task ends with the ANR proposal as one can expect code development and tuning until the end of the SuperB detector commissioning and also during the first ('low' luminosity) phase of the data taking.

The two sequential tasks integration+installation cover the whole duration of this proposal: the CRT work and the related tests will allow one to converge on a final design for the FDIRC structure, taking into account the available space, the various services (HV, LV, data lines, etc.) needed to operate the detector and the expected levels of backgrounds. This integrated design and the associated integration procedure will then be applied during the FDIRC installation into the SuperB detector.

Task	Deliverable	Date
1 – Management	Reports to the ANR	Every six months
2 – CRT tests	Final FDIRC design	December 2014
3 – Electronics	FDIRC front-end boards	December 2014
4 – Simulation	C++ code simulating the FDIRC	June 2015
5 – Reconstruction	C++ code used to reconstruct the FDIRC data	June 2015
6 – Background	Document describing the expected FDIRC background, the assumptions & methods used to compute these numbers and the actions taken to mitigate them – when significant	June 2015
7 – Integration	Final design of the FDIRC structure and integration procedure into SuperB	June 2014
8 – Installation	FDIRC installed into the SuperB detector	June 2015

Table 1: Summary of the main deliverables of the present ANR proposal – see text for details.

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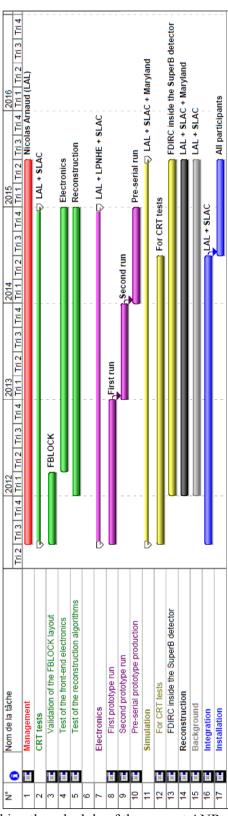


Fig. 10: Gantt diagram describing the schedule of the present ANR proposal – see text for details.



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Table 1 above shows the main deliverable for each of the ANR task – in particular, the proposal coordinator will send written reports to the ANR every six months. These reports will summarize the status of each task, describe the results achieved, the difficulties encountered, the methods used to fix these problems and the plans for the coming six months. An appendix will list the public documents presenting the work funded by the ANR: talks at open sessions of SuperB meetings; talks at international conferences; articles in peer-reviewed scientific journals.

For each task, intermediate and partial deliverables will be provided to the SuperB community each time a significant result is obtained – they are listed in the sections describing these tasks. A given task will be called 'completed' when its deliverable is final and ready to be used by the SuperB detector to take physics data.

A first milestone will be the writing of the SuperB detector "Technical Design Report", foreseen for the end of 2011 or the beginning of 2012. This document will describe in details the different components of the SuperB detector – among which the FDIRC. It will also detail the studies needed to reach a final design, such as the methods to be followed to achieve these goals. About two years later, SuperB should publish its Physics Book for which realistic detector performances are needed as input. It is also clear that the SuperB experiment will undergo various reviews at different levels between now and the start of the data taking. Each time the FDIRC will be in the scope of a review, the participants to this ANR proposal will contribute to it.

4. DISSEMINATION AND EXPLOITATION OF RESULTS, INTELLECTUAL PROPERTY

All results achieved by the participants of this ANR proposal will be presented to the SuperB collaboration and to the particle physics community – through talks in international conferences and journal articles – when relevant. They will help the SuperB experiment to achieve its goals in terms of detector performances, amount of integrated luminosity and physics results obtained by the analysis of the huge dataset.

5. Consortium description

5.1. Partners description and relevance, complementarity

This ANR proposal brings together physicists, engineers and technicians from four labs: LAL, LPNHE, SLAC and Maryland University. All four institutions have been and are still deeply involved with the BaBar experiment, from the detector to the physics analysis.

The SLAC group is made up of three senior physicists who are among the "inventors" of the DIRC: Blair Ratcliff, Jerry Va'Vra and David Aston. With the technical support from Matt McCulloch – who has been taking care of the key DIRC hardware components (among which the quartz bars) since the detector construction until its disassembly in 2009-2010 – they have proposed the FDIRC concept for SuperB. They are currently ordering the raw quartz material in which the FLOCK prototype will be carved and started thinking of its first test in the CRT, with the help of the SuperB Padova and Bari groups. In addition, the SLAC and Maryland groups started simulating the FDIRC.



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The LAL and LPNHE electronics engineers have already designed together the front-end electronics for the BaBar DIRC: 168 boards running in parallel to readout the whole detector plus about 25 spare boards. These boards have all worked perfectly over the 10 years of data taking. The new chips they will design for SuperB are based on other chips designed for the LSST and NEMO experiments. The specifications of these chips will be upgraded and adapted to match the FDIRC requirements: high background levels and trigger rate, etc. The new chips will also be of interest in various other physics fields where timing measurements with a ~ 100 ps accuracy will be needed – in particular biomedical applications. Moreover, the design of the front-end boards and the final choice of architecture will also benefit from the experience gained while designing chips for the LHC experiments ATLAS and LHCb.

Finally, the LAL and LPNHE physicists have been working in BaBar for a while. Both groups are also involved in SuperB since the Conceptual Design Report published mid-2007. Since then, the LAL group in particular has been one of the most active groups in SuperB, taking various responsibilities in the project (physics group co-leadership, global detector design co-leadership, PID group co-leadership, electronics group co-leadership, etc.) and actively working on a wide range of topics: physics analysis, fast and full simulation of the detector, design of a TOF detector to improve the PID on the forward side of SuperB, the upgrade of the DAFNE interaction region in Frascati, etc.

5.2. QUALIFICATION OF THE PROPOSAL COORDINATOR

I (Nicolas ARNAUD) have been a member of the LAL BaBar group since I got a CNRS permanent position in October 2003. I have a deep knowledge of the BaBar experiment in general and of the DIRC in particular. I have spent four years at SLAC (2005-2008), on leave from the CNRS, and during which I have mostly worked on the BaBar detector. Regarding the DIRC, I have been successfully monitoring manager, reconstruction software manager, commissioner and operations manager (that is responsible for the smooth and efficient running of the DIRC during the data taking), background expert and finally co-system manager since mid 2006. In addition, I have been working for the experiment as a whole: six months as co-coordinator of the BaBar data taking in 2007 and one year as responsible for the overall BaBar data quality (2008). During this period, I have been in charge of the final reprocessing of the full Y(4S) BaBar dataset and I have also helped analysts to get a quick access to the new Y(3S) and Y(2S) data taken during the last months of the BaBar running (12/2007 → 04/2008). Prof. Hassan Jawahery (jawahery@physics.umd.edu), BaBar spokesman at the time I was having these major commitments, is a reference for my SLAC period. In addition, I am currently coordinating the writing of an update of the BaBar detector NIM paper, aiming at describing the BaBar experiment during the high luminosity data taking period (2002-2008).

In Summer 2007 I started working in the **LUMI collaboration** which was designing luminosity and background monitors for the upgrade of the DAFNE interaction region. Although I made several trips to Frascati before the data taking started and during the operation of the accelerator, most of my contributions were software-oriented as my BaBar commitments obliged me to spend most of my time at SLAC. I worked on the simulation of the experiment with Geant3 and on the real-time and offline data analysis. Finally I am the main author of the two LUMI papers [2,3].

Since I came back to Orsay in January 2009, I have been a key member of the Orsay SuperB group. I am involved in the PID group (as co-coordinator and as a physicist working on the FDIRC and on the proposal of a TOF DIRC-like detector to improve the PID performances on the forward side of SuperB) and in simulation developments.



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While at SLAC, I have supervised various PhD students and postdocs who were doing their service work³ on the BaBar detector or within the Data Quality group. Since I am back at Orsay I'm cosupervising a SuperB PhD student, Leonid Burmistrov, whose PhD advisor is Prof. Achille Stocchi. The above summary of my past and current activities show that I am already familiar with the management of a group; at LAL, I am currently the youngest of the group leaders.

5.3. QUALIFICATION AND CONTRIBUTION OF EACH PARTNER

	Name	First name	Position	Field of research	Personne. mois* / PM	Rôle/Responsabilité dans la proposition de projet/ Contribution to the proposal 4 lignes max	
ANR proposal responsable LAL	ARNAUD	Nicolas	Staff physicist	Particle physics	36	Involved in all tasks listed above, in particular the CRT tests, the electronics validation, the FDIRC simulation and reconstruction software	
LAL	STOCCHI	Achille	Staff physicist	Particle physics	5	Potential of the FDIRC for physics analysis	
LAL	BEIGBEDER	Christophe	Staff electronics engineer		24	Design of the FDIRC electronics; integration of electronics and related utilities (HV, LV, data cables) on the FDIRC structure.	
LAL	TOCUT	Vanessa	Staff electronics engineer		15	Design of the FDIRC TDC and front- end chips; global design of the FDIRC front-end electronics board	
LAL	BRETON	Dominique	Staff electronics engineer		10	Supervision of the FDIRC electronics board design; integration within the global SuperB electronics system	
LAL	EL BERNI	Abdelmowafack	Staff electronics engineer		10	Design of the FDIRC TDC chip; global design of the FDIRC front-end electronics board	
LAL	PUILL	Véronique	Staff engineer		5	MaPMT and electronics board test in the LAL-Orsay test bench	
LAL	???	???	Postdoc physicist	Particle physics	48	Paid by the ANR grant. He/she will be involved in most of the tasks as described above.	
LPNHE	LEBBOLO	Hervé	Staff electronics engineer		At least 5, up to $10^{(a)}$	Design of the FDIRC front-end chip; global design of the FDIRC front-end electronics board	
LPNHE	BEN-HAIM	Eli	Staff physicist	Particle physics	5	Potential of the FDIRC for physics analysis; electronics design	
SLAC National Accelerator	VA′VRA	Jaroslav (Jerry)	Staff physicist	Particle Physics	24	FDIRC design; CRT tests; electronics design; mechanical integration,	

³ Each BaBar member must work part-time on a task which benefits to the whole collaboration: detector operations, computing, etc.

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Laboratory						background estimation and mitigation
SLAC National Accelerator Laboratory	RATCLIFF	Blair	Staff physicist	Particle Physics		FDIRC design; reconstruction algorithm; background estimation and mitigation
SLAC National Accelerator Laboratory	ASTON	David	Staff physicist	Particle Physics	10	CRT tests; simulation; reconstruction
SLAC National Accelerator Laboratory	MC CULLOCH	Matt	Staff technician		10	Support for the CRT tests
Maryland University	ROBERTS	Douglas	Staff physicist	Particle Physics		FDIRC design; simulation; reconstruction

^{*} à renseigner par rapport à la durée totale du projet

In addition, the LAL group is opening a PhD position for next Fall. Should a good candidate be found and the PhD position be granted, the 'instrumentation' part of this thesis will be focused on the FDIRC. Therefore, the student would be involved in some of the tasks defined in this ANR proposal and would help the above listed participants. Yet, as it is too early to be sure that this position will indeed be filled, it has not been included in the current proposal to be conservative.

Finally, some of the Person.Month numbers displayed in the above table are quite low. This comes from the fact that they are integrated over the duration (4 years) of this long ANR proposal. The people who are only involved in a specific task (for instance the specialized electronics engineers) will spend a significant fraction of their research time on it while it is ongoing; when it is completed, they will move on to other projects.

6. SCIENTIFIC JUSTIFICATION OF REQUESTED RESSOURCES

This ANR proposal presents several R&D activities focused on achieving a realistic and powerful design for the FDIRC detector of the SuperB experiment. It does not aim at covering all the topics which need to be studied to fulfill this ambitious goal (for instance the purchase of raw pieces of quartz from which the FLOCKs will be carved and polished or electronics utilities like power supplies, backplanes, the cooling system, etc.). The idea is that our effort – which must start as soon as possible to introduce no delay in the overall SuperB planning, which foresees a start of the data taking around 2016 – will put this project on track and that it will get additional resources when the SuperB funding system is balanced. The money coming from the funding agencies participating to SuperB will allow the FDIRC to move from the prototype phase to the serial production. This transition phase should occur while the current ANR proposal proceeds.

^(a) Hervé Lebbolo's participation to the FDIRC barrel electronics design is already approved at the 10% FTE level by the LPNHE. If agreed during a future meeting of the LPNHE "Conseil Scientifique", his FTE percentage could be doubled following the SuperB approbation by the Italian government, reaching thus a level of 20%. In this scenario, another electronics engineer with a CDD contract at LPNHE, Yixian Guo, would join this project at the level of 50% FTE.



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Equipment

The main equipment resource requested by this ANR proposal is the funding to design the FDIRC front-end electronics board – the mass production needed to instrument the whole SuperB detector will be paid later by the collaboration.

- Front-end board: 5 k€ to produce three prototypes. So, assuming two iterations plus the final pre-serial production, the total cost for this part is 15 k€
- Chips
 - o Front-end: 10 k€ per multi-project wafer run (20 chips produced, among which 5 encapsulated and 15 available as spares or for other tests)
 - o TDC: 25 k€ per multi-project wafer run (20 chips produced, among which 5 encapsulated and 15 available as spares or for other tests)

Assuming as well three iterations for each chip (the last one being the pre-serial production), the total cost for this part is $105 \text{ k} \in$

• Test setup: 10 k€for its operation, maintenance and utilities.

The test stand will be located at LAL. Part of this equipment will be funded by the SuperB LAL group and by the laboratory itself. That is why we only request 10 k€ for this part.

Summing up all the numbers above, the total cost for the whole FDIRC electronics prototype chain is 130 k€

Staff

The LAL group is requesting a postdoc for the whole duration of this ANR proposal. The total associated cost is $55 \text{ k} \in / \text{ year} \times 4 \text{ years} = 220 \text{ k} \in \text{This person will contribute to most of the tasks identified in the present proposal, from detector works (electronics and CRT tests) to computing activities (simulation and reconstruction). He/she will work under the supervision of the proposal coordinator and in close contact with Christophe Beigbeder who will coordinate all the technical work related to the FDIRC front-end electronics design.$

Subcontracting

No resource requested in this category.

Travel

The institutions which the groups participating to this ANR proposal belong to are supporting the SuperB experiment. Therefore, part of the travel money needed to work on this project (for instance to attend the SuperB collaboration meetings, about four times a year) will be provided by the home laboratories. The funds we ask through this ANR proposal will be dedicated to trips to SLAC (in order to support and operate the FDIRC tests ongoing at the SLAC CRT facility) and to the future SuperB site.

- For each of the first two years of the ANR proposal dominated by the CRT tests (including the electronics), we request funds for
 - o Three 'long term' (1 month) stays at SLAC: 3×4 k€ = 12 k€
 - o Eight 'short' (1 week) trips at SLAC: 8×1.8 k€ = 14.4 k€



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- For the third year, a transition year between the SLAC-based CRT tests and the activities on the SuperB site (location currently unknown but certainly in Italy), we requests funds for
 - o Five 'short' (1 week) trips at SLAC: 5×1.8 k€ = 9 k€
 - o Five 'short' (1 week) trips to the SuperB site: 5×1.3 k€ = 6.5 k€
 - o One 'long term' (1 month) stay at the SuperB site: 3.5 k€
- During the final year of this ANR proposal, most of the on-site work should be done at the SuperB site for the FDIRC installation. So we request the following travel funds for the 4th year:
 - o 6 months on-site: 20 k€
 - o Ten 'short' (1 week) trips to the SuperB site: 10×1.3 k€ = 13 k€

The table below summarizes the travel money needs associated with this proposal.

Travel Funds	Year 1	Year 2	Year 3	Year 4	Total
(k€)	26.4	26.4	19	33	104.8

Costs justified by internal invoices

No resource requested in this category.

Other expenses

In this category we request 2.5 k€/year (hence 10 k€ total) for our running costs: laptops, utilities, etc.



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7. ANNEXES

7.1. REFERENCES

- [1] INFN press release: "The Italian Government Funds the Super-B Accelerator" http://www.interactions.org/cms/?pid=1030355 and http://www.infn.it/news/newsen.php?id=594
- [2] Luminosity and background measurements at the e⁺e⁻ DAFNE collider upgraded with the crab waist scheme, http://dx.doi.org/10.1016/j.nima.2010.04.044
- [3] Description and performances of luminosity and background detectors at the upgraded e⁺e⁻ DAFNE collider, http://dx.doi.org/10.1016/j.nima.2010.04.057
- [4] The DIRC Particle Identification System for the BABAR Experiment, http://www.slac.stanford.edu/cgi-wrap/getdoc/slac-pub-10516.pdf
- [5] The SuperB Conceptual Design Report, http://arxiv.org/abs/0709.0451
- [6] The SuperB Progress Report Detector, http://arxiv.org/abs/1007.4241
- [7] The SLAC Cosmic Ray Telescope Facility, http://www.slac.stanford.edu/pubs/slacpubs/13750/slac-pub-13873.pdf
- [8] The Panda experiment, http://www-panda.gsi.de
- [9] V. Tocut *et al*, "SuperNemo Absolute Time Stamper, a high resolution and large dynamic range TDC for SuperNemo experiment", TWEPP 2009 http://indico.cern.ch/getFile.py/access?contribId=106&sessionId=27&resId=0&materialId=slides&confld=49682

7.2. CV, RESUME

This section provides the résumés of the ANR proposal participants whose contributions integrated over the four years of the proposal exceeds fifteen months: **Nicolas Arnaud** (the proposal coordinator, from LAL), Christophe Beigbeder (the main engineer associated with this proposal, from LAL), Vanessa Tocut (LAL electronics engineer as well) and Jerry Va'Vra (responsible for the CRT facility at SLAC and co-coordinator of the BaBar DIRC and SuperB FDIRC groups).



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Nicolas Arnaud (proposal coordinator)

Age: 36 ans

Cursus et Situation actuelle:

Chargé de recherche 1^{ère} classe au laboratoire de l'Accélérateur Linéaire (CNRS-IN2P3 et Université Paris Sud XI). Je suis membre du groupe BaBar-LAL depuis mon entrée au CNRS (1^{er} octobre 2003) et du groupe SuperB-LAL depuis sa fondation. Auparavant, j'ai fait ma thèse sur l'expérience Virgo sous la direction de M. le professeur Michel Davier puis un an de fellow au CERN sur l'expérience LHCb avec MM. Philippe Charpentier et Olivier Callot. Je suis également ingénieur de l'École Nationale des Ponts et Chaussées.

De 2005 à 2008 j'ai été expatrié quatre ans au SLAC National Accelerator Center pour travailler principalement sur le détecteur BaBar. J'ai en particulier exercé un certain nombre de fonctions au niveau du détecteur Cherenkov DIRC, détaillées dans le chapitre 5.2 de ce proposal ; je suis le responsable français du DIRC depuis mi-2006. J'ai également contribué au bon fonctionnement de l'expérience dans sa globalité, d'abord comme co-coordinateur de la prise des données entre janvier et juin 2007, puis comme responsable de la qualité des données en 2008, année où ont lieu le reprocessing final des données Y(4S) et BaBar et le processing accéléré des données accumulées aux énergies des résonances Y(3S) et Y(2S).

En parallèle, j'étais membre de la collaboration LUMI qui a construit des détecteurs de luminosité et de bruit de fond pour l'étude de la région d'interaction DAFNE, modifiée pour tester le « crab waist scheme ». Nos mesures, associées à celles d'autres détecteurs, ont permis d'établir le succès de ces tests et donc de valider une partie clef du *design* du futur accélérateur SuperB.

Pour ce qui est de mon travail dans la collaboration SuperB, je suis co-coordinateur du groupe PID et impliqué dans la simulation rapide du détecteur. Je suis également responsable du groupe BaBar-LAL depuis fin 2009.

En plus de mon travail de physicien, je me suis beaucoup impliqué dans des activités de vulgarisation à destination des élèves du secondaire et du supérieur, de leurs professeurs et du grand public : revue « Élémentaire », projet « Passeport pour les deux infinis » (dont le livre éponyme rencontre un grand succès depuis sa sortie au mois de septembre, tant auprès du public que des enseignants qui peuvent en recevoir un exemplaire gratuit sur demande), Masterclasses du CERN, etc.

Liste des 5 publications (ou brevets) les plus significatives des cinq dernières années:

- Measurement of CP-Violating Asymmetries in $B^0 \to (\rho \pi)^0$ Using a Time-Dependent Dalitz Plot Analysis, By BABAR Collaboration Phys. Rev. D 76, 012004,2007
- Luminosity and background measurements at the e⁺e⁻ DAFNE collider upgraded with the crab waist scheme, http://dx.doi.org/10.1016/j.nima.2010.04.044 (2010)
- Description and performances of luminosity and background detectors at the upgraded e⁺e⁻ DAFNE collider, http://dx.doi.org/10.1016/j.nima.2010.04.057 (2010)
- The SuperB Progress Report Detector, http://arxiv.org/abs/1007.4241 (2010)



DOCUMENT SCIENTIFIQUE

Christophe Beigbeder (leading engineer in charge of the proposal)

Age: 51 ans.

Cursus et Situation actuelle:

Ingénieur de recherche en électronique au Laboratoire de l'Accélérateur Linéaire (IN2P3 / CNRS) – Orsay.

2008-2010:

- Participation à la définition de l'architecture de l'électronique de l'expérience SuperB
- Installation des cartes d'acquisition du calorimètre de l'expérience LHCb au CERN.
- Responsable de la conception et la réalisation d'une carte d'acquisition pour l'expérience BAO radio.

1998-2008:

- Maintenance du DIRC de l'expérience BaBar.
- Responsable de la conception d'un ensemble de 256 cartes d'acquisition pour le calorimètre hadronique et électromagnétique de l'expérience LHCb au CERN.
- Etude de la partie numérique d'un ASIC mixte générateur d'horloge à retard programmable.

1991-1998:

• Conception, réalisation des cartes d'acquisition du DIRC de l'expérience BaBar à SLAC (Stanford, Etats-Unis).

1986-1991:

- Conception, réalisation de l'électronique du trigger de deuxième niveau de l'expérience H1 à Desy (Hambourg, Allemagne).
- Développement d'un ASIC numérique pour la recherche de Cluster.

1985-1986 :

Développement d'une carte processeur pour l'expérience NA31 à base de DSP.

Liste des 5 publications (ou brevets) les plus significatives des cinq dernières années:

Modelisation of SuperB Front-End Electronics Beigbeder C., Breton D., Maalmi J. *SuperB Workshop*, Orsay: France (2009) - http://hal.in2p3.fr/in2p3-00420900/fr/

The front end electronics for LHCb calorimeters Beigbeder C., Bernier R., Breton D., Caceres T., Callot O. et al Rapport de recherche (2000) - http://hal.in2p3.fr/in2p3-00008060/fr/

The dirc front-end electronics chain for babar. Bailly P., Chauveau J., Del Buono L., Genat J.F., Lebbolo H. et al Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 433 (1999) 450-455 - http://hal.in2p3.fr/in2p3-00006543/fr/



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Vanessa Tocut

Age: 37 ans

Cursus et Situation actuelle:

Depuis Décembre 1996 : <u>Ingénieur de Recherche en conception de circuits intégrés analogiques bas brui</u>t et mixtes (front-to-back) au Laboratoire de l'Accélérateur Linéaire (IN2P3 / CNRS) – Orsay.

2010-2006:

- Responsable du développement de <u>l'ASIC 'ASPIC' de lecture des signaux des CCD</u> de la caméra de LSST. Technologie AMS CMOS 0.35µm.
- Responsable d'une étude R&D pour un <u>ASIC de contrôle des horloges et de polarisation des CCD</u> de la caméra de LSST. Technologie à définir.
- Participation en collaboration avec le LPC Caen à <u>l'ASIC 'SCATS' chargé de la mesure du temps (TDC)</u> pour le détecteur SuperB. Technologie AMS CMOS 0.35μm.
- Participation en collaboration avec le LPC Caen à <u>1'ASIC 'SNATS' chargé de la mesure du temps (TDC)</u> pour le détecteur SuperNemo. Technologie AMS CMOS 0.35μm.

2007-2000:

- Conception d'un <u>ASIC générateur d'horloges à retard programmable</u> pour une horloge d'entrée de 40MHz pour les calorimètres du détecteur ATLAS, la calibration des photomultiplicateurs, le détecteur Preshower. Réalisation du banc de test et mise en production de 3500 exemplaires distribués a la collaboration (CERN, Université de Barcelone, LPSC Clermont Ferrand) Technologie AMS CMOS 0.8µm
- Conception d'un ASIC de type <u>'shaper' 4 voies pour le front-end du calorimètre de LHCb</u>.
 Conception du banc de test, réalisation des tests de vieillissement et mise en production de 3500 exemplaires.
- Participation à la <u>conception d'une mémoire analogique de type pipeline</u> en collaboration avec le DAPNIA/CEA & Columbia Nevis Lab. Fréquence d'échantillonnage : 40MHz, fréquence de lecture 5MHz, profondeur de 144 points. Technologie durcie DMILL. Participation au <u>transfert vers l'industrie</u> de la mémoire analogique pour la société METRIX.
- Participation en collaboration avec le LPNHE de Jussieu à l'upgrade de l'ASIC chargé de la mesure du temps (TDC) pour le détecteur BaBar. Mise en place du circuit sur le site du Stanford Linear Accelerator, San Francisco pour équiper 11.000 voies.
- Développement d'un <u>semi-flash ADC 10 bits/100Mhz</u> moins de 100mW projet AUGER.
 Technologie AMS CMOS 0.35μm & BiCMOS SiGe 0.35μm.

Liste des 5 publications (ou brevets) les plus significatives des cinq dernières années:

- "Large Dynamic Range Integrated Front-End Electronics for Photomultiplier Tubes" GENOLINI B., RAUX L., de LA TAILLE C., POUTHAS J., TOCUT V., 2005, Nuclear Instruments and Methods in Physics Research A, In press (Presented at the 2005 Beaune conference on Photodetection)
- A 100Ms/s-10 bits Two Step Flash ADC with Auto Zero CMOS Input Comparators Tocut V. Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Porto Rico (2005) [in2p3-00195405 version 1]



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Jaroslav Va'Vra

The résumé of Jerry Va'Vra can be found online at the URL http://www.slac.stanford.edu/~jjv/.

7.3. STAFF INVOLVMENT IN OTHER CONTRACTS

	Nom de la personne participant au projet / name	Personne . Mois / PM	Intitulé de l'appel à projets, source de financement, montant attribué / Project name, financing institution, grant allocated	Titre du projet : Project title	Nom du coordinateur / coordinator name	Date début & Date fin / Start and end dates
N°	TOCUT Vanessa	14	ANR Programme blanc	LSST	P. Antilogus	10/2011 → 10/2013
N°	PUILL Véronique	14.4	ANR Programme blanc	SIPMED	L. Menard	07/2011 → 06/2015
N°	PUILL Véronique	9.6	ANR Programme blanc	VITESSE	A. Lounis	01/2009 → 12/2013
N°	LEBBOLO Hervé	12	ANR Programme blanc 2011	LSST	P. Antilogus	10/2011 → 10/2013
N°	LEBBOLO Hervé	12	ANR Programme blanc	EASIER	Letessier	10/2011 → 10/2014