



French-Ukrainian WORKSHOP

Instrumentation developments
for high energy physics



October 12-14, 2026

IJCLab, Orsay - France

université
PARIS-SACLAY



Module production for the ATLAS Inner Tracker (ITk)

Dmytro Hohov on behalf of the IJCLab-ITk team

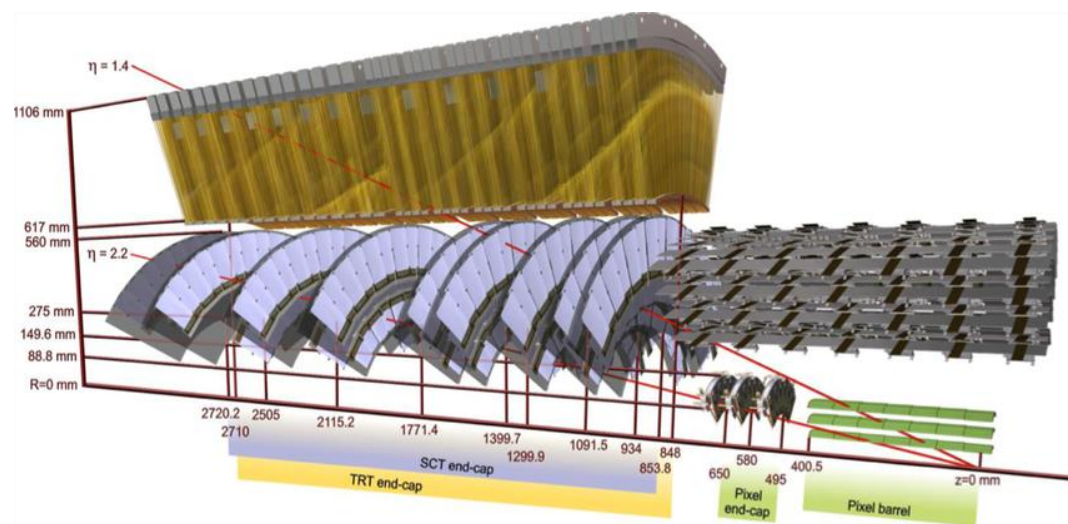
ijcLab
Irène Joliot-Curie
Laboratoire de Physique
des 2 Infinis





ATLAS Upgrade: Inner Detector -> Inner Tracker

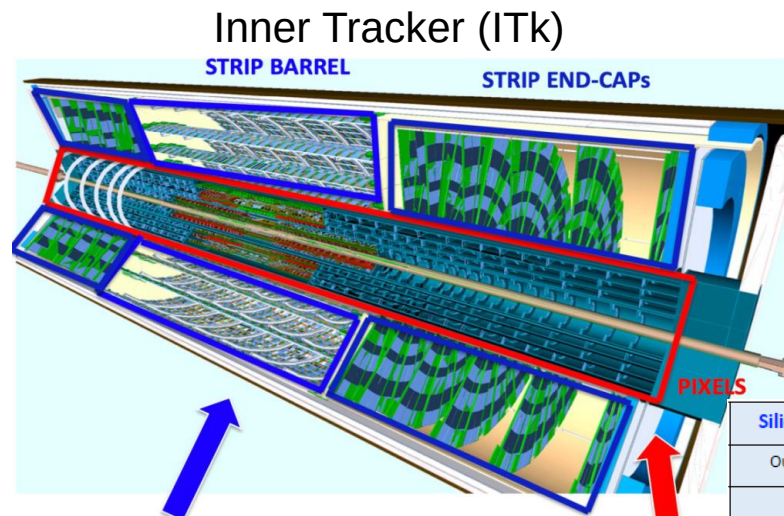
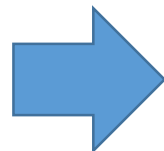
ID is an innermost detector, 6.2 m long and 1.2 m in radius.
Composed of **TRT**, **SCT** and **Pixel Detector**



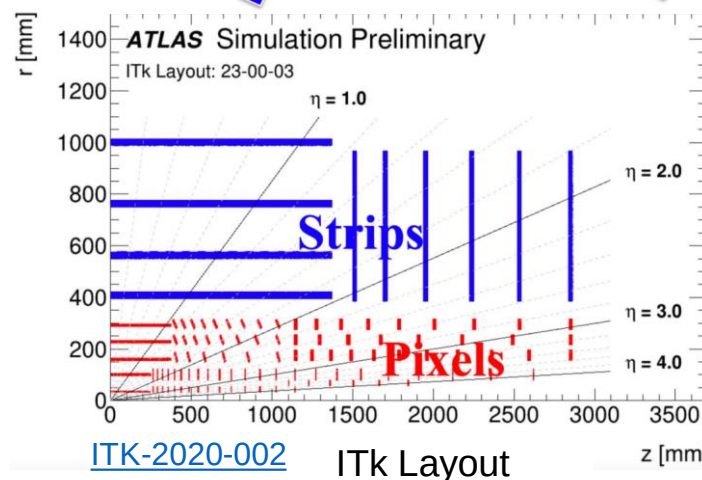
[The ATLAS Collaboration et al 2008 JINST 3 S08003](#)

Pixel Detector:

composed of 4 barrel Layers (IBL, B-Layer, L1, L2) 3 disks in two end caps, 2 m² of active area, $|\eta| < 2.5$
92 millions of pixels, 200 (250) μm thick, pitch 50 x 250 (400) μm^2



CERN-LHCC-2017-005



[ITK-2020-002](#)

ITk Layout

Silicon Strips
Outer layers
165 m ²
17 888 modules
60 Million channels
Silicon Pixels
Inner layers
13 m ²
8372 modules
5 Billion channels

$|\eta| < 4$

50x50 μm^2
25x100 μm^2



Silicon pixel detector technologies

❑ **Planar sensors:** highly doped implant on top of low-doped Si bulk **n-in-n (ID)**, **n-in-p (ITk)**

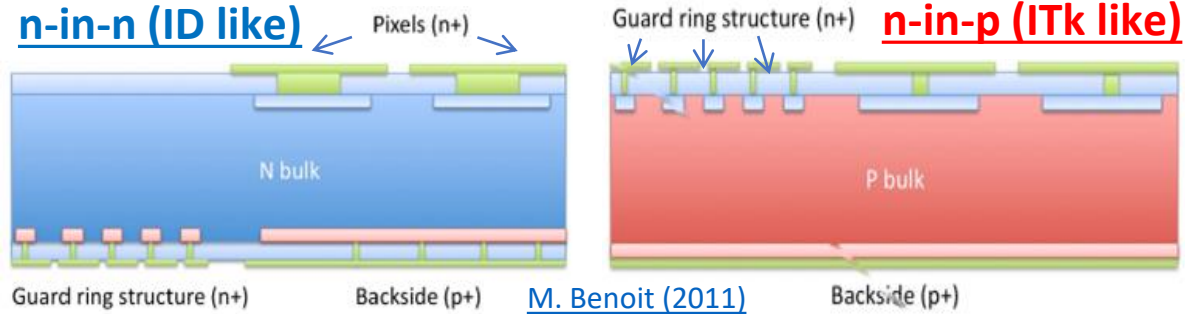
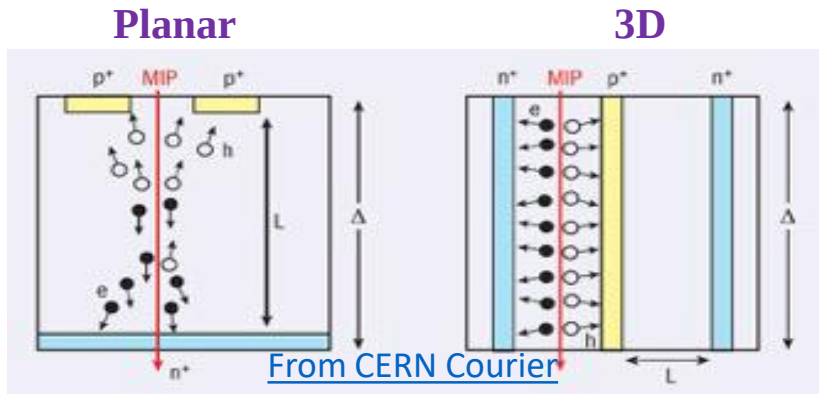
✓ Simpler production process than 3D

❑ **3D sensors:** highly doped Si columns (p^+ and n^+) implanted vertically through low-doped Si bulk

✓ Higher electric field for the same applied voltage → low depletion voltage

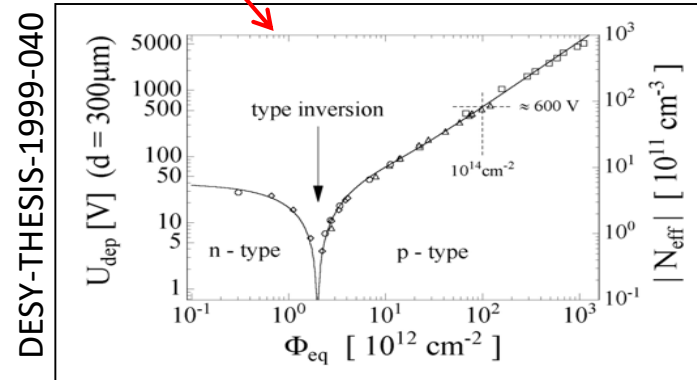
✓ Smaller drift time → fast response

✓ **Smaller drift distance** → **less trapping probability** → **improved radiation hardness**



- Collect electrons
- Guard rings are not on a front side
- Double-sided processing
- Type inversion of a bulk

- Collect electrons (3 times faster than holes)
- No type inversion
- Can be operated partially depleted
- Single-sided processing
- Guard rings are on a front-end side

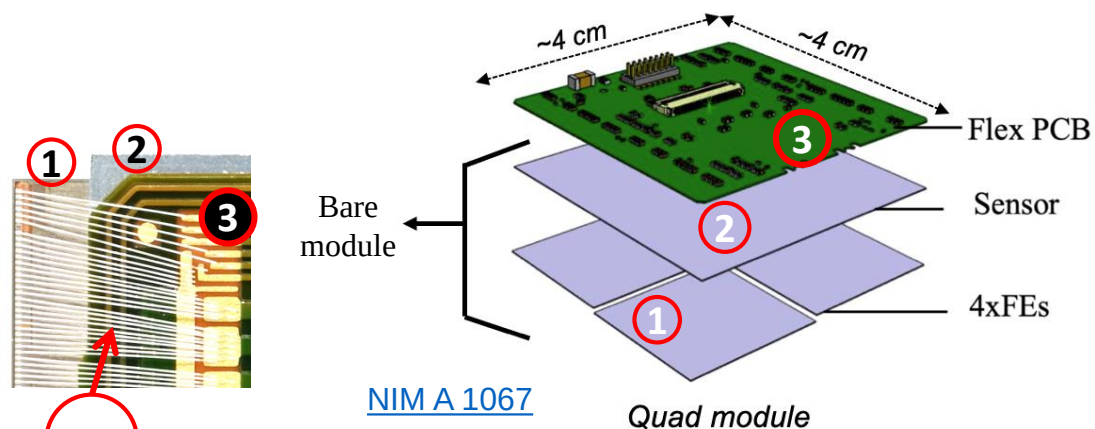


Space charge sign inversion (SCSI) NIM A426 (1999)

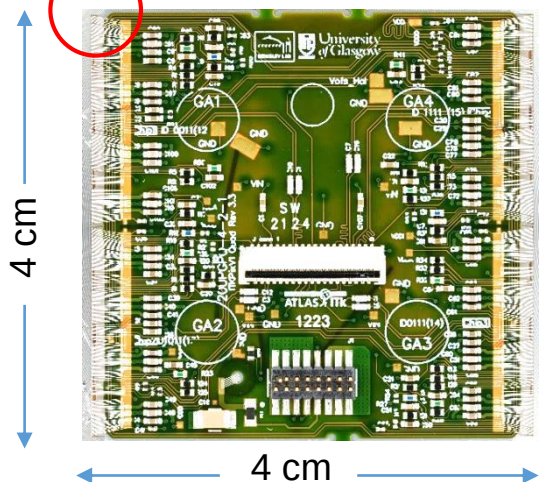


Hybrid Pixel Modules in ITk

Hybrid detector: FE readout chip connected to the sensor by bump-bonds



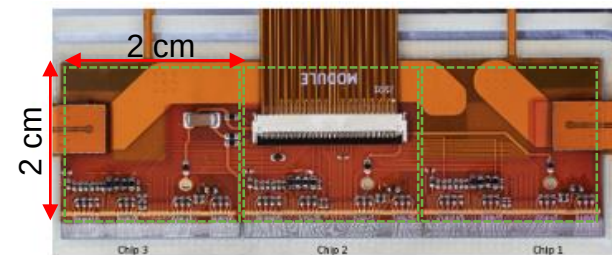
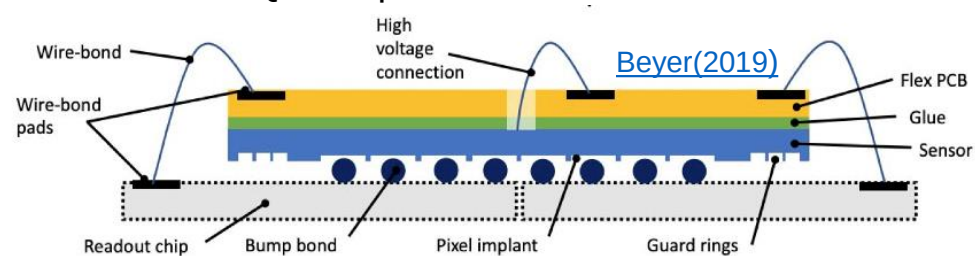
[NIM A 1067](#)



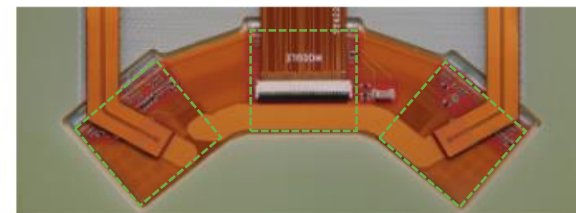
Two types of modules in ITk:

- **Quad** modules: quad bare module (4 FEs bump bonded to one sensor) + a flexible PCB
- **Triplet** modules 3 single FE bare modules connected to the same flexible PCB

Quadruplet module cross-section



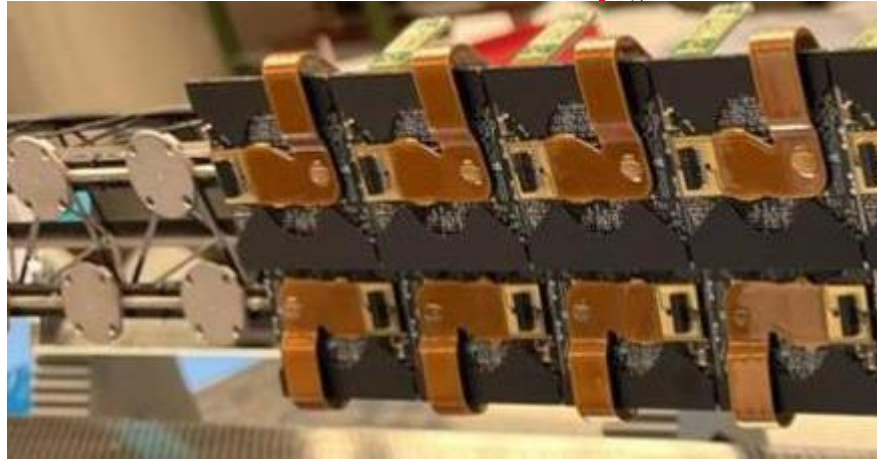
a) 3D triplet for the Inner System barrel stave



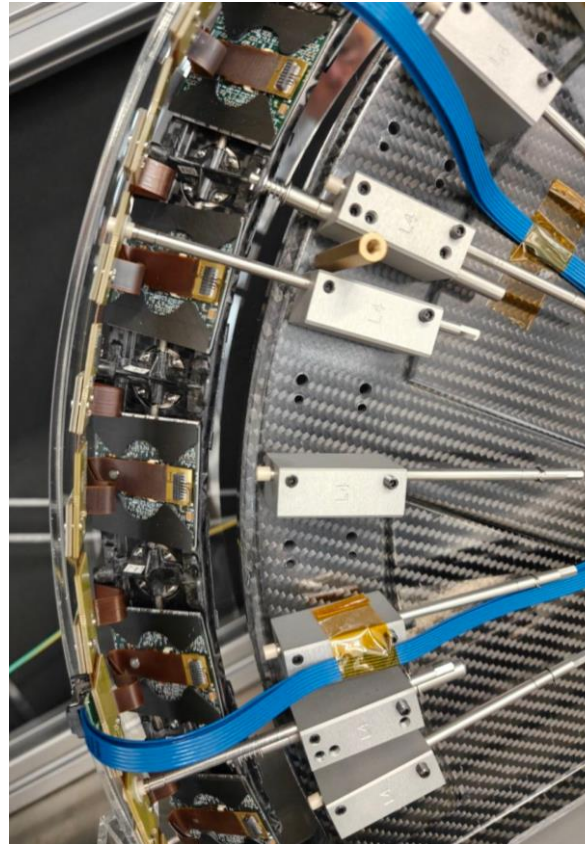
b) 3D triplet for the Inner System endcap ring



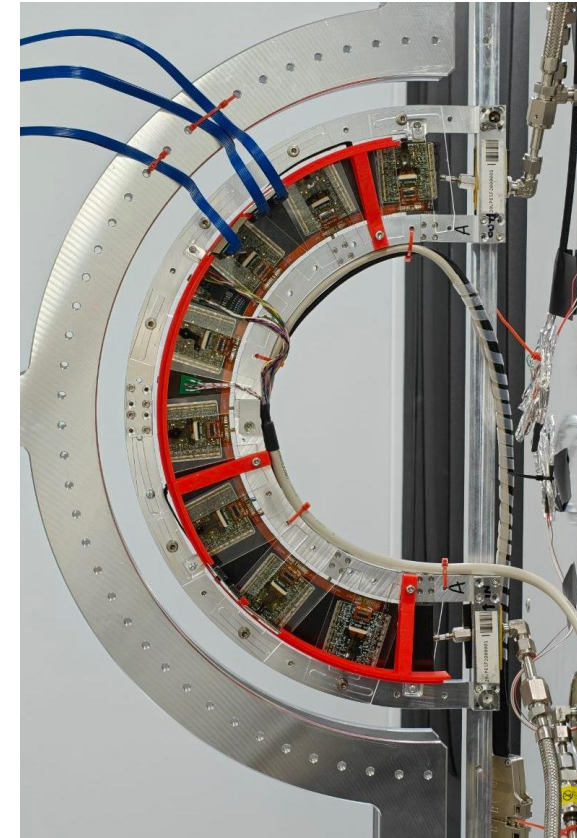
Loaded ITk support structures



Flat section: Longerons



Inclined Half-Ring



Outer Endcap Half-Ring



ITk Pixel Detector layout

The ITk Pixel detector sensor technologies:

- *L2, L3, L4 - **Planar** n-in-p sensors (150 μm)*
- *L1, R1 - **Planar** n-in-p sensors (100 μm)*
- *L0 : barrel layer (B0) + ring layers (R0, R0.5) - **3D** n-in-p sensors 250 μm (150 active + 100 support)*

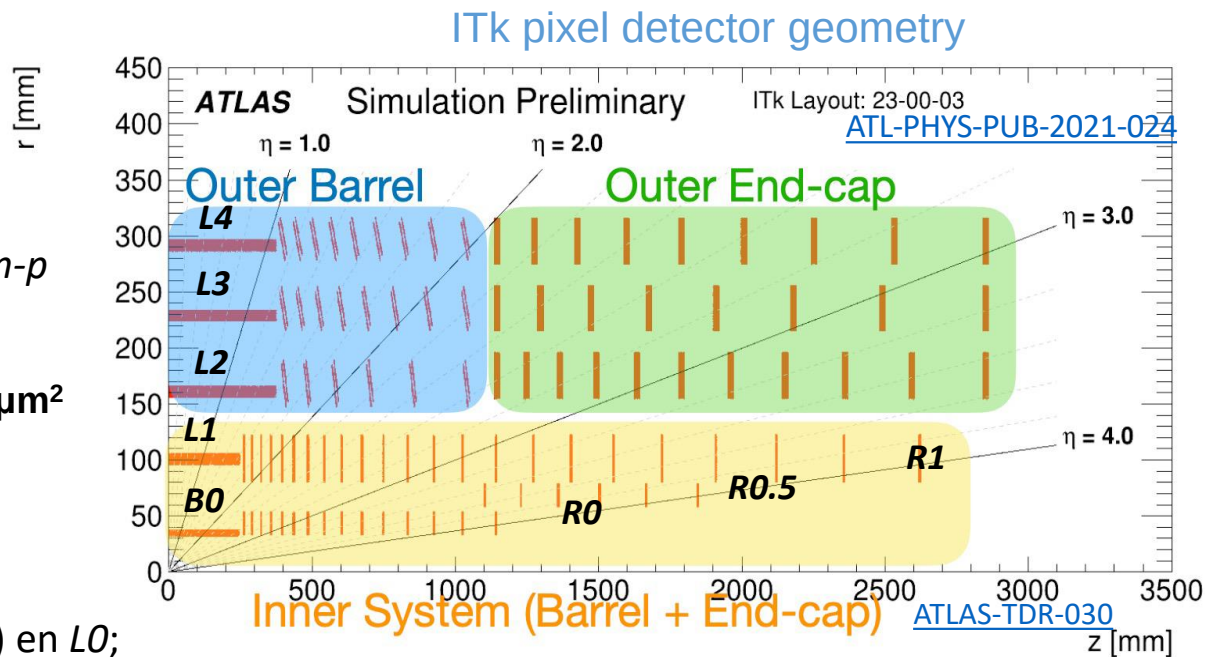
Pixel pitch **50 x 50 μm^2** in all layers, only in *B0* – **25 x 100 μm^2** to improve the resolution of tracks in transverse direction.

Inner System (*L0, L1*) - will be replaced after 2000 fb^{-1} :

- **396 triplets** (3 capteurs + 3 puces FE sur un flex PCB) en *L0*;
- **1160 quads** (1 capteur + 4 puces FE sur un flex PCB) en *L1*.

Outer System (*L2, L3, L4*) :

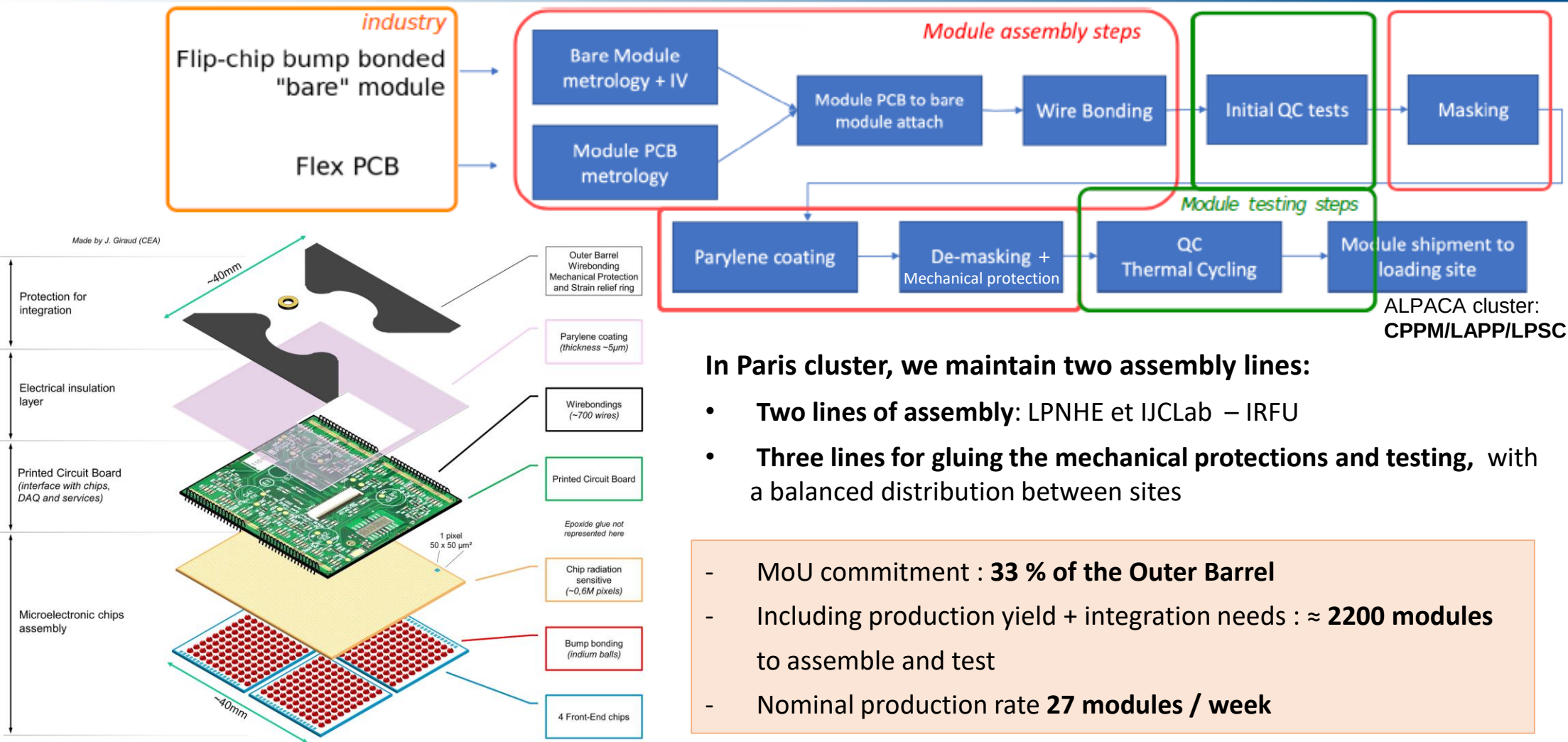
- **Outer Barrel (OB)** - (3 layers) : **4472 quads**;
- Outer Endcap (3 ring layers)) : **2344 quads**.



Type	Manufacturer
planar 100 μm thick	MICRON (UK), FBK (IT)
planar 150 μm thick	MICRON (UK), HPK (JP)
3D 50x50 μm^2 cell	FBK (IT), SINTEF (NO)
3D 25x100 μm^2 cell	FBK (IT)



Module Production Chain (Paris Cluster)

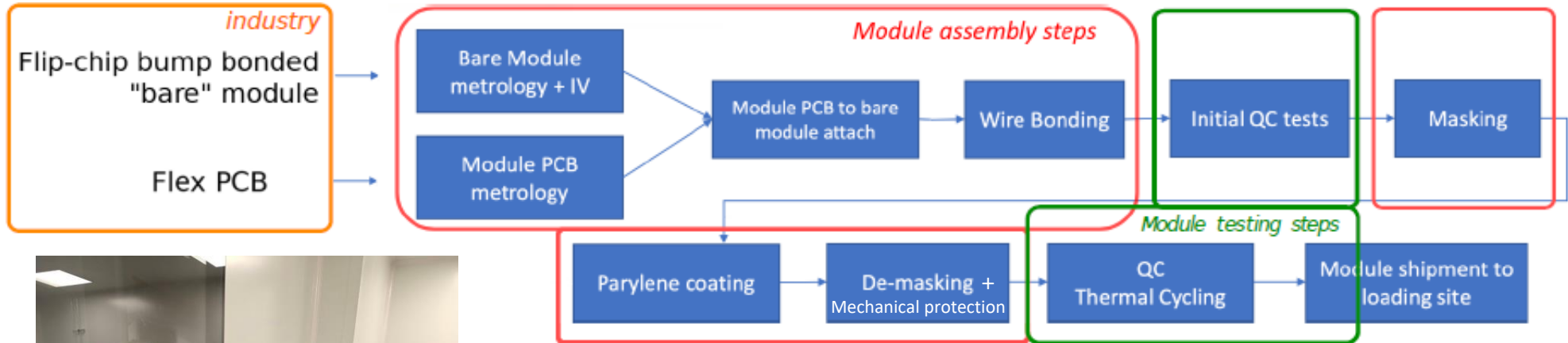


In Paris cluster, we maintain two assembly lines:

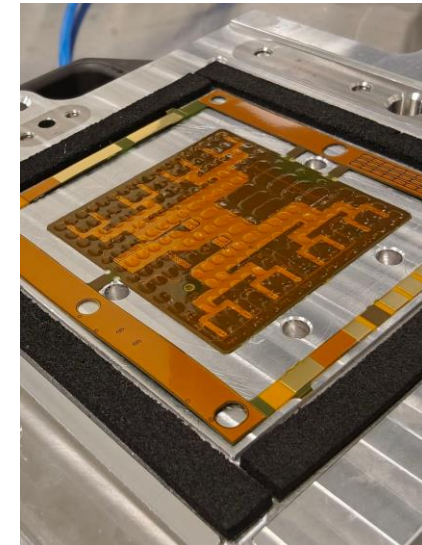
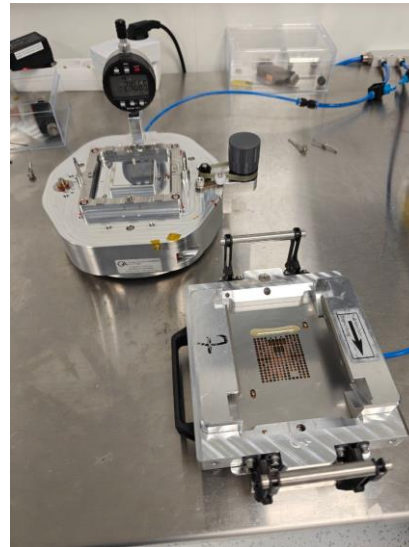
- **Two lines of assembly:** LPNHE et IJCLab – IRFU
 - **Three lines for gluing the mechanical protections and testing,** with a balanced distribution between sites
- MoU commitment : **33 % of the Outer Barrel**
 - Including production yield + integration needs : **≈ 2200 modules** to assemble and test
 - Nominal production rate **27 modules / week**



Module Production Chain (Paris Cluster)

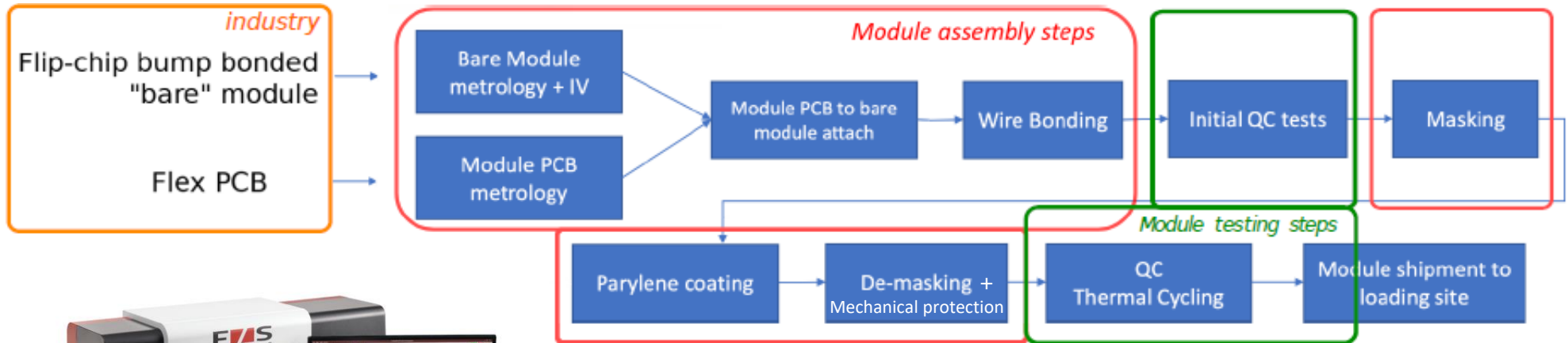


Gluing

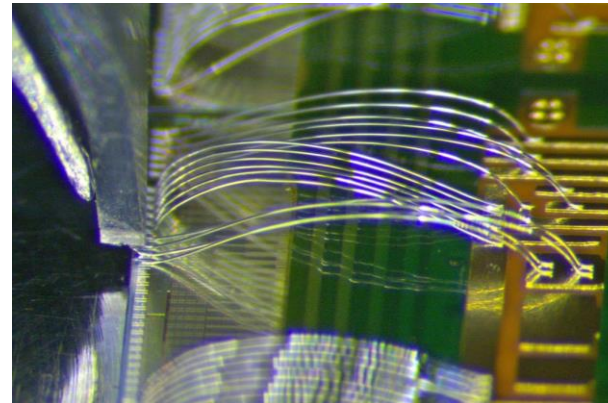




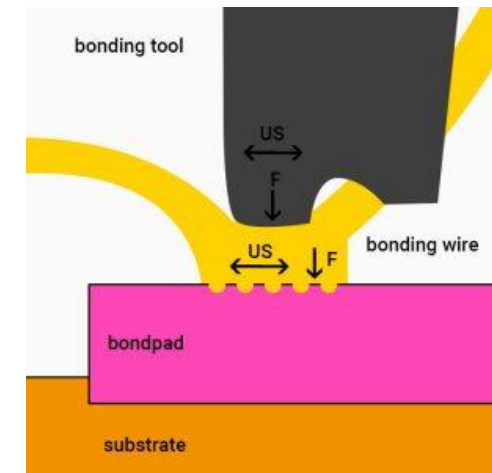
Module Production Chain (Paris Cluster)



Wire Bonding



Wedge bonding principle

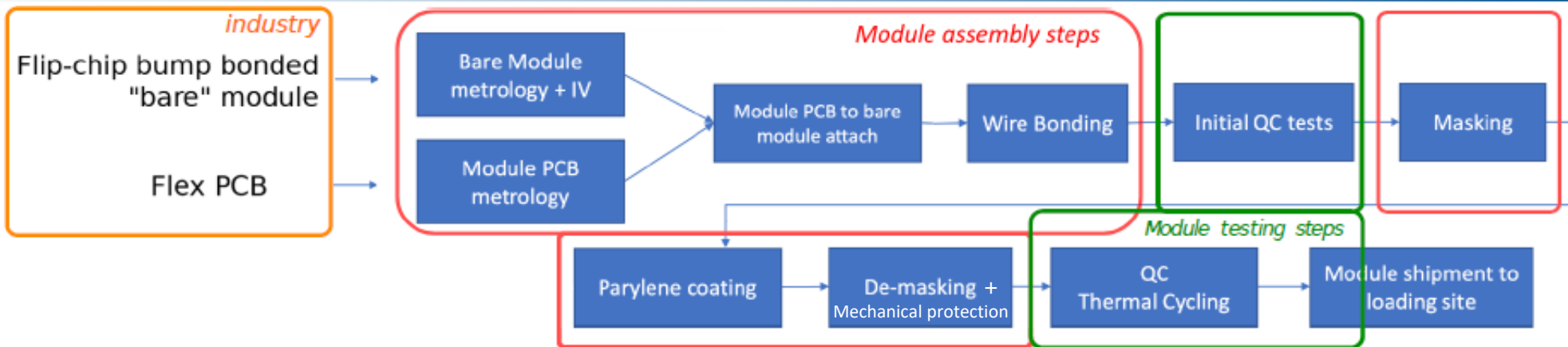


710 wirebonds (aluminium 25 μ m) per quad module

Bond formation: Force + Ultrasonic power



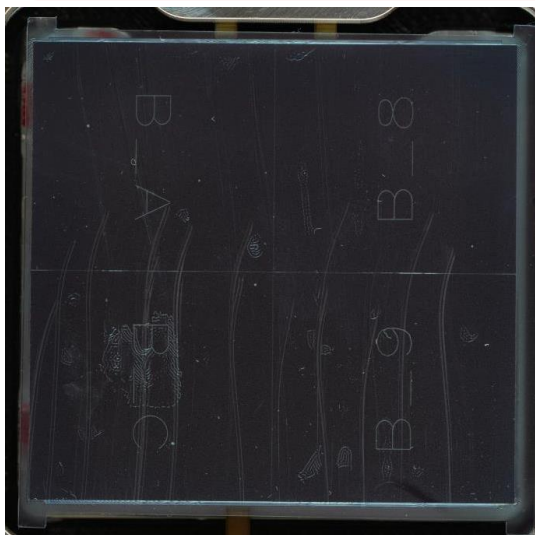
Module Production Chain (Paris Cluster)



Coating + Canopies



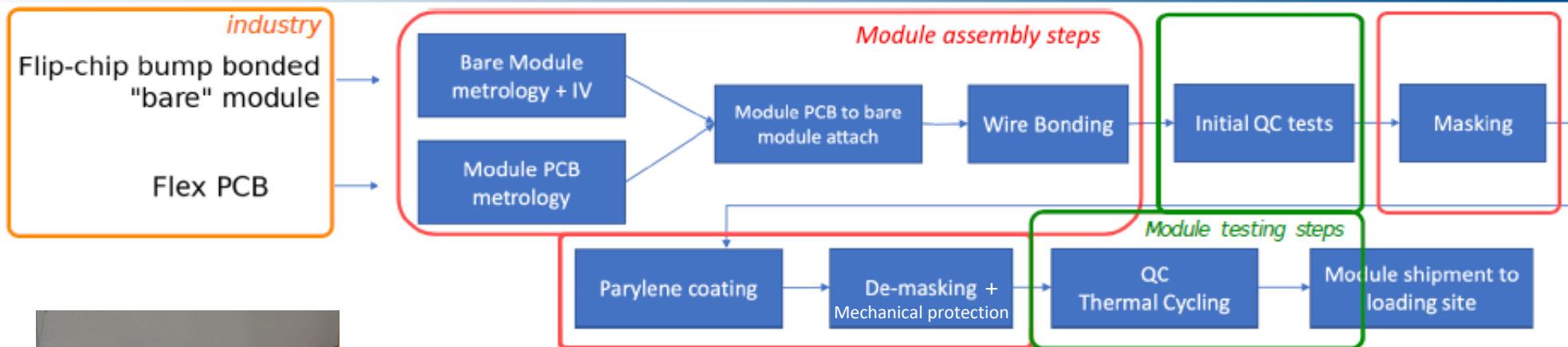
Masking before parylene coating



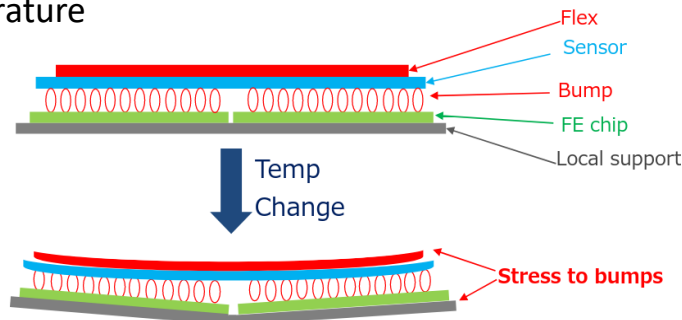
Wire-bond protection canopies



Module Production Chain (Paris Cluster)



- Thermal cycles between **-45 °C and +40 °C**
- Soak time: > **15 min** to stabilize the module temperature



[ATL-ITK-PROC-2024-018](#)

Electrical Quality Control (e-QC)

- Used to verify the proper functioning of the module
- Characterization at **warm** and **cold** temperatures: 20 °C / -15 °C
- Typical duration of one e-QC sequence: ~ **2-4 h**



e-QC Testing

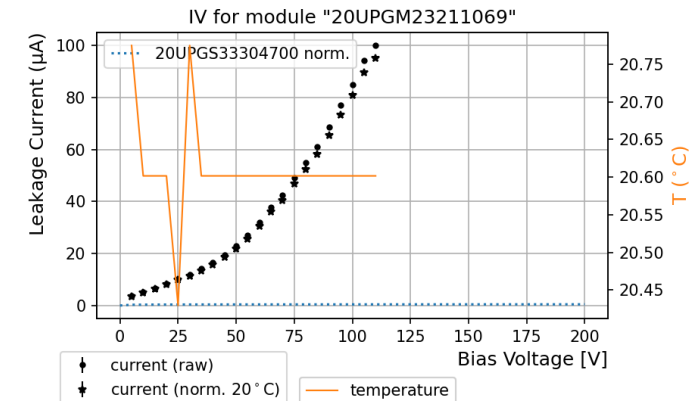
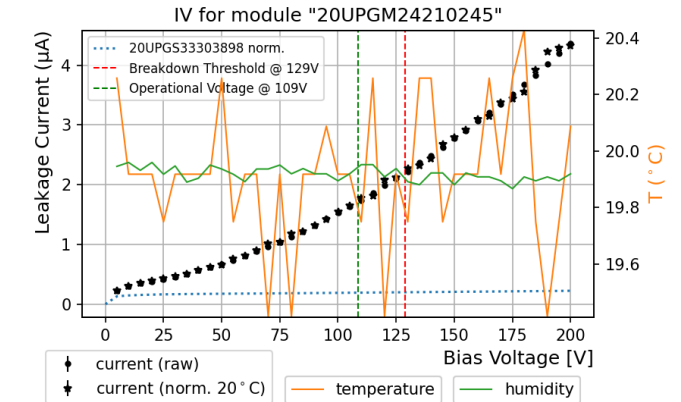
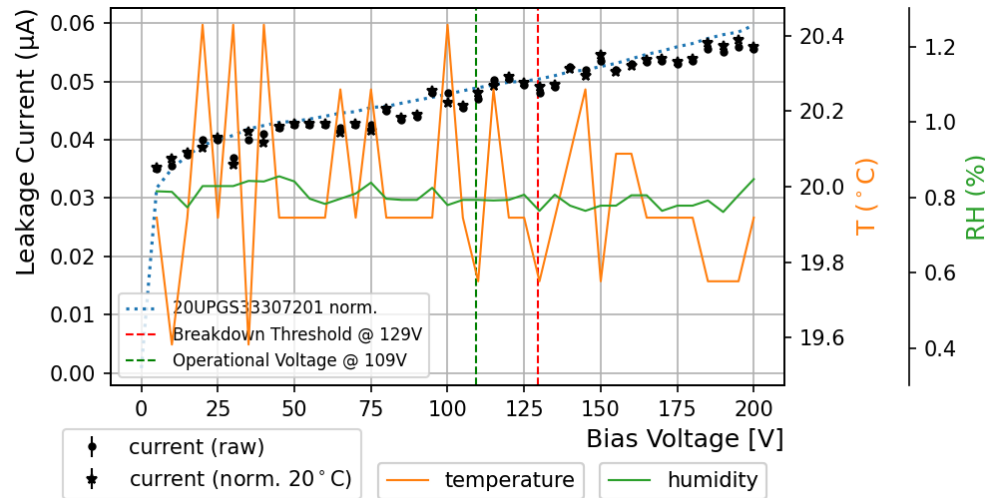


Electrical QC tests

e-QC procedure:

progressive sequence: from low level to advanced tests

➤ Sensor IV



- ✓ Verification of the sensor functionality before continuing the QC sequence
- ✓ To check: **leakage current** and **breakdown voltage**



e-QC procedure:

progressive sequence: from low level to advanced tests

- Sensor IV
- **ADC calibration**
- **Analog readback**
- **Shunt-LDO test**
- **VCAL calibration**
- **Injection capacitance**
- **LP mode**
- **Data transmission**

Readout chip characterization

- Calibration and monitoring of internal voltages, currents and temperatures
- Powering: Serial Powering and Low Power mode
- Calibration of the injection (DAC, Capacitance)
- Validation of FE → DAQ data transmission links and aggregation modes



e-QC procedure:

- Sensor IV
- ADC calibration
- Analog readback
- **Shunt-LDO test**
- VCAL calibration
- Injection capacitance
- LP mode
- Data transmission

Shunt-LDO for **serial powering**

Several modules are powered in series with the same current

- Lower current in services → lower power losses
- Higher cable resistance becomes acceptable → thinner cables and less material
- Fewer independent power lines inside the detector
- Main constraint: the module must present a stable effective impedance to the power supply

SLDO : stabilizes VDDA / VDDD around 1.2 V and the effective module impedance. Absorbs excess current through the shunt branch.



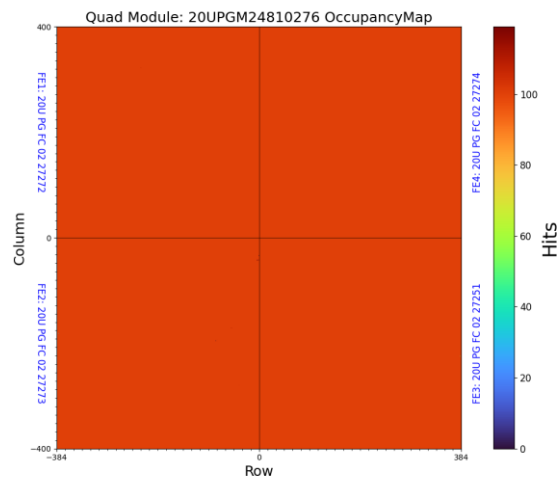
e-QC procedure:

- Sensor IV
- ADC calibration
- Analog readback
- Shunt-LDO test
- VCAL calibration
- Injection capacitance
- LP mode
- Data transmission
- **Pixel matrix scans and tuning**

► MHT ► TUNING ► PFA

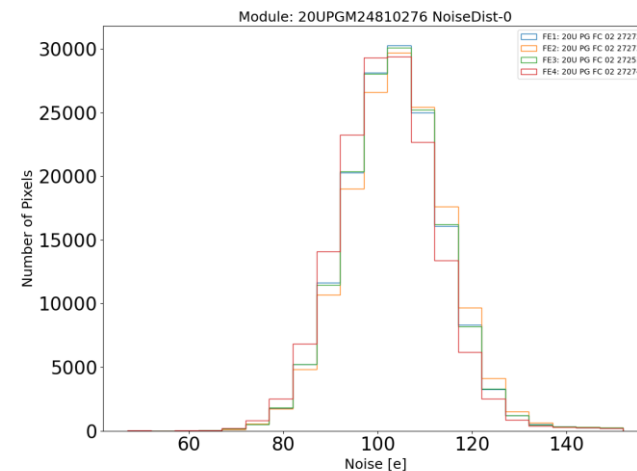
Minimal Health Test

- ✓ **Quick verification** of the pixel matrix functionality
- ✓ Minimal set of scans: Digital, Analog, Threshold and ToT (Time over Threshold)



Digital / analog scans : pixel response to 100 injections

- Failure : $|N_{\text{hits}} - N_{\text{inj}}| > 2$



ENC distribution (Equivalent Noise Charge) :

- Distribution below the 300 électrons
- High-ENC pixels < 1 % (1536 pixels)



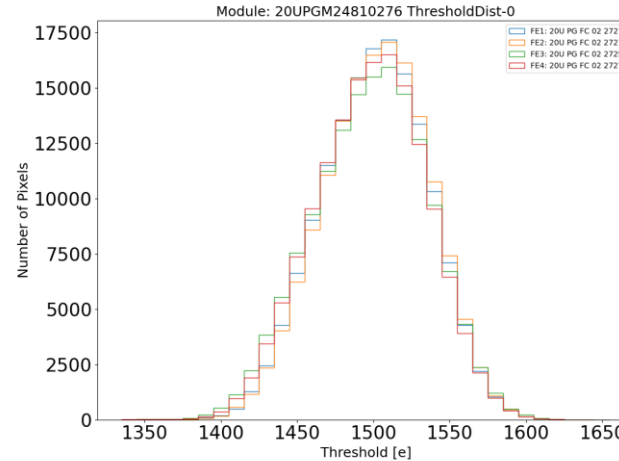
e-QC procédure:

- Sensor IV
- ADC calibration
- Analog readback
- Shunt-LDO test
- VCAL calibration
- Injection capacitance
- LP mode
- Data transmission
- **Pixel matrix scans and tuning**

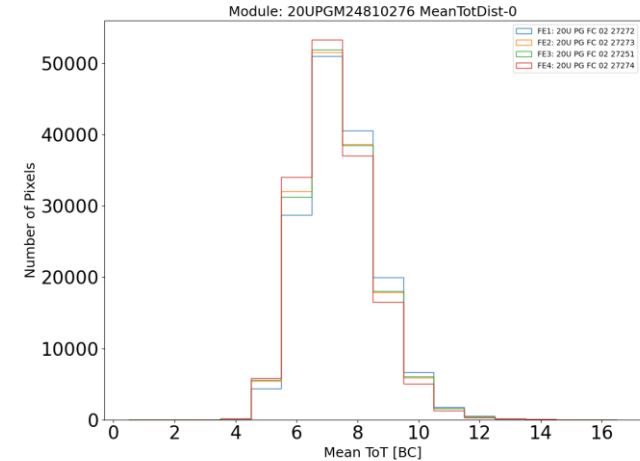
► MHT ► **TUNING** ► PFA

Tuning of the pixel matrix

- ✓ Adjustment of pixel **thresholds** and **ToT** around the target values
- ✓ Control of threshold dispersion, noise and ToT response
- ✓ Verification that the pixel matrix tuning is successful



- Mean threshold after tuning:
 $1500 \pm 150 \text{ e}^-$
- Dispersion RMS < 100 e^-



Target ToT response: **$7 \pm 1 \text{ BC}$**
(Bunch Crossing = 25ns) for an injected charge of **6000 e^-**



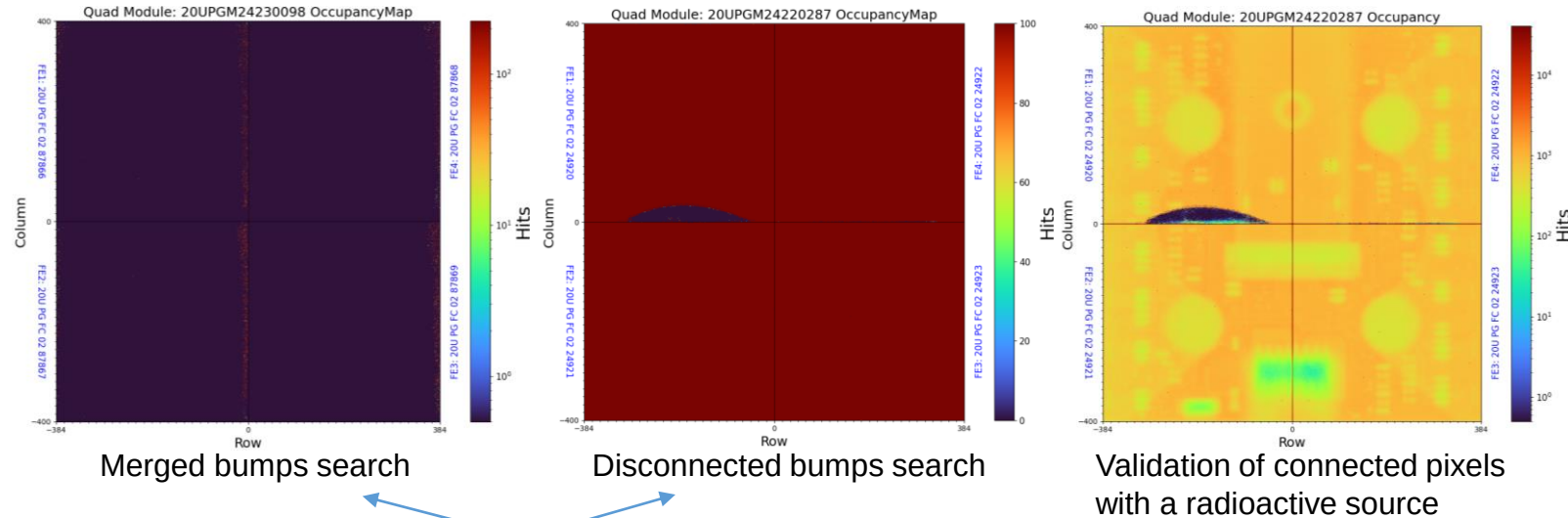
e-QC procédure:

- Sensor IV
- ADC calibration
- Analog readback
- Shunt-LDO test
- VCAL calibration
- Injection capacitance
- LP mode
- Data transmission
- **Pixel matrix scans and tuning**

► MHT ► TUNING ► PFA

Pixel Failure Analysis

- ✓ Identification of non-functional pixels after tuning
- ✓ Search for **bump bonding defects**: disconnected / merged bumps



Cross-talk scans

Current global criterion:

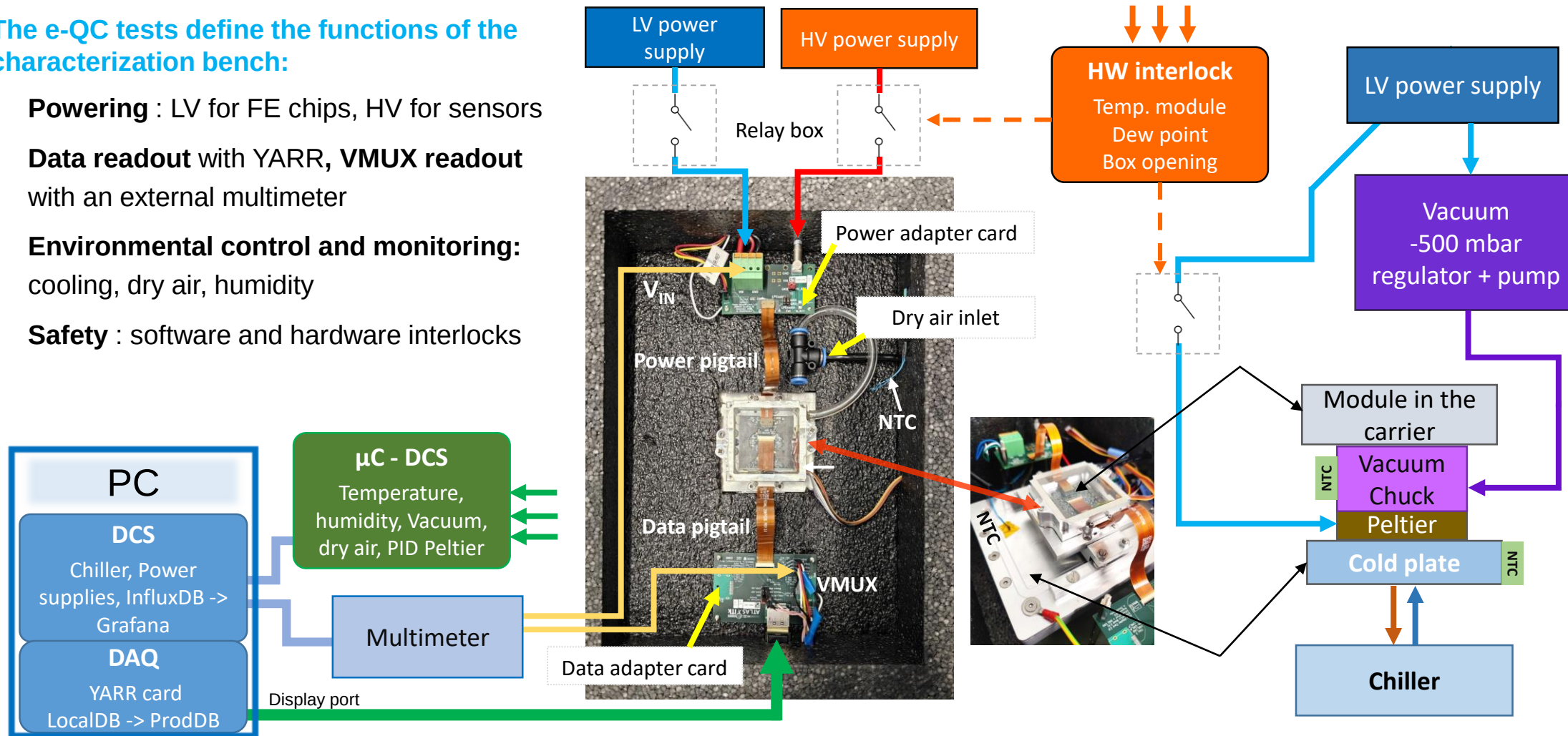
- Non-functional pixels < 5 % (7680 pixels) per FE chip

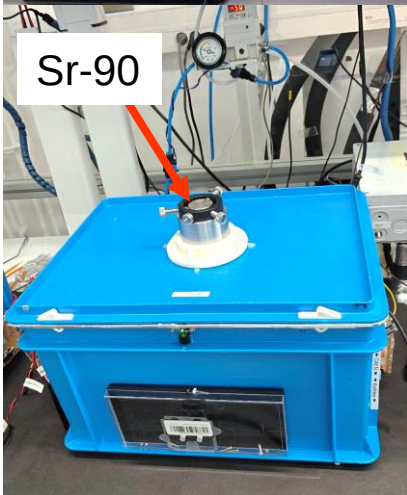
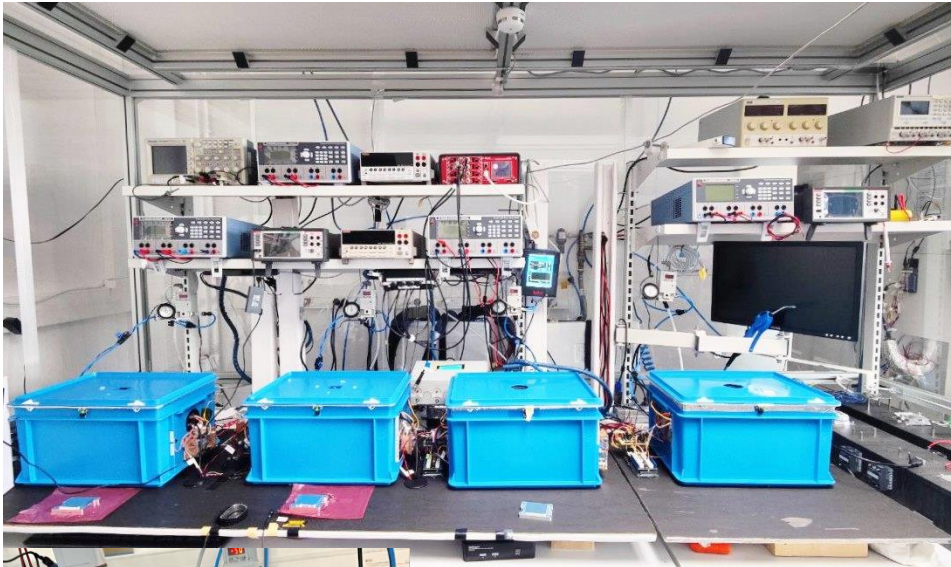


Test bench e-QC: main components

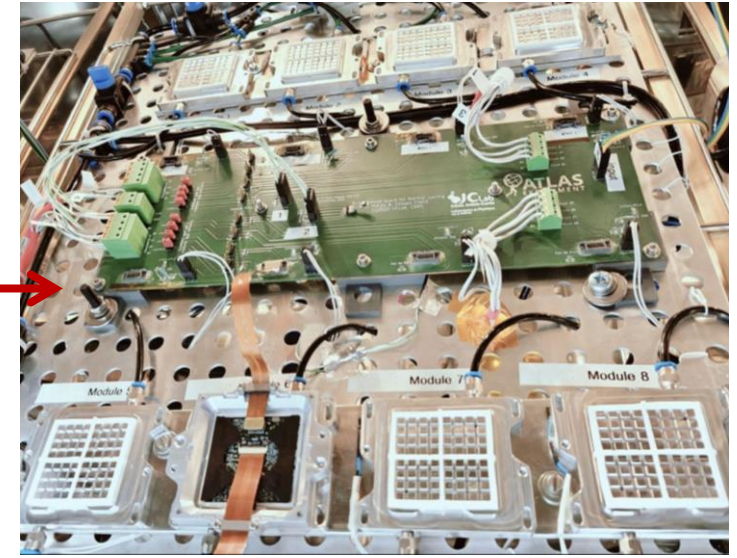
The e-QC tests define the functions of the characterization bench:

- **Powering** : LV for FE chips, HV for sensors
- **Data readout** with YARR, **VMUX readout** with an external multimeter
- **Environmental control and monitoring**: cooling, dry air, humidity
- **Safety** : software and hardware interlocks





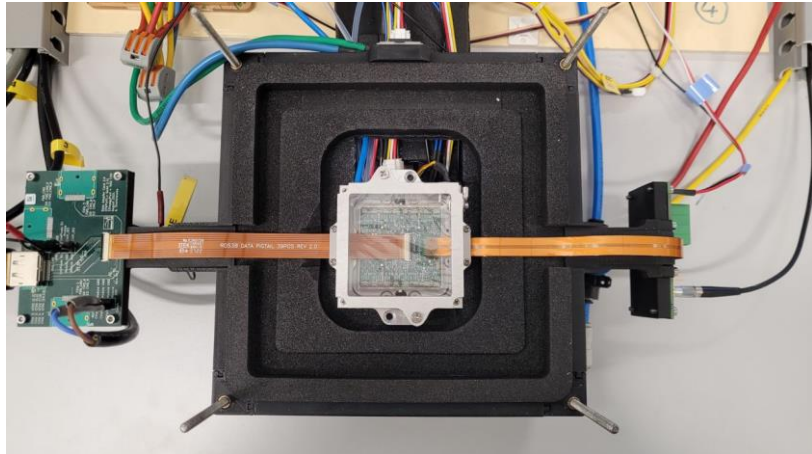
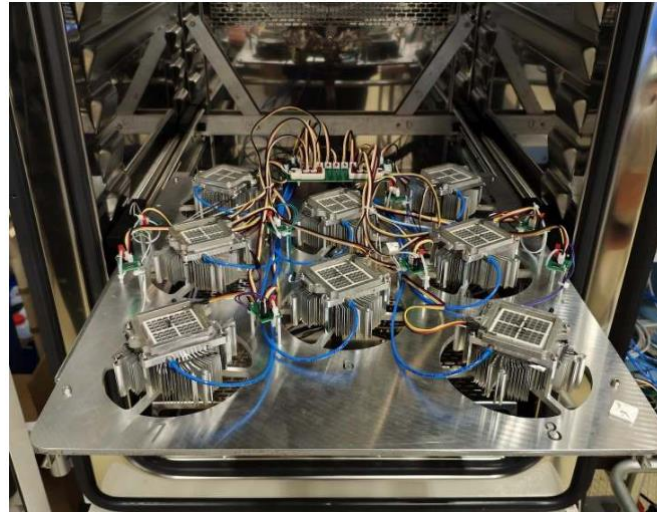
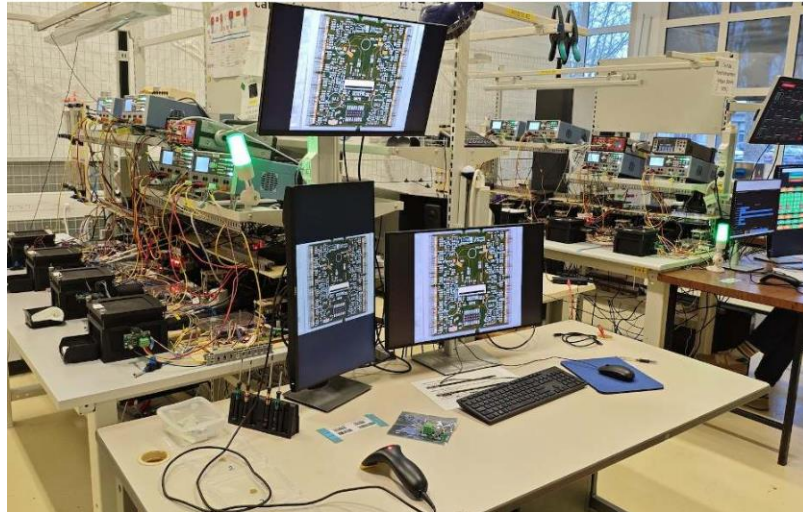
- 4 (+ 1) cold boxes for warm and cold tests
- Each cold box can be used for source scans
- One shared 37 MBq Sr-90 source



- Climate chamber for thermal cycling
- Capacity: up to 8 modules in parallel



IRFU test infrastructure



- 12 cold boxes for warm and cold tests
- Thermal cycling in a climate chamber: up to 8 modules in parallel
- 4 cold boxes dedicated to source scans with four 10 MBq Sr-90 sources

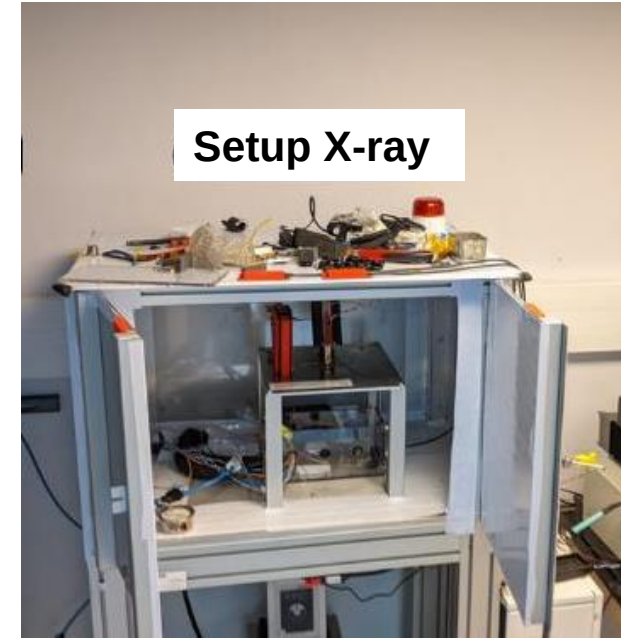
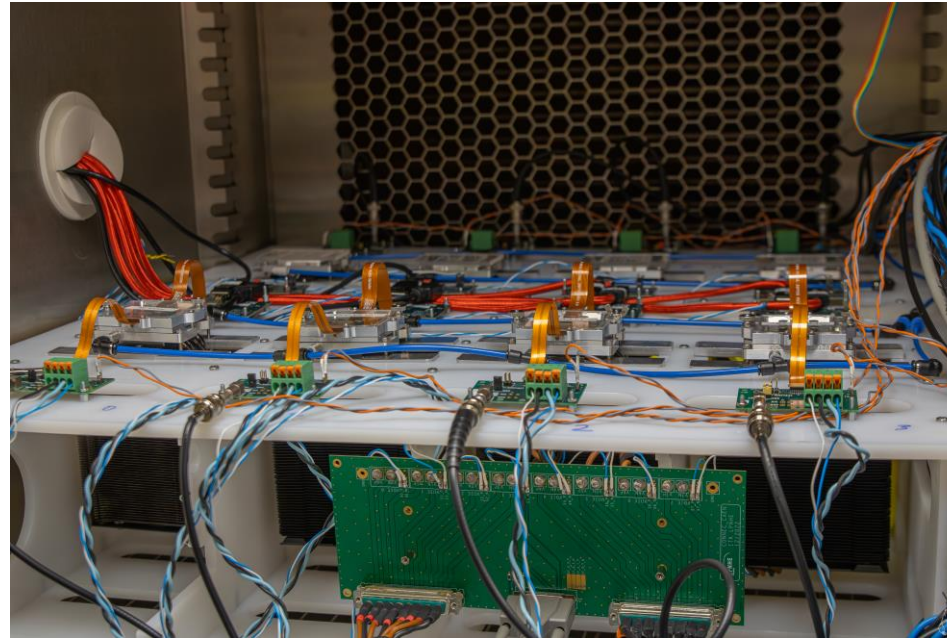




LPNHE test infrastructure



Full e-QC test chain performed in a climate chamber



Setup X-ray

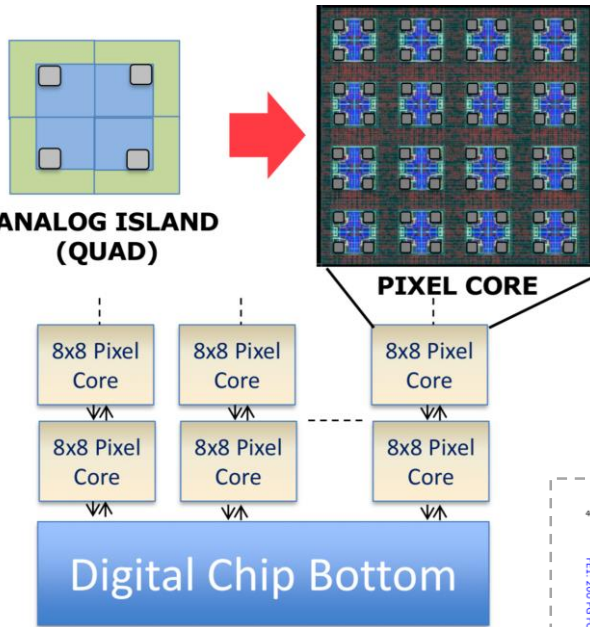
- Fully equipped setup for 8 modules
- Two monitored vacuum lines, each for 4 modules
- Individual powering and monitoring: LV, HV, temperature
- X-ray setup for source scans



Issues observed during e-QC tests

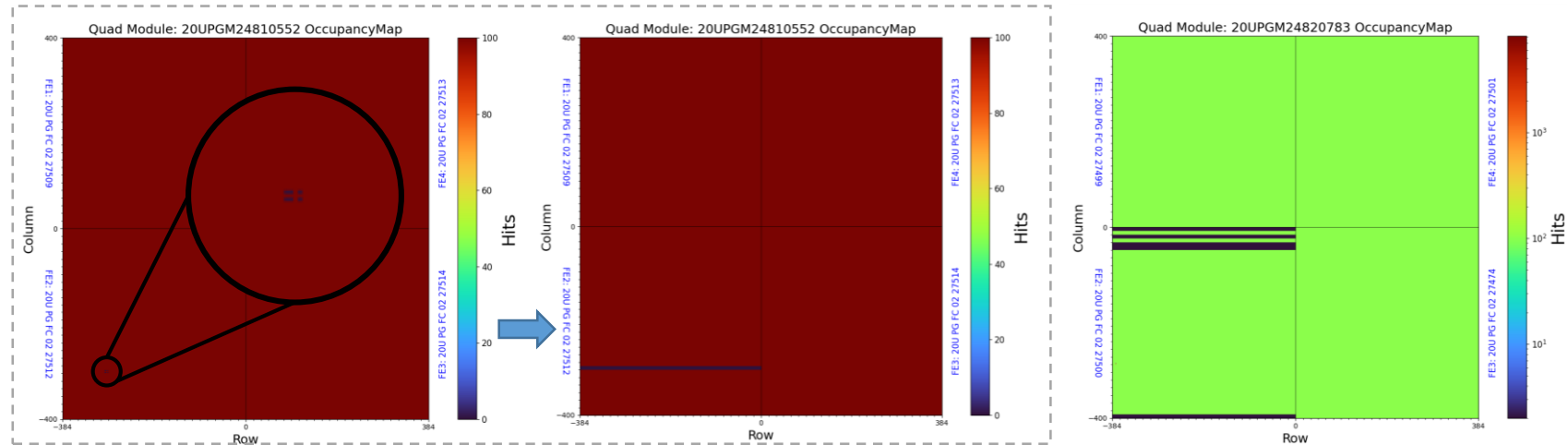
Core-column (CC) issue →

- Abnormal behaviour affecting one core column
- Mainly observed during injection / calibration scans
- **Symptoms** : readout processor deadlock, lost hits, data corruption, internal chip timing issues
- **Possible origin**: mechanical damage related to hybridisation or dicing
- **Mitigation** : disabling the affected core column (-> dead region)



Core column - Vertical chain of digital cores 8×8 pixels

- Carries timing, trigger, configuration and readout

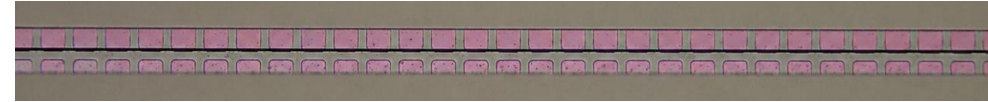




Main yield drivers

1. Assembly and handling (~94%)

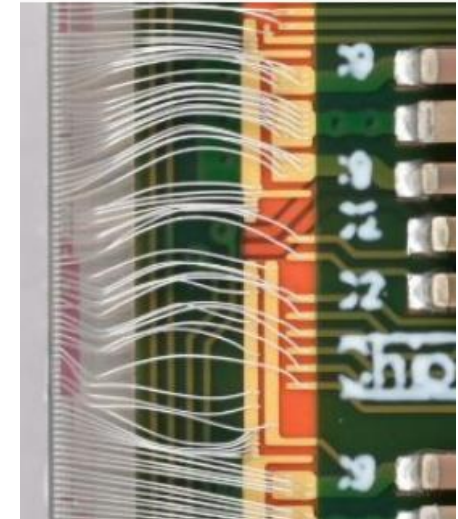
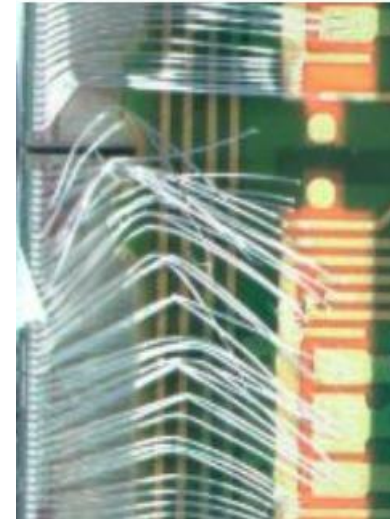
- Dominated by **handling / gluing accidents / sensor cleavage**
- Wire bonding yield is already high: **~98.8%**



Sensor cleavage leads to a strong leakage-current increase and permanent module failure

2. Parylene and masking steps

- Several masking / unmasking operations before coating increase handling risk
- Significant number of damaged modules, 2.5% of modules classified as dead
- Strong improvement observed over time



Broken wire-bonds



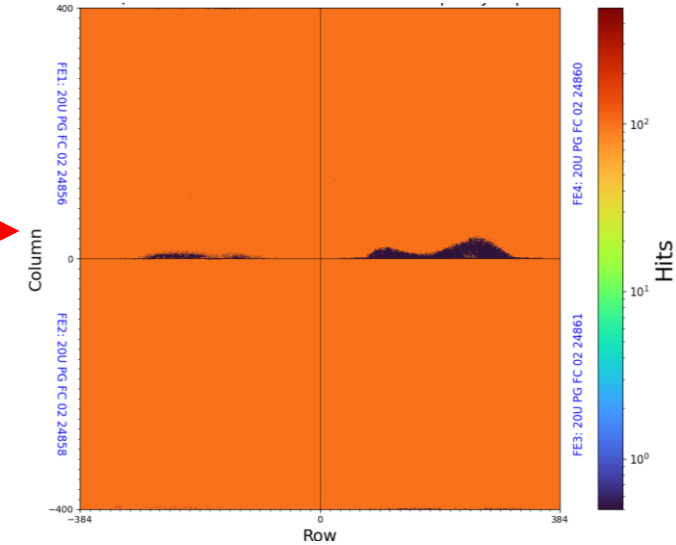
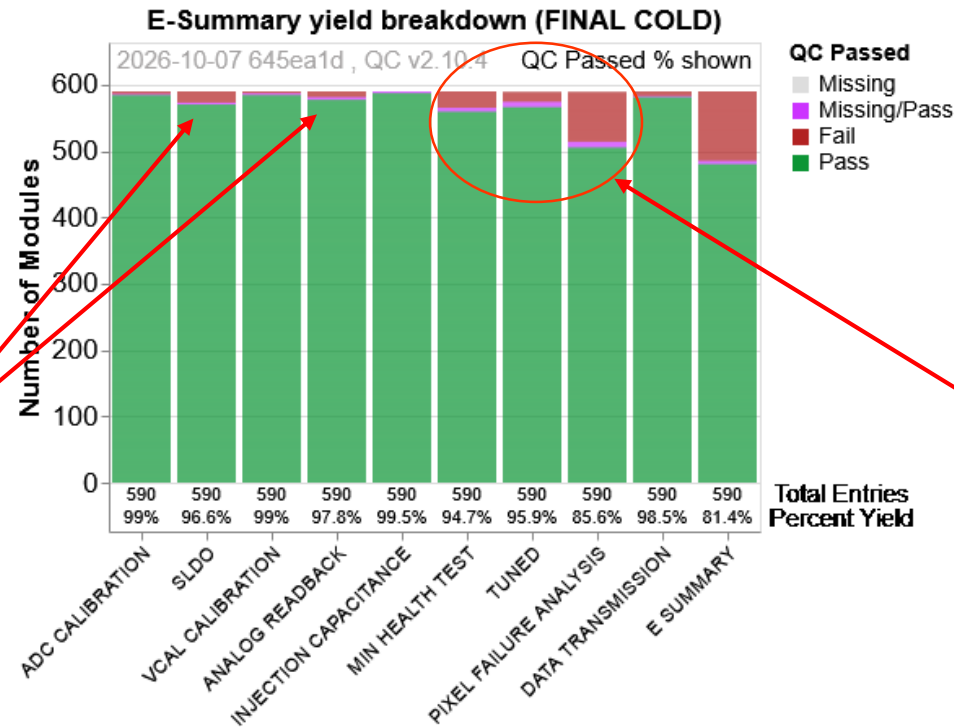
Main yield drivers

3. Hybridization

- Delamination or poor bump bonding can affect large regions of a chip
- Produces disconnected or failing pixels, visible in PFA/source-scan results

4. Electrical QC effects

Early **VDDA/VDDD trim saturation issues**
→ largely mitigated by the **IREF+1** wire-bonding adjustment

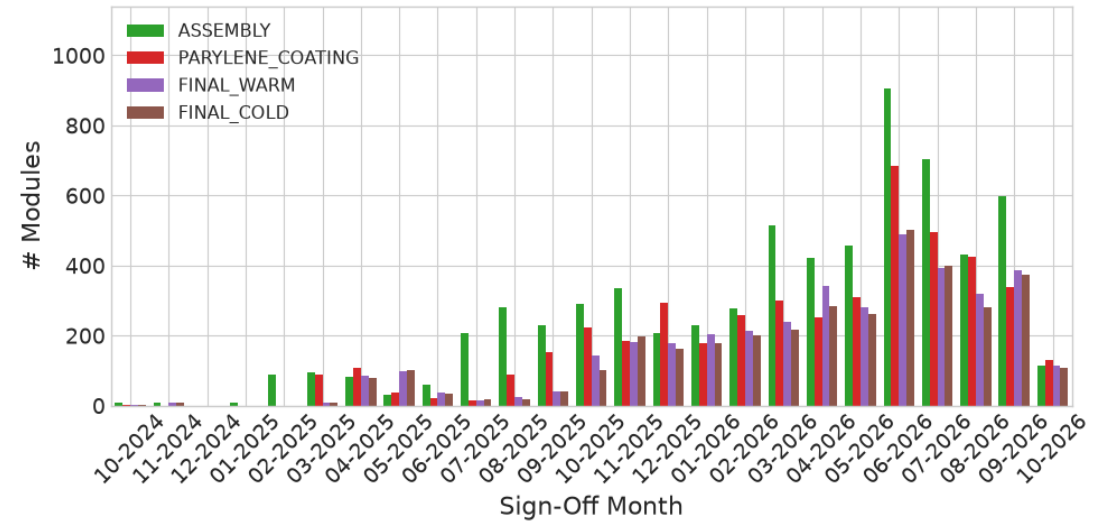
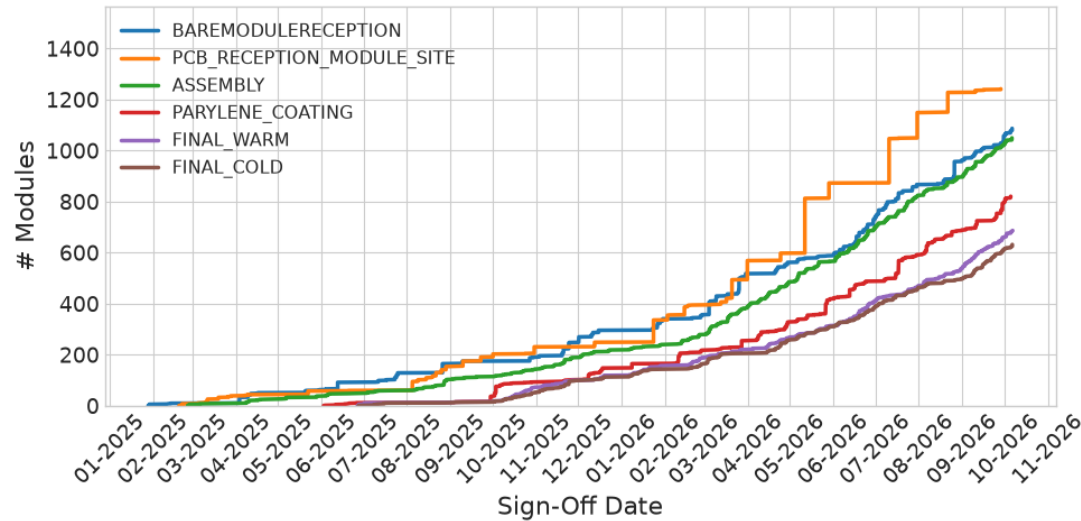


Electrical losses dominated by failing pixels:

- **core-column issues (~20%)**
- **bad delamination**

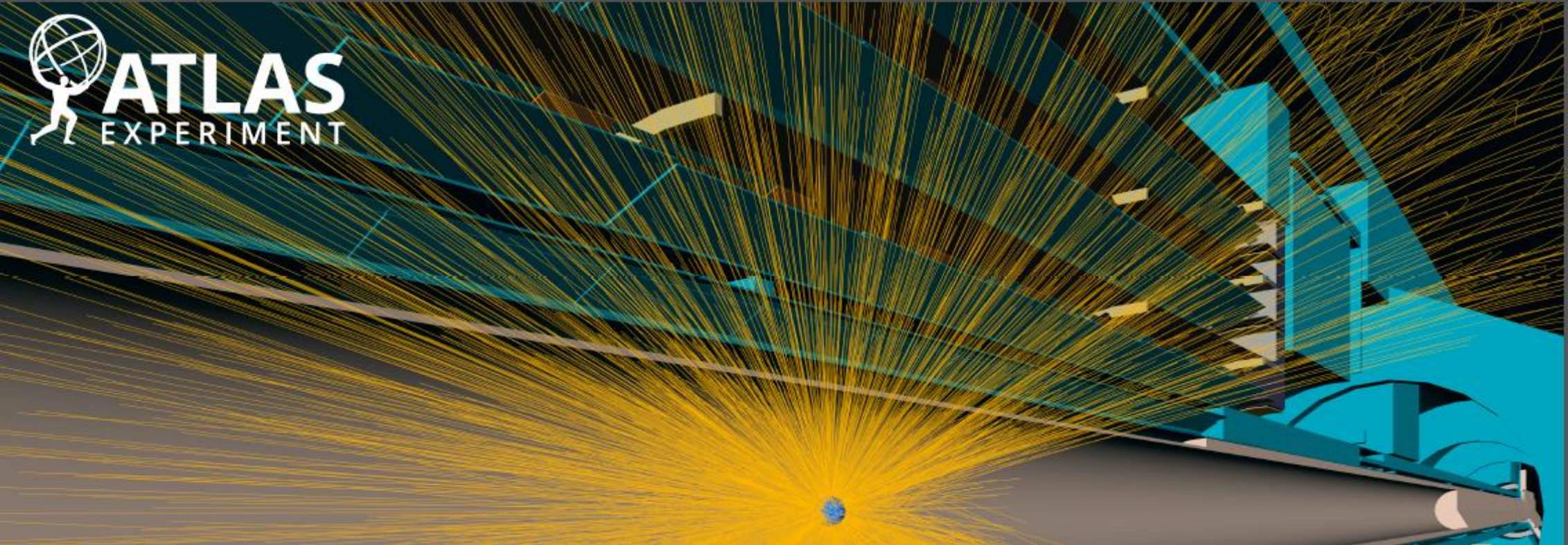


Production ramp-up and outlook



- Around 1000 modules assembled (~50%)
- Production rate is increasing, with completion targeted **by end of Sep. 2027**
- QC workflow is being optimized to match the production rate -> reduction of redundant test steps
- Current yield estimate: ~74%, close to the minimum required yield for project viability: ~75%
- Further improvement expected from process stabilization and reassessment of selected criteria, such as CC-related acceptance

Thank you for your attention. I will be happy to answer your questions.

A 3D visualization of a particle detector, likely the ATLAS experiment. It shows a complex structure with many layers and a central point where a particle collision is occurring, with numerous yellow lines radiating outwards, representing the paths of particles or the detector's internal structure.

Thank you for your attention!!!