The High Granularity Timing Detector

Status and construction progress

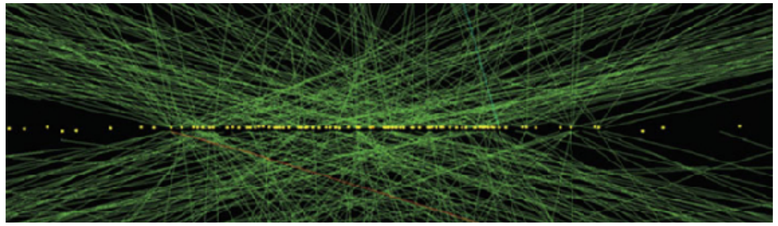
Luca Cadamuro

IJCLab, CNRS/IN2P3, Université de Paris-Saclay

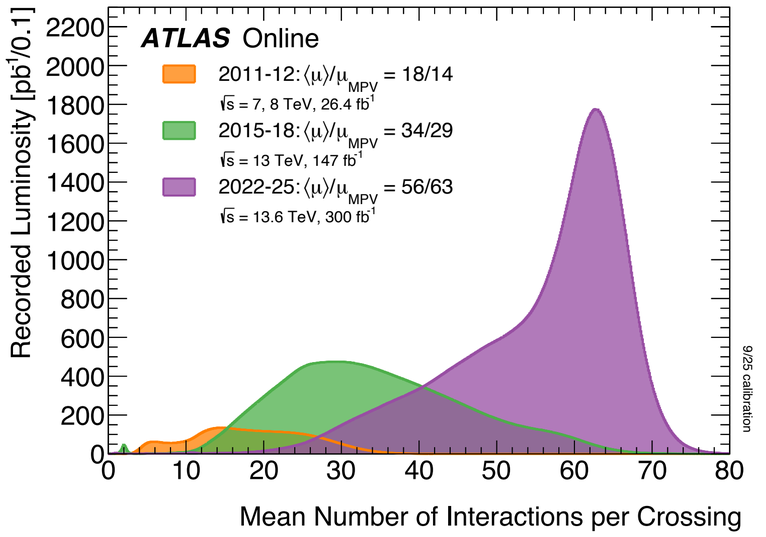
October 14th, 2026

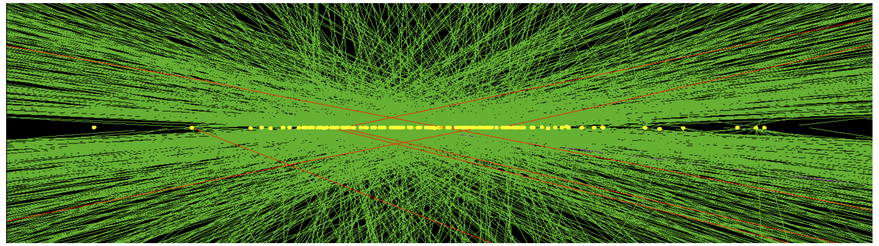
French-Ukrainian Workshop 2026

The HL-LHC challenge

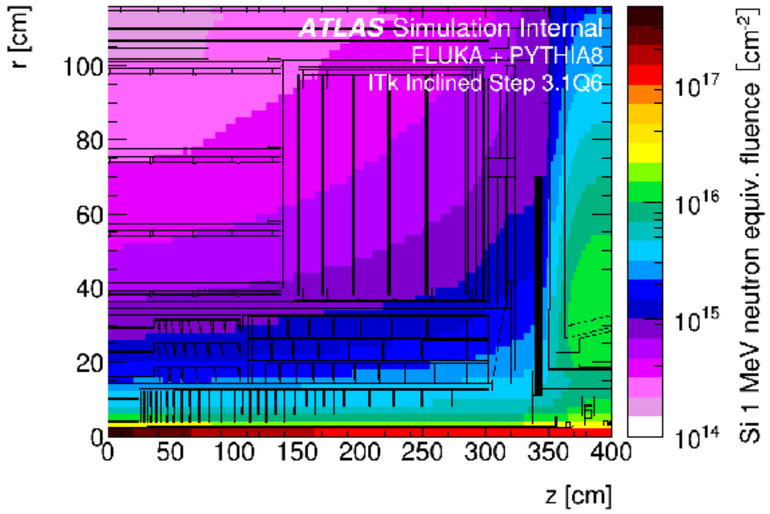


$\langle\mu\rangle \approx 80$ **: max achieved in Run 3**





$\langle\mu\rangle = 200$ **: HL-LHC**

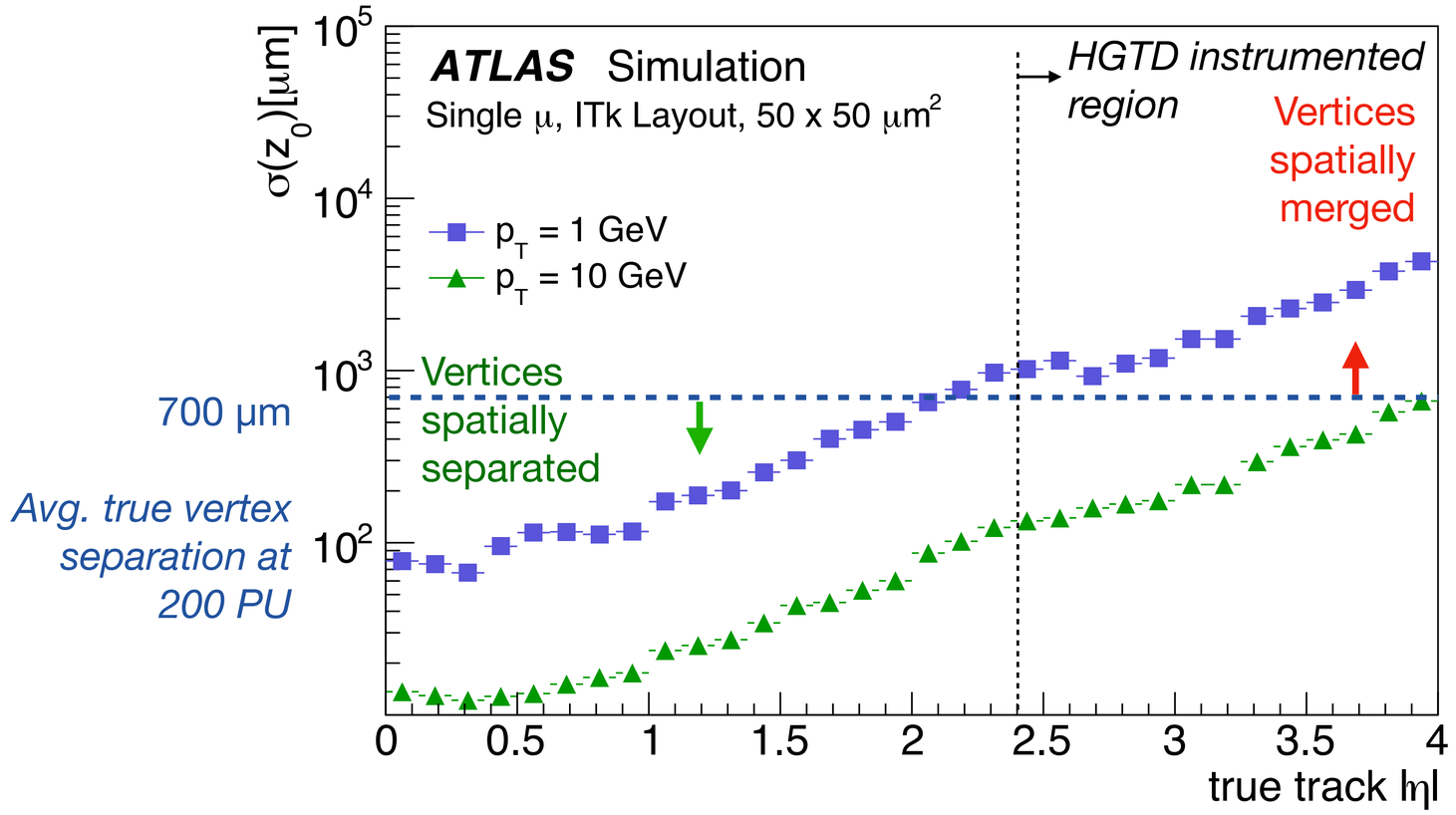


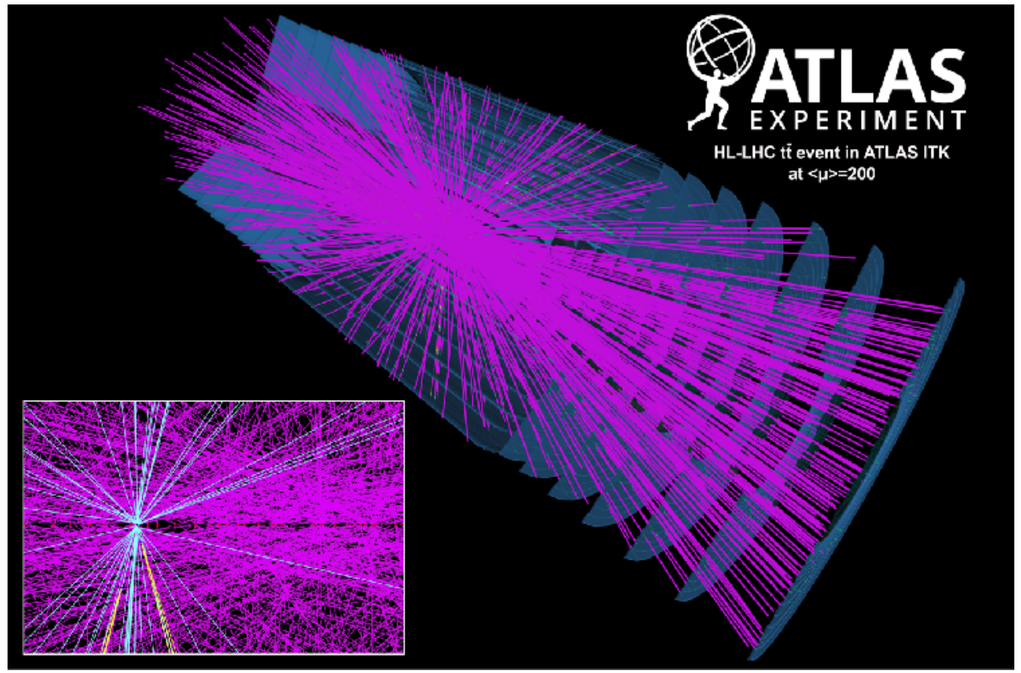
- Radiation hardness for fluences up to 10^{16} n_{eq}/cm^2
- Increased nr. particles
  - higher occupancy
  - larger event size
  - higher trigger rates
  - more complex reconstruction

A major programme of detector upgrade is ongoing to face the HL-LHC conditions

Pileup in ATLAS at the HL-LHC

- HL-LHC: instantaneous luminosity 5 times higher than Run 2 → 200 simultaneous interactions on average
  - 1.4 vertices / mm @ PU = 200 → avg. spacing of 700 μm

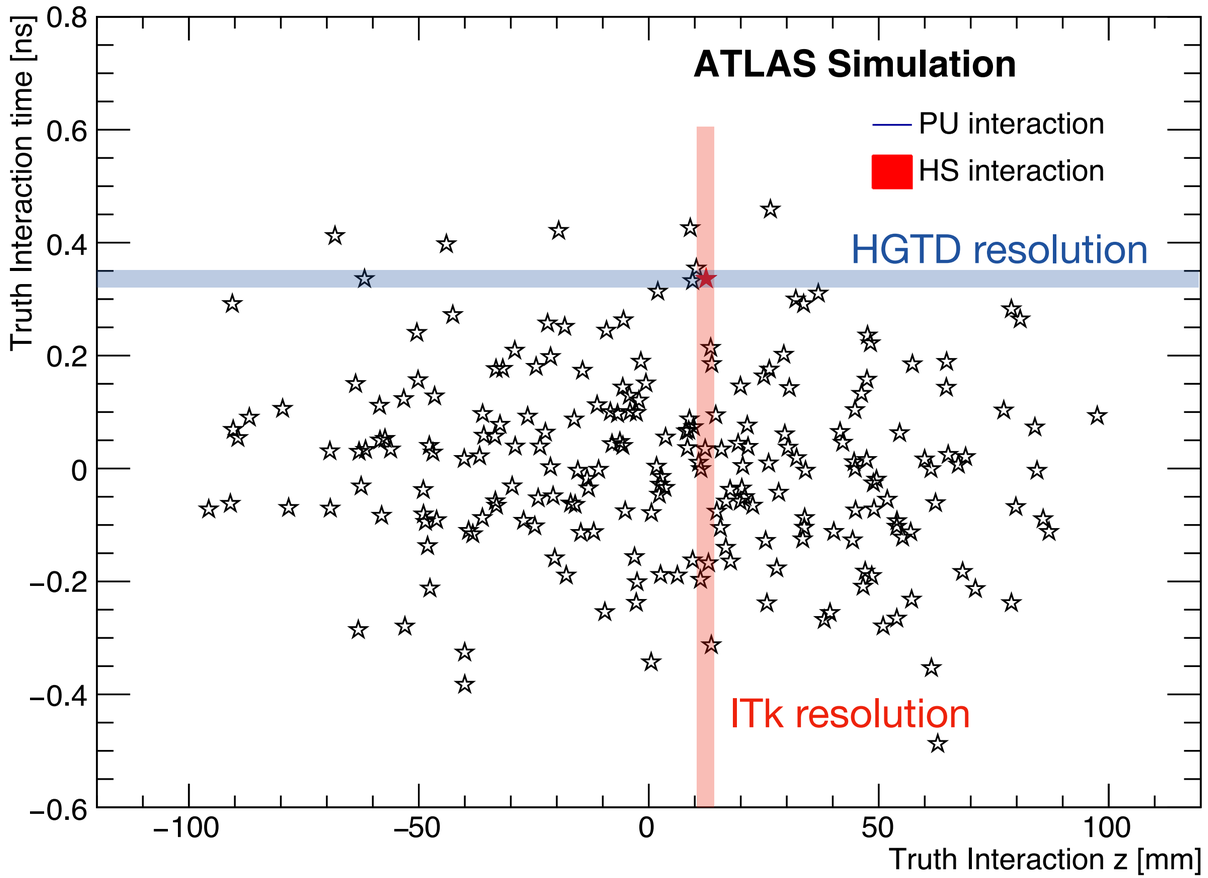


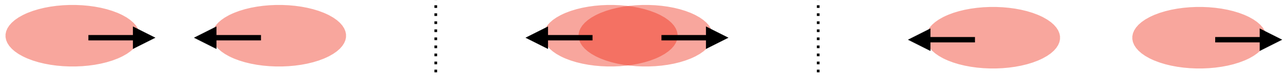


Challenge of separating the interesting collision vertex from pileup in the forward region

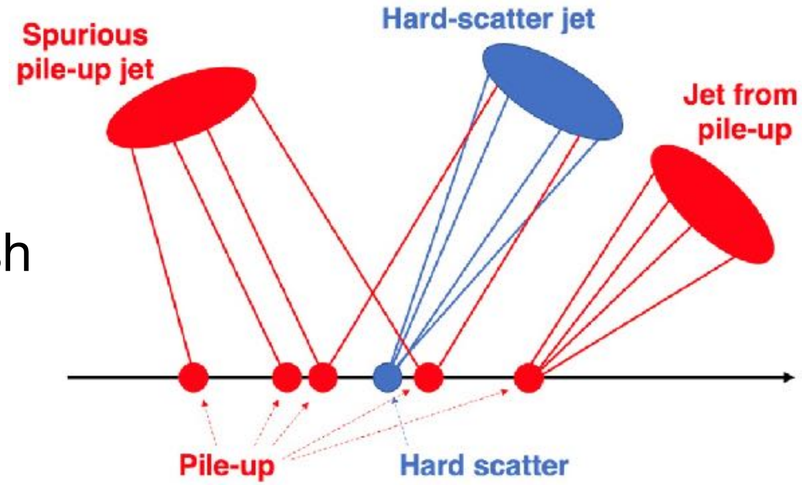
HGTD working principle

HGTD TDR





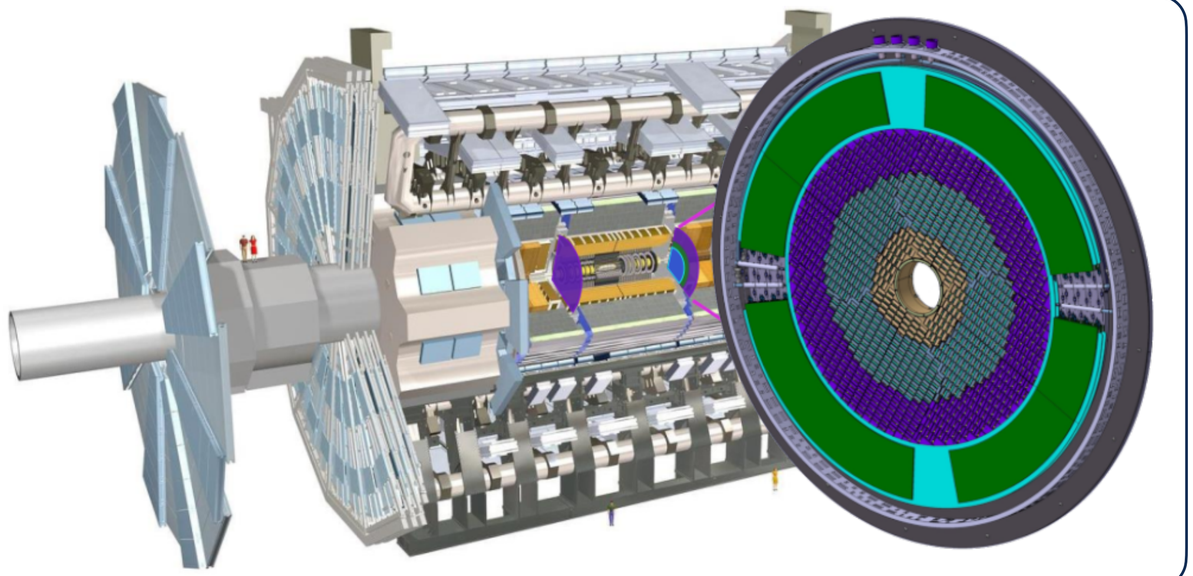
- Interactions overlapping in space happen at different times during the bunch crossing
  - gaussian with rms spread of 50 mm ≈ 175 ps
- Per-track timing information can distinguish overlapping interactions



Vertex time information : a new dimension to identify pileup

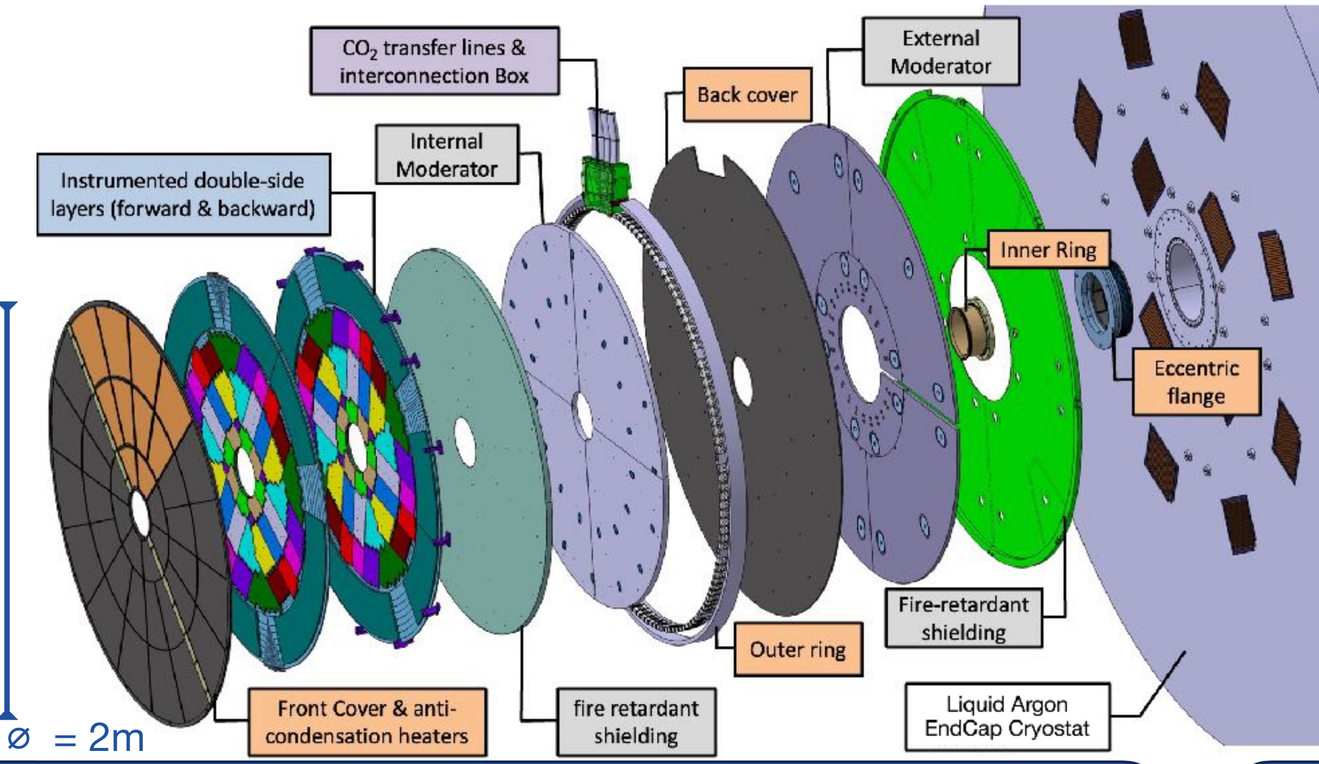
Requires a time resolution ≤ ~50 ps/track

HGTD detector overview



- Two double sided CO_2-cooled instrumented disks per endcap
  - 2—2.6 hits / track → 50 (70) ps resolution/hit to achieve 35 (50) ps/track at start (end) of lifetime
  - 3.6M readout channels
  - rad hardness : up to 2.5×10^{15} N_{eq}/cm^2, 2 MGy
- Timing + per-bunch luminosity measurement (target 1% lumi precision)

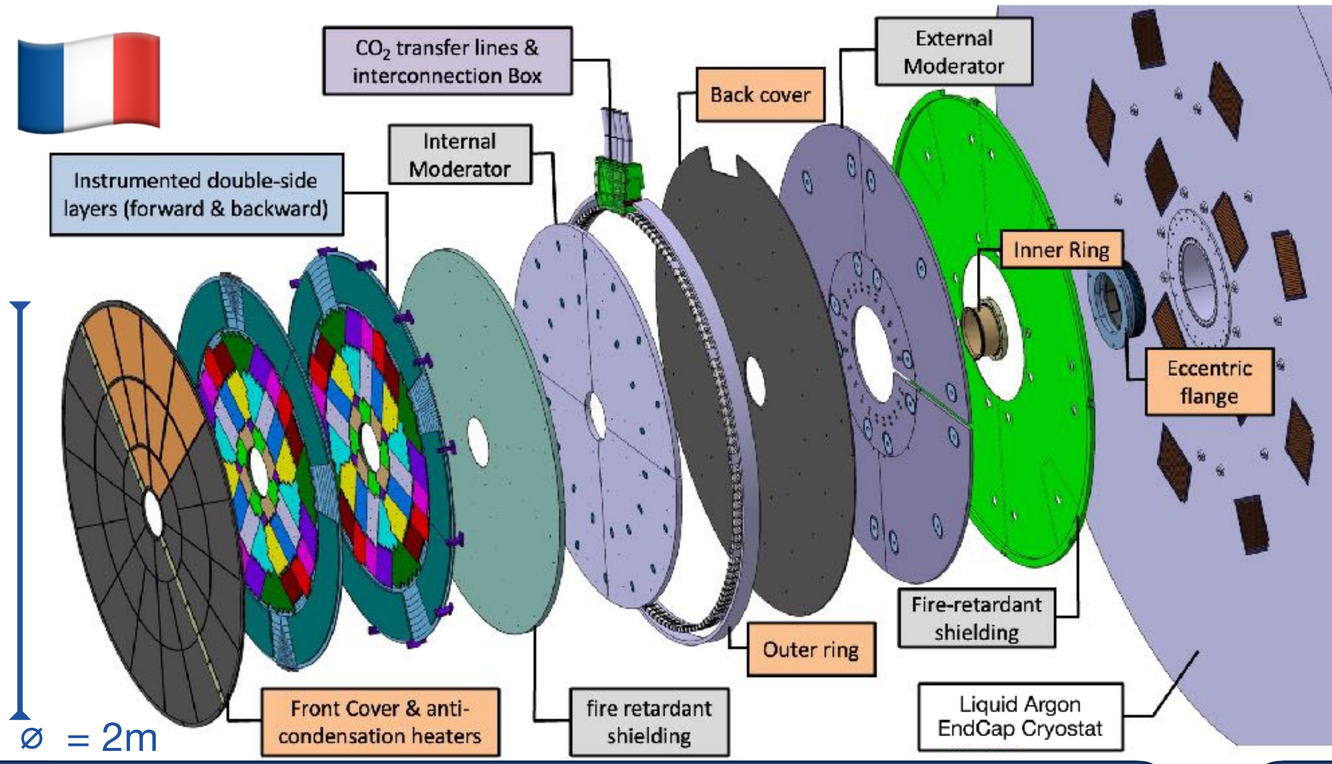
- Instruments the forward region $2.4 < |\eta| < 4$
  - active region $12 < r < 64$ cm
- LGAD technology for particle detection
- Tightly constrained z envelope of 12.5 cm



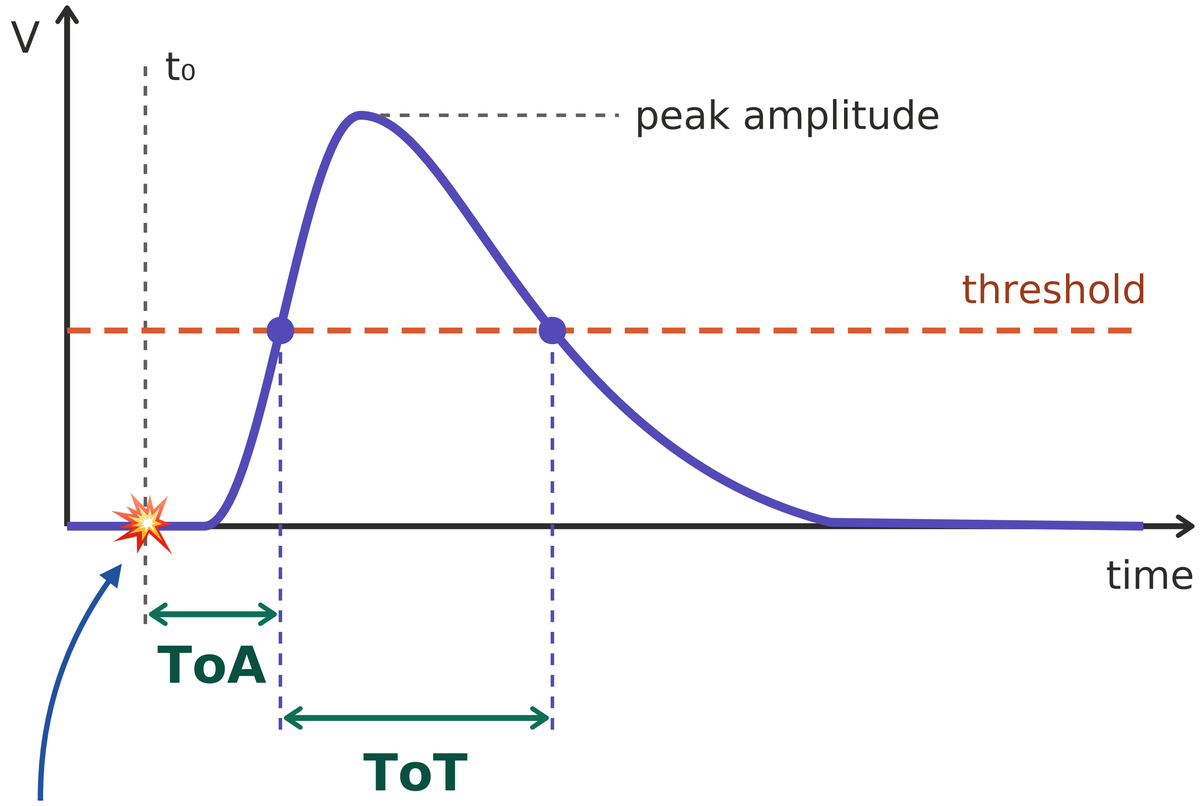
French contributions to HGTD

- Mechanics
- ASIC development and testing
- Module assembly and testing
- Testbeam
- Surface commissioning
- Simulation and performance

Large implication of French IN2P3 laboratories in several areas of the HGTD project



How to measure time?



Particle crossing the detector

Charged particle crosses the sensor creating a signal of charge Q

Signal preamplified and shaped

Hit : signal compared against a fixed reference threshold

Time of arrival (TOA)
Time over threshold (TOT)

× N pixels

Time resolution

HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

Time resolution

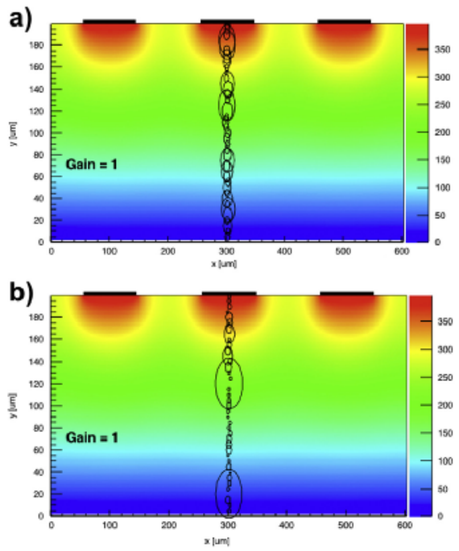
HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

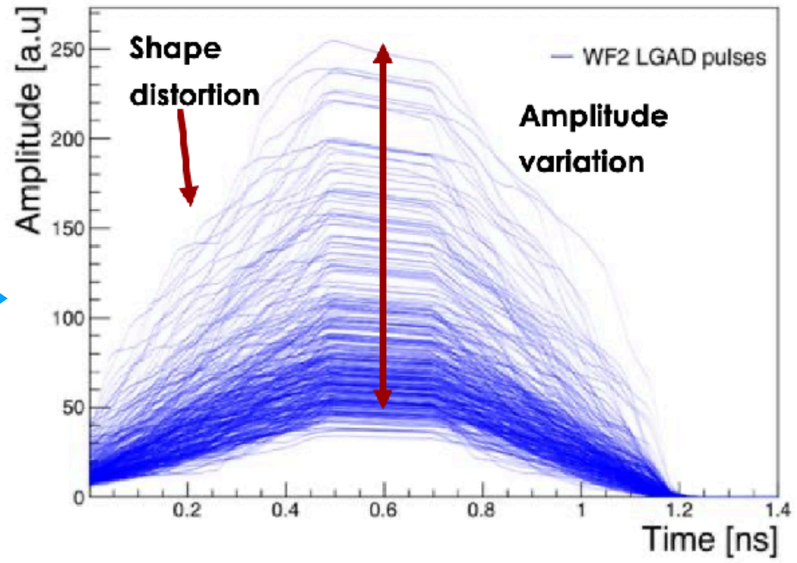
$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

25 ps

Sensor contribution : *non uniform ionisation along the particle track*

Intrinsic limitation from a silicon detector





Time resolution

HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

25 ps — σ_{Landau}

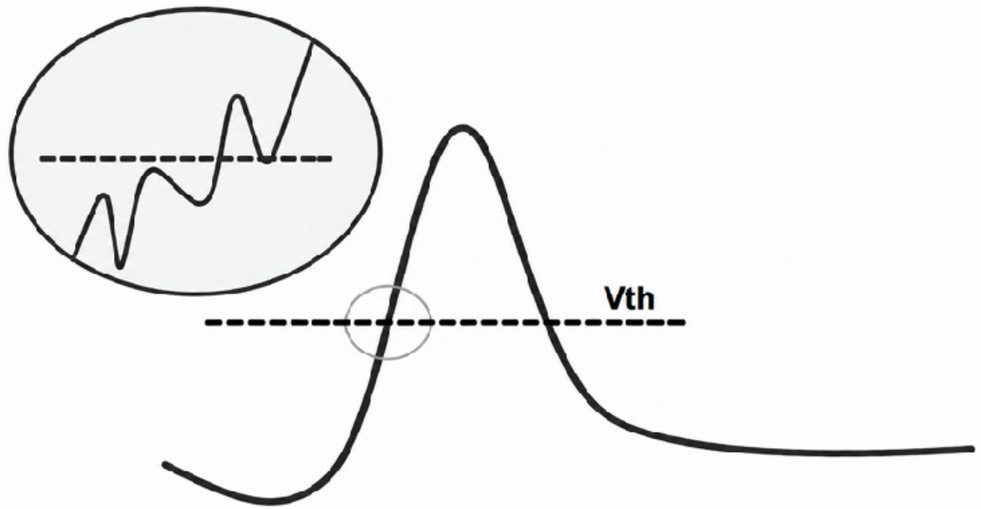
25 ps [10 fC]
65 ps [4 fC] — σ_{jitter}

ASIC contribution : *electronic noise causes variations of threshold crossing time*

$$\sigma_{jitter} = N/(dV/dt) \approx t_{rise}/(S/N)$$

$$N \propto \sqrt{BW}\,, \quad dV/dt \propto BW \longrightarrow \sigma_{jitter} \propto 1/\sqrt{BW}$$

High S/N and fast electronics to minimise jitter



Time resolution

HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

25 ps
25 ps [10 fC]
65 ps [4 fC]
< 10 ps (corrected)

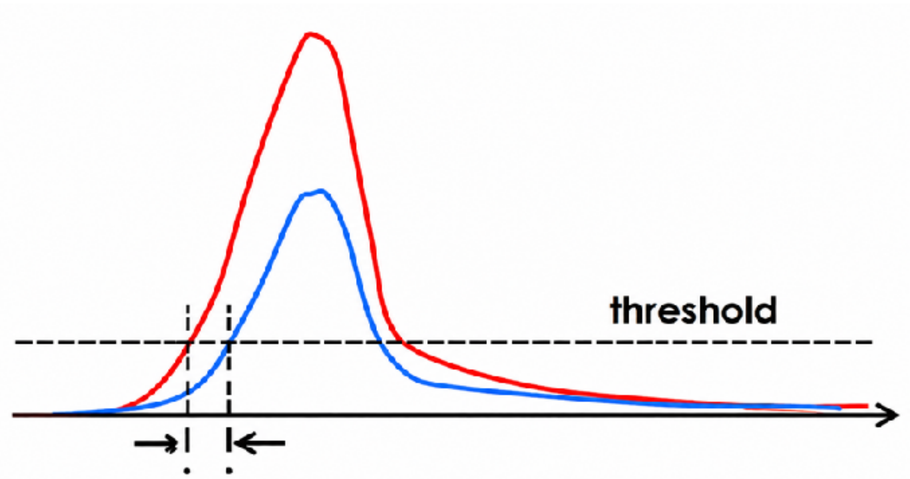
ASIC+sensor contribution

Landau fluctuations cause variations of the signal amplitude, crossing time changes

Corrected offline from the amplitude measurement

Requires time-over-threshold (TOT) information

$$\sigma_{timewalk} = \left[\frac{V_{th}}{S/t_{rise}} \right]_{RMS}$$



Time resolution

HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

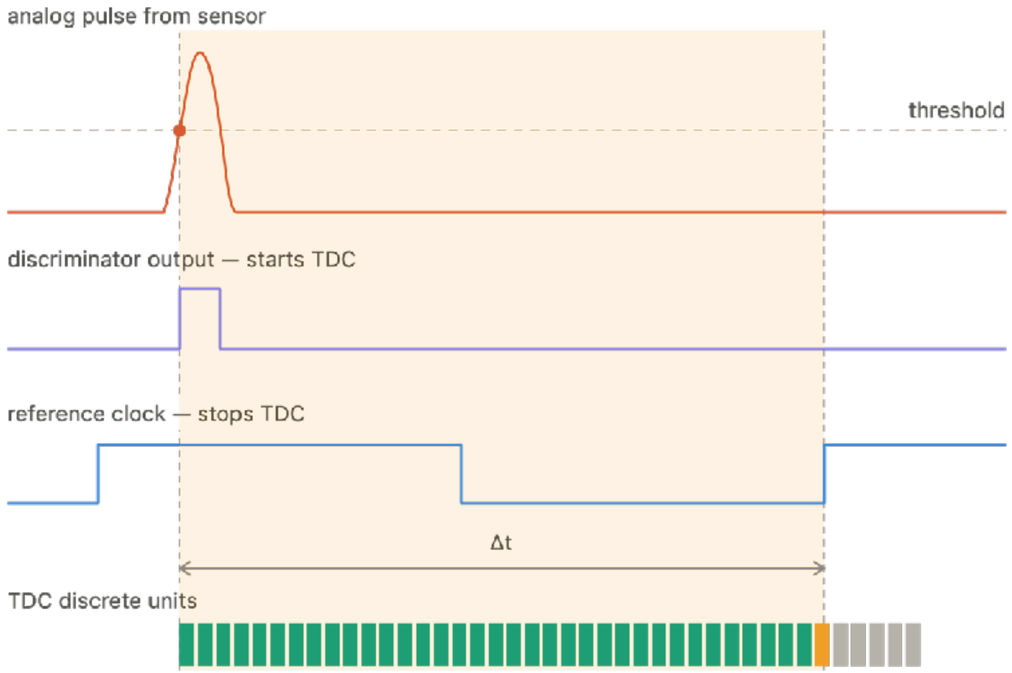
$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

25 ps — *25 ps [10 fC]* / *65 ps [4 fC]* — *< 10 ps (corrected)* — *6-7 ps*

ASIC contribution

requires sufficiently small TDC quantisation step (LSB) and excellent linearity and stability of the TDC

$$\sigma_{TDC} = LSB/\sqrt{12}$$



Time resolution

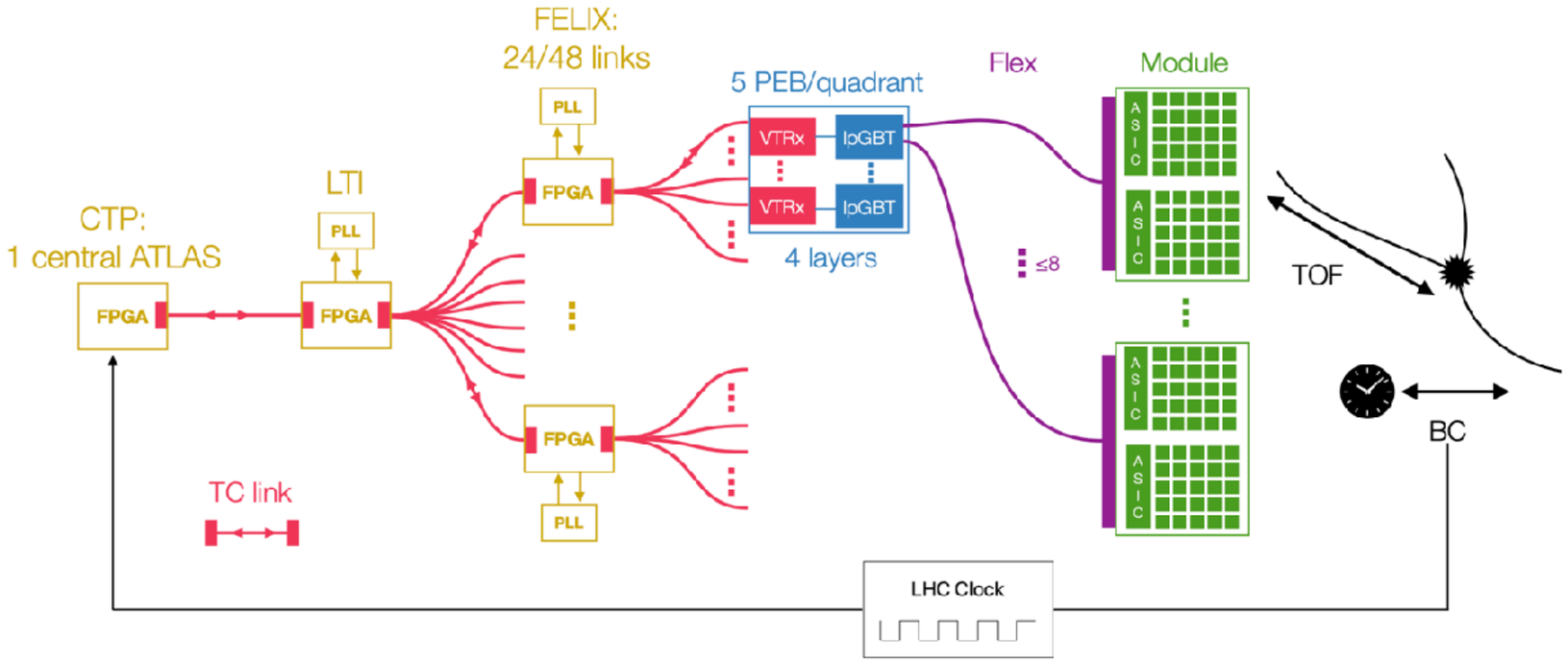
HGTD requirement :
30 - 50 ps
(begin - end of detector lifetime)

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

25 ps — *25 ps [10 fC]* / *65 ps [4 fC]* — *< 10 ps (corrected)* — *6-7 ps* — *< 10 ps*

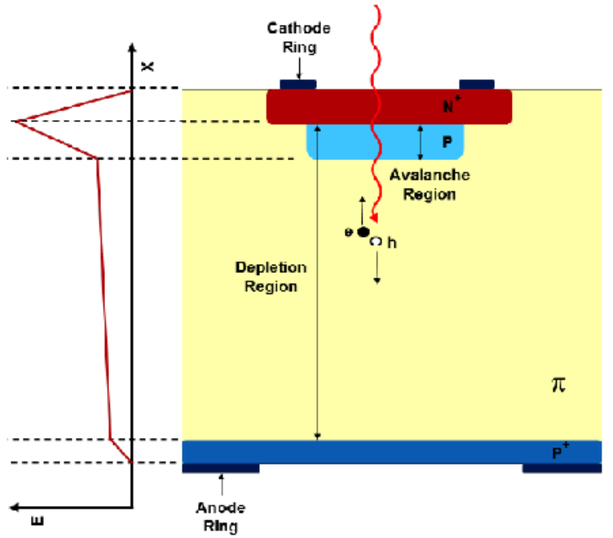
System-level contribution

Precise distribution of the clock over the entire detector

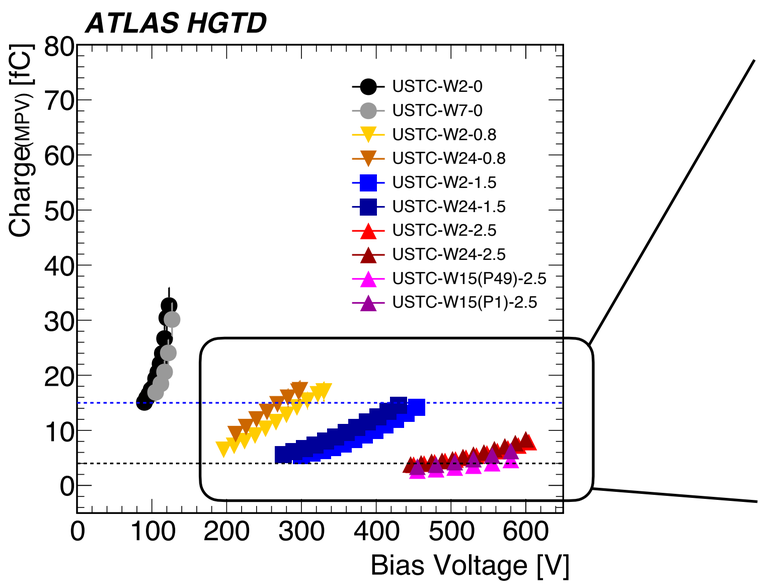


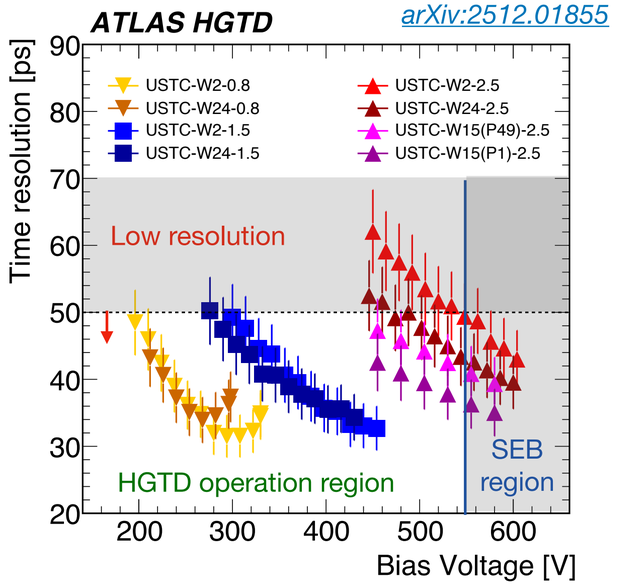
Sensors : LGADs

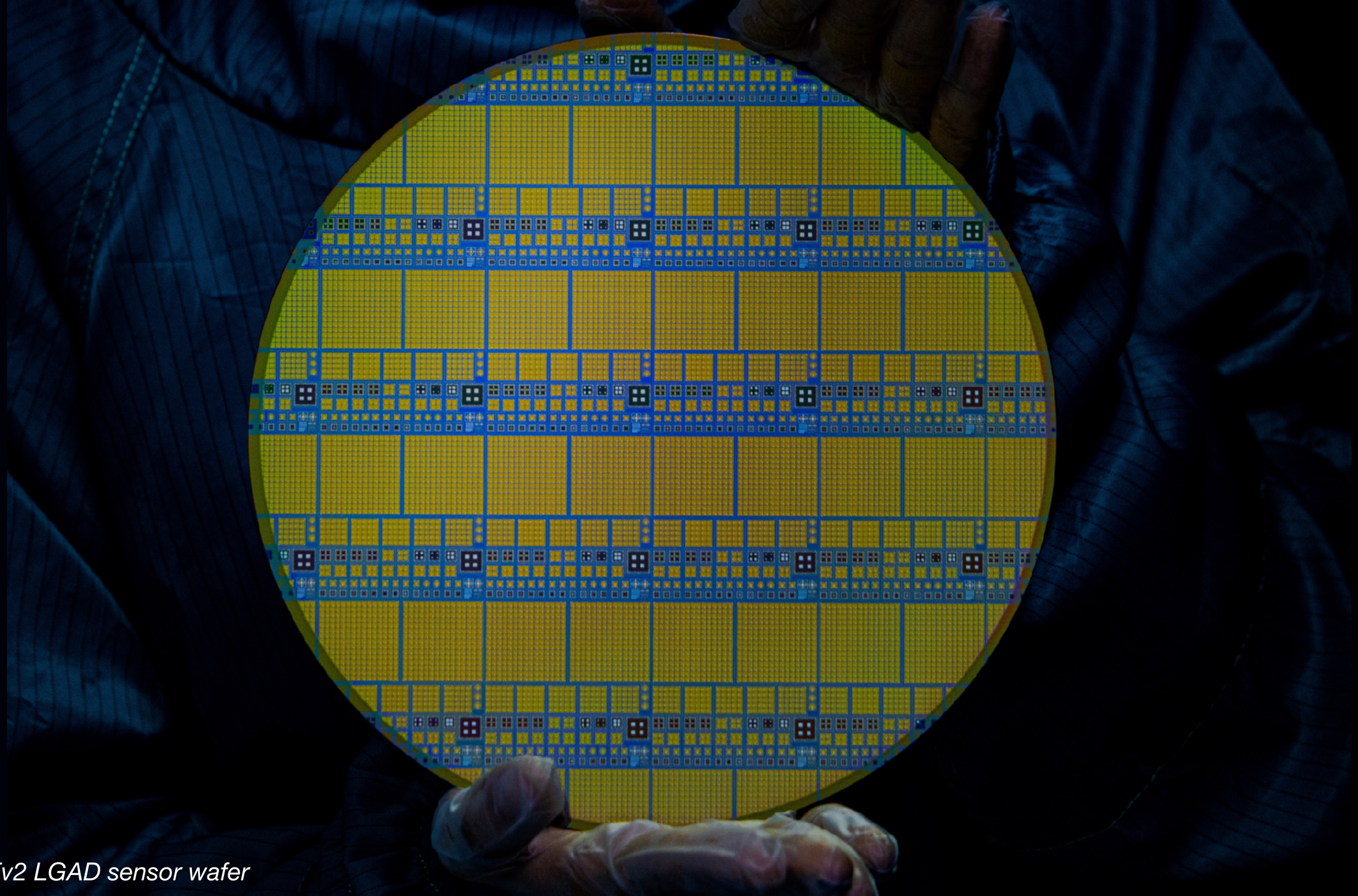
- Low Gain Avalanche Diodes technology
  - n-in-p diode structure + additional p-type gain layer : 10-40 gain
  - fast rise time, good S/N ratio → ideal for timing
- HGTD LGAD design
  - 15×15 pads, 1.3×1.3 mm^2 pad size, 775 µm device thickness, 50 µm active region
  - 2 designs (IHEP and USTC) deployed in the final detector



- Problem : acceptor removal from irradiation causes gain loss → recovered by increasing V_{bias} → local breakdown causing single event burnout (SEB)
- Solution : carbon-enriched gain layer for lower operation voltages
- Pre-production completed, characterised and validated



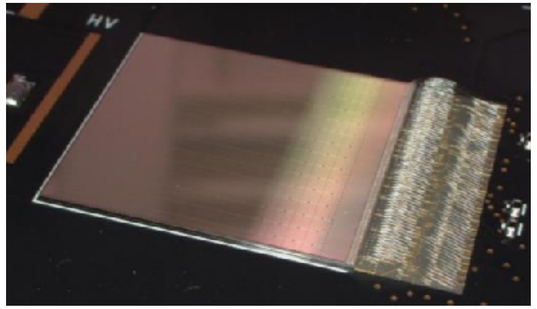




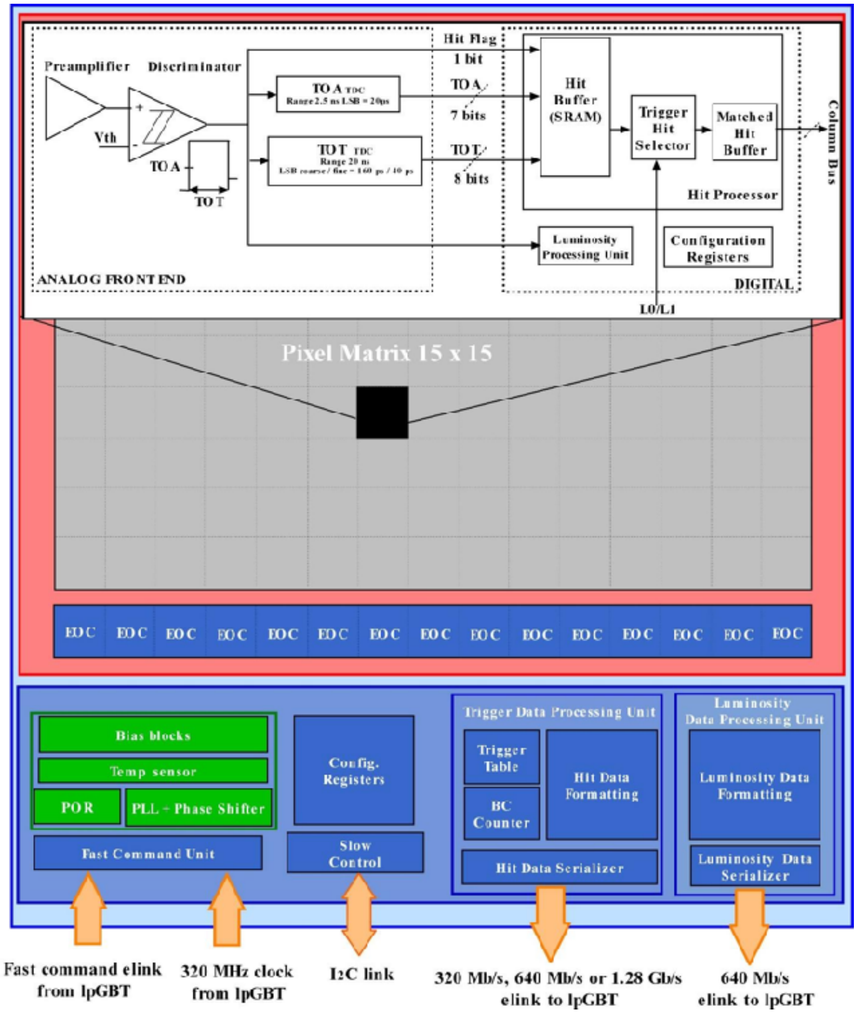
IHEP-IMEv2 LGAD sensor wafer

Readout chip : ALTIROC

- 130 nm CMOS technology from TSMC
- 15×15 matrix providing for every pixel:
  - time-of-arrival (TOA) and time-over-threshold (TOT) with 20 ps least significant bit (LSB)
  - number of hits in two windows: per-bunch luminosity
- Power dissipation < 1.2 W
- Achieves jitter < 25 (65) ps @ 10 (4) fC
- Minimal detectable charge of 2 fC
- Triplicated architecture : radiation hard up to 2 MGy
- Begin of R&D (2016) ALTIROC 0 → 1 → 2 → 3 → A - production version (2025)



ALTIROC-A on a test board
Chip size 19.9 × 22.5 mm²

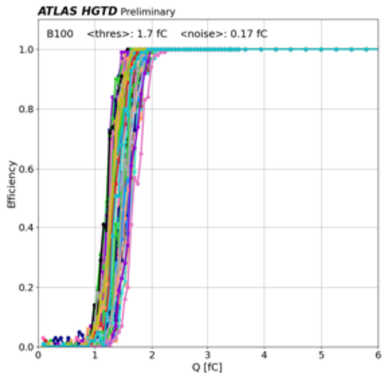


ALTIROC characterisation

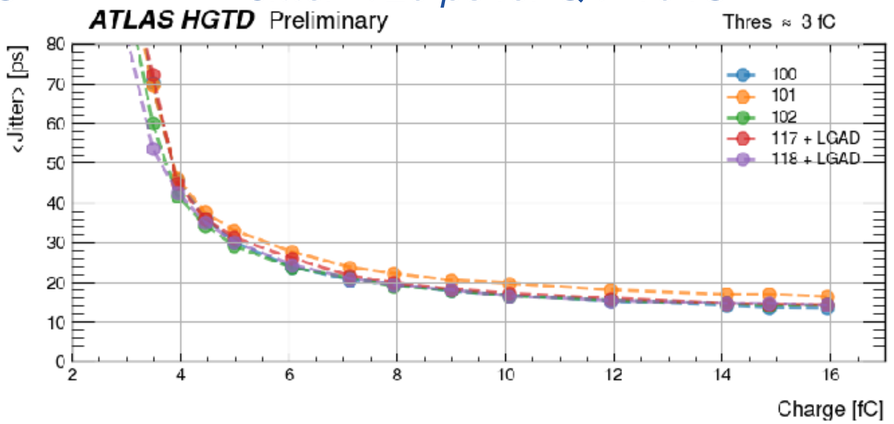
HGTD Public plots

Full characterisation of the ASIC in lab test bench ▶

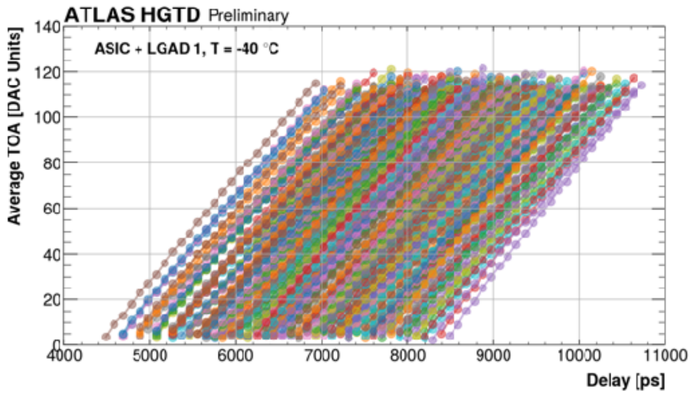
> 95% eff. for Q > 1.7 fC

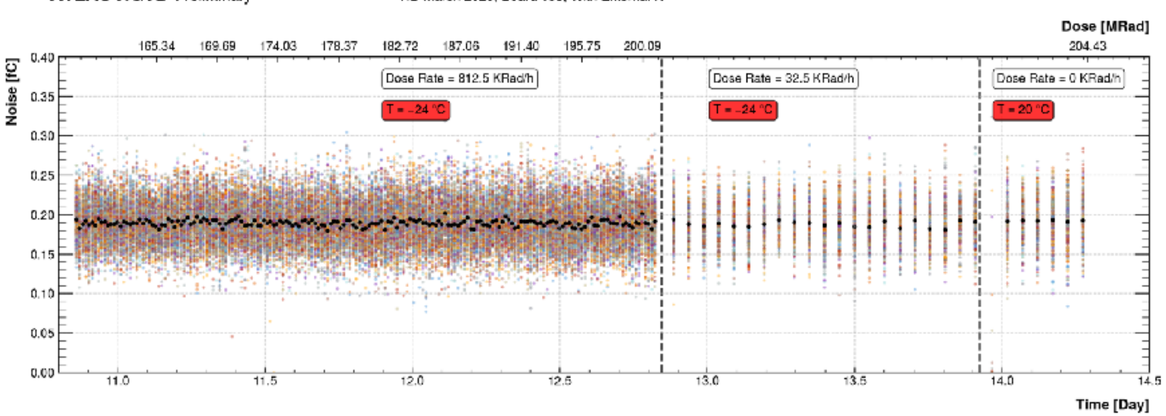


Jitter < 20 ps for Q > 10 fC



TDC linearity verification



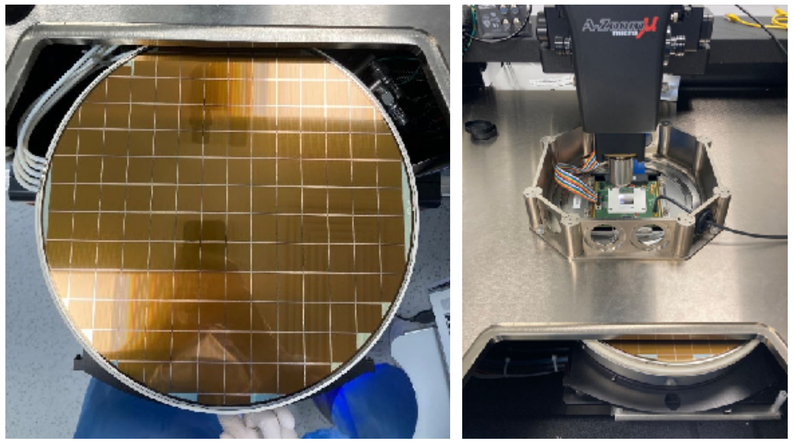


Chip performance is stable at various doses received

◀ Radiation hardness tests : TID and SEU

ASIC probing at wafer level for ASIC QC ▶

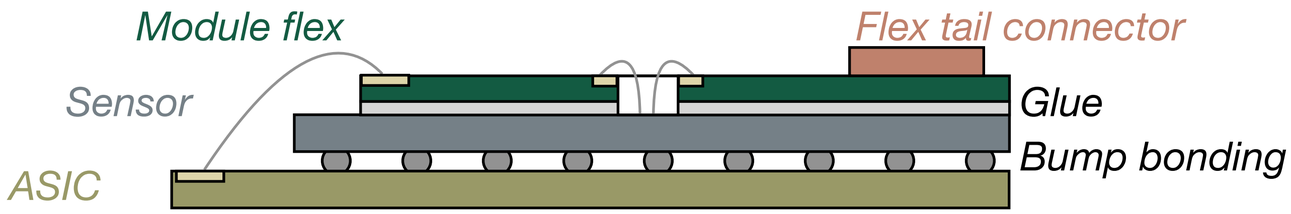
12” wafers, ~130 ASIC/wafer

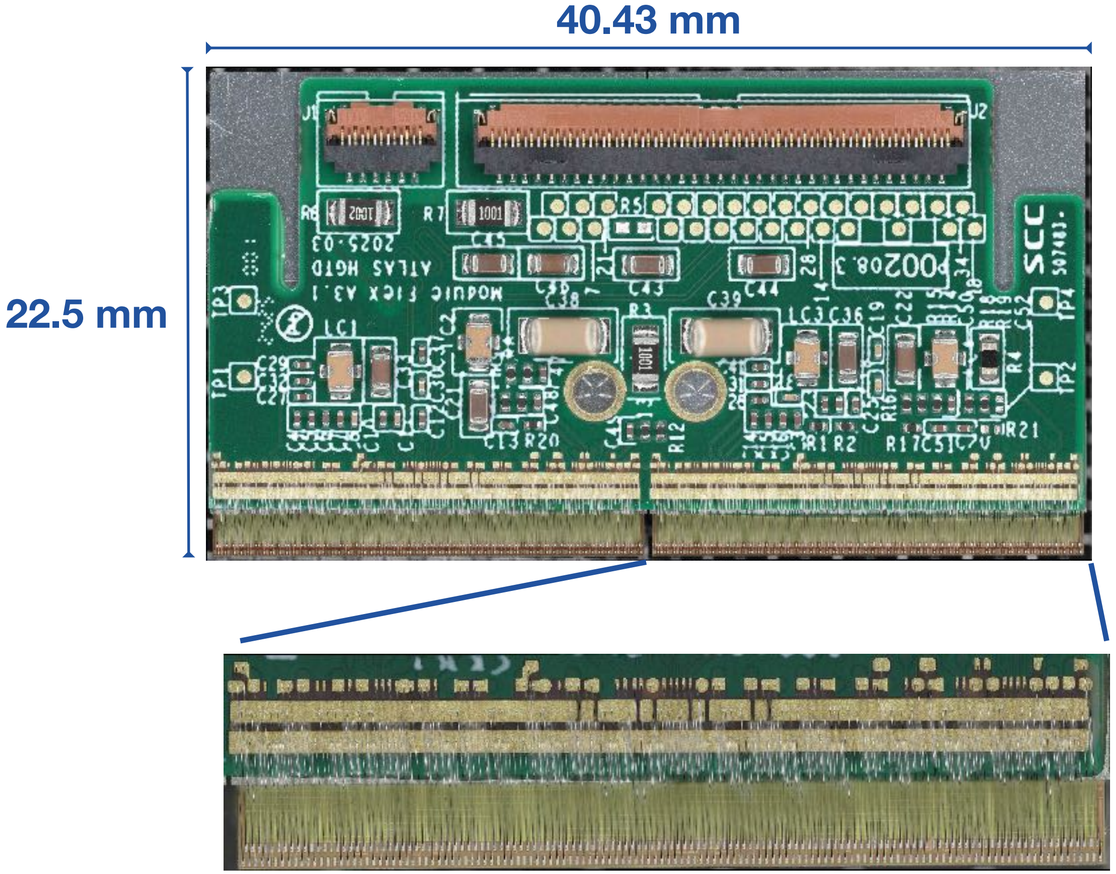


17 wafers ≈ 2000 ASIC probed for preproduction
Yield ~ 80%

Very extensive campaign of study and characterisation

HGTD modules

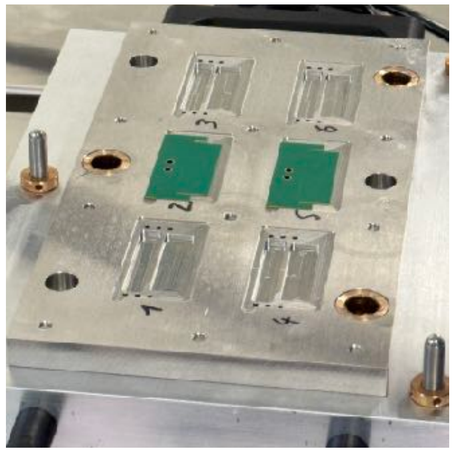
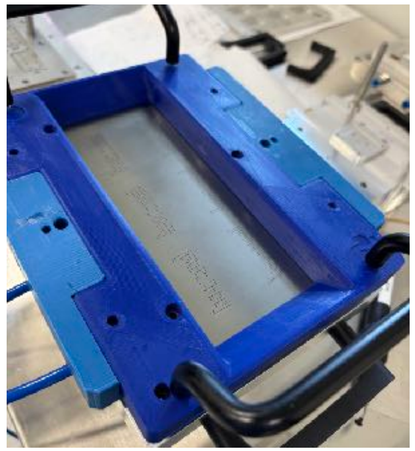
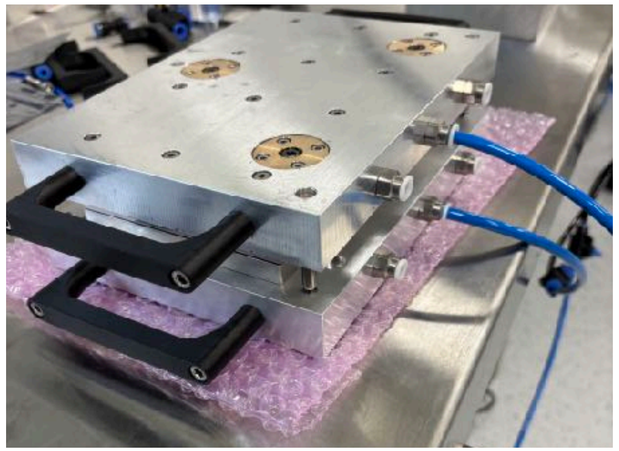




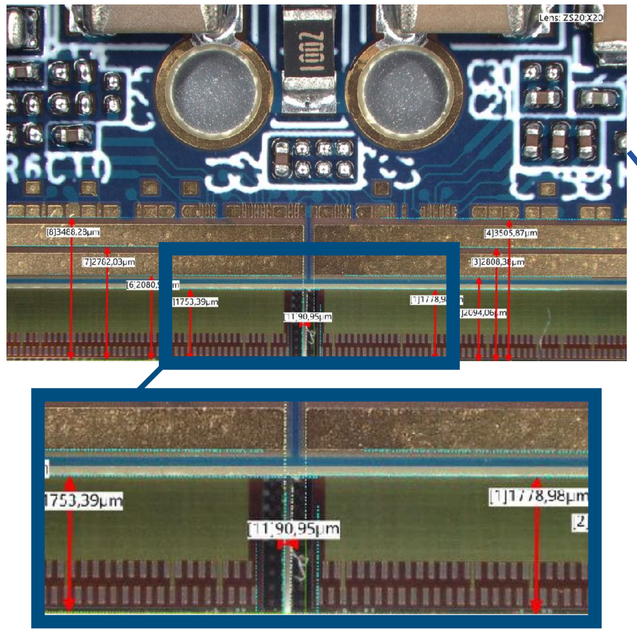
High density wire bonding with staggered pads

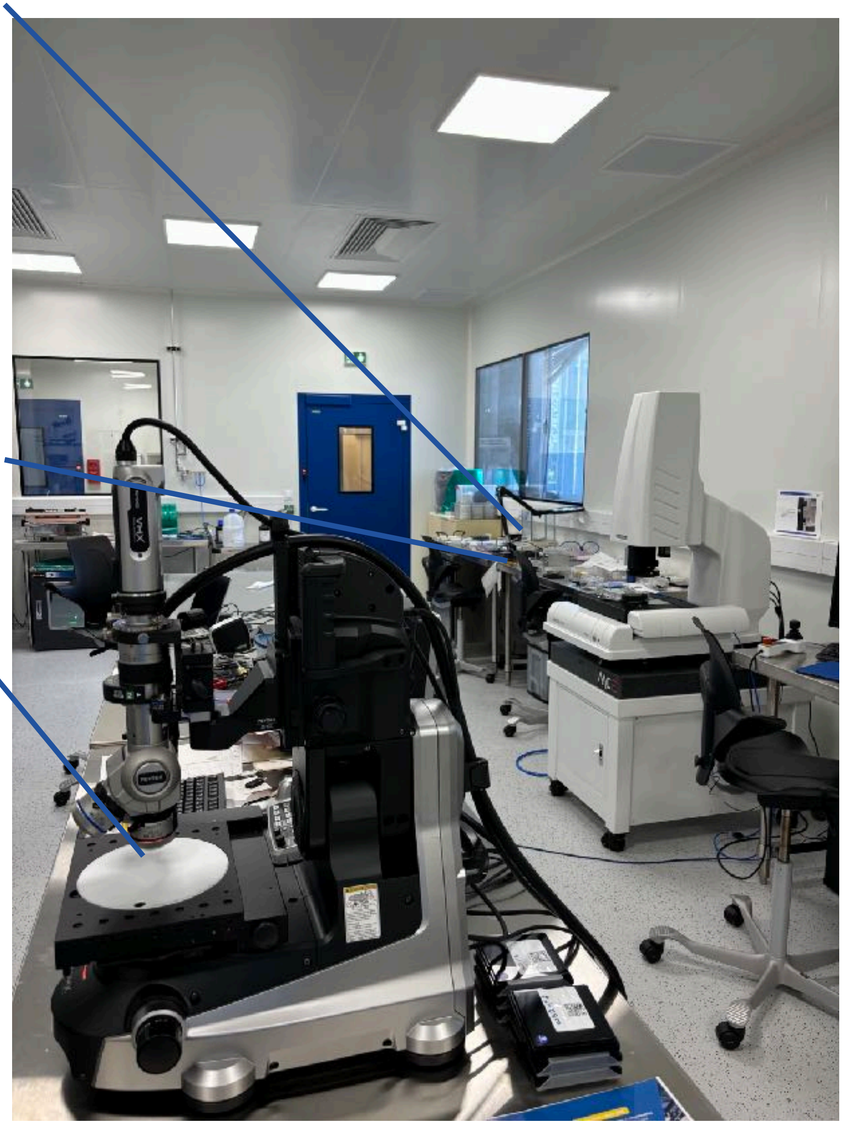
- Hybrid = sensor+ALTIROC (bump-bonded)
- Two hybrids glued with epoxy to a PCB module flex
  - wire bonding from ASIC to module flex
- Tight assembly tolerances with ~100 µm precision positioning
  - both manual (jig) and automated (gantry) methods
- In total 8032 modules in the HGTD, assembled in a total of 6 sites

Module assembly at IJCLab

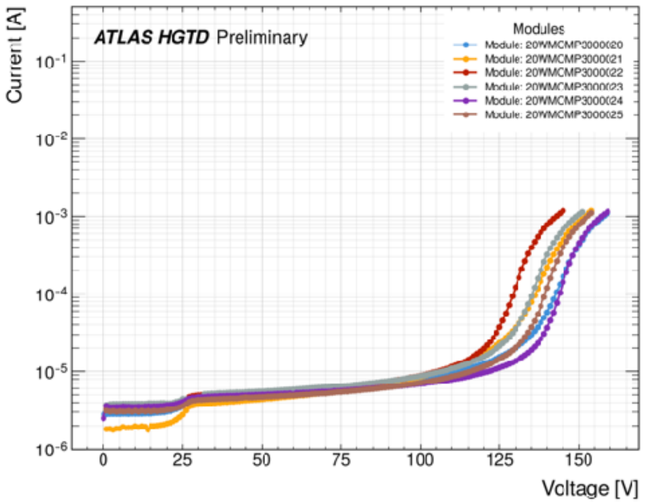
- Modules are assembled in a clean room in bldg. 200
- Mechanical process
  - alignment with jigs
  - glue dot deposition with stencil
  - parallel setup, 6 modules/jig
- Automated metrology

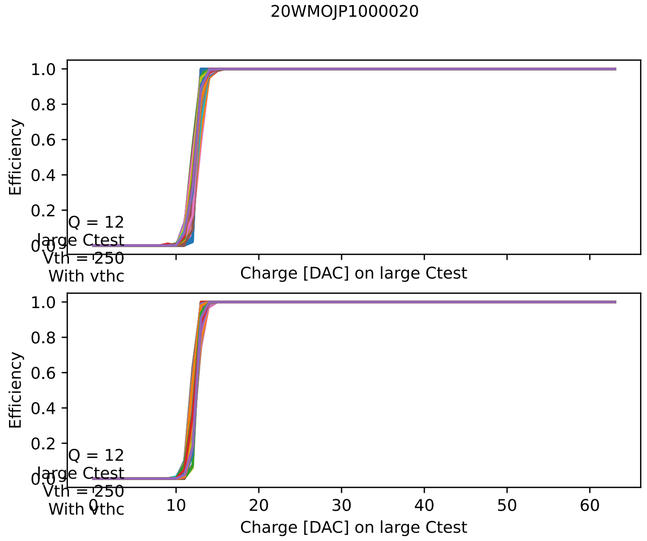


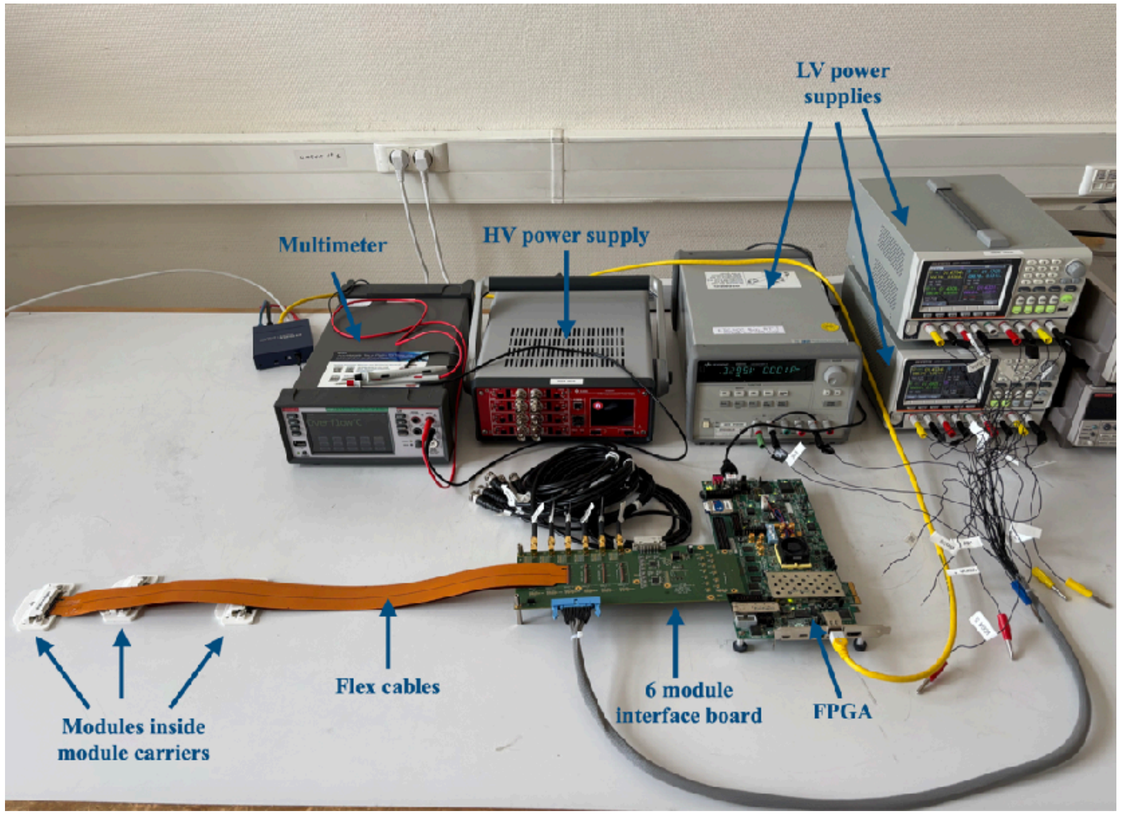


Module testing at IJCLab

- Custom FPGA-based readout setup
- Electrical tests and thermal stresses cycles





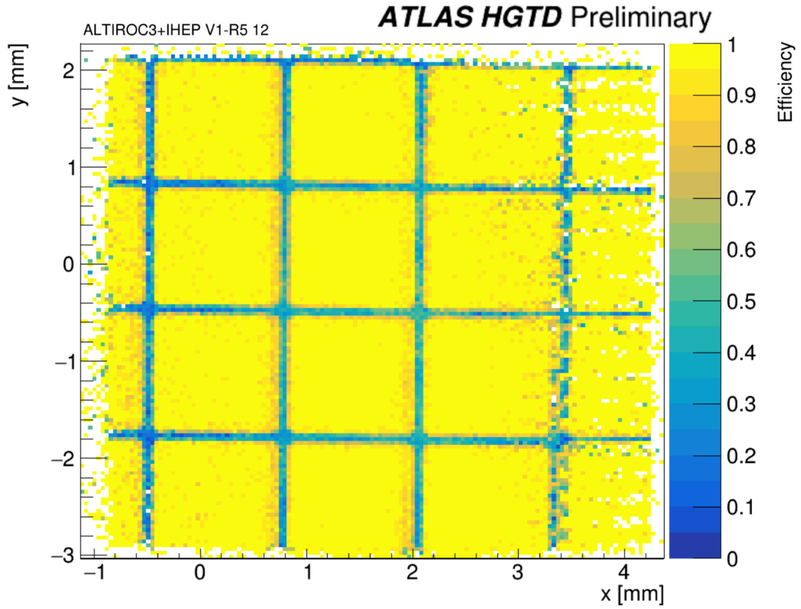


→ ***internship of A. Pauchkov (Kyiv U.)*** *for the characterisation of the module performance at various operating temperature conditions*

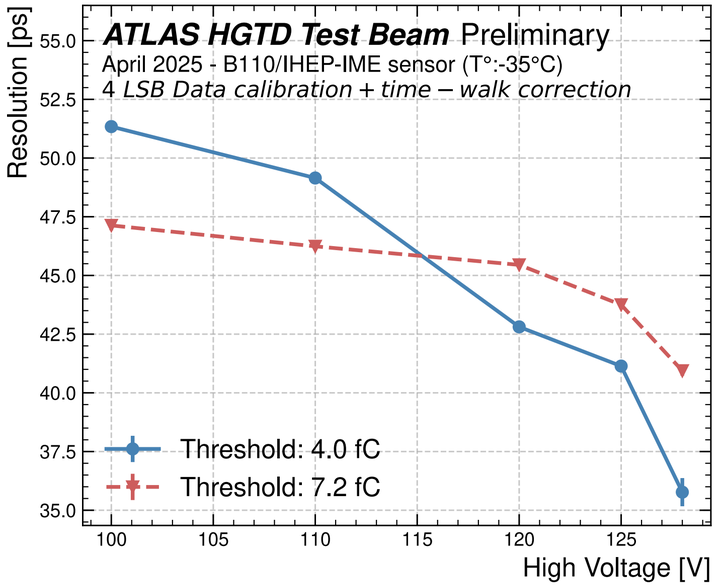
Performance measurements

- Ongoing campaigns of characterization in testbeams at SPS and DESY and with ^{90}Sr source setup
  - 120 GeV pions (SPS), 5 GeV e^- (DESY), ≤ 2 MeV (^{90}Sr)
  - time reference provided by MCP-PMT, spatial reference by beam telescope
- Extensive studies of performance and TOA calibration (time walk correction, LSB calibration)

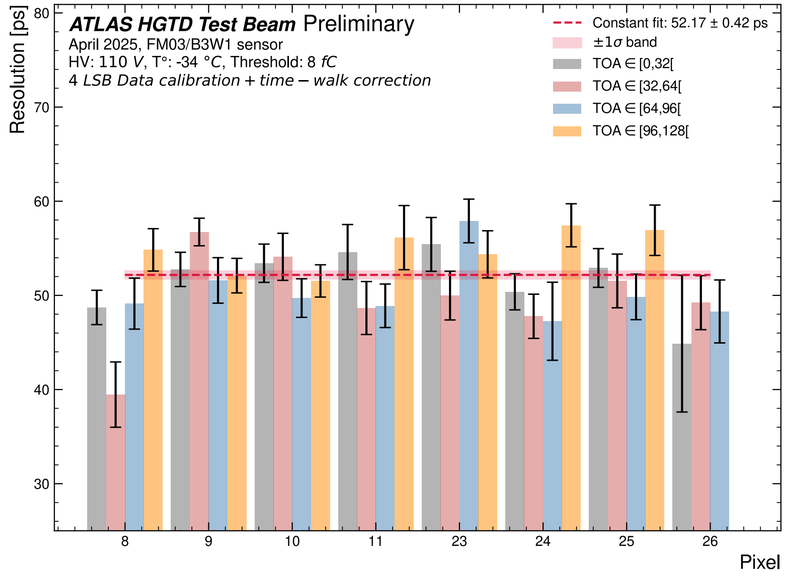
Hybrids mounted on test board



Fully efficient at the center of the pixels (reference : ALTIROC 3 TB results)



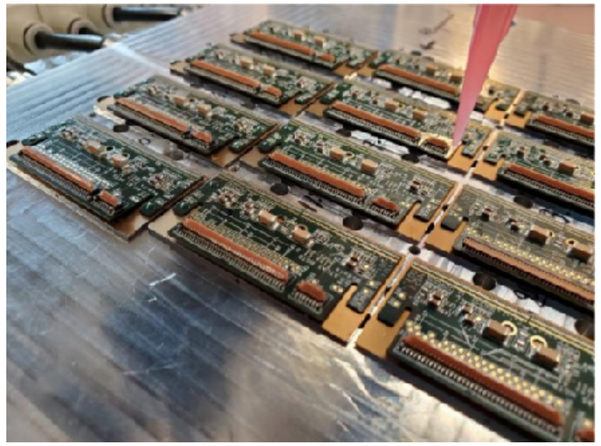
Full module

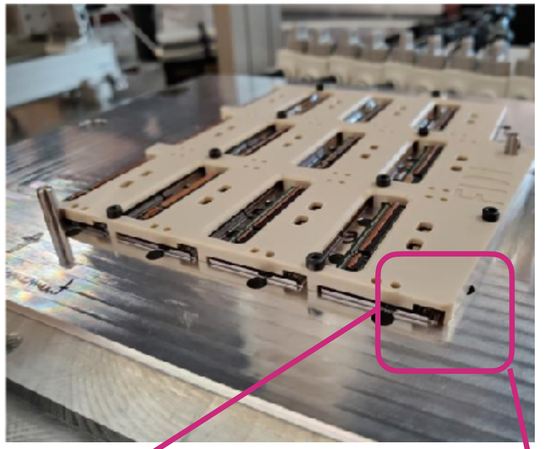


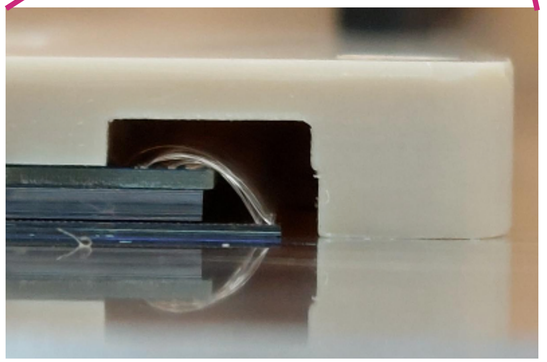
Resolutions at 40-50 ps / hit are obtained (reference : ALTIROC A TB results)

HGTD detector units and loading

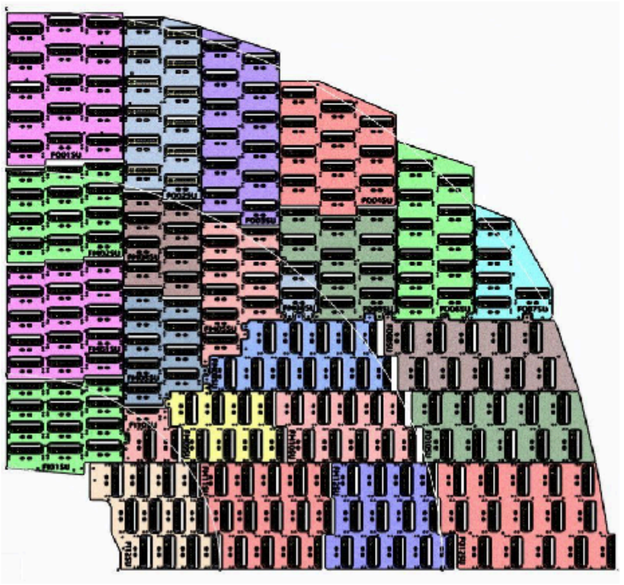
- Modules are glued in groups onto Support Units (SU) to form Detector Units (DU)
  - SU material : PEEK (radiation hard)
  - provide mechanical protection and handling
- Loading procedure via gantry or mechanical alignment with dedicated plate + glue dispensing robot









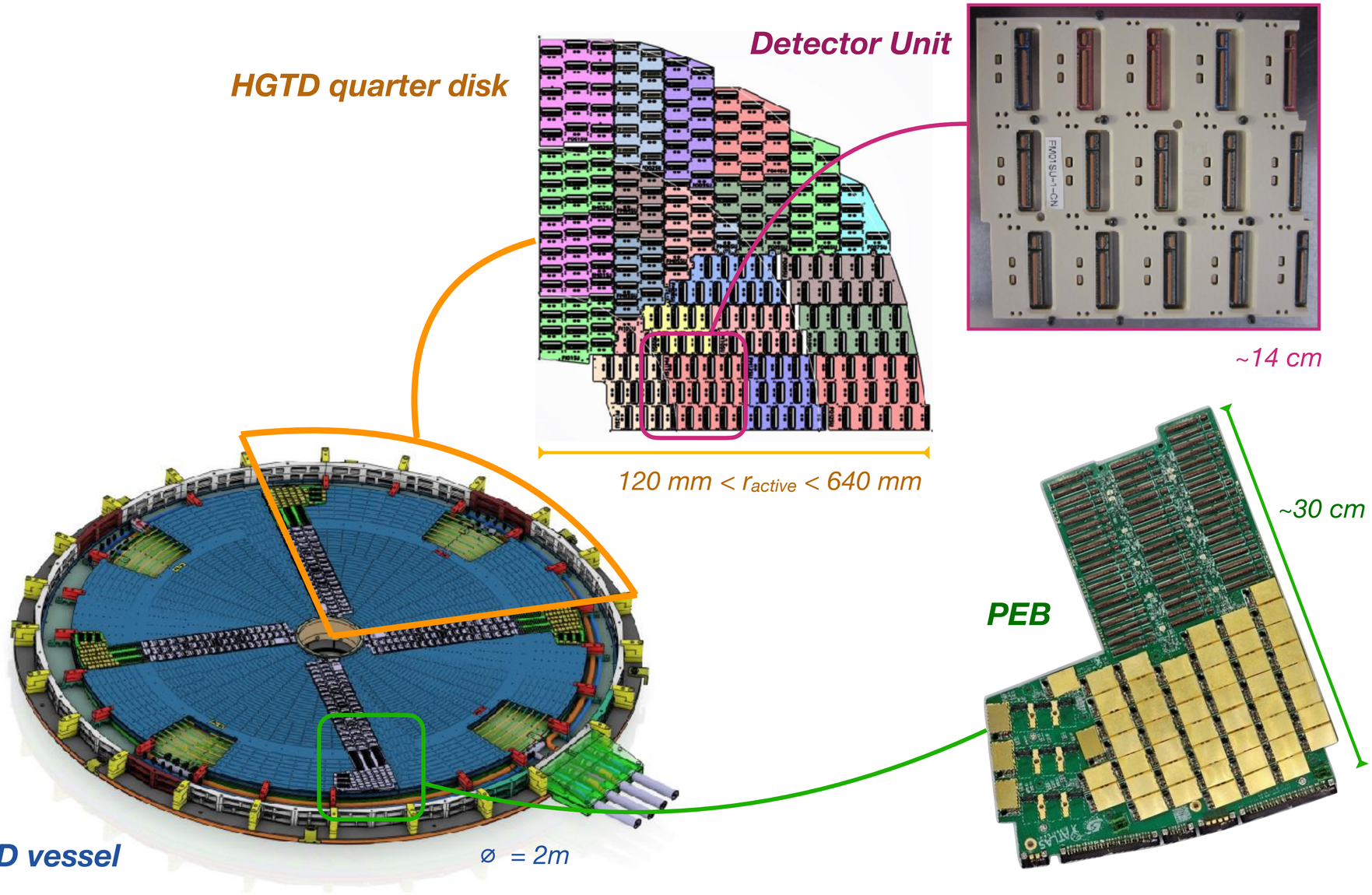


24 “front” type + 24 “back” types for each quadrant

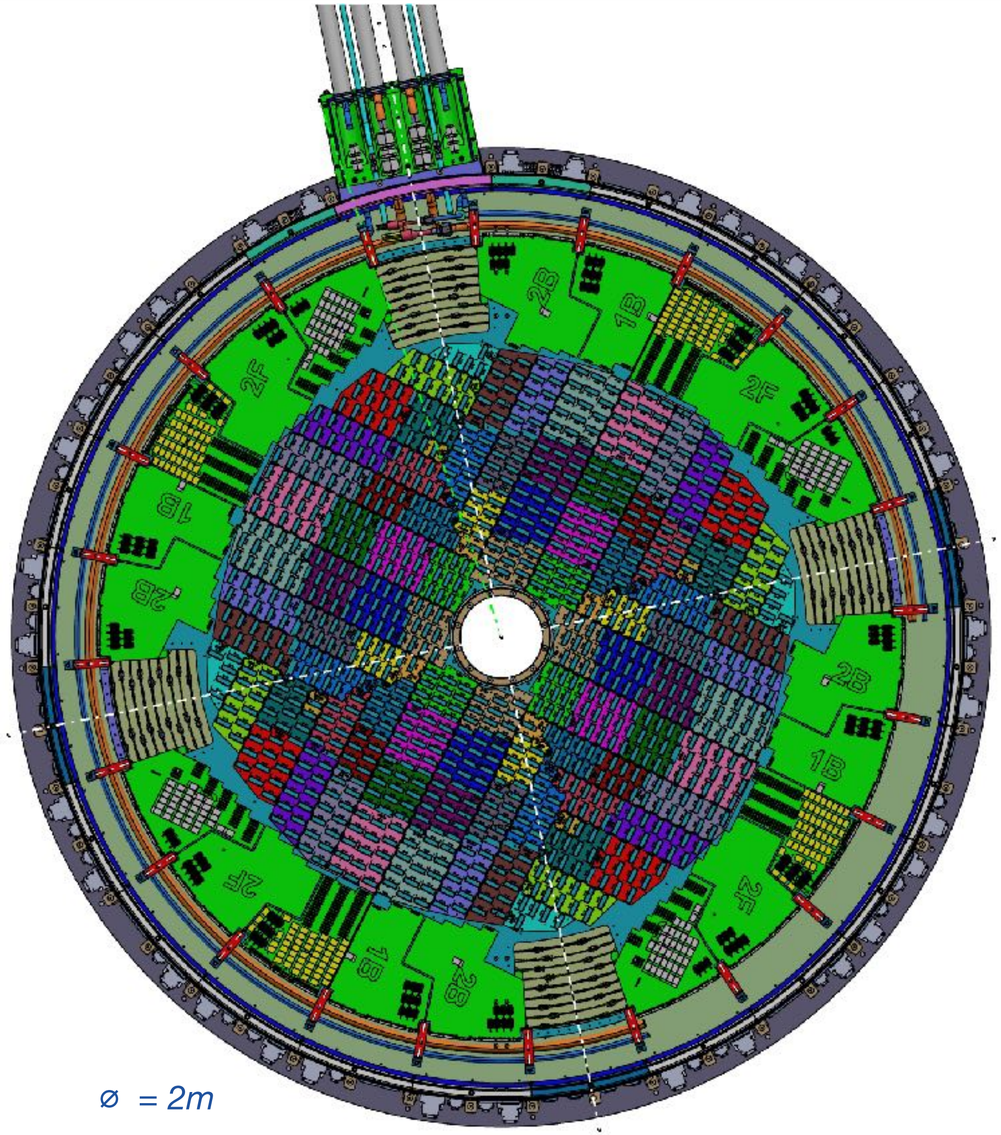
In total 768 DU to be loaded and installed in HGTD

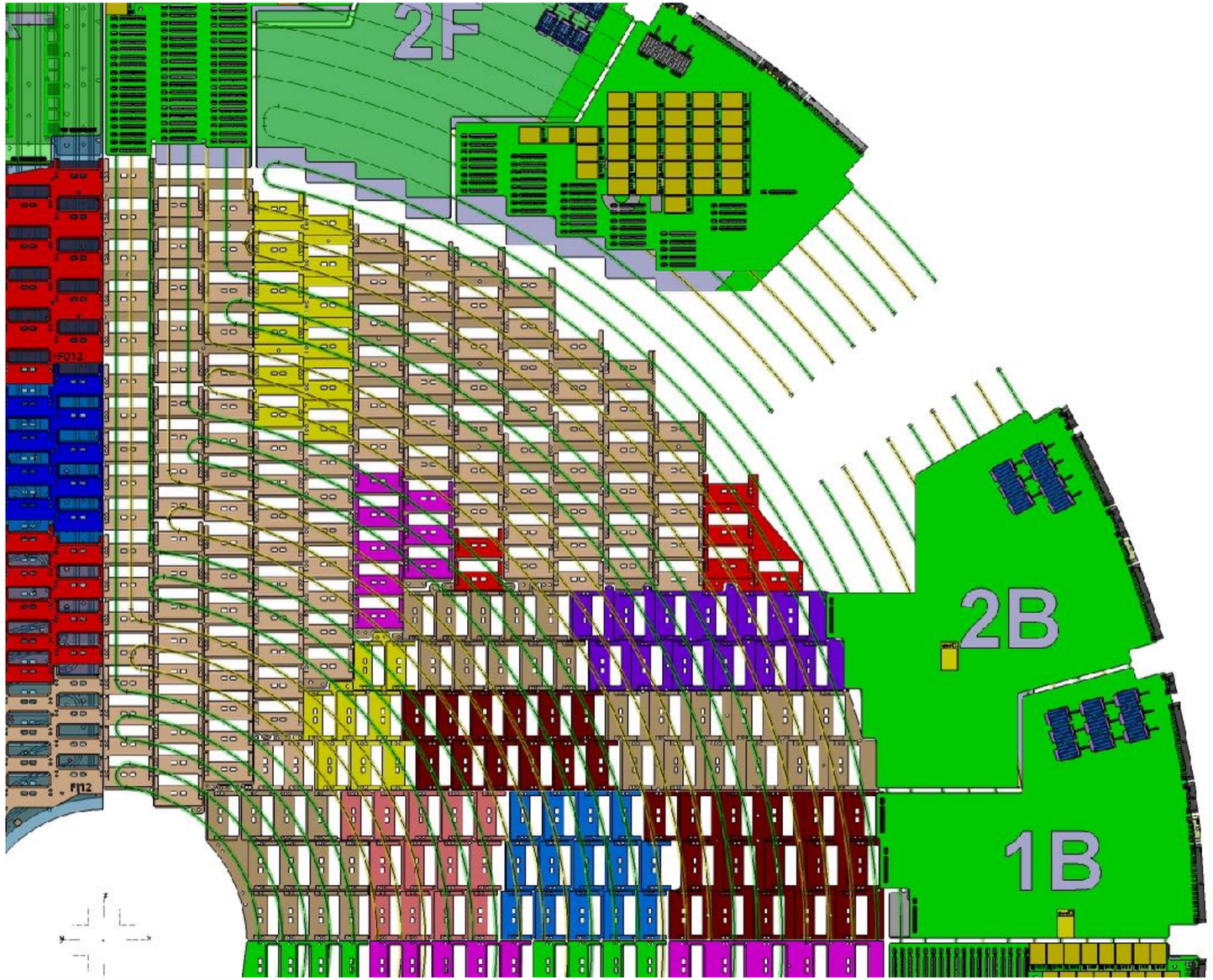
Integration and readout

- DUs are integrated on the cooling plate with the ASIC in direct contact with the cold surface
- Peripheral Electronic Boards (PEBs) are connected to modules via flex tails and provide the interface with the ATLAS experiment
  - PEBs handle power and HV distribution, slow control, interlocks, and readout



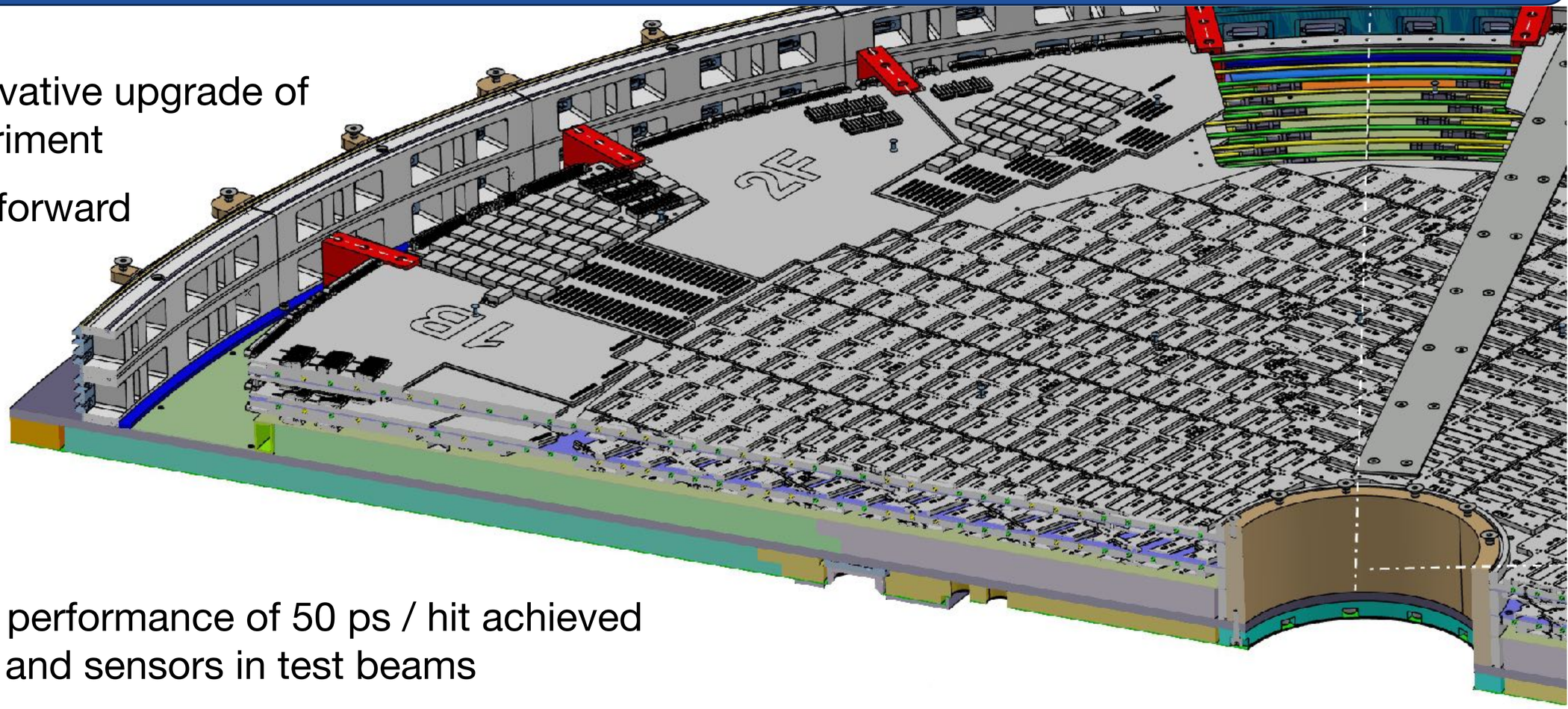
A view of the HGTD structure





Conclusions

- HGTD is an innovative upgrade of the ATLAS experiment
- Instruments the forward rapidity region and provides timing information with 35-50 ps/track resolution



- Required timing performance of 50 ps / hit achieved with final ASICs and sensors in test beams
- A large effort ongoing in characterising the design and to scale up for the detector construction
  → target completion of vessel 1 in Fall 2027 and vessel 2 in Spring 2028

Additional material

ATLAS Phase-II upgrades

Muon spectrometer

New RPC and sMDT detectors in barrel

Extended forward coverage with TGC

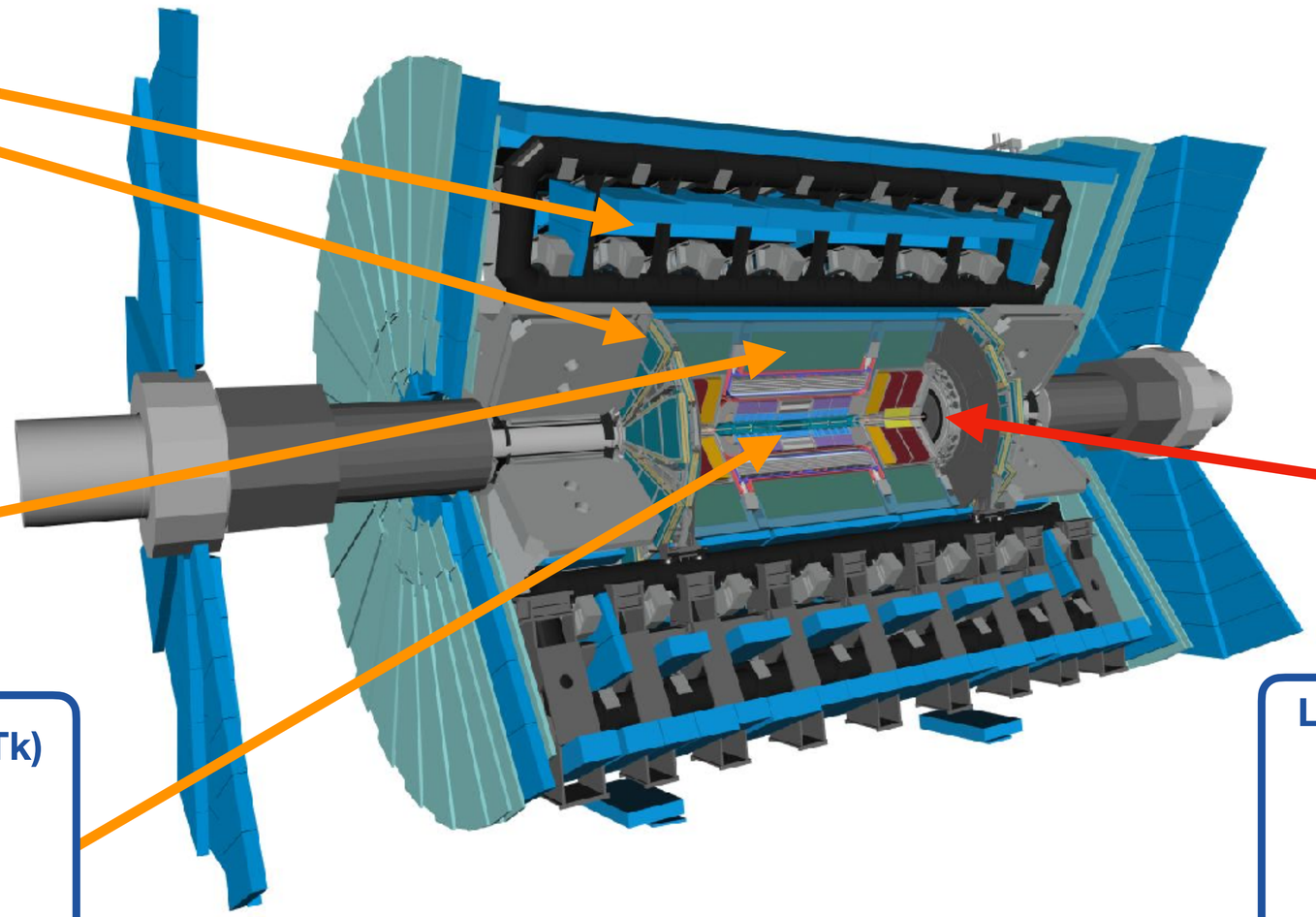
Improved trigger efficiency and resolution, reduce fakes

LAr and Tile calorimeter

Electronics upgrade
40 MHz readout for trigger

Inner Tracking detector (ITk)

All silicon
Reduced pixel size
5 pixel + 4 strip layers
Coverage up to $|\eta| < 4$



Trigger + DAQ

L1 Trigger : 1 MHz output (×10 w.r.t now)

High Level Trigger : 10 kHz output (×3-5 w.r.t now)

HGTD

Timing information

Luminosity and beam conditions monitor

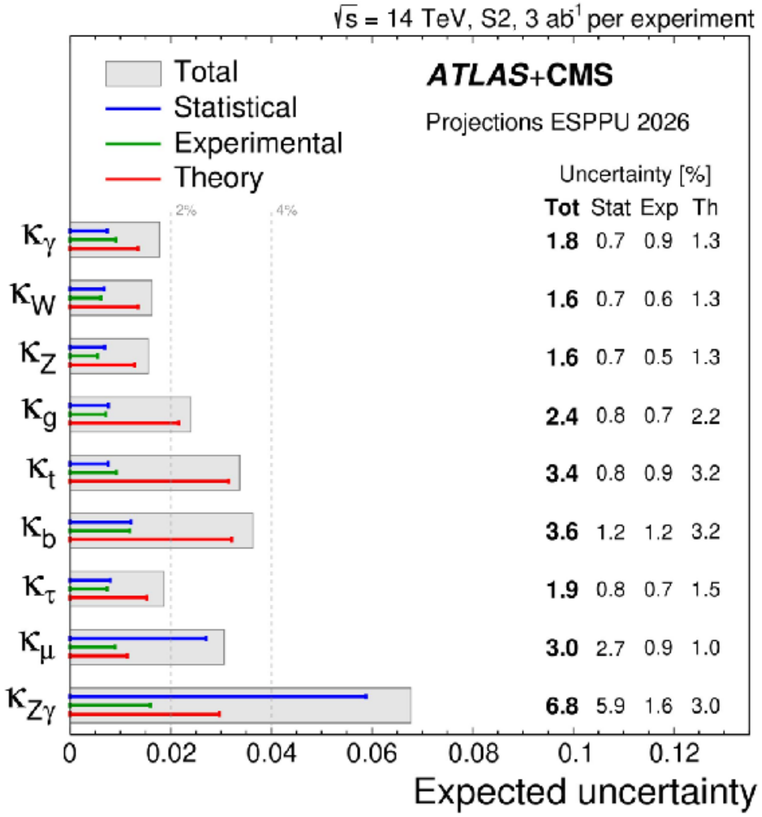
LUCID redesigned
New 3D-diamond beam monitor
New pixel lumi ring
HGTD lumi info

The high-luminosity LHC

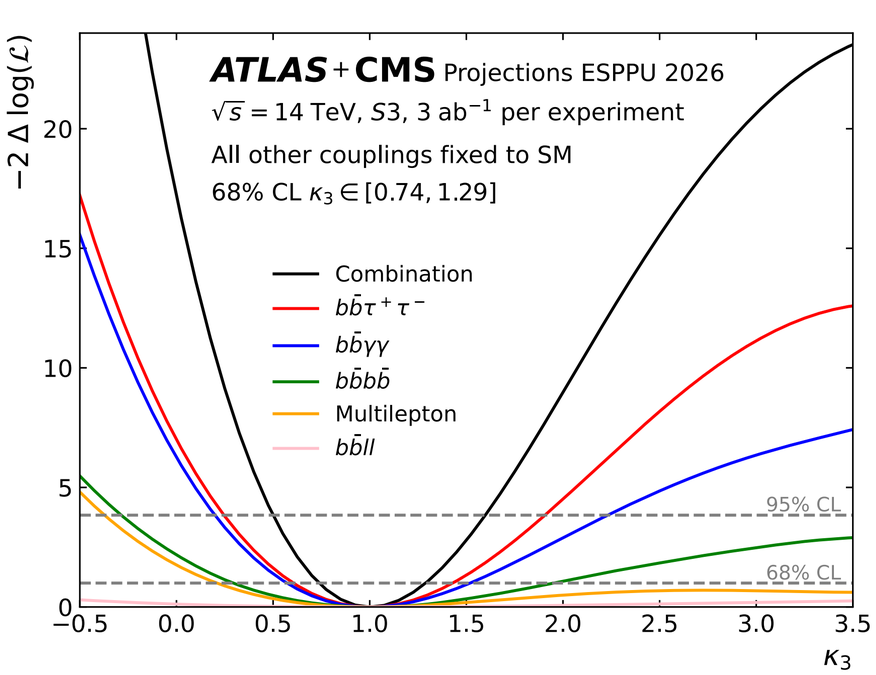


- HL-LHC will deliver ~3000 fb^{-1} to each of ATLAS/CMS in ~10 years of operations
  - to be compared against the currently available data set of 500 fb^{-1}
  - machine upgrade to increase instantaneous luminosity (up to 7.5 $\times$ 10^{34} cm^{-2} s^{-1}) : 5$\times$ nominal luminosity

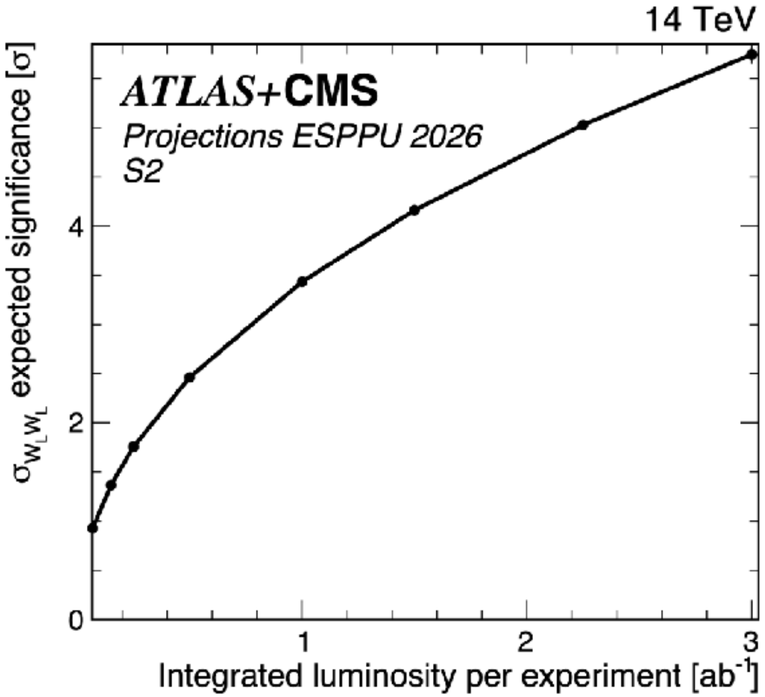
The HL-LHC physics reach



2-7% determination of Higgs couplings



Observation of HH production
(4.5σ per exp., 7.6σ comb)
30% precision on the Higgs boson self-coupling



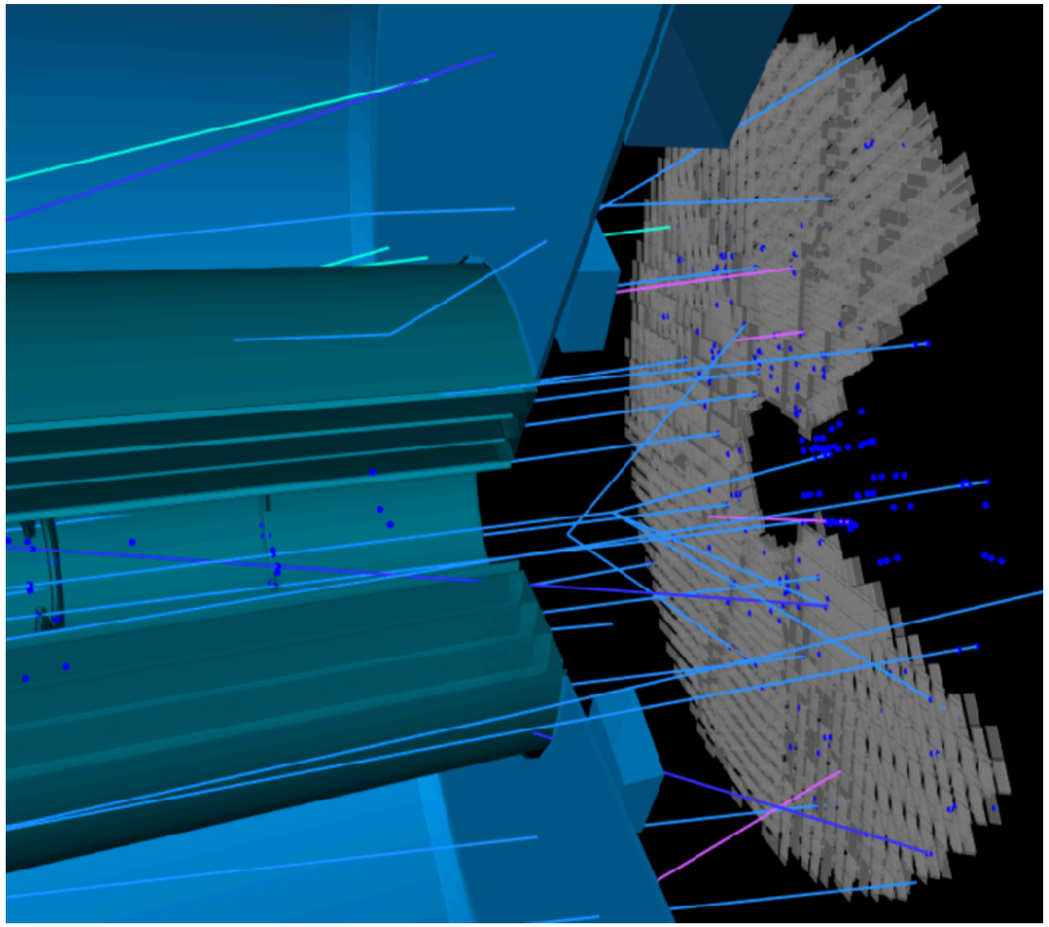
Observation of W_LW_L scattering

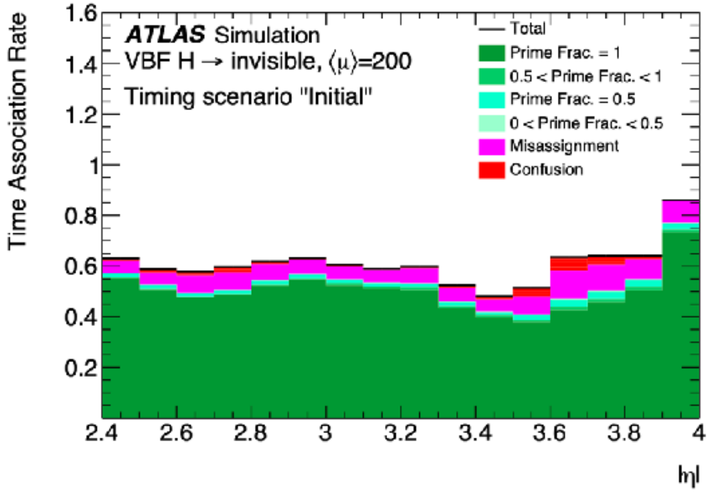
arXiv:2504.00672

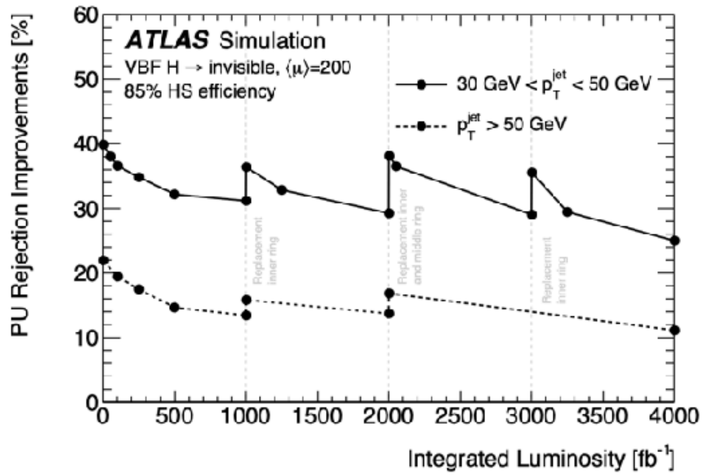
+ *Observation of rare SM processes (e.g. tttt)*
+ *Precise SM test at the TeV scale*
+ *Searches for BSM physics*

Unprecedented precision in the SM characterisation and exploration

Impact on pileup rejection



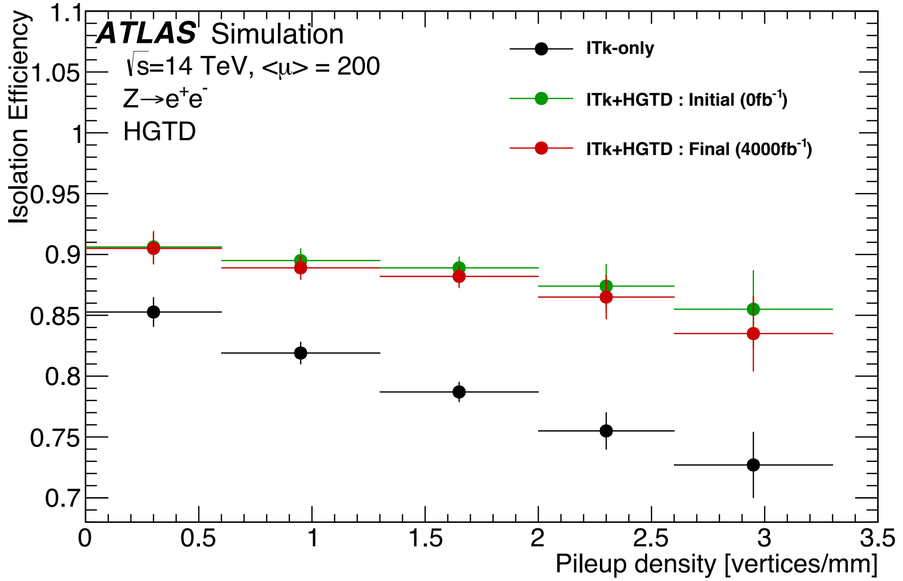




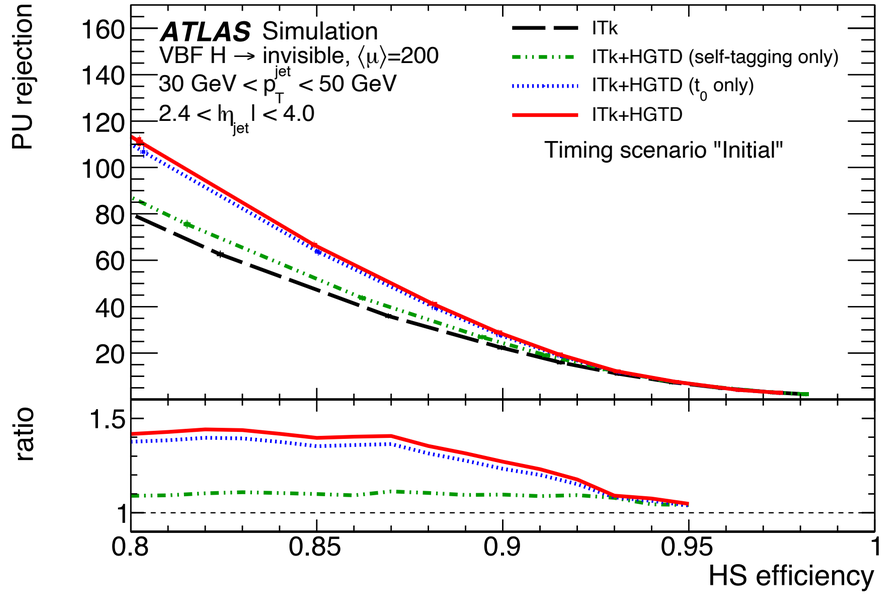
- Association of HGTD timestamp to track to arbitrate the association of tracks to the hard scatter interaction
- 20-40% better rejection of pileup contribution, especially at lower p_T

Impact on reconstruction

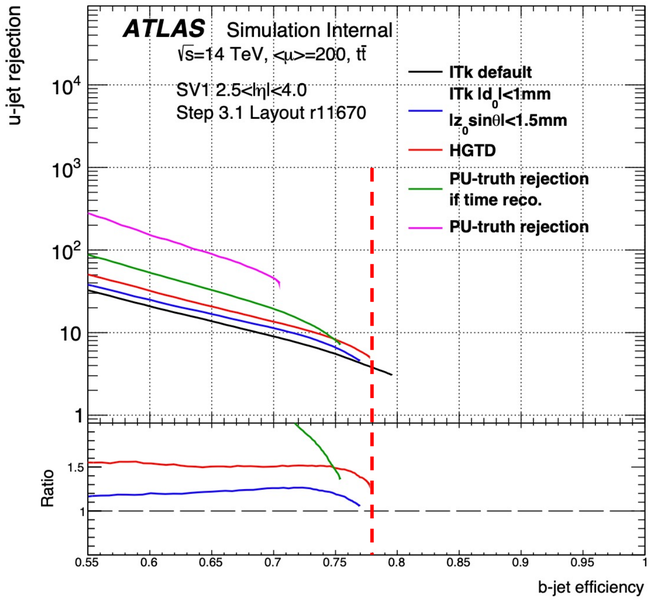
HGTD TDR



Improved isolation for e, γ



Improved rejection of PU jets



Reduced b-tagging mistag rate

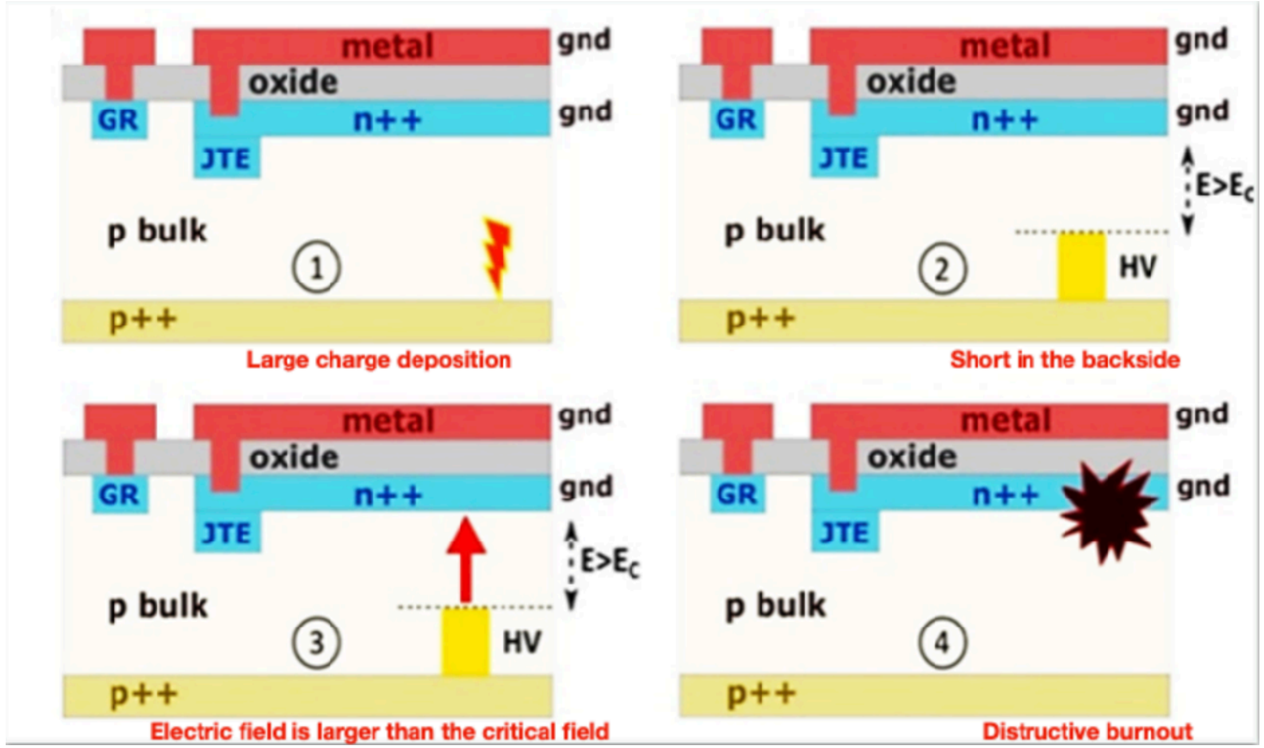
Rejection of pileup at the individual track level

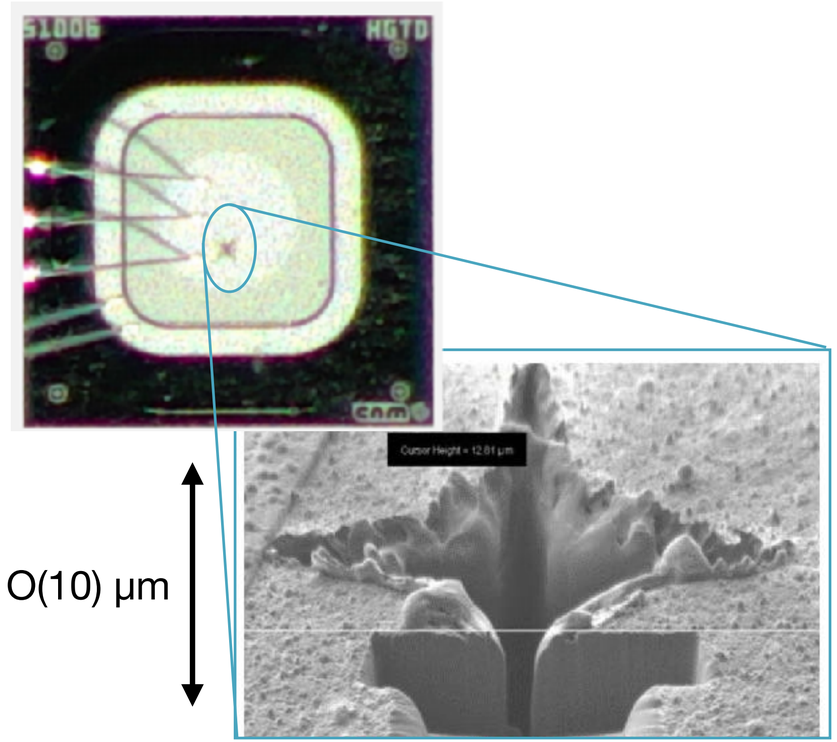
Important impact on most physics objects performance

- Impact for all physics processes with forward objects (e.g. vector boson fusion)
- A lot of work ongoing to include HGTD information in software and update reco algorithms

Single Event Burnout

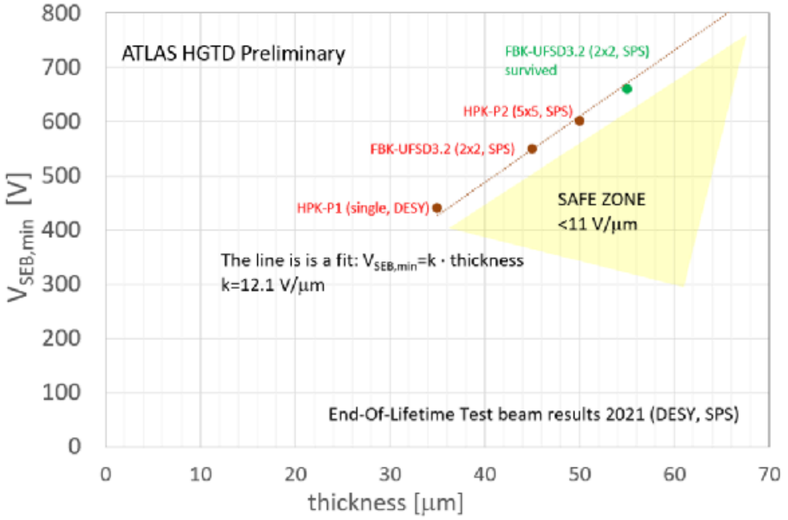
- Acceptor removal from irradiation causes gain loss → recovered by increasing V_{bias} → local breakdown causing single event burnout (SEB)
- SEB discovered in test beam in 2017-2019 : sensors lost with fluences > 1.5×10^{15} n_{eq}/cm^2
  - caused by field collapse under high concentrations of free carriers

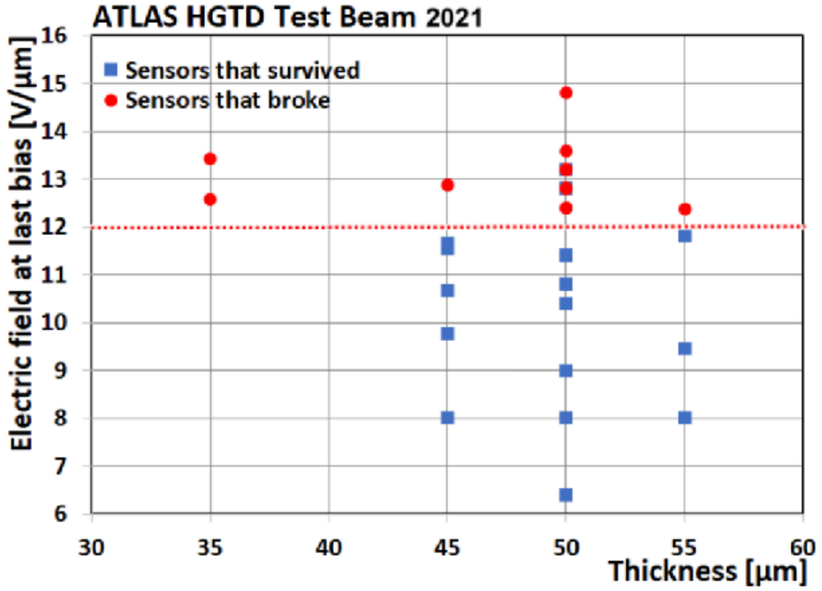




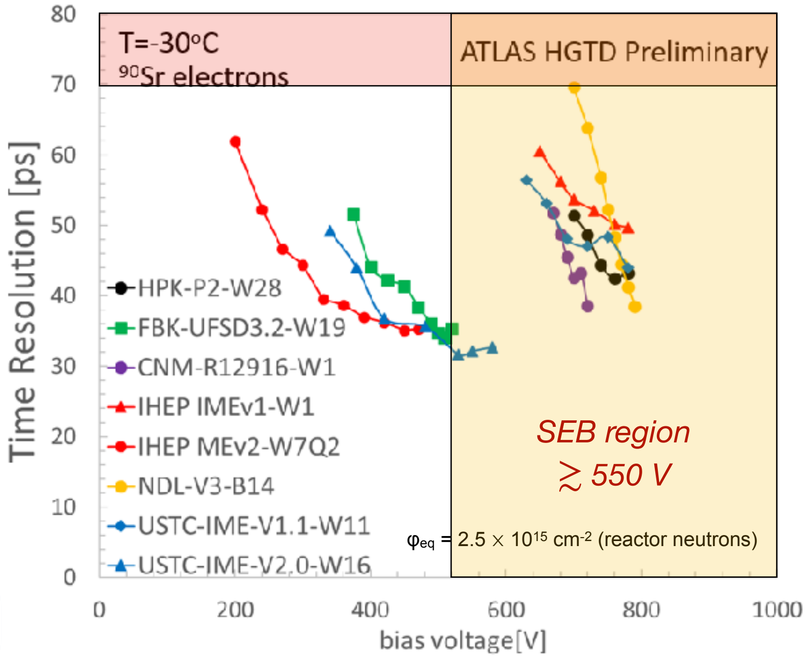
SEB and safe operation region

- A safe operation region is defined and requires $V_{op} < 11$ V / µm
- For HGTD sensors (50 µm) : operating voltage $V_{op} < 550$ V ⟹ additional constraints to keep lower V_{op} while preserving gain
- Solution : carbon-enriched gain layer to lower V_{op} while keeping similar gain





Insufficient resolution



Carbon implanted LGADs in HGTD

ALTIROC

×225

- Pixel analog front-end
  - 1 GHz preamplifier + high-speed discriminator
  - Two TDC for TOA and TOT
- Pixel digital part
  - one SRAM buffer with 38.4 µs latency
  - zero suppress logic (trigger hit selector + matched hit buffer)

×15

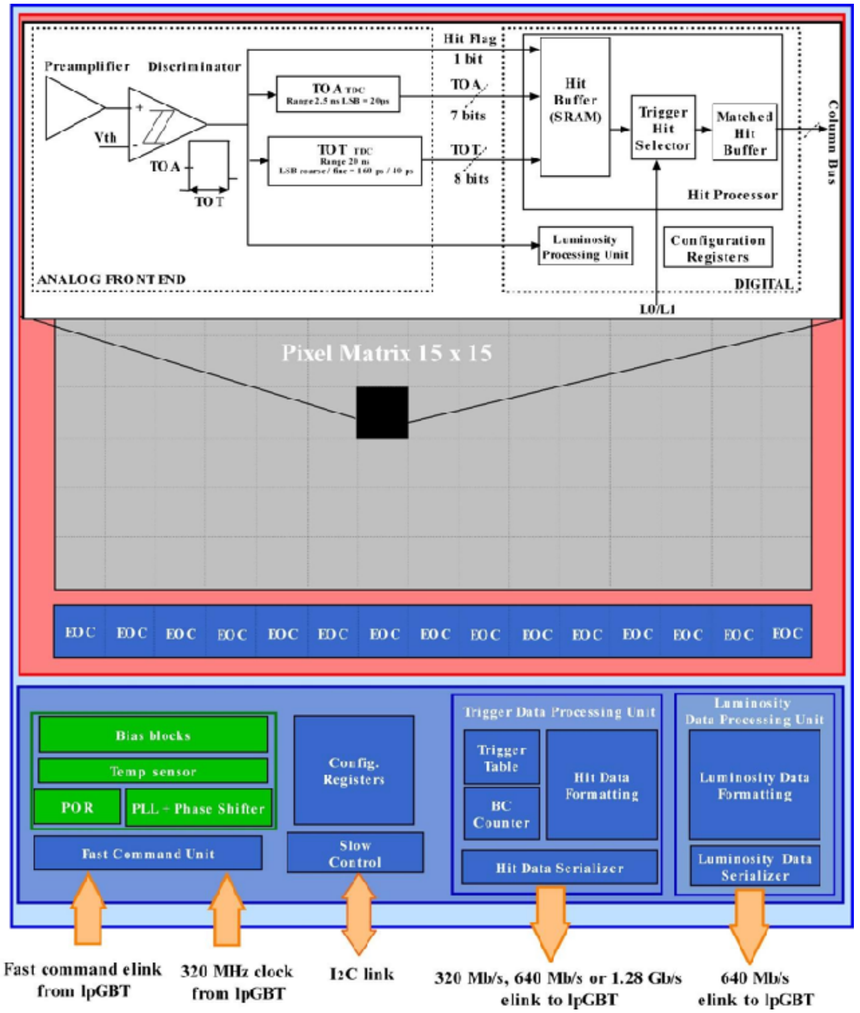
- End of Column : readout of pixel column + transfer data to trigger and lumi data processing units

- Analog periphery for bias, threshold DAC, PLL, phase shifter, clock, …
- Digital periphery : fast command decoder, I2C slow control, timing and lumi data transmission

Matrix

EOC

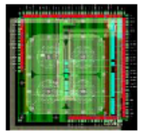
Periphery



ALTIROC versions and R&D

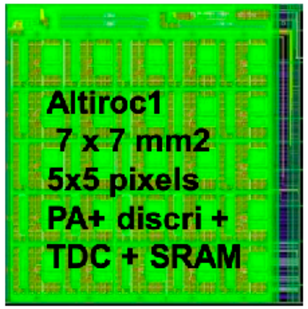
Nathalie Seguin-Moreau (link)

2016



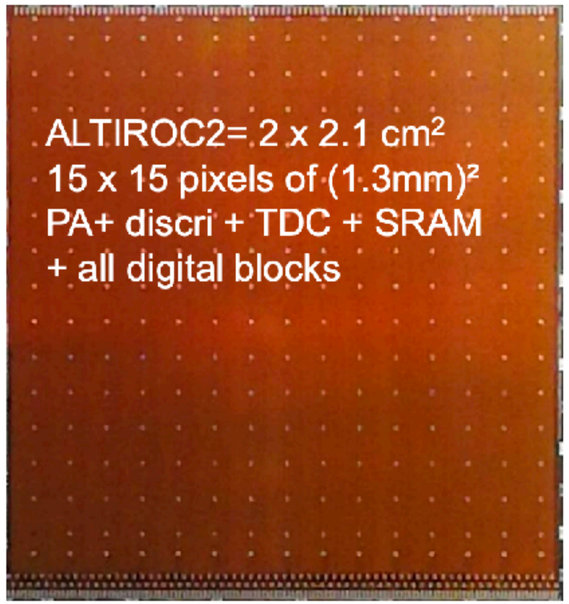
Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

2017-2018



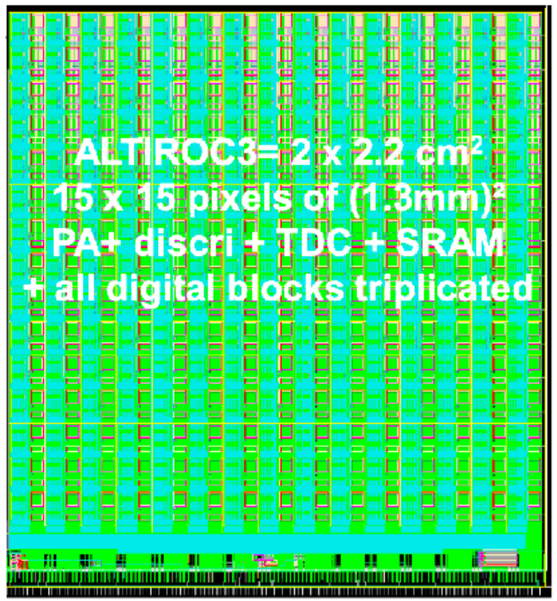
Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

Engineering run 2021



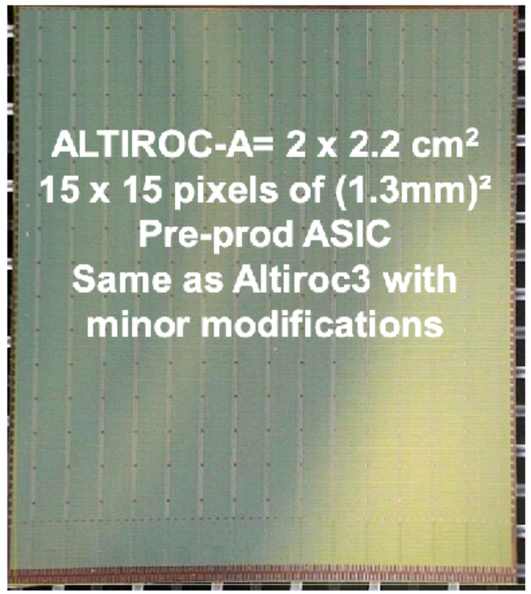
ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

Eng run June 2022



ALTIROC3:
Last full chip prototype before pre-production
Full Digital-On-Top
Same as Altiroc2 but fully triplicated
New pinout (TDC IR drops)

Eng run March 2024

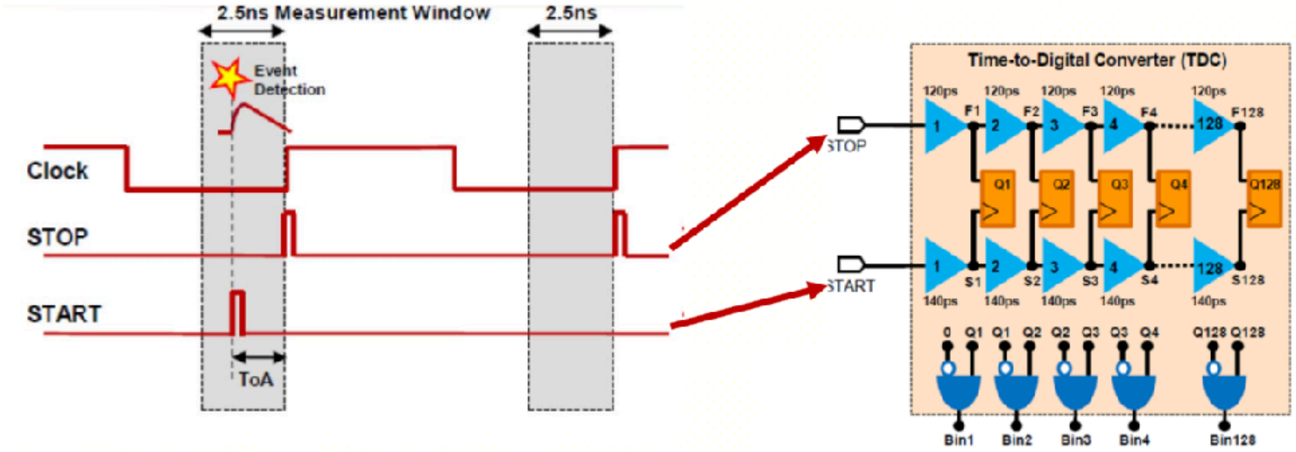


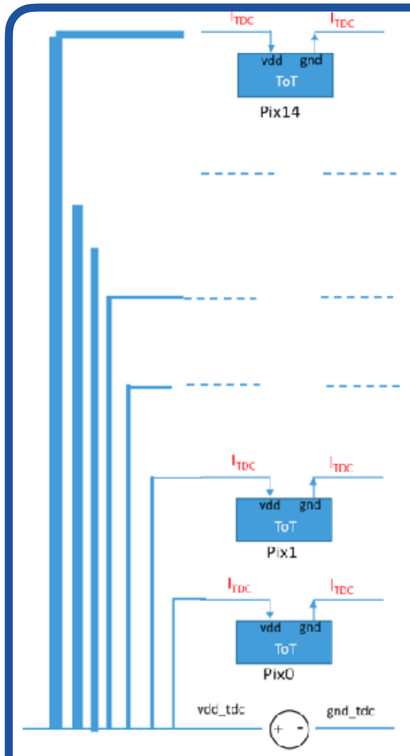
ALTIROCA:
pre-production ASIC
Same masks to be used for the production
Same as Altiroc3 with minor modifications

~10 years of R&D from initial prototypes to final production version

Time measurements with ALTIROC

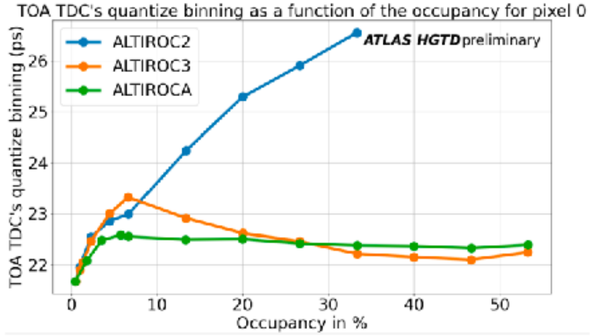
- Challenge : TOA TDC with 20 ps binning
  - cfr : 100 ps in CERN Timepix4
- Vernier Delay Lines with LSB adjusted via Vctrl
  - TOA : configuration in pair (120 ps STOP line catching up the 140 ps START line)
  - TOT : 160 ps LSB line
- High power consumption from TDCs → conversion only when a hit is present





Main challenge : ensure stability with voltage drops inside the chip

Higher occupancy → higher current recalled by the TDCs → IR drop → changes in the Vctrl

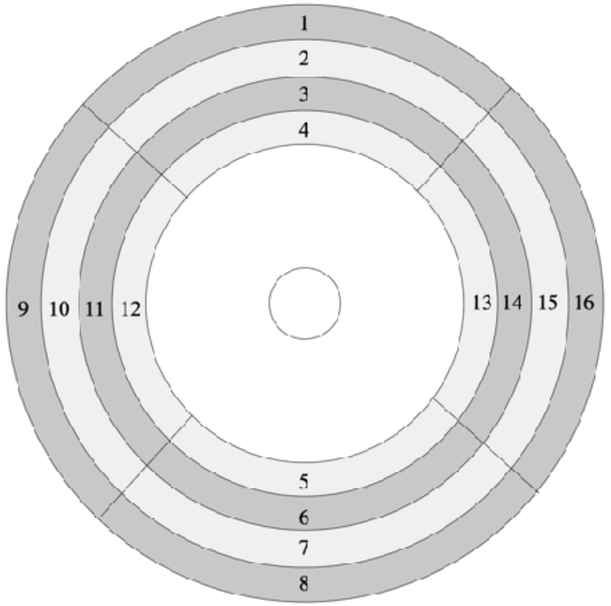


Solved in ALTIROC 3 by introducing separated TDC power bus

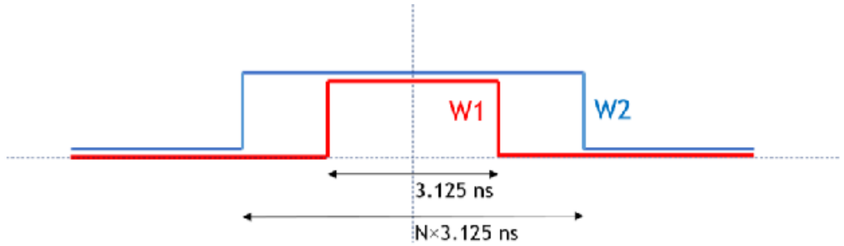
Drawback : duplicated I/O pad row → much more complicated wire bonding

Luminosity measurement

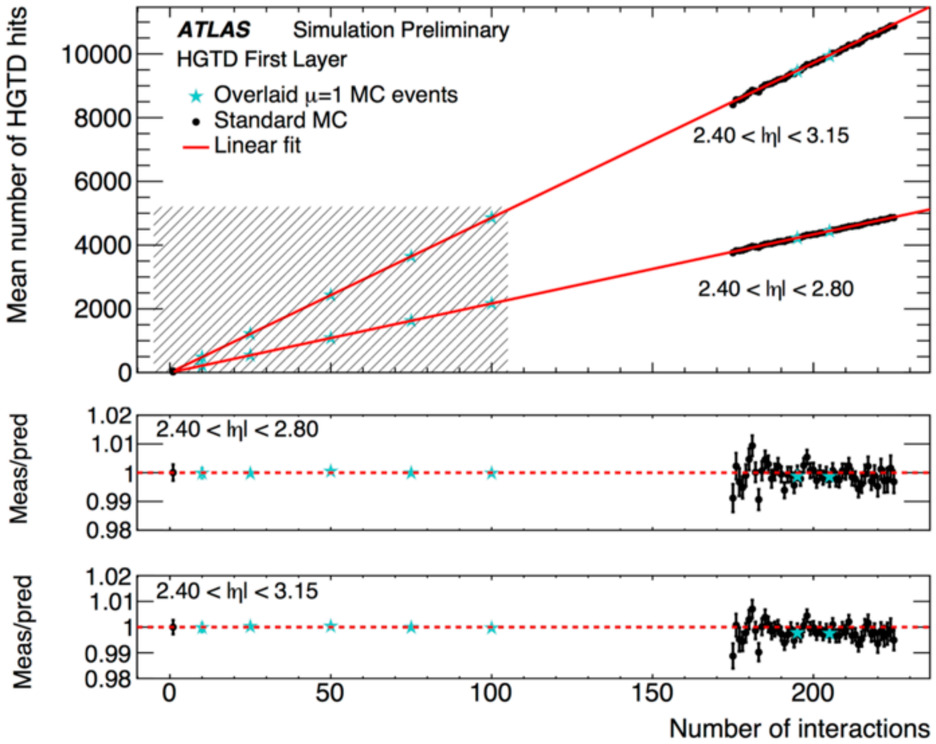
- ALTIROCs in the outer ring stream the total number of hits in two windows at 40 Mhz
- Readout off-detector boards (FELIX) boards aggregate the hits in 16 independent regions



16 independent region in the outer ring (470 < r < 640 mm)



Central time window counts (7 bits)
Sideband time window counts (5 bits)

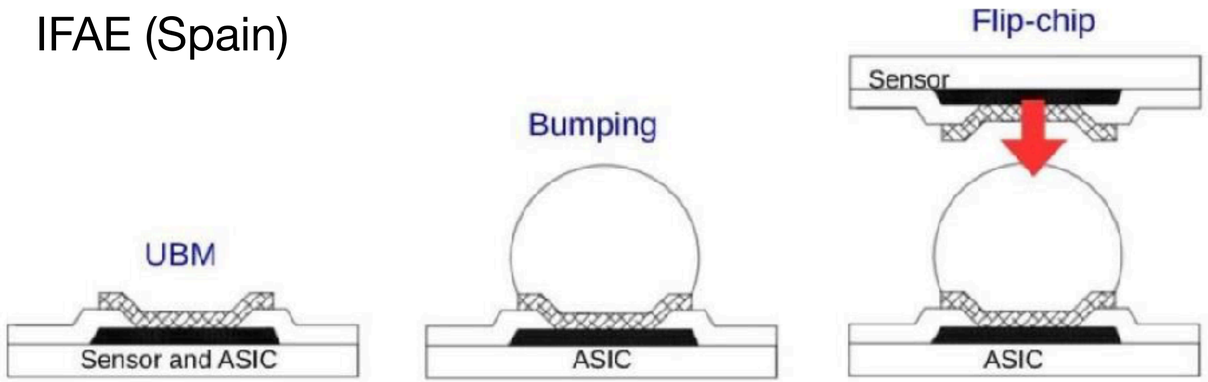


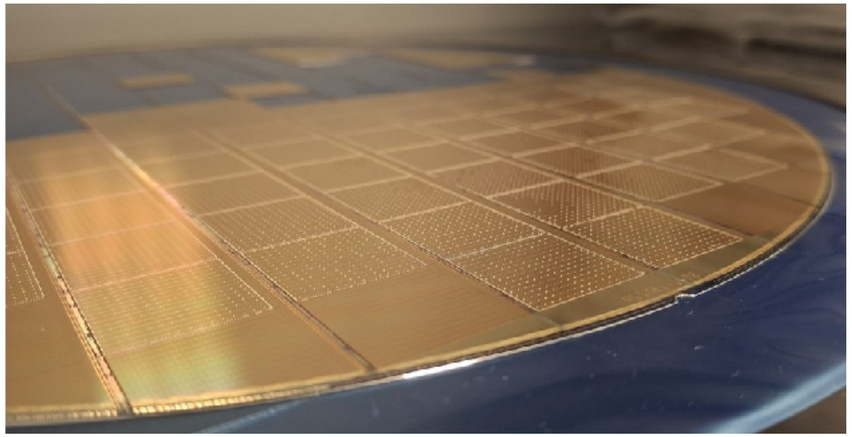
Bunch-by-bunch luminosity determination

Target : 1% precision

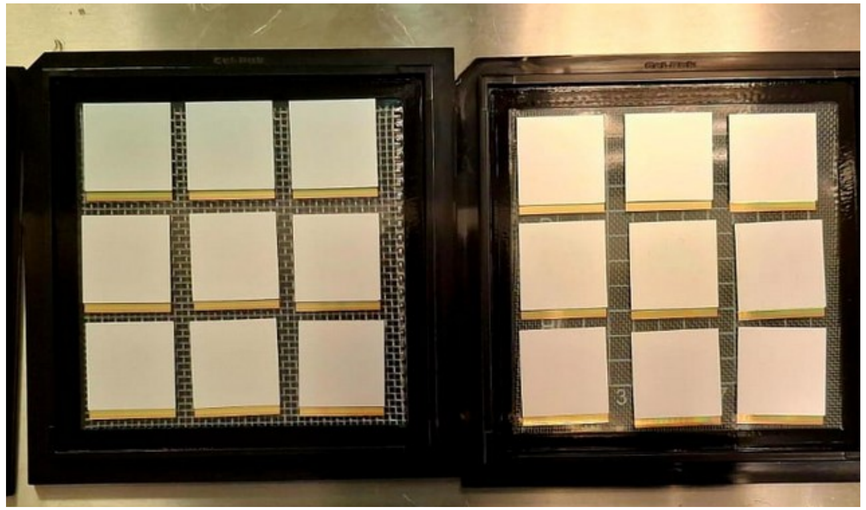
Hybridization

- HGTD Hybrid = sensor+ALTIROC (bump-bonded)
- Bump bond process
  - under-bump metallisation : deposition of metal on the sensor and ASIC pads
  - placement of solder ball on the ASIC
  - dicing of the wafers to obtain individual sensor and ASIC dies
  - flip-chip to connect ASIC and sensor pads
- Two hybridisation sites
  - NCAP (China)
  - IFAE (Spain)





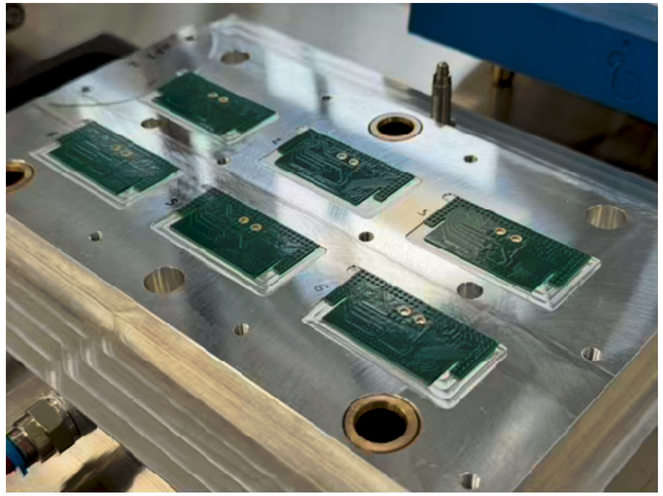
Diced ALTIROC wafer with bumps deposited

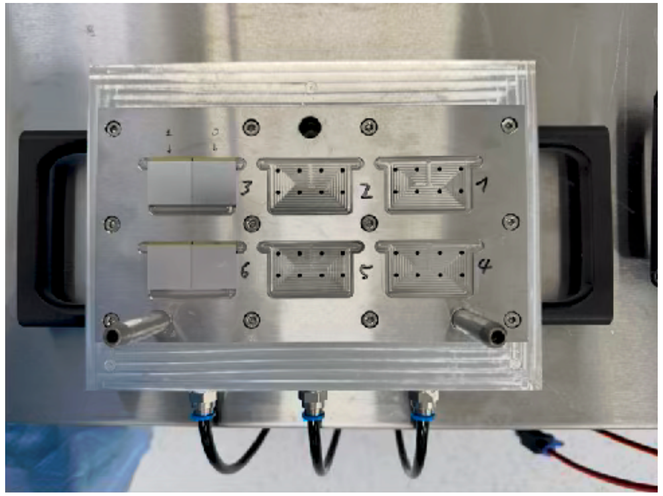


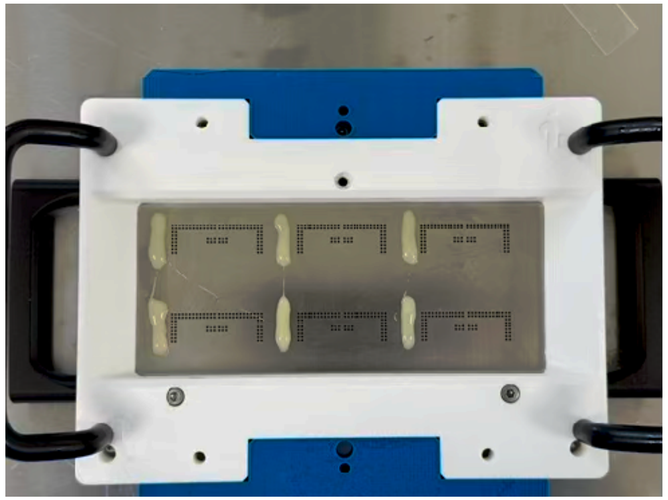
Hybrids ready after flip chip

Assembly of HGTD modules

Jig based (manual)







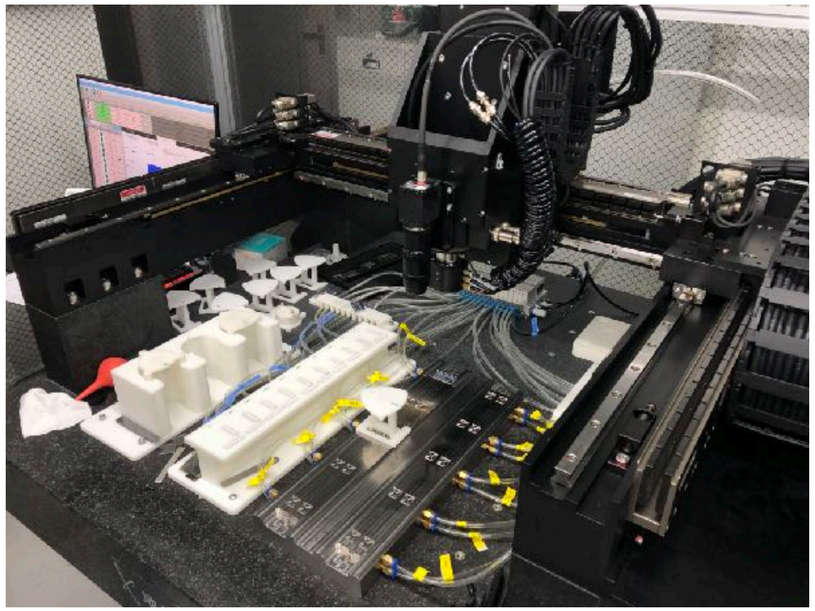
Mechanical alignment of parts

6 modules glued in parallel

Glue deposition using dispensing robot or stencil

EU + Morocco assembly sites

Gantry based (semi-automatic)



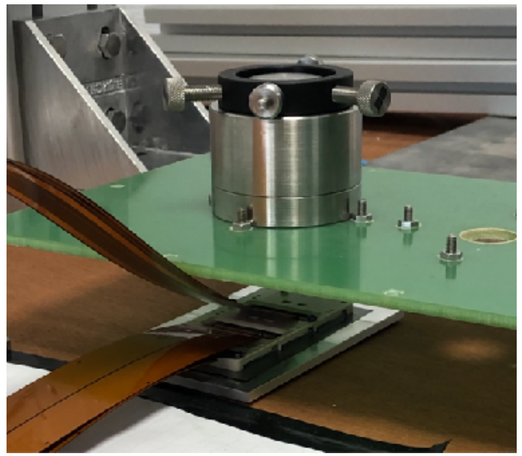
Glue deposition + alignement automated with a gantry with a camera for image recognition

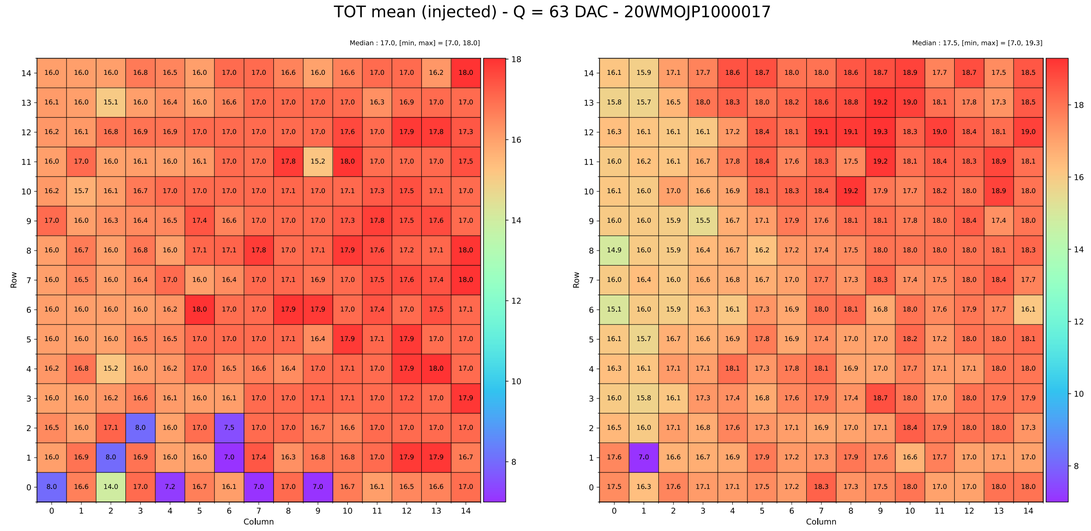
Assembly in China

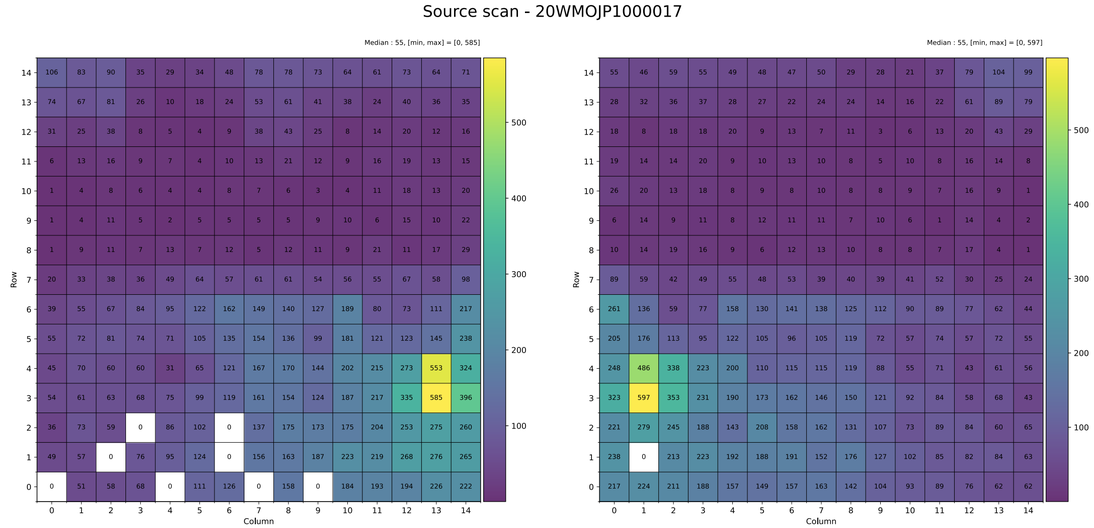
Bump connectivity

- Several redundant bump connectivity tests
  - gain measurement : $V_{out} = Q_{inj} G_{pa} / C_d$: detect disconnected pixels (smaller C_d) : from the measurement of the DAC threshold for two different Q_{inj}
  - TOT measurement : $t_{fall} \propto R_{in} C_d$: smaller TOT for disconnected pixels
  - source scan with ^{90}Sr beta source : direct measurement

Verification of individual bump connectivity

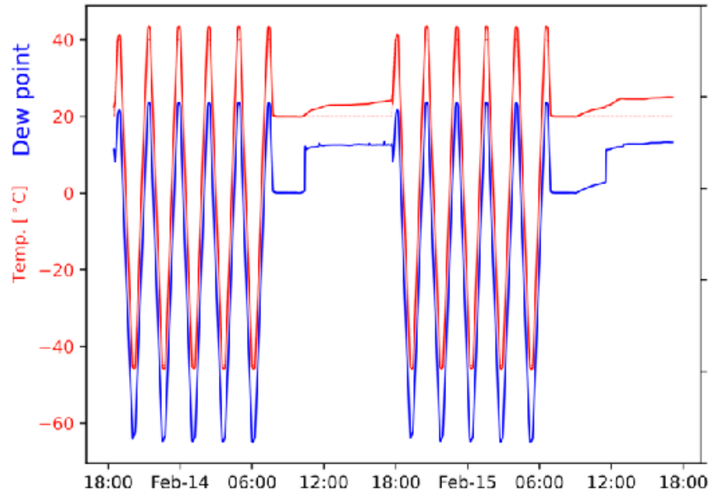






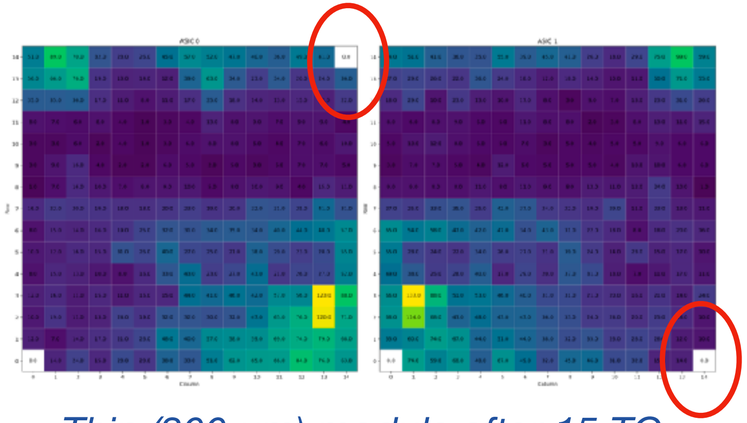
Module thermal cycling

- Silicon and module flex (w/ copper) have different CTE : stress on bumps under thermal cycles
  - large failures observed in first prototypes with ALTIROC 3
- Extensive test of thermal stress properties (arXiv;2509.14045)
  - finite element simulation + lab measurements with thermal cycles of HGTD modules
- Choice of unthinned sensors (775 µm) for better resistance against thermal cycles + optimal glue pattern

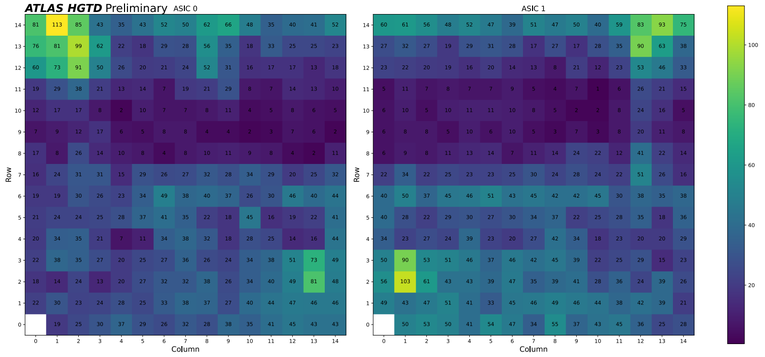


Extreme TC beyond HGTD operating range

Estimated to fulfil the HGTD lifetime requirements



Thin (300 µm) module after 15 TC

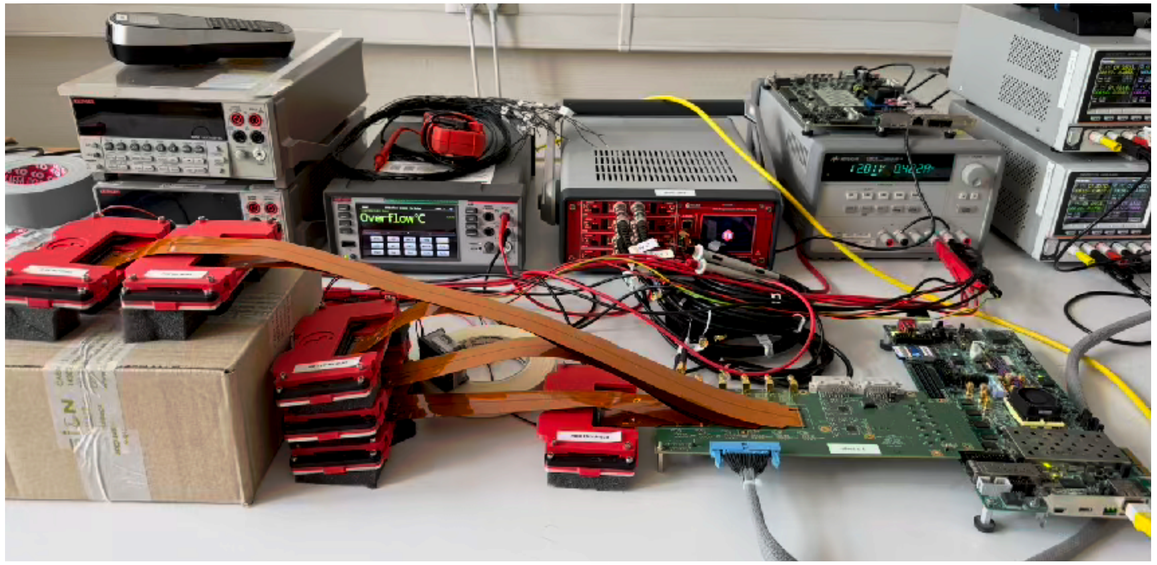


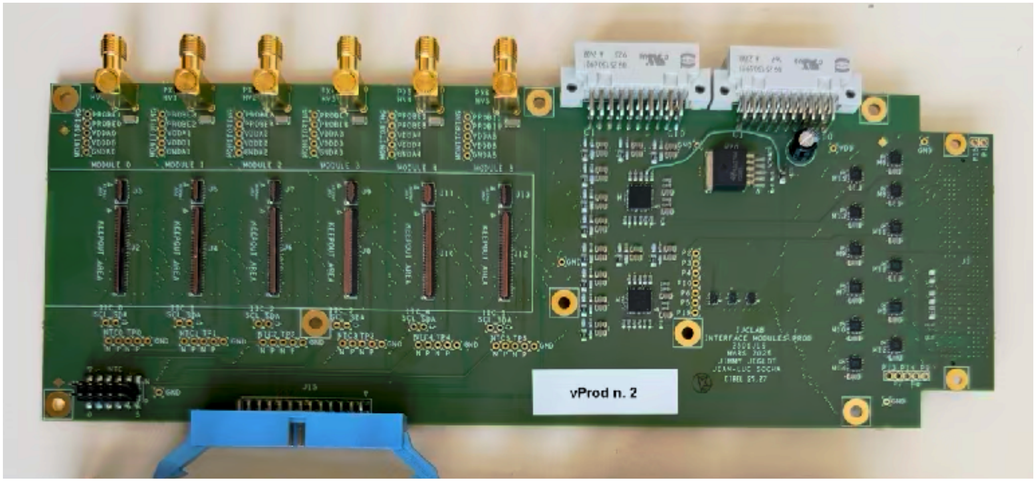
Thick (775 µm) module after 120 TC

Note : pixel 0 (bottom left) intentionally disconnected

Module test setup

- FPGA-based readout system
  - two readout firmware and software developed
- Readout system scaled up to read 6 modules in parallel (12 ASICs) to improve testing speed
- Results stored in an ATLAS-wide production DB

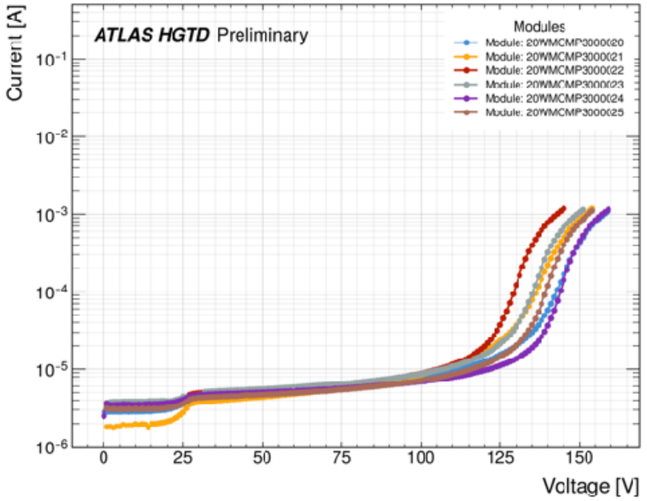


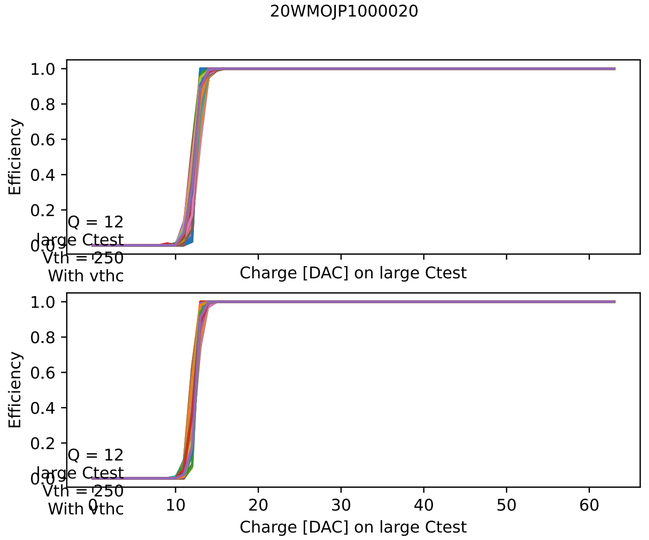


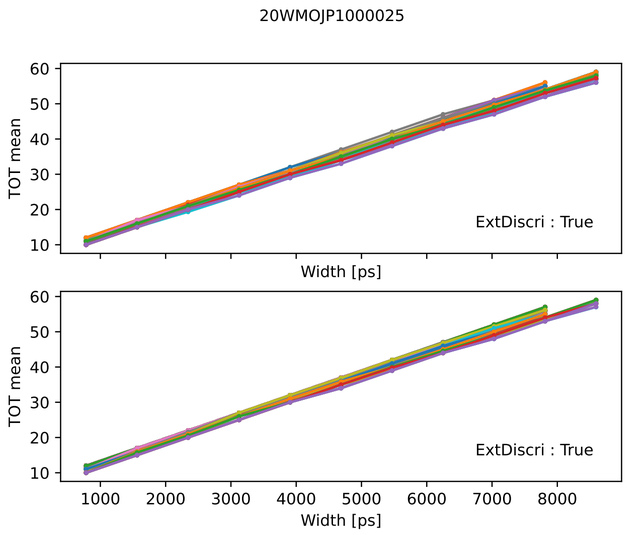
Test setup ready and deployed at all assembly sites, 6 modules characterised in parallel

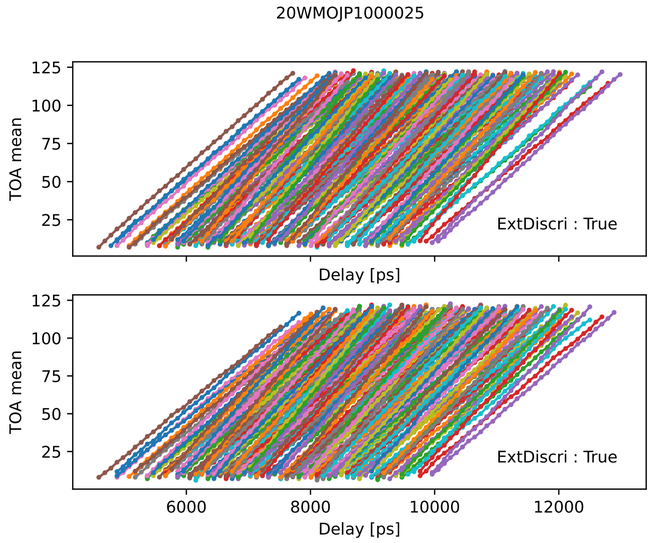
Modules QA / QC procedures

- IV characteristic curve
- Alignement of pixel thresholds and verification of response for a standard charge Q ~ 5 fC
- Verification of the linearity of the TOA and TOT TDCs
- Bump connectivity and source scan verification
- Currently preproduction ongoing (~5% of HGTD), full production will run until early 2028



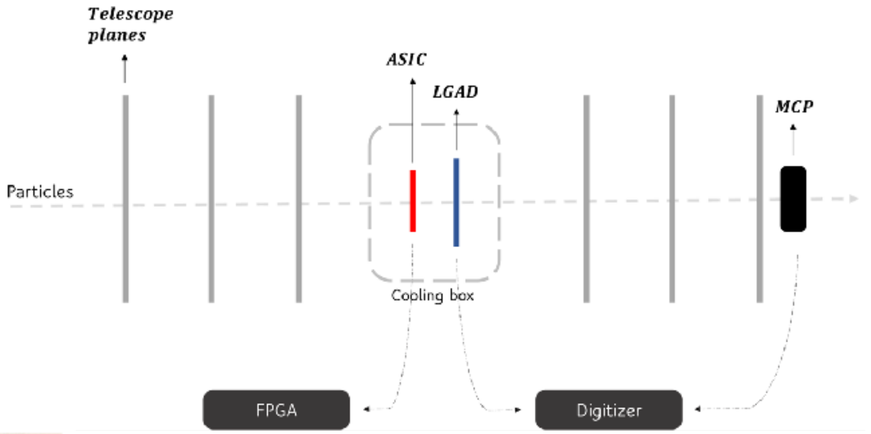


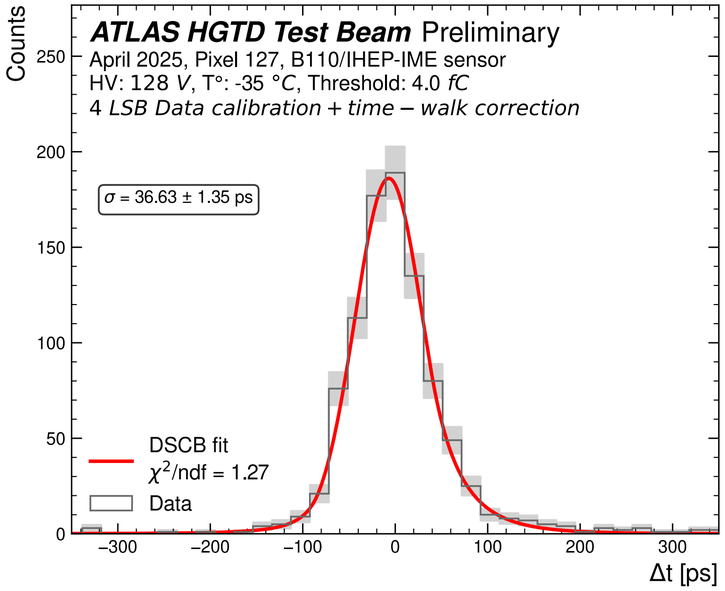




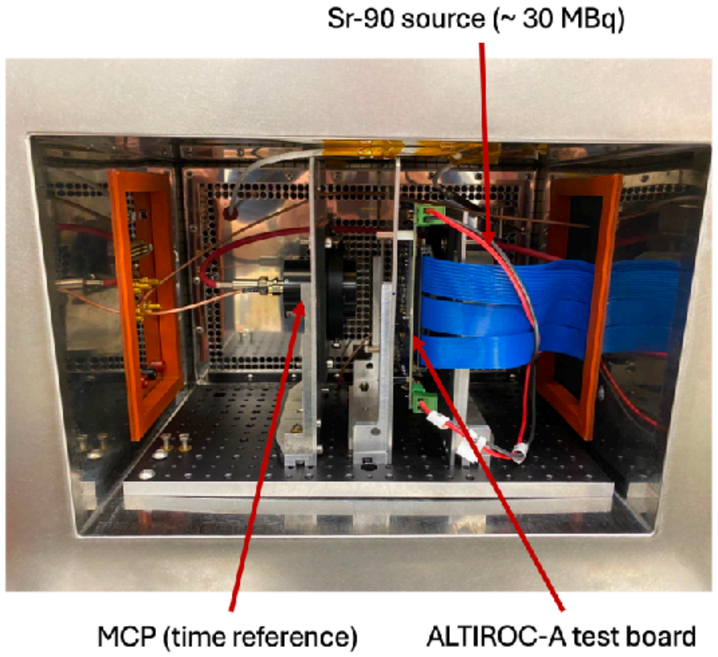
Testbeam and source measurements

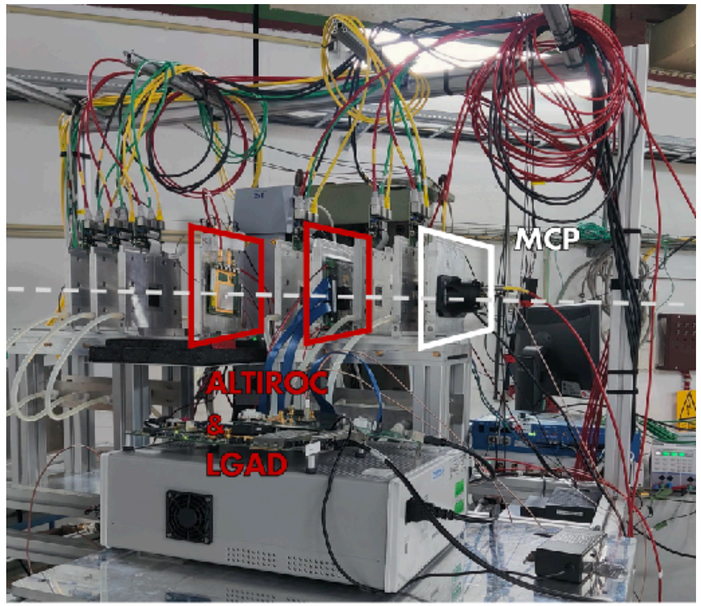
- Two types of setup for performance characterisation
  - test beam (includes tracking)
  - source setup (no tracking, limited rate, higher availability)
- Time reference provided by MCP-PMT, spatial reference by beam telescope





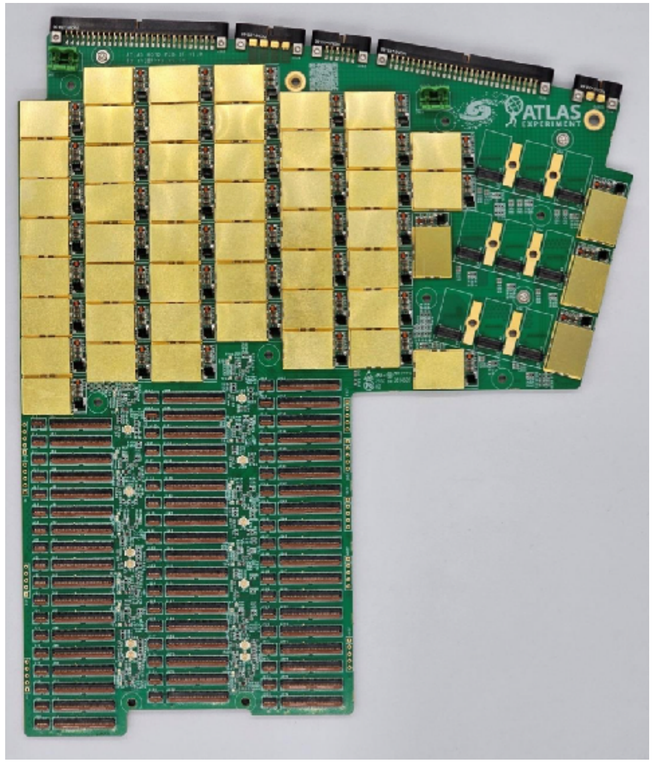
$$\Delta t = \mathrm{TOA} \times \mathrm{LSB} - (t_{clock} - t_{MCP})$$

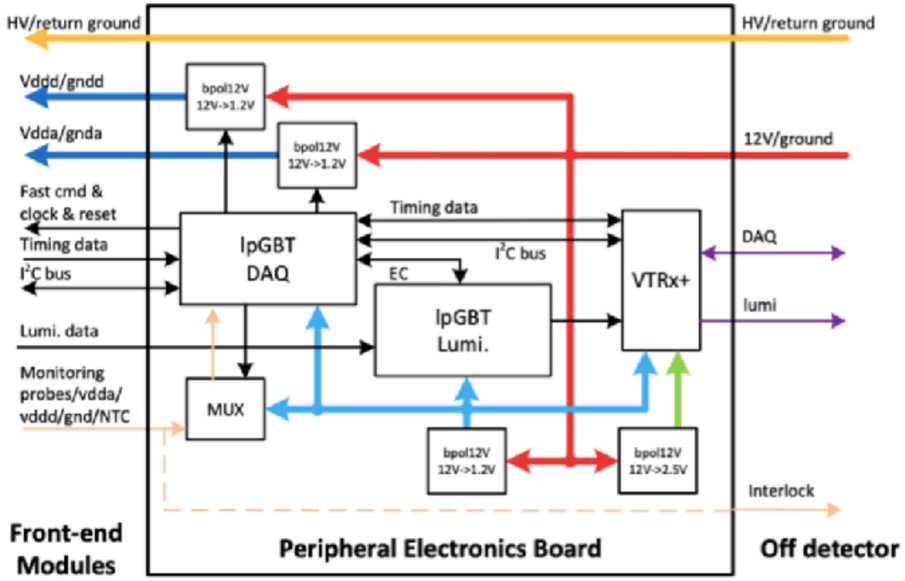




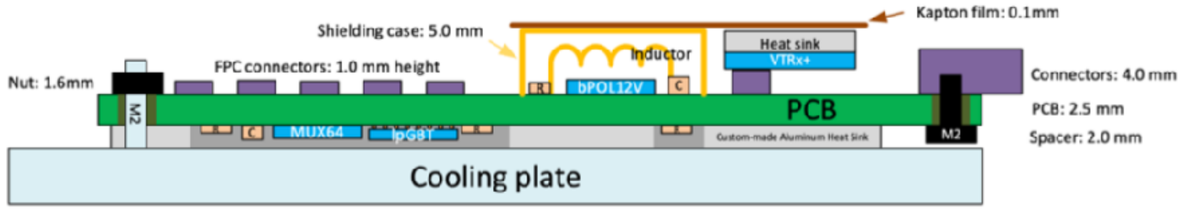
Peripheral Electronic Boards

- Peripheral Electronic Boards handle power and HV distribution, slow control, interlocks, and readout
- Very complex board (22 layers PCB)
  - lpGBT and VTRx+ for timing and lumi data
  - bPOL 12V DC-DC converters (up to 28 per LV channel) : mitigation strategies being designed for the current bPOL issue
  - independent HV channel (1 per module)



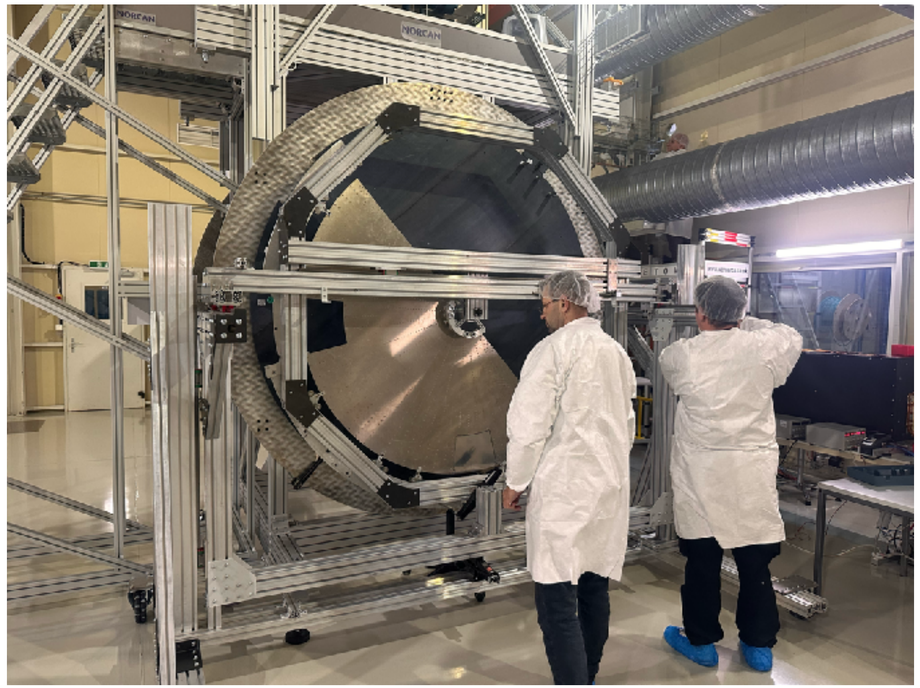


6 different flavours of PEB, all with very tight geometrical envelope



Assembly at CERN

- Assembly tooling in a clean room at b180 @ CERN
- Used to install SU onto cooling plate, and test at surface each assembled half-disk at the operation temperature of -30 °C with CO_2 cooling

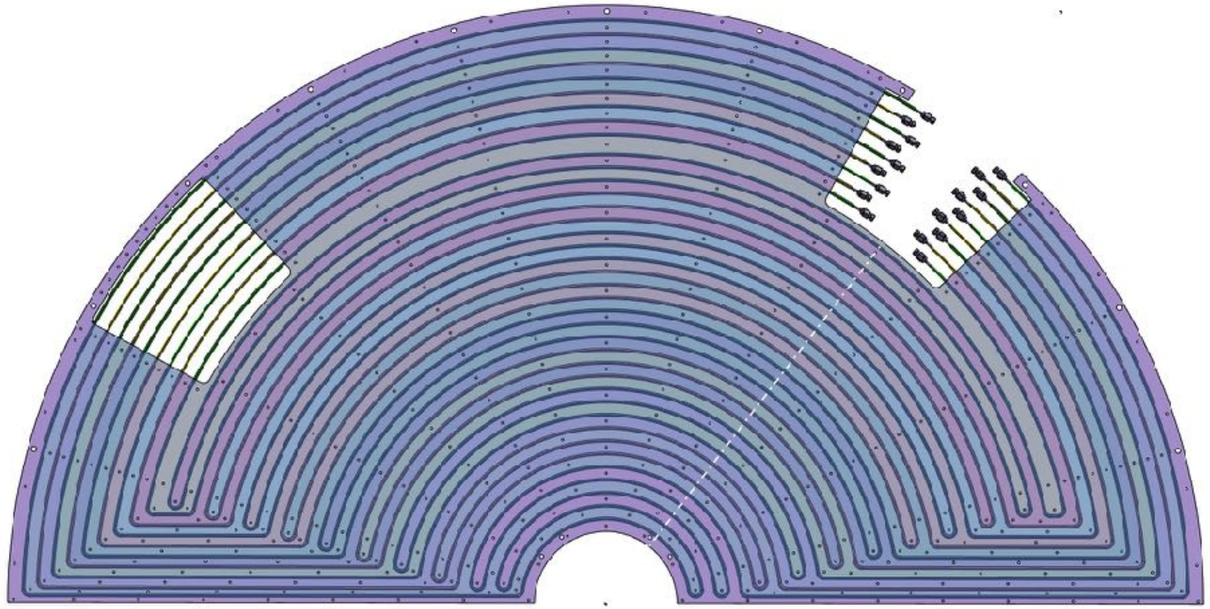


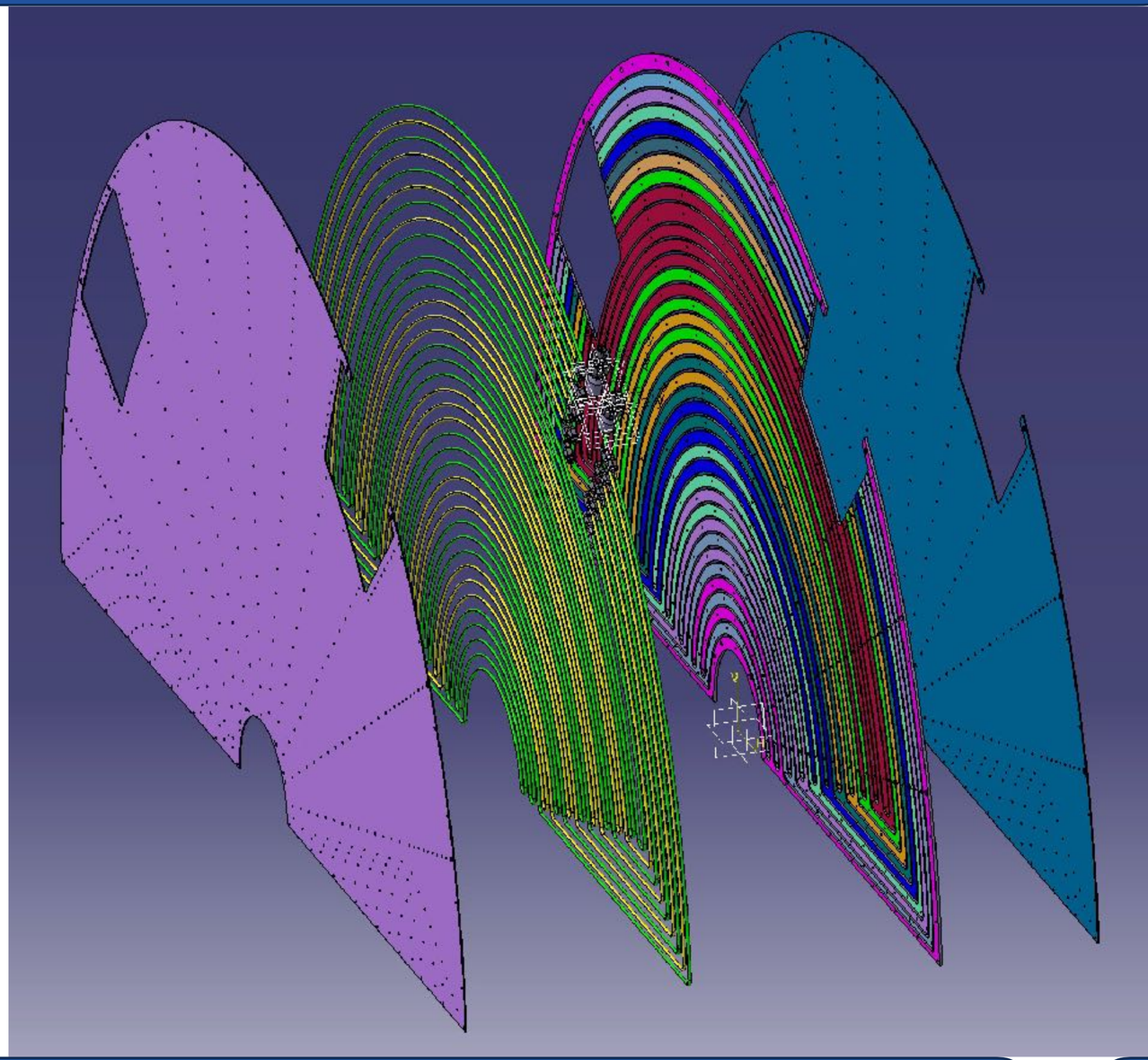




CO_2 cooling

- CO_2 dual phase cooling system
- The detector will be operated at -35 °C
- ASICs are in direct contact with the cooling plate (highest heat load)
- Cooling power of 20 kW/end-cap



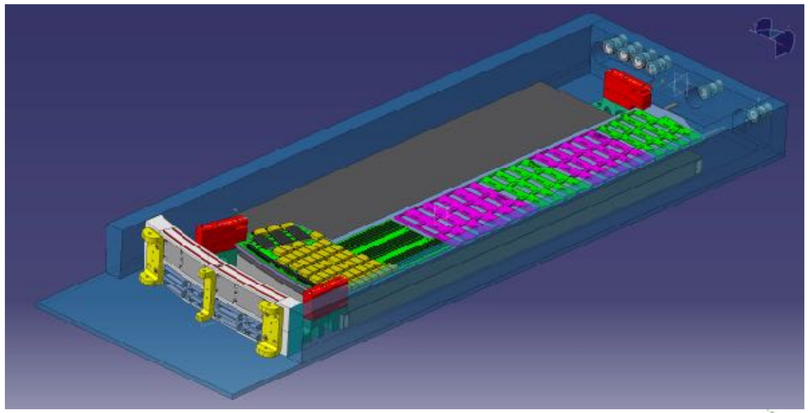


Demonstrator and Module-0

- Early thermal demonstrators
- 1st generation demonstrator assembled with R&D modules of type ALTIROC-2 and 3
  - test of the installation procedures, test of PEB readout (JINST 19 (2024) C12012), cooling tests
- 2nd generation demonstrator to be assembled in 2026
  - ALTIROC A modules : full study of the final system performance
- A one-side full quarter of HGTD (Module-0) will be built in 2026
  - practice full scale test and integration procedures

First generation demonstrator *(ALTIROC 2 + 3)*





Second generation demonstrator *(ALTIROC A)*

Module-0 *(ALTIROC A)*

