Tests and performance of the LAr Phase-II calibration ASICs and board

Oleksii Kurdysh

12Oct26 / French-Ukrainian Workshop 2026

LAr Calibration electronics team and scope

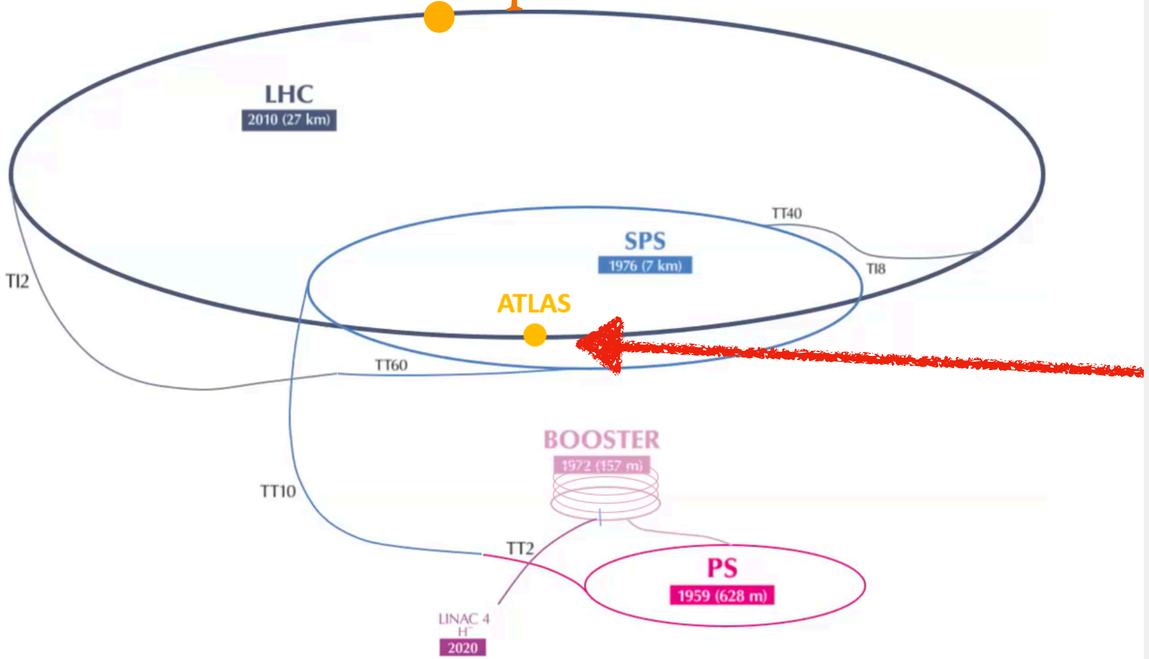
- LAPP Annecy:
  - Olivier Arnaez
  - Florent Bernon
  - Marco Delmastro
  - Oleksii Kurdysh
- IJCLab Orsay:
  - Laurent Duflot
  - Nicolas Morange
  - Laurent Serin
  - Stefan Simion
- OMEGA Palaiseau:
  - Ludovic Raux
  - Christophe de La Taille

- Aim: design, manufacture, and characterize 150 LAr calibration boards that will be used by ATLAS during HL-LHC

Introduction

- Most of the data-taking done with proton-proton collisions

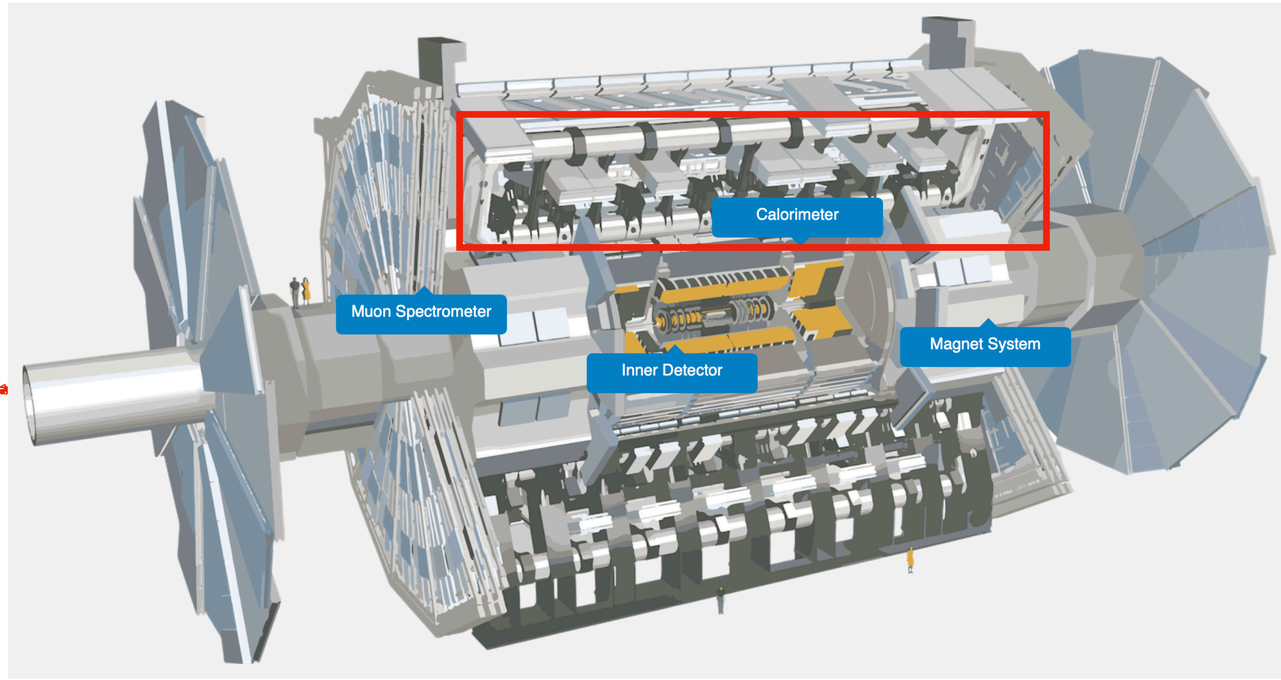
Our twin/competitor CMS



- Beam energy 6.8 TeV

- Cylindrical, ~hermetic

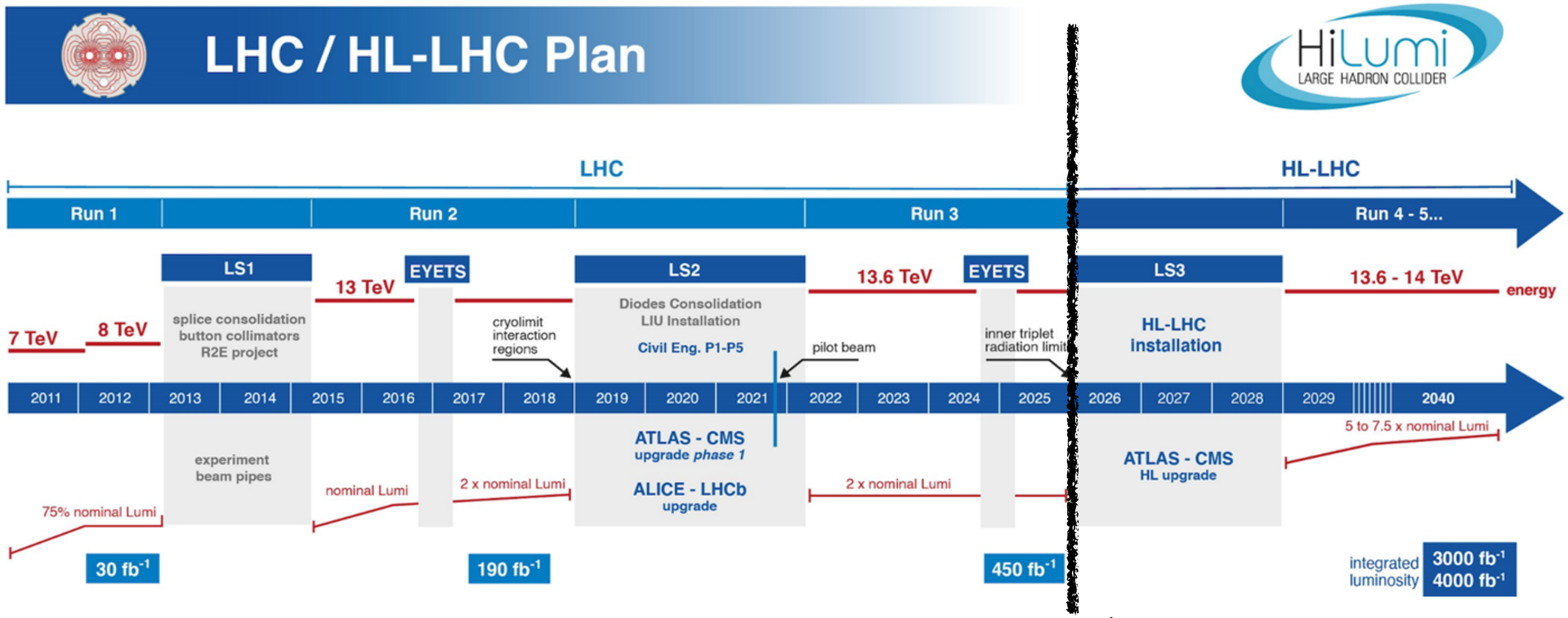
- Layers of sub-detectors



- Reconstruction of all types of objects useful for physics analyses like electrons, muon, jets

Introduction

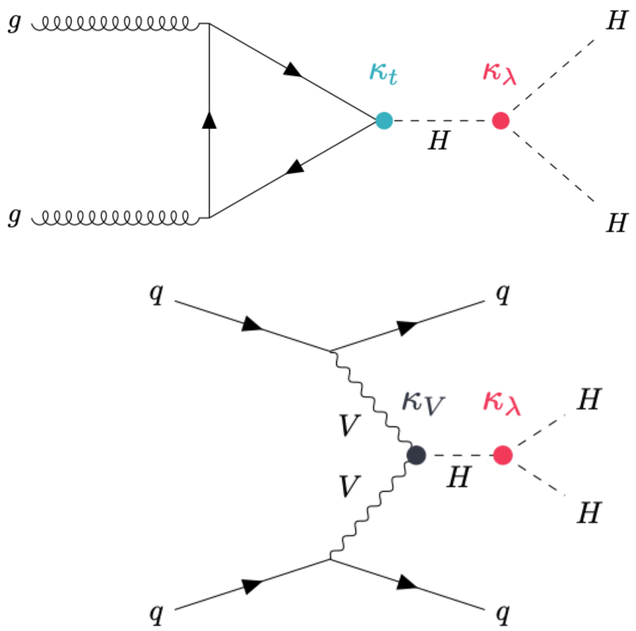
- 2008: first collisions
- 2026: collected ~450 1/fb
- 2030: supposed to restart with higher luminosity; aim: 3000 1/fb

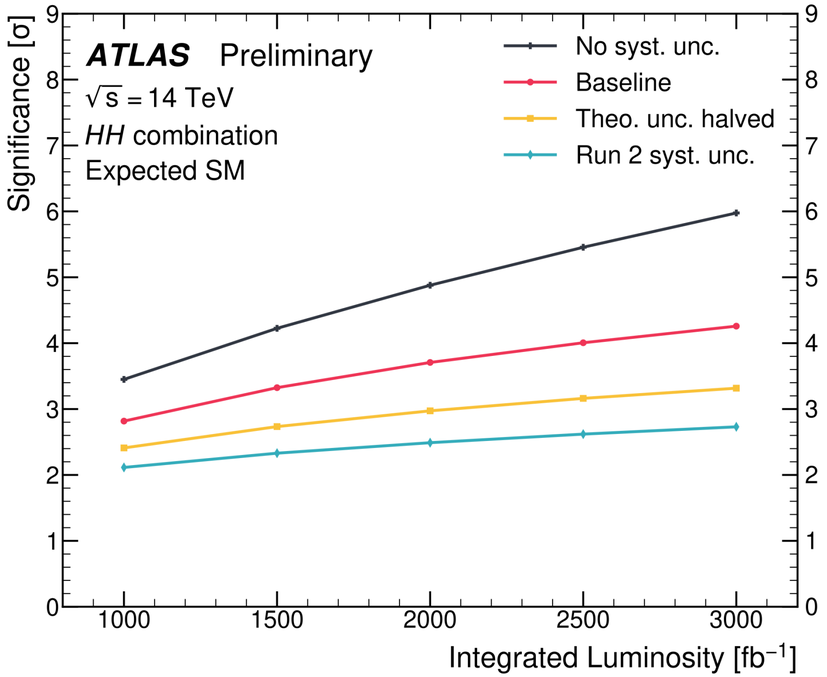


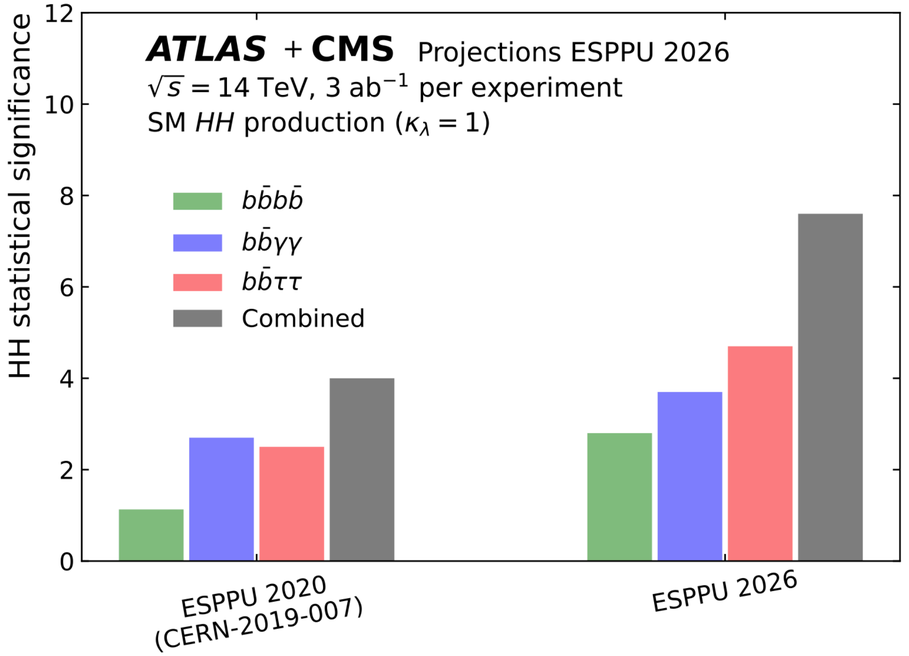
We are here

Introduction

- Ref: ATL-PHYS-PUB-2025-006, ATL-PHYS-PUB-2025-018
- Why higher luminosity? E.g observation of rare processes like di-Higgs production, together with CMS



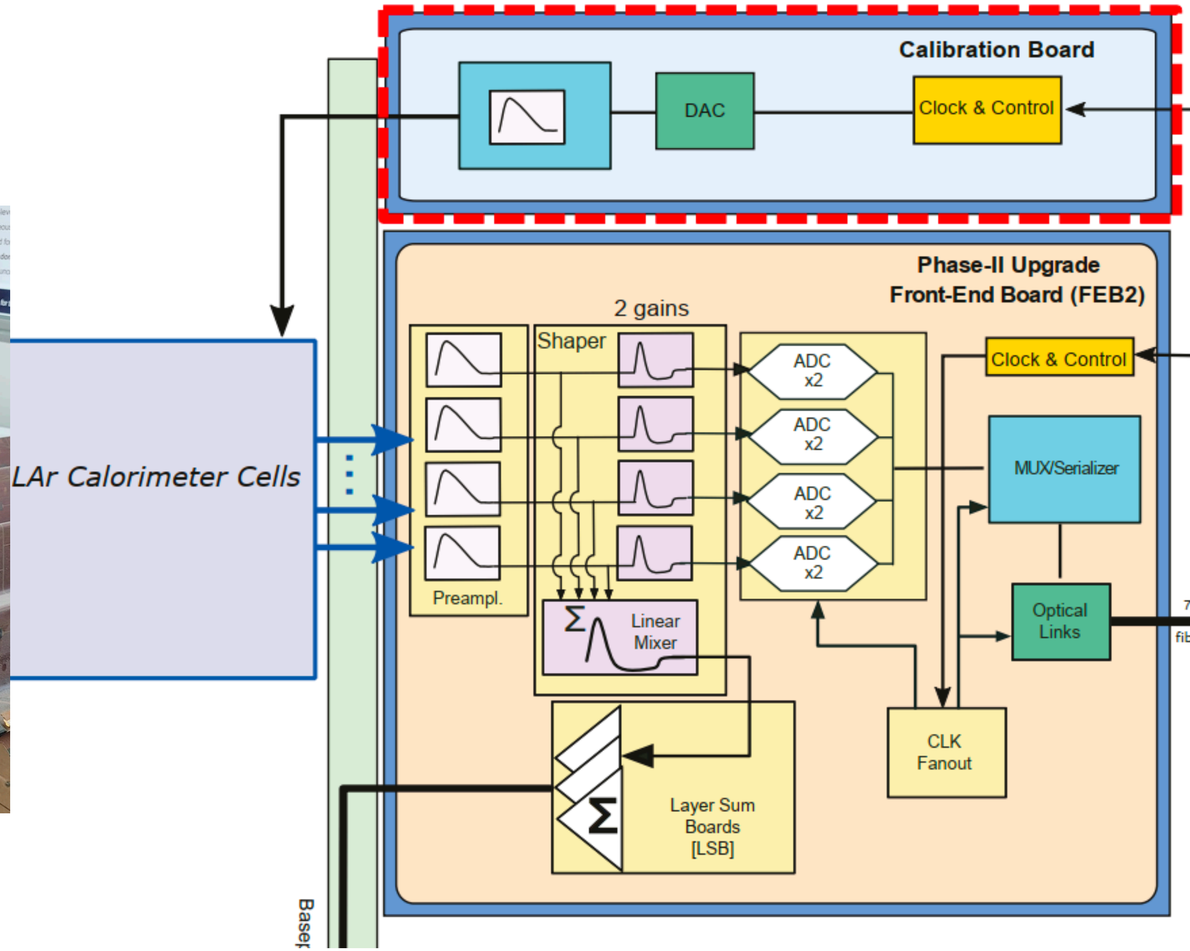


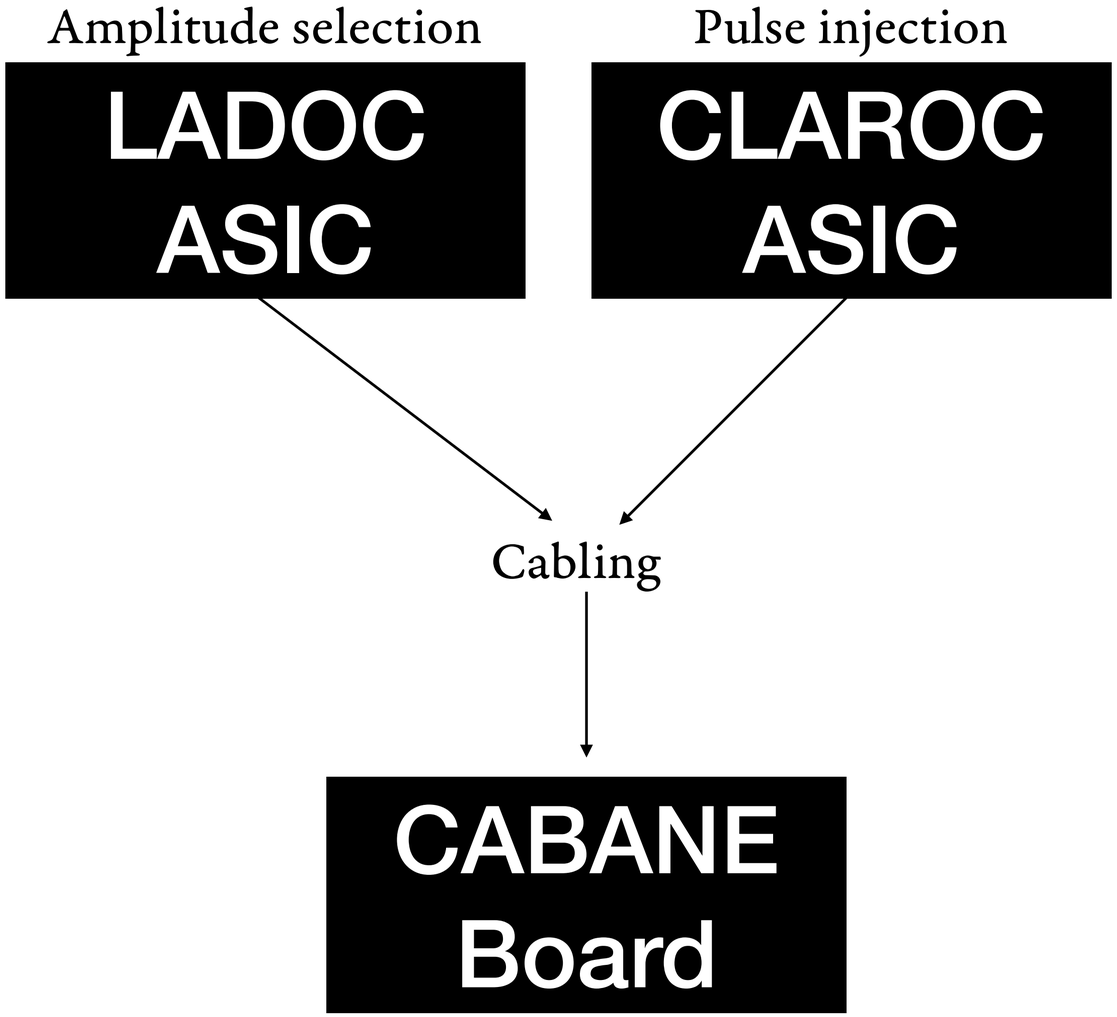


Overview

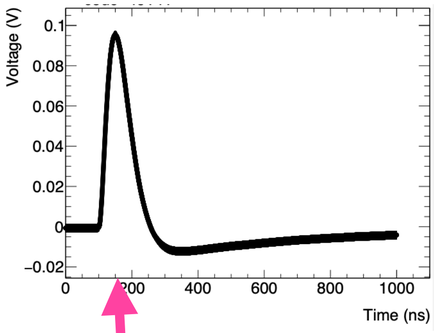
- Calibration boards (CB, CABANE) is part of LAr FE electronics
- CBs are used to inject accurately calibrated signals directly onto the calorimeter cells
- Electronics should provide very well-known pulses, similar in all channels
- Requirements on:
  - Linearity
  - Uniformity

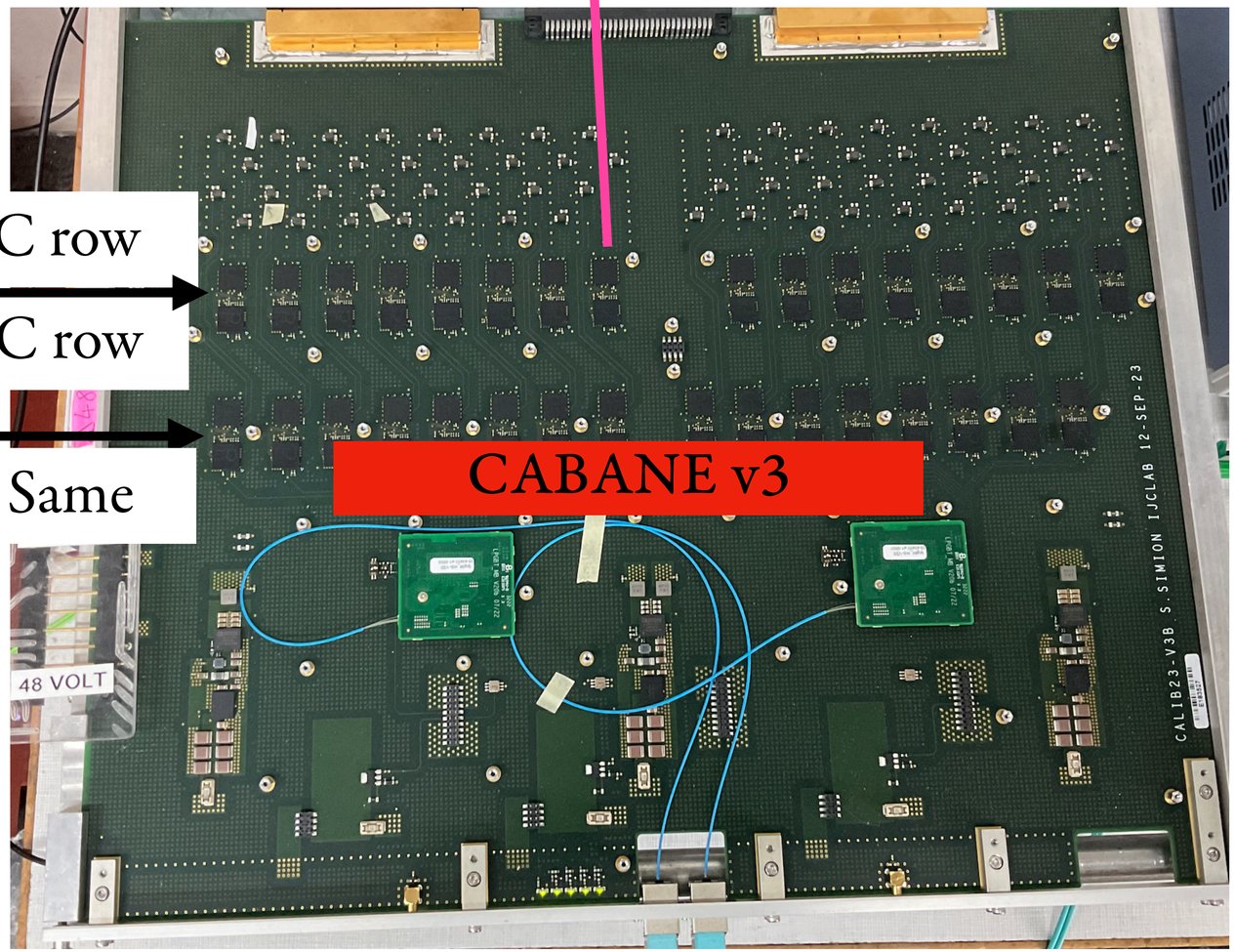




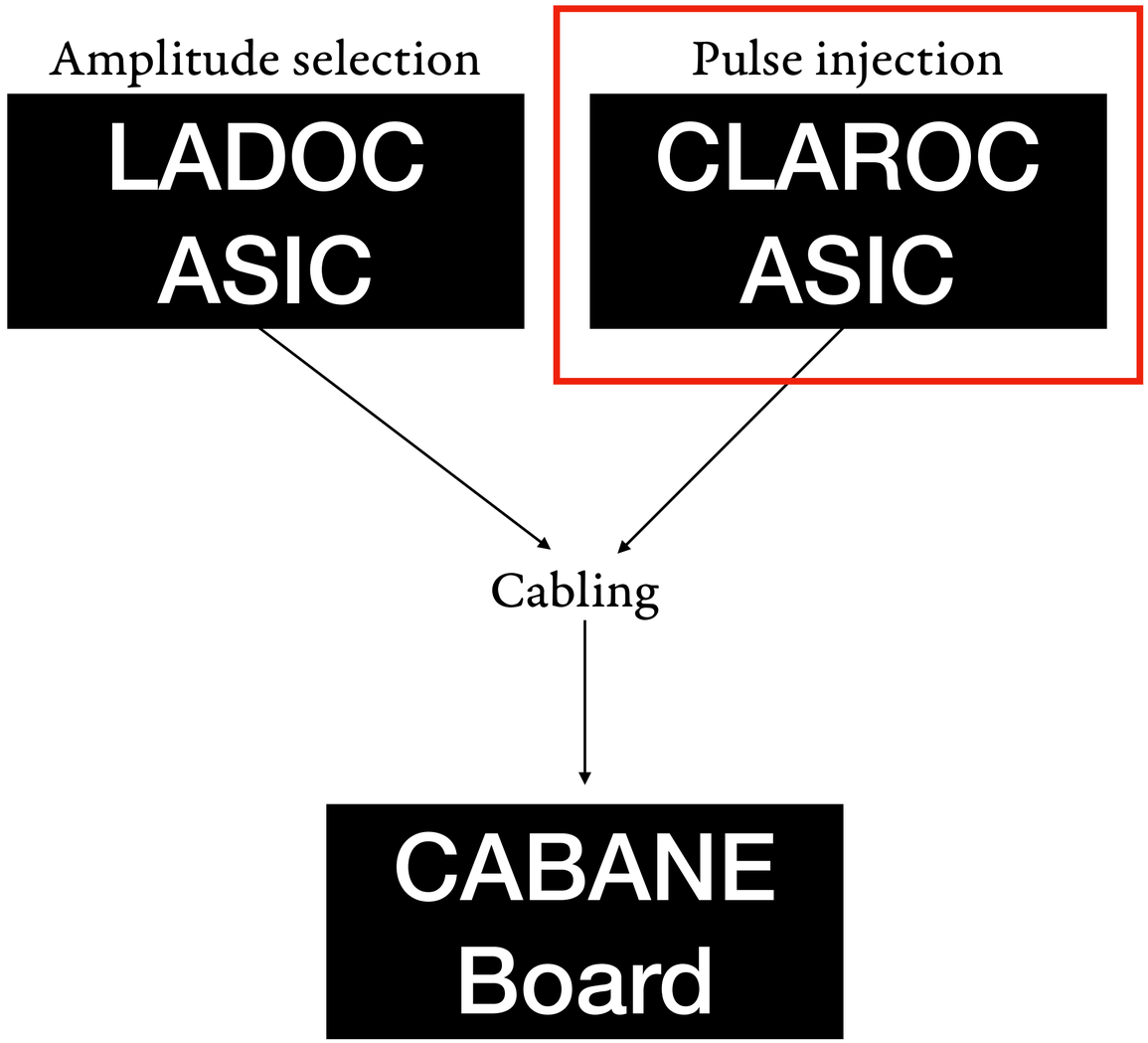

Amplitude selection
Pulse injection
LADOC ASIC
CLAROC ASIC
Cabling
CABANE Board

Overview



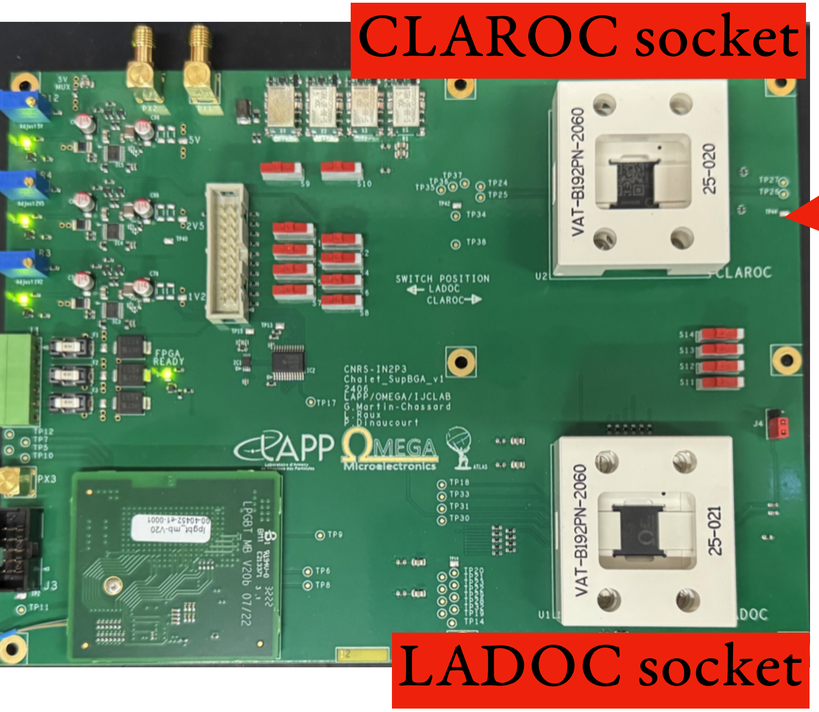


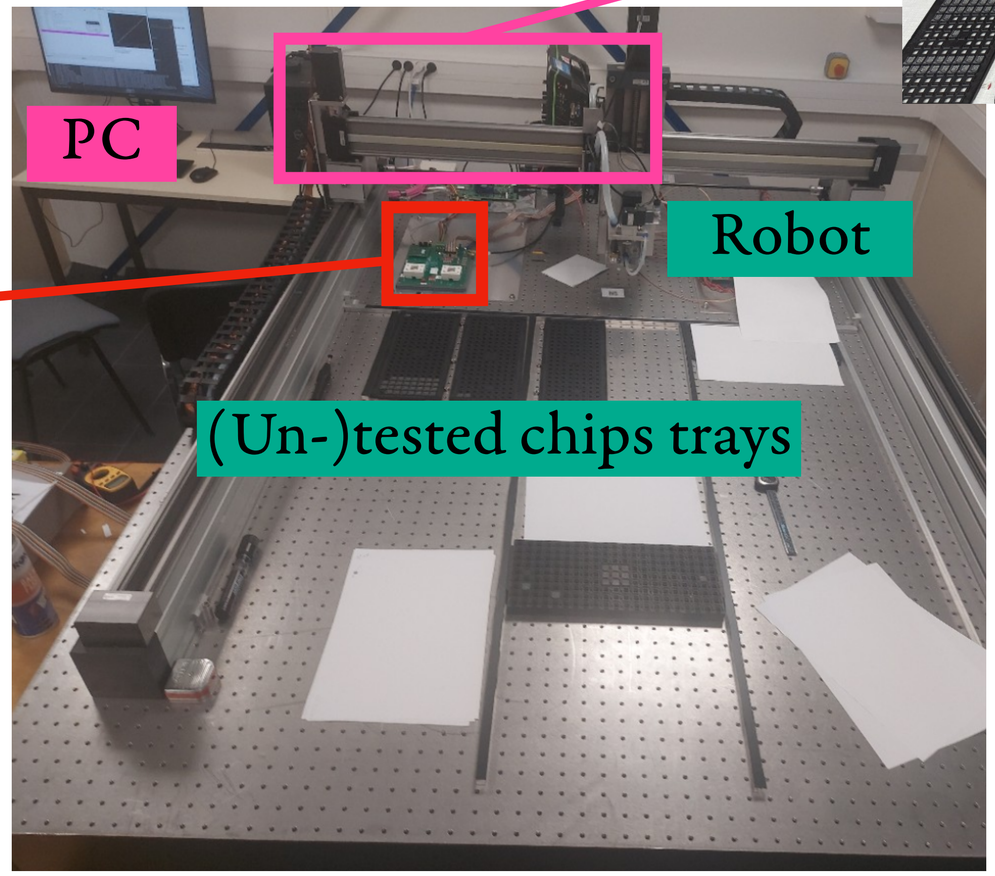
- Two chips, LADOC and CLAROC, designed by Omega (Palaiseau), are components of CB and undergo separate characterization
- CABANE Preliminary Design Review passed
- Both LADOC and CLAROC passed separate Production Readiness Revsiew

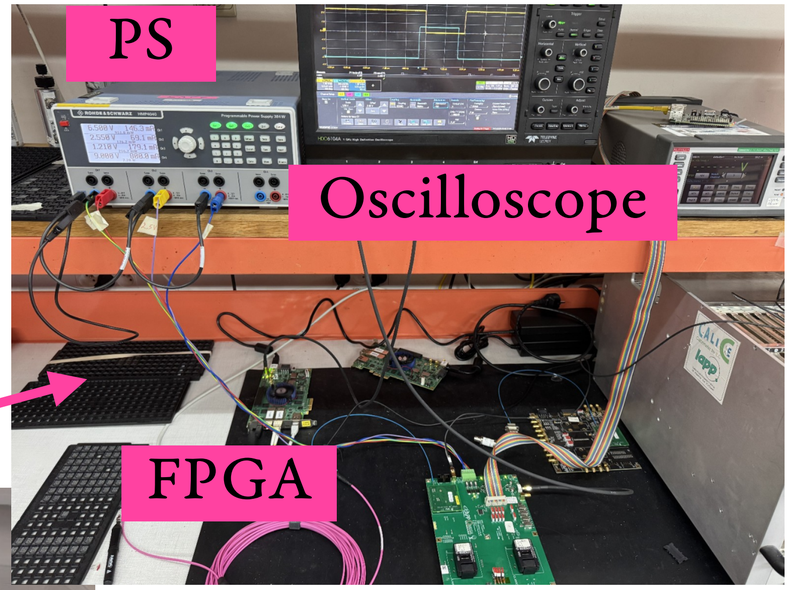

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Robotic test setup

- LADOC/CLAROC testbench is integrated with robot in IJClab Orsay
- All (5830) CLAROC chips tested



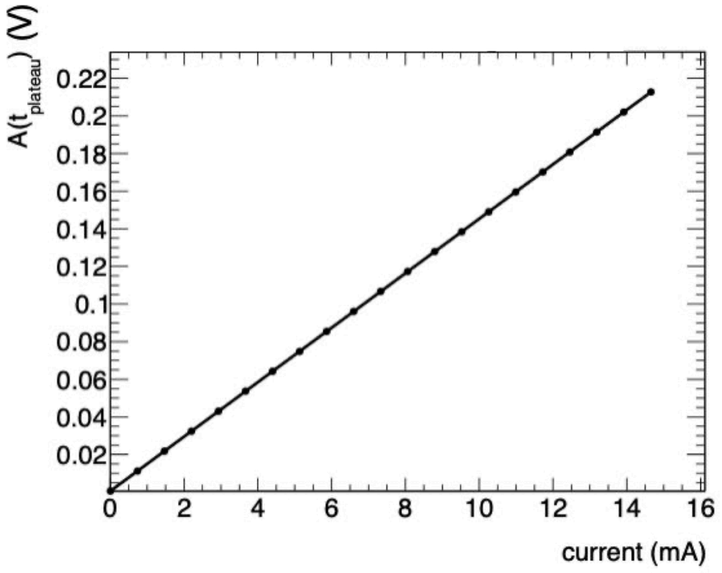


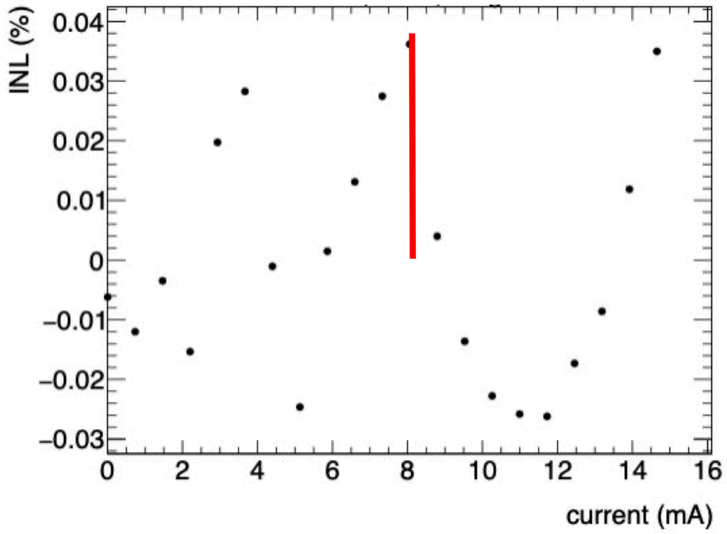


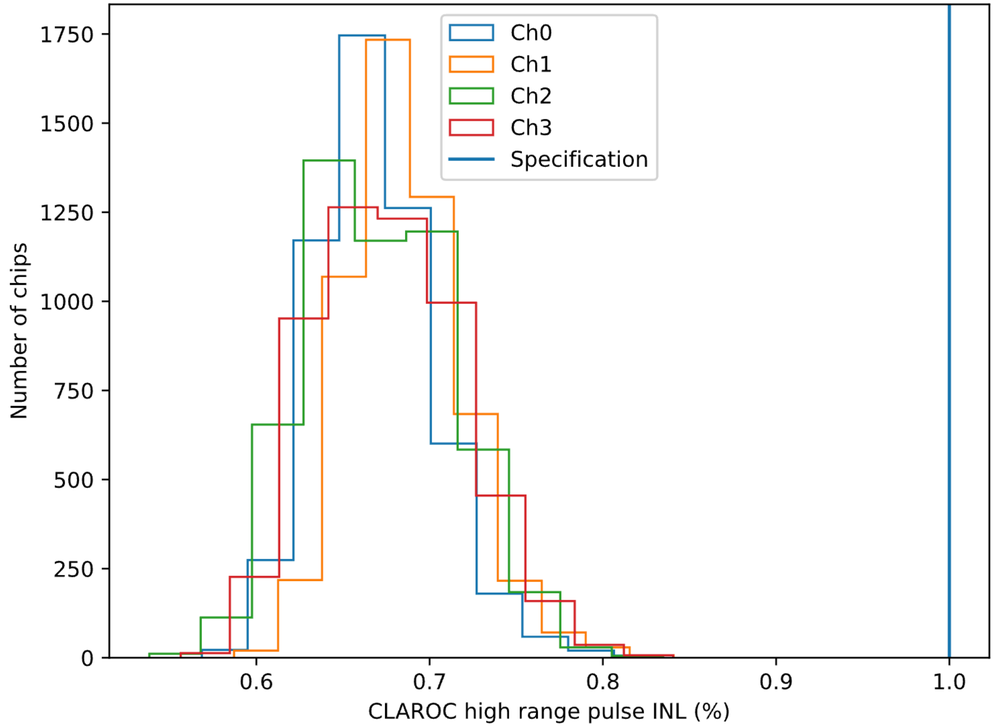
- For each chip first test if current consumption and reference voltages are fine - exit if not
- Then set certain DAC, record pulse with oscilloscope, repeat for other DAC - obtain data for linearity and uniformity tests

5830 chips - linearity w/o irradiation

- Want CLAROC output pulse amplitude to be linear vs input DAC
- Non-linearity quantified as normalized max residue from linear fit $INL_d = (I^d_{fit} - I^d_{meas})/I^r_{max}$
- Subject to specification: <0.1% for 0-15mA (low range) and <1% for 15-320mA (high range)
- 395 chips rejected

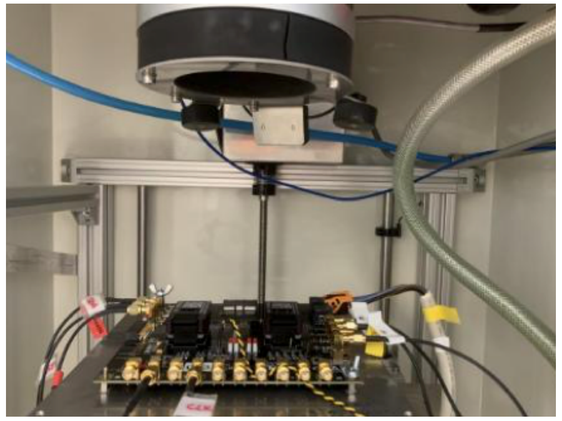


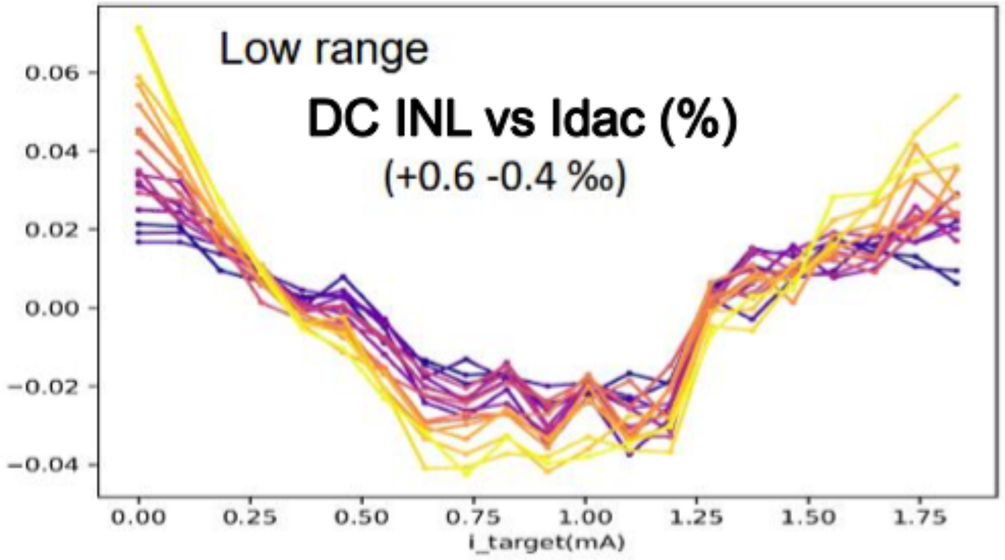




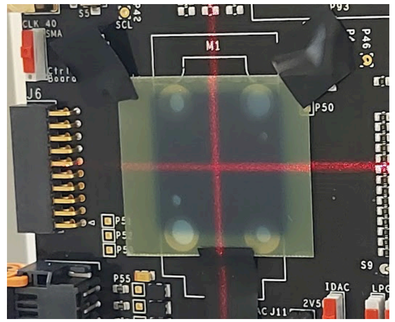
1 CLAROC chip - linearity w/ irradiation

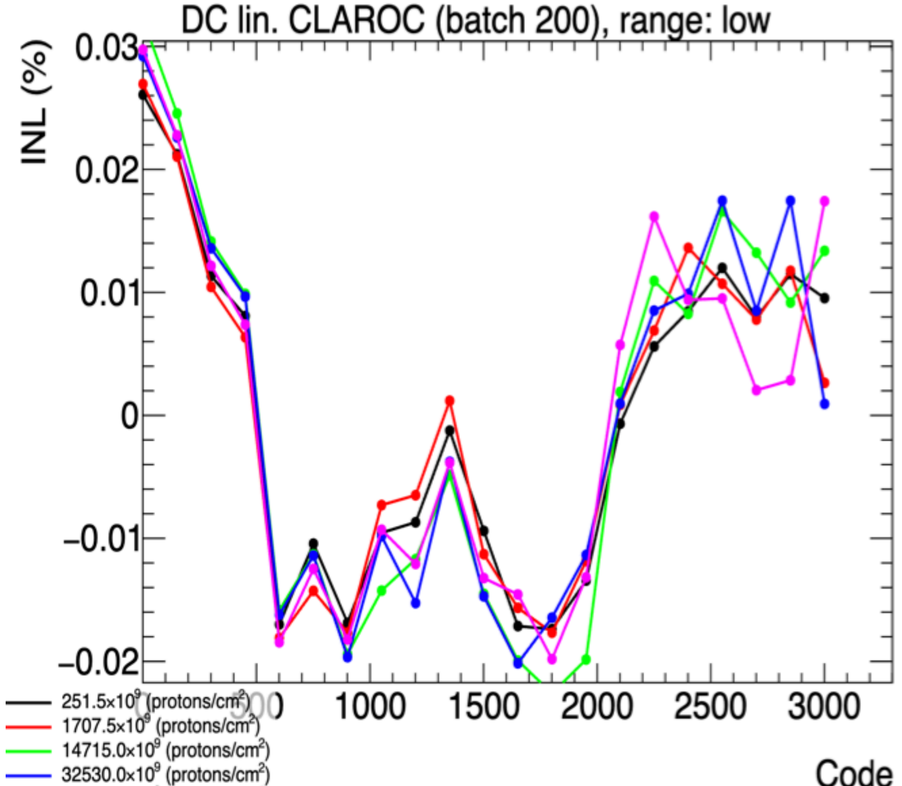
X-ray @ CERN irradiation until target 140krad → passed





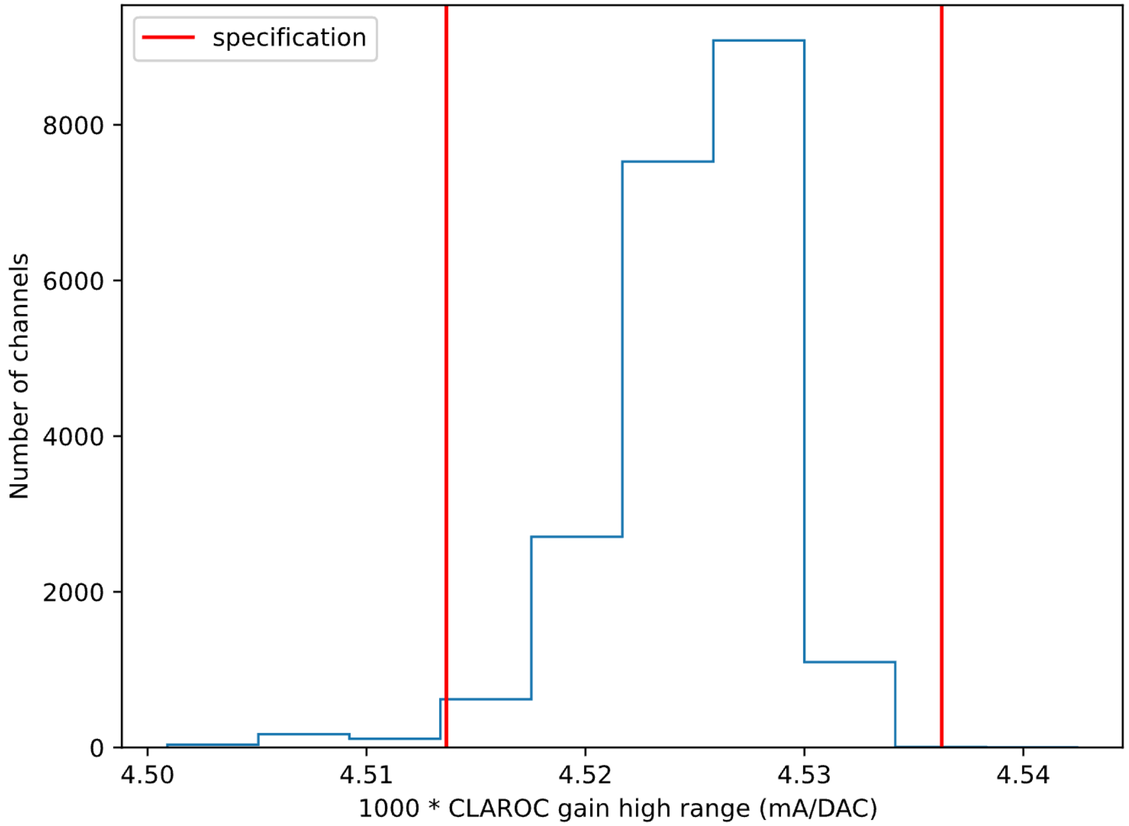
Protons @ Arronax(Nantes) irradiation until target $2.65 \times 10^{13} p/cm^2$ → passed

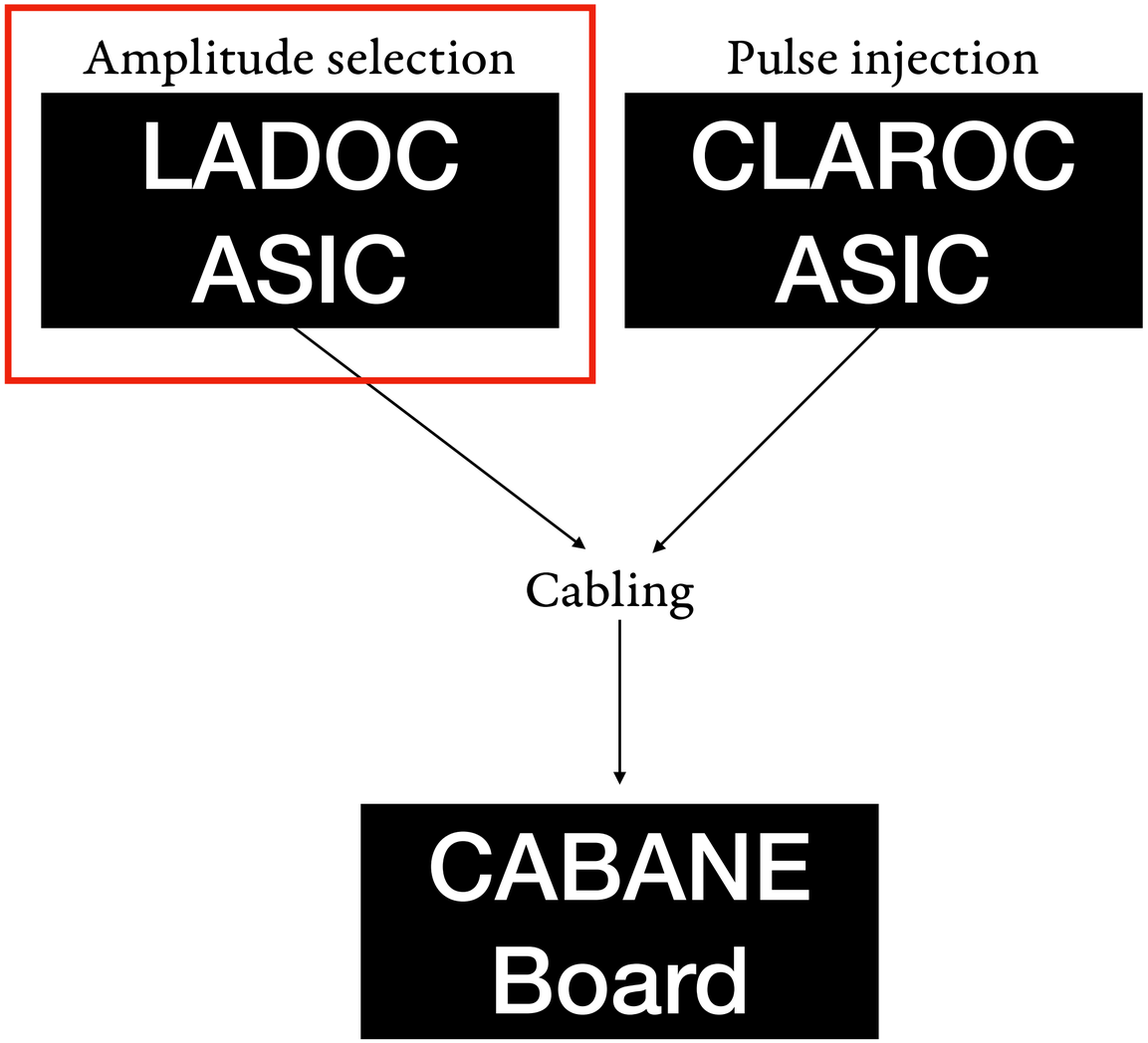




5830 chips - gain uniformity

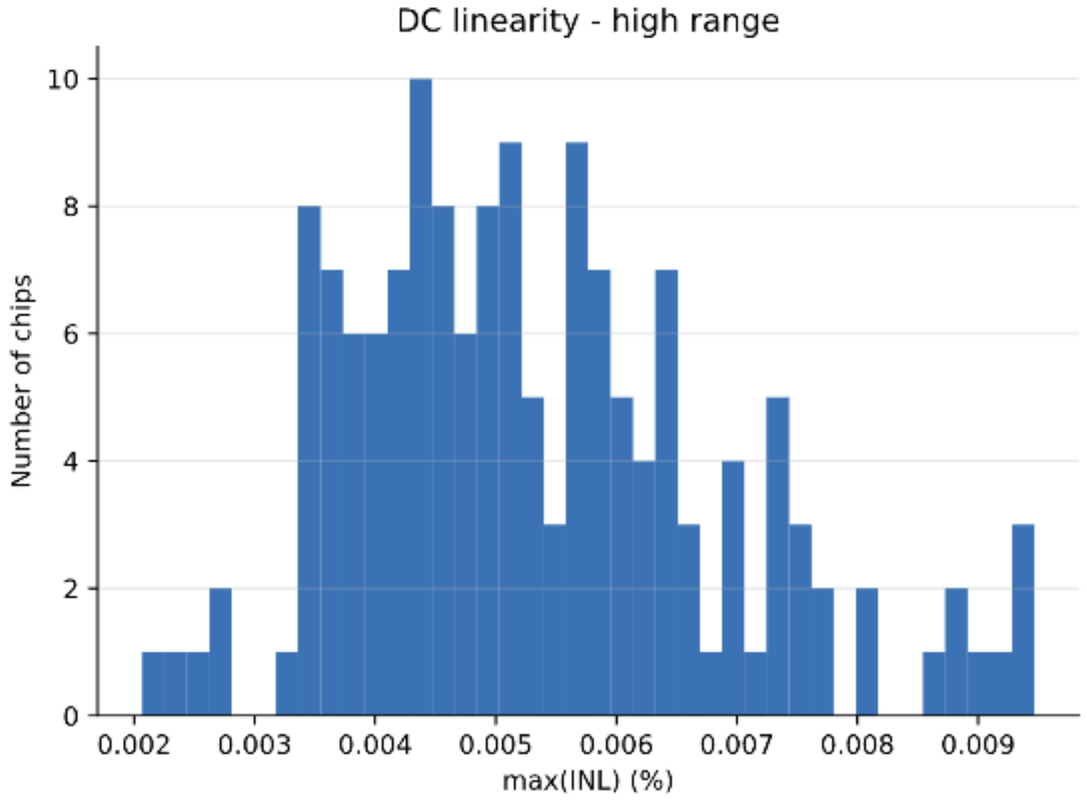
- Want all CLAROC chips (all channels of) used to have similar gain
- Quantified by deviation from mean, subject to specification: <0.25%
- 495 chips rejected

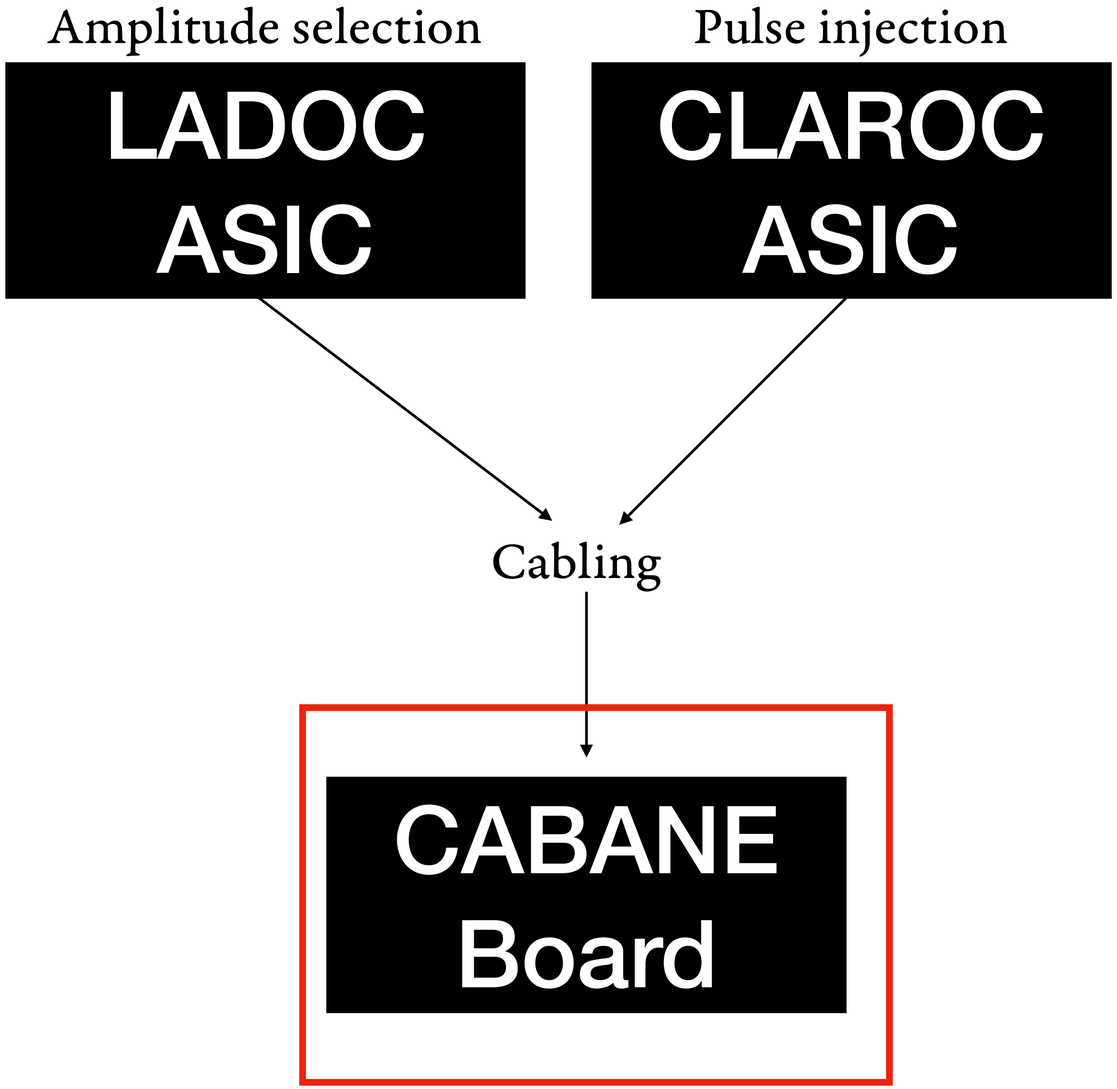



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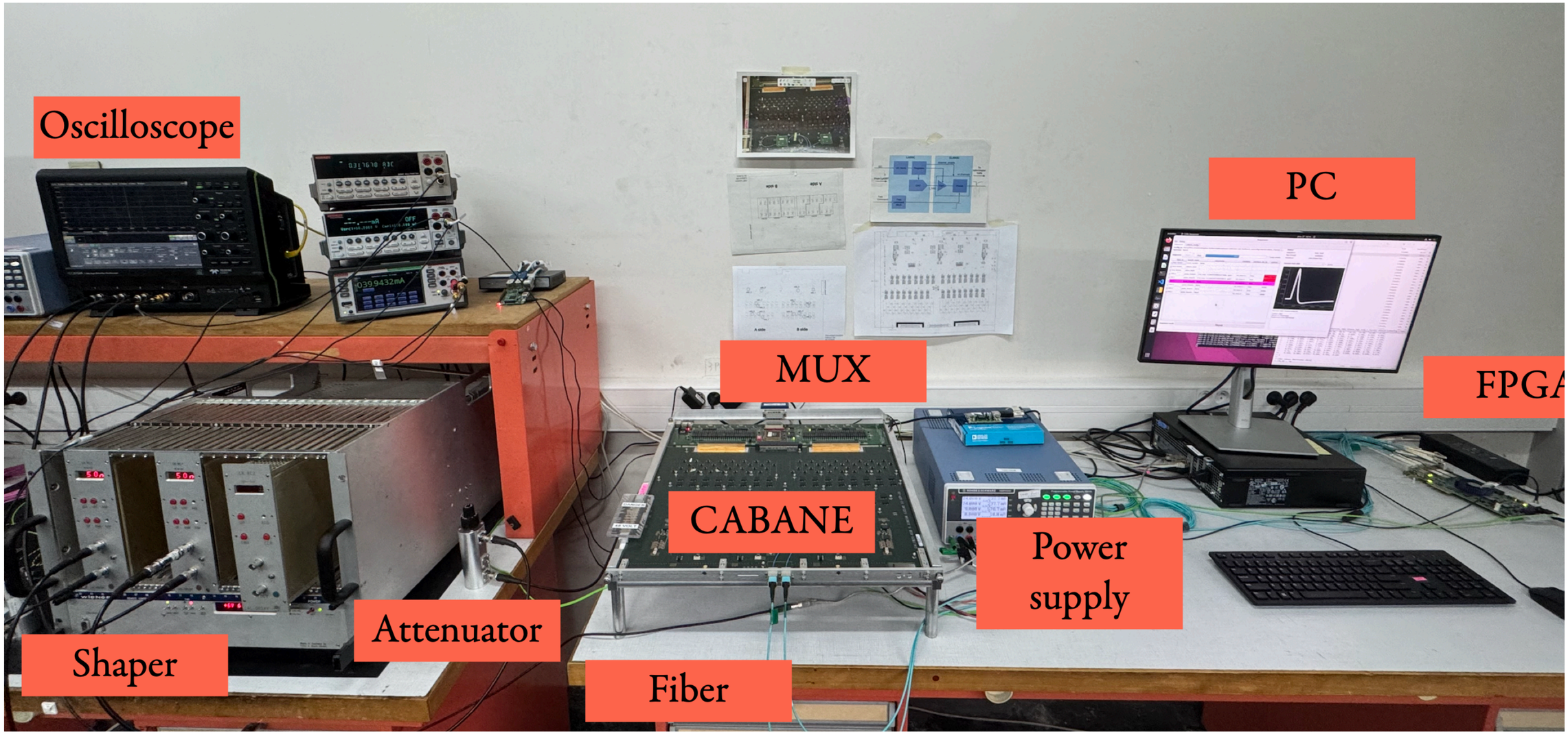
150 chips performance

- Also need to test ~6000 chips, thus far only 150 of them arrived
- A similar to CLAROC robotic setup is used
- No chips rejected due to non-linearity
- No anomalous behaviour in other tests
- 100% yield



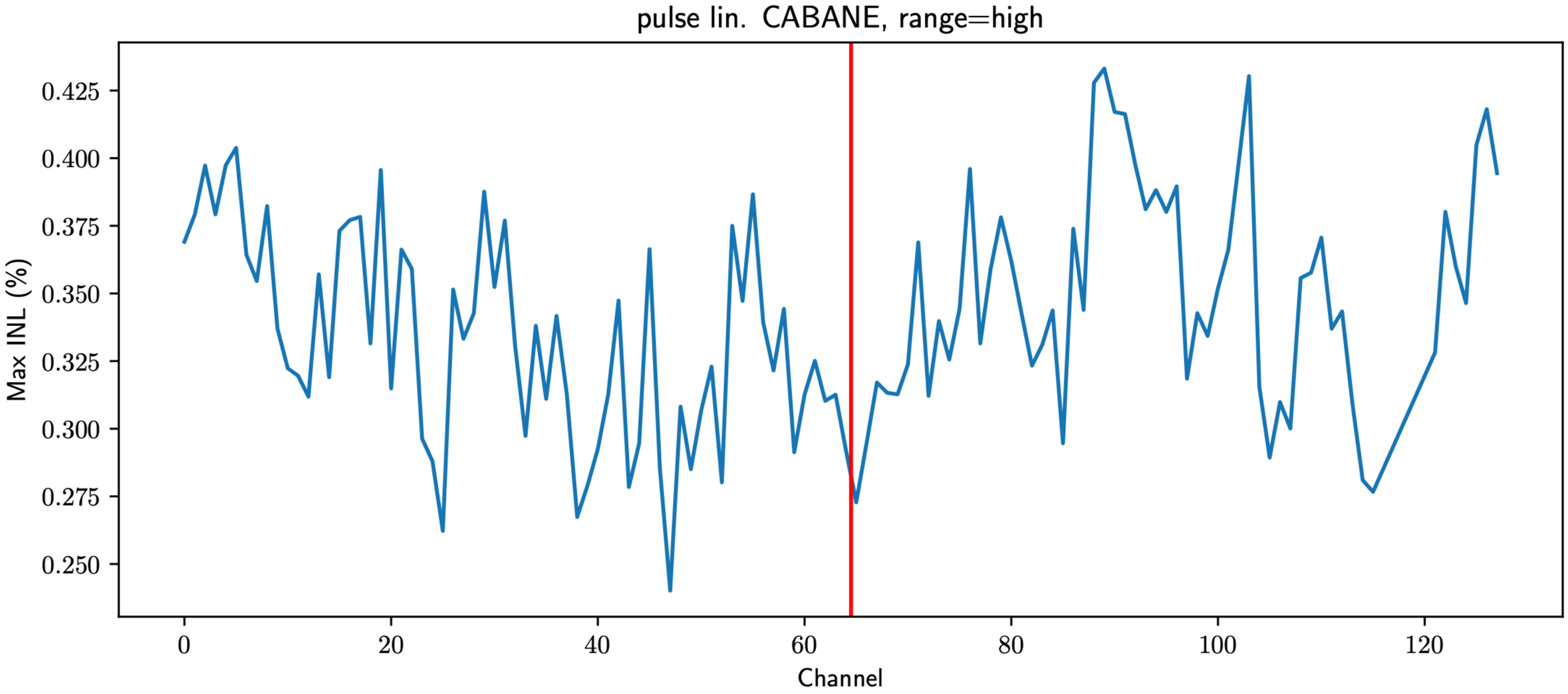

Amplitude selection
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Setup


Oscilloscope
PC
MUX
FPGA
CABANE
Power supply
Attenuator
Shaper
Fiber

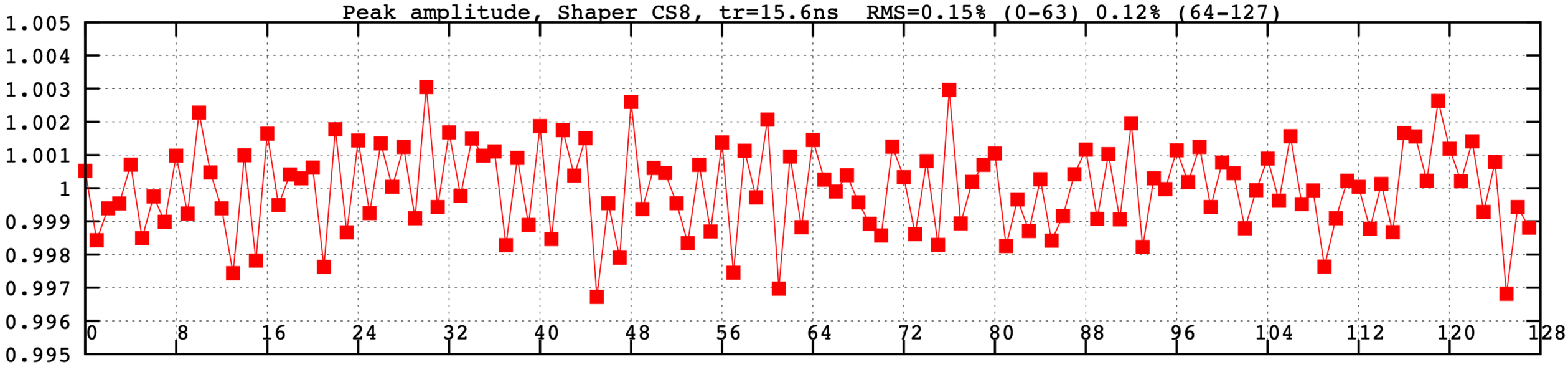
Performance - linearity

- Within specification



Performance - uniformity

- Not far from specification but result convoluted with MUX which needs to be replaced

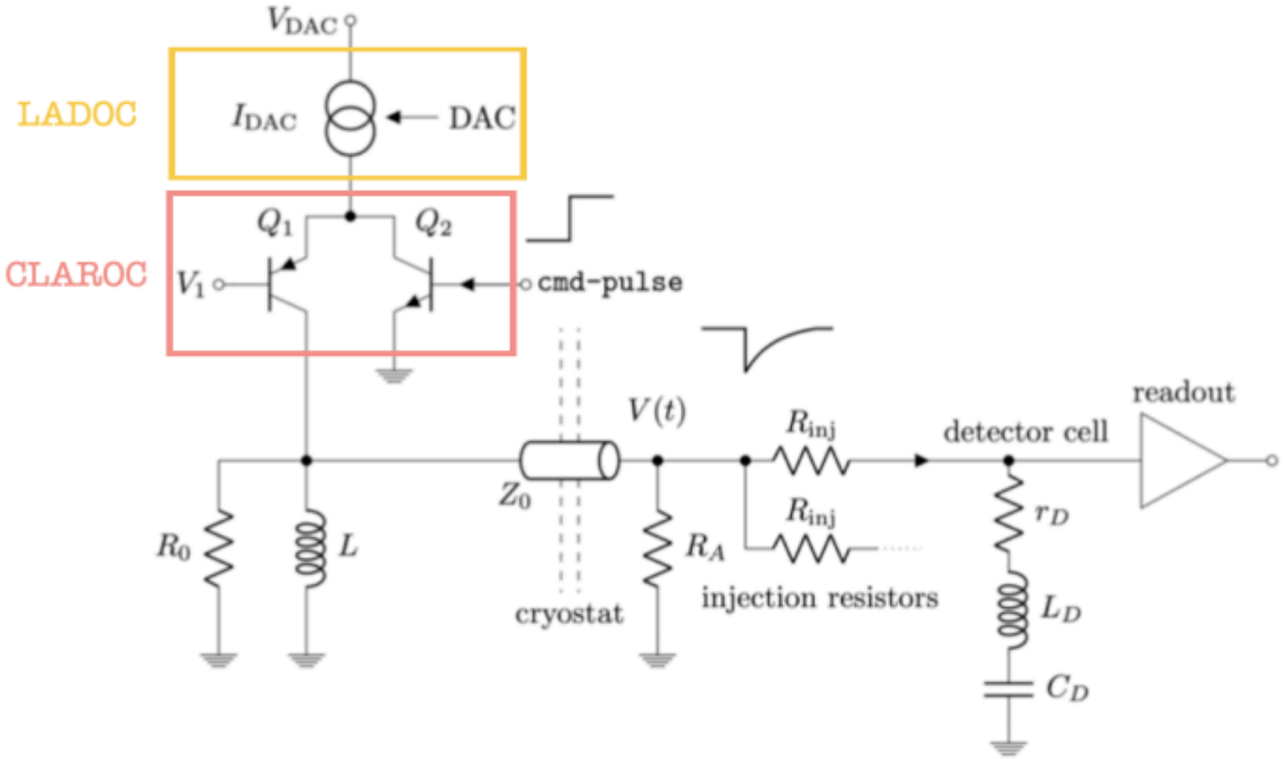


Summary

- Three components of Phase II LAr electronics, each tested separately
  - Two ASICs: CLAROC and LADOC
  - Board built from them
- All CLAROC chips tested - necessary for 150 boards number of chips satisfying project requirement
- 2.5% of LADOC chips tested (others being produced) - 100% yield
- Performance of boards equipped with previous version of chip satisfies requirement

The End

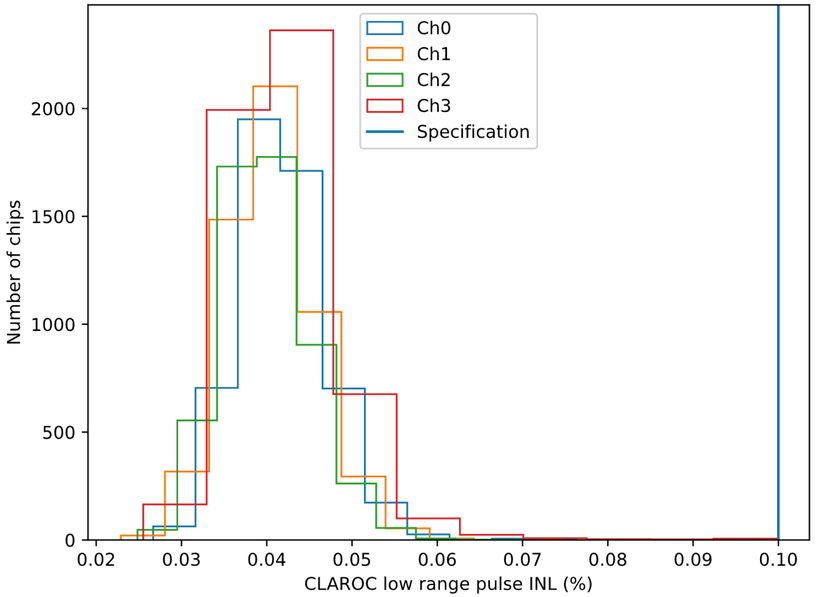
LADOC and CLAROC

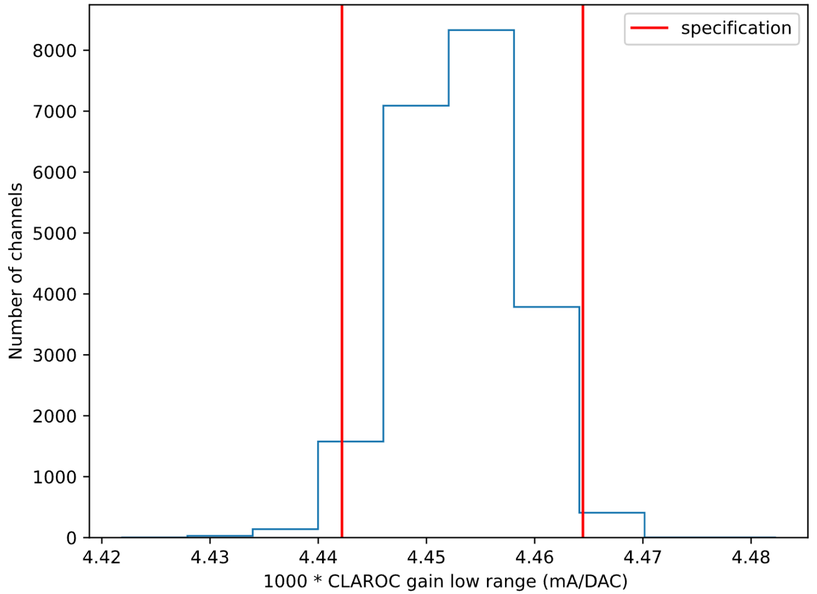


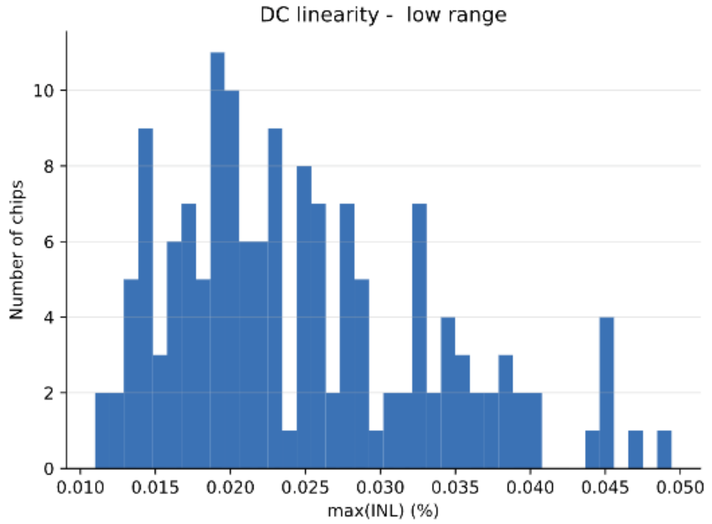
The pulse is generated by the opening of the high-frequency switch, constituted by the Q_1 and Q_2 transistors and commanded by the `cmd-pulse` signal, over the R_0 and L network. Two ASICs have been developed to provide these features:

- CLAROC (Calibration of Liquid ARgon Output Chip): this ASIC, developed in XFAB HV CMOS technology by Omega team, contains the two transistors Q_1 and Q_2, as well as mirror current to provide the full dynamic range up to 300 mA. It contains 4 identical channels
- LADOC (Link And DAC Of CLAROC): this ASIC has also been developed by Omega team in CMOS TSMC 130 nm technology. It contains a 13-bits (16-bits) DAC as well as the slow-control I2C architecture to communicate with CLAROC.

Low range plots - ASIC







Low range plots - board

