

# Calice - ILD activités au LPNHE Paris

Réunion Calice IN2P3 – Octobre 2011

Didier Lacour

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Etapas de l'année écoulée

Personnes impliquées

Activités en cours

Budget 2011 et demandes 2012

## Les étapes de l'année 2011

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Janvier : début de la prise de responsabilité

Février - Mai : prises de contact, étude des possibles contributions

*Décision d'une implication dans la calorimétrie électromagnétique Si-W*

24 mars réunion au LLR sur le collage

30 mai réunion au LLR sur la caractérisation des wafers

16 juin : rapport d'étape au conseil scientifique du LPNHE

21 septembre : présentation à la biennale du LPNHE

*Octobre : intégration « officielle » dans la collaboration Calice ?*

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## Personnes impliquées

Jacques David : ingénieur d'étude - électronicien

Patrick Ghislain : assistant ingénieur - mécanicien

Didier Imbault : ingénieur de recherche - mécanicien

Laurence Lavergne : ingénieur de recherche – instrumentation

Jean-Eudes Augustin : directeur de recherche émérite

Didier Lacour : directeur de recherche (aussi sur ATLAS)

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### Organisation locale:

Une réunion hebdomadaire ouverte aux chefs des services électronique et mécanique  
(D. Vincent, P. Nayman)

Assurance qualité « légère »

Liste d'action, minutes, définition des priorités, suivi des activités

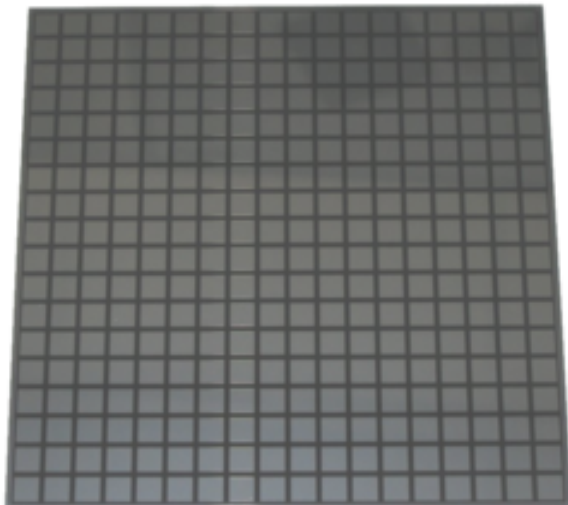
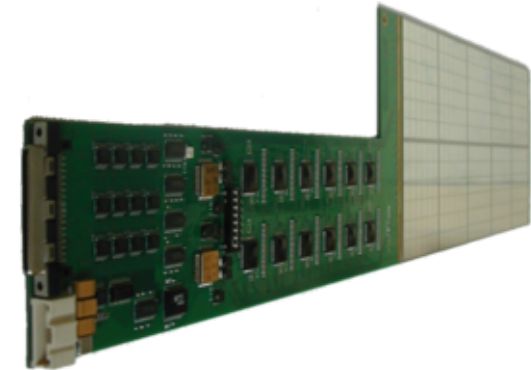
## Activities : focused on the silicon sensors part

An active layer is placed on each side of the layer of the tungsten absorber.

**Active layer:** a chain of identical Active Sensors Units (ASUs).

**ASU:** a Printed Circuit Board (PCB) integrating the silicon sensors, Front-End electronics and electrical infrastructure.

**Sensors:** based on high resistivity silicon ( $5\text{K}\Omega\cdot\text{cm}$ ) and single-sided process, with individual pin-diodes of  $5 \times 5 \text{ mm}^2$ ,



LPNHE group involvements:

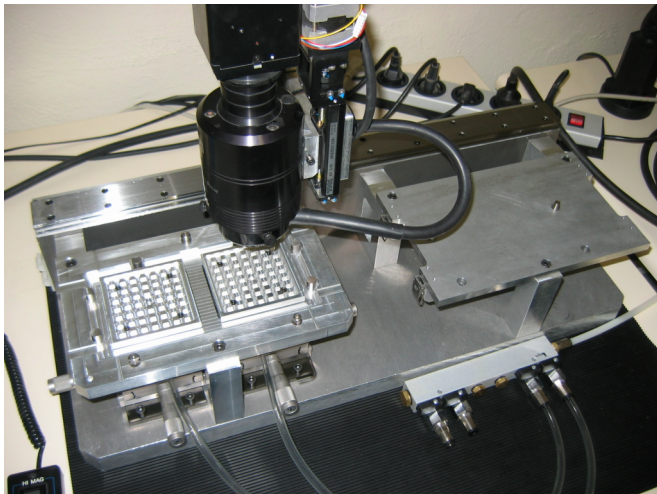
The gluing of the Si sensors onto the PCB using a controlled technique

The characterisation of the wafers  
Leakage current and capacitance versus voltage

Relationship with the Silicon manufacturers

$5 \times 5 \text{ mm}^2$  pad Hamamatsu sensor,  $18 \times 18 \text{ cm}^2$

## Gluing of the sensors onto the PCB



A part of the system: positioning system and gluing machine

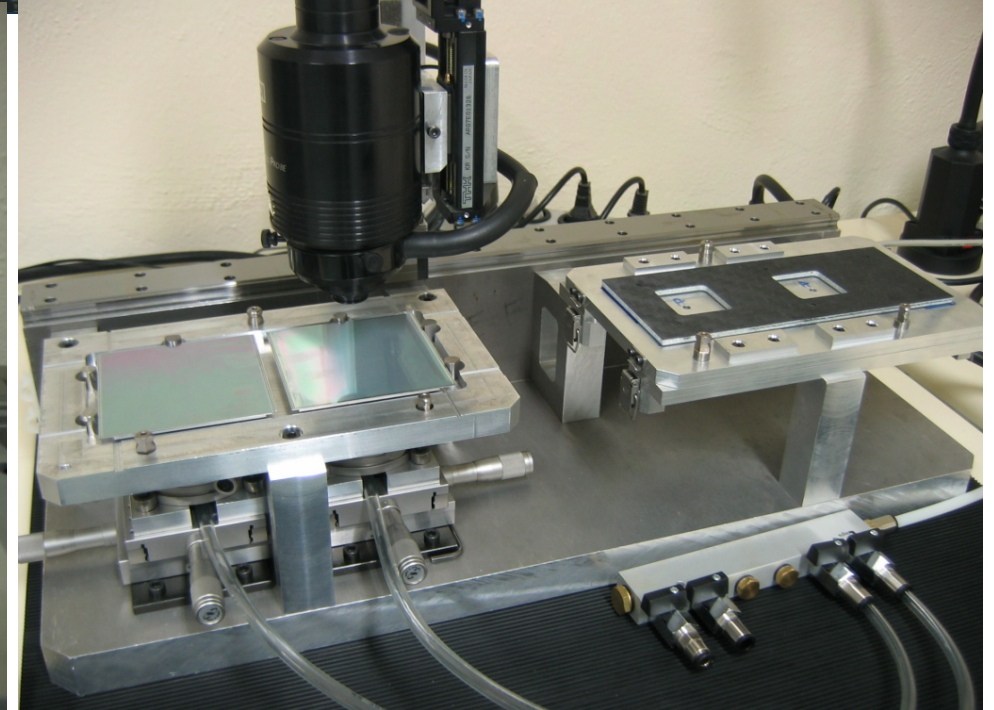
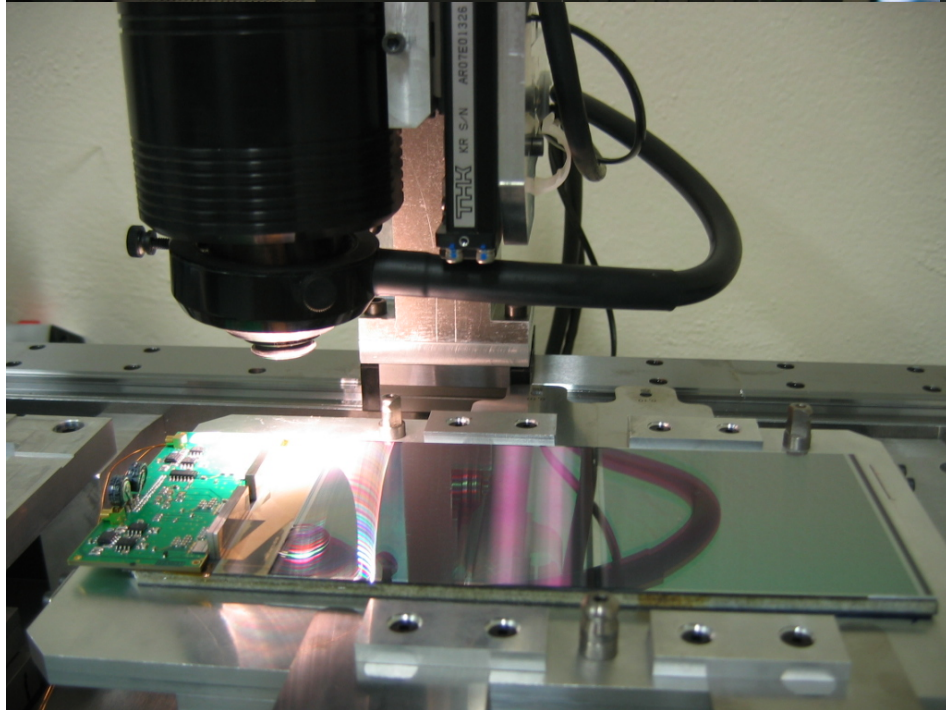
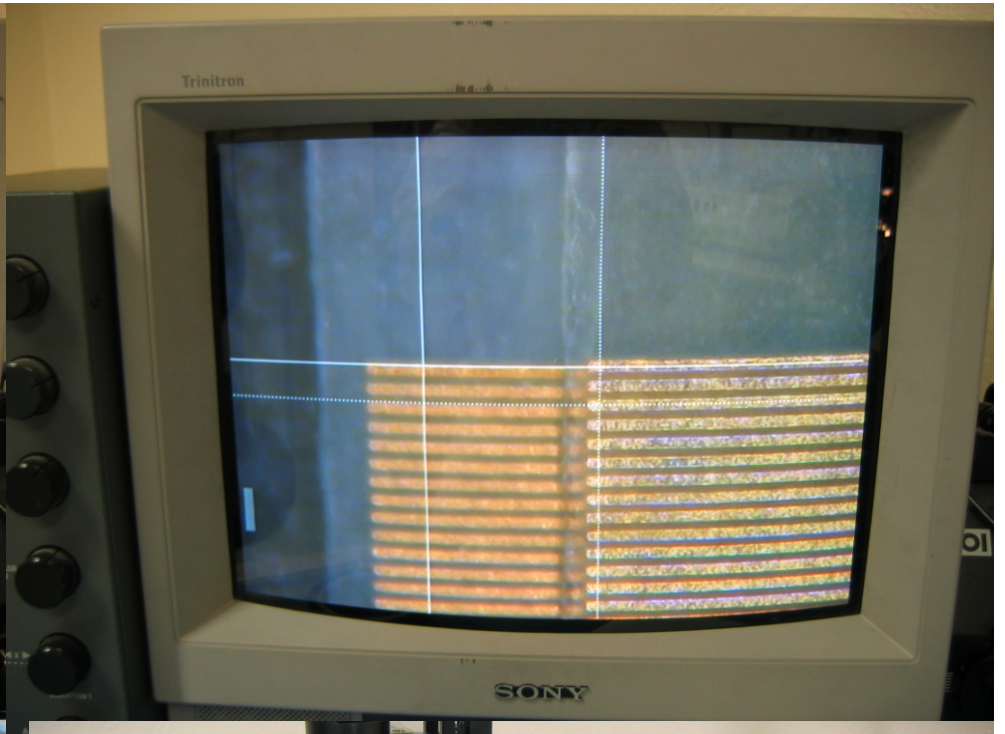
A well controlled gluing technique:

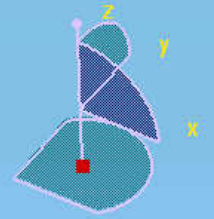
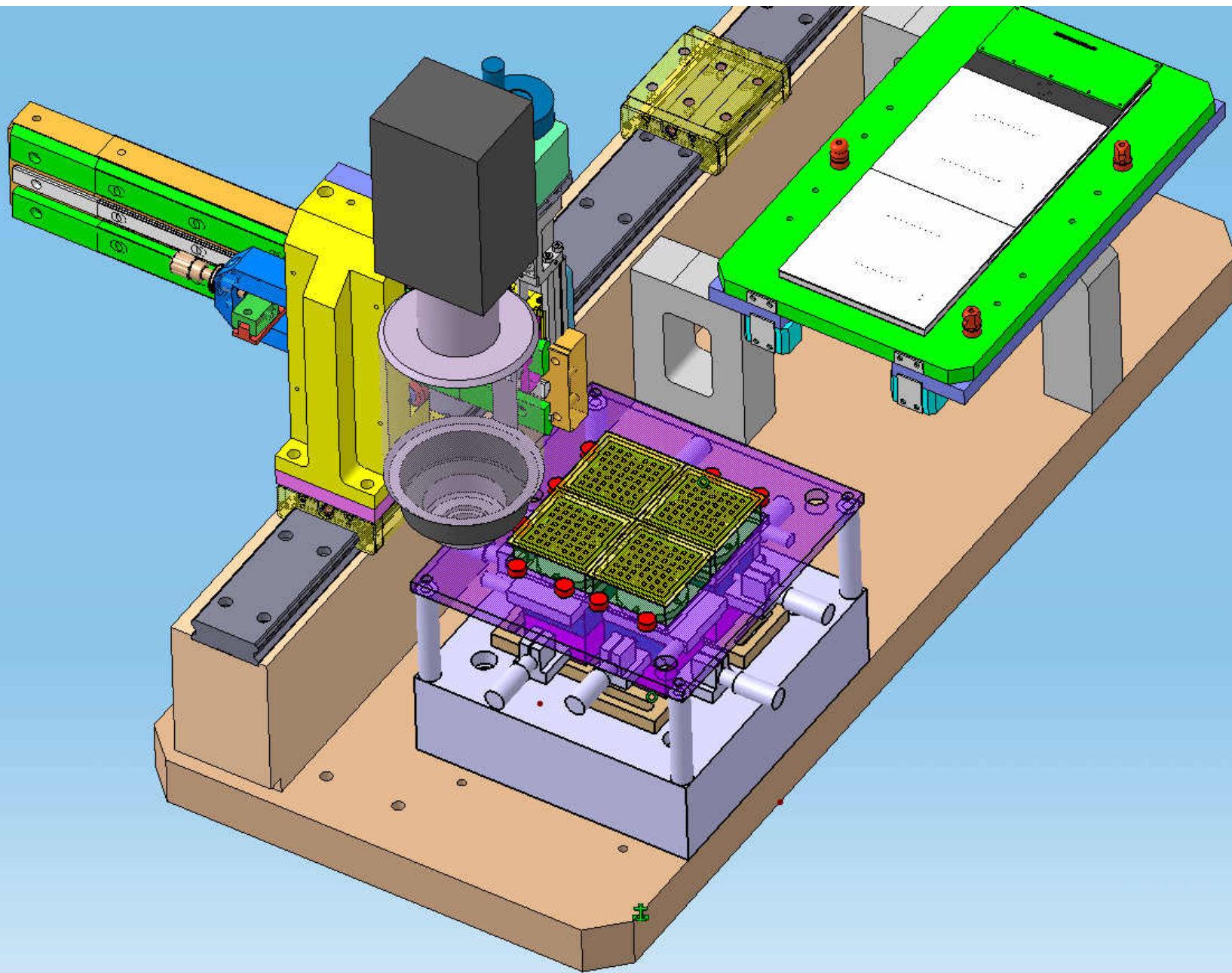
Standard conductive glue (EPOTEK 410) is applied by a robotic gluing machine. Several tests are in progress, using the robot we have.

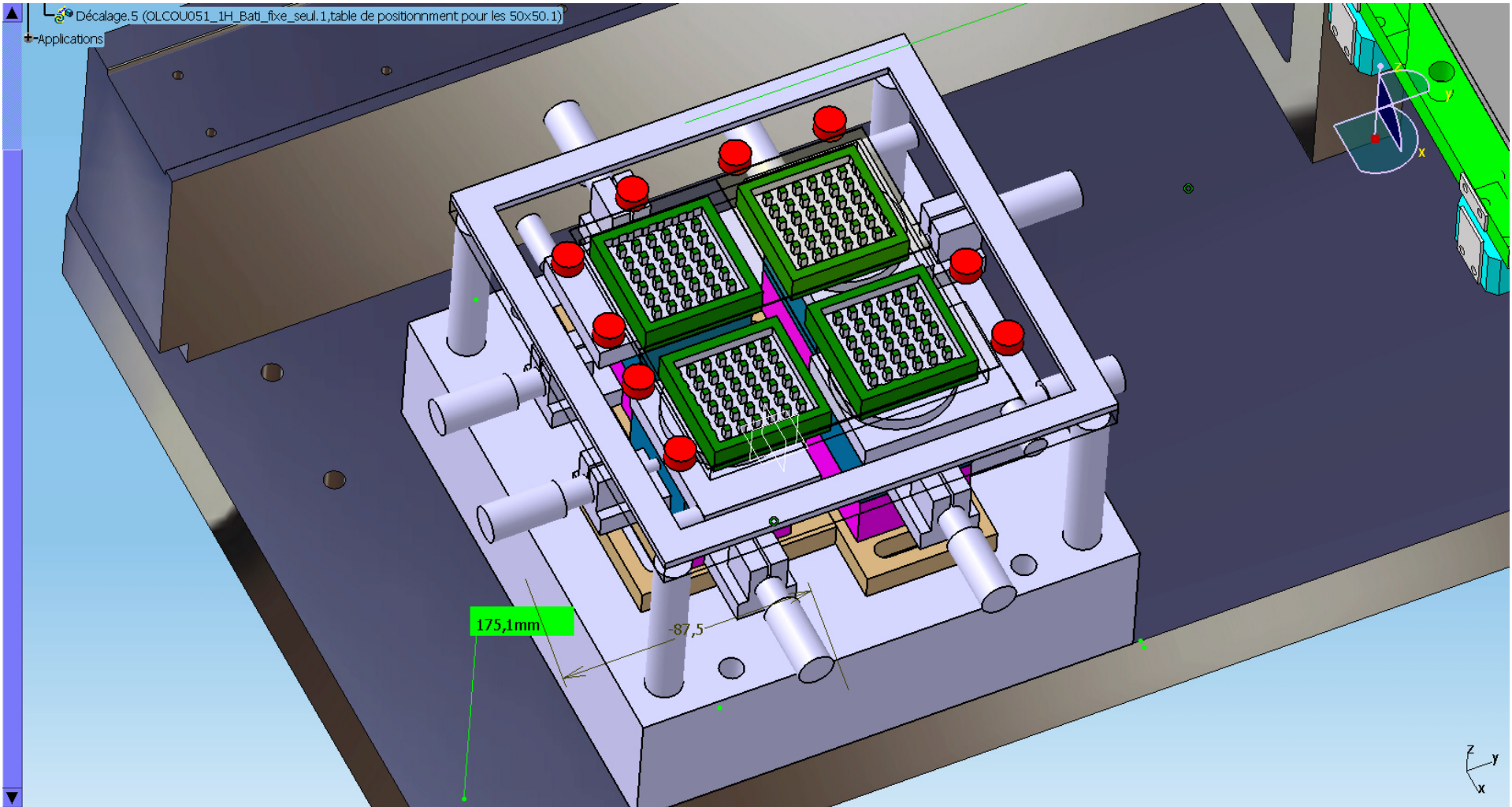
Tests of the glue are performed in the standard room.

The gluing will be done in a clean room (ISO8). Some new equipment will be necessary and should be bought.

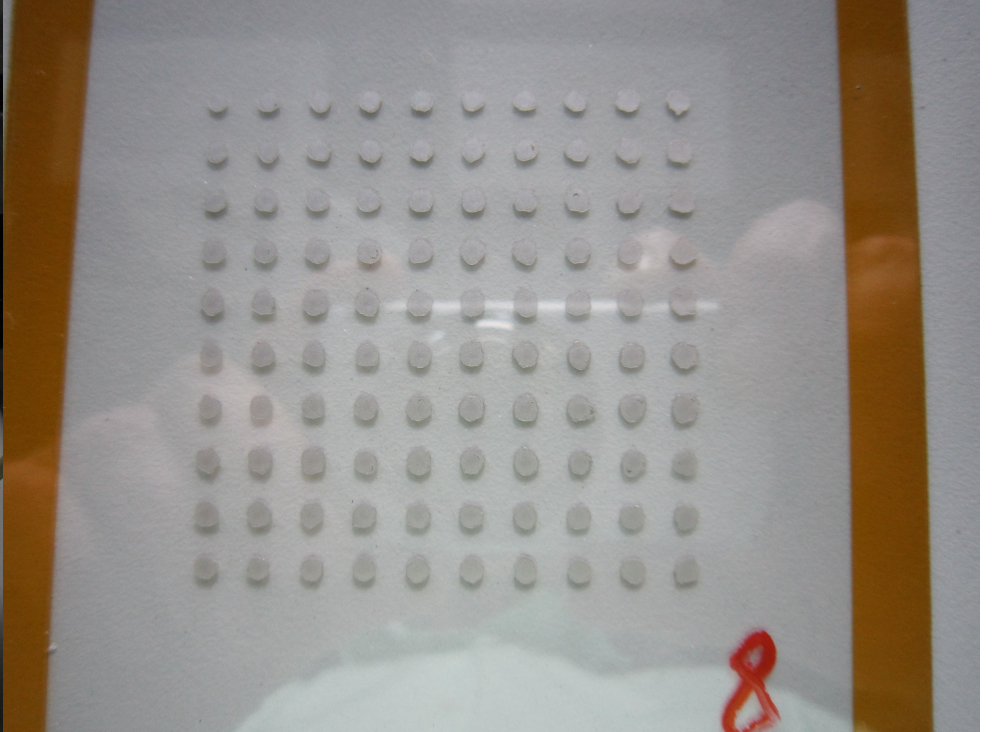
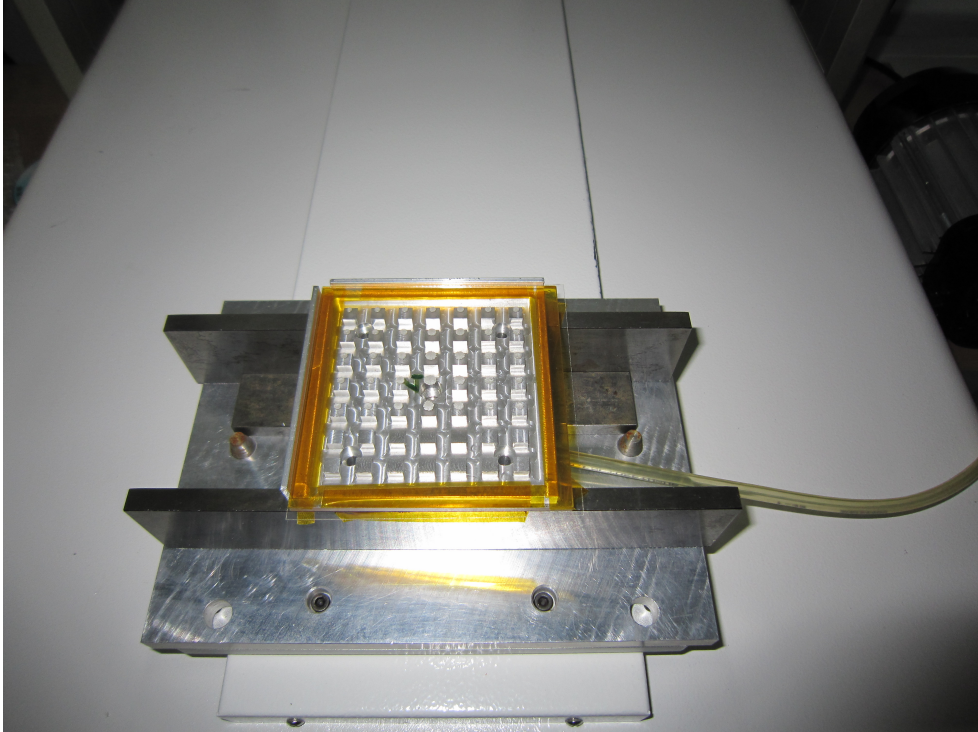
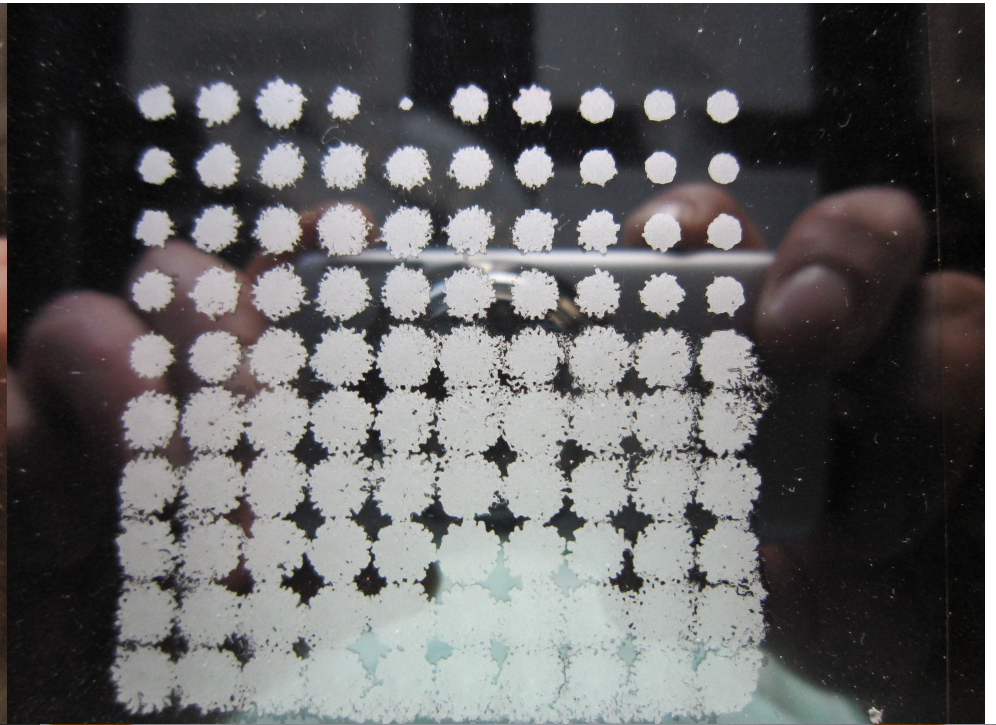
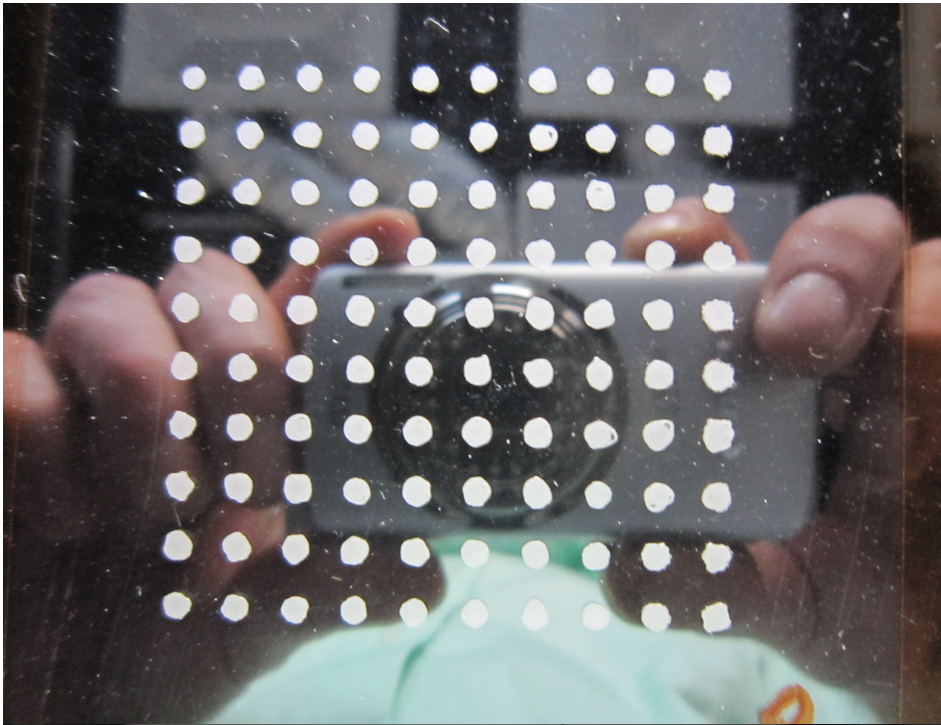
The process should be adaptable to the series (2500 m<sup>2</sup> of wafers).



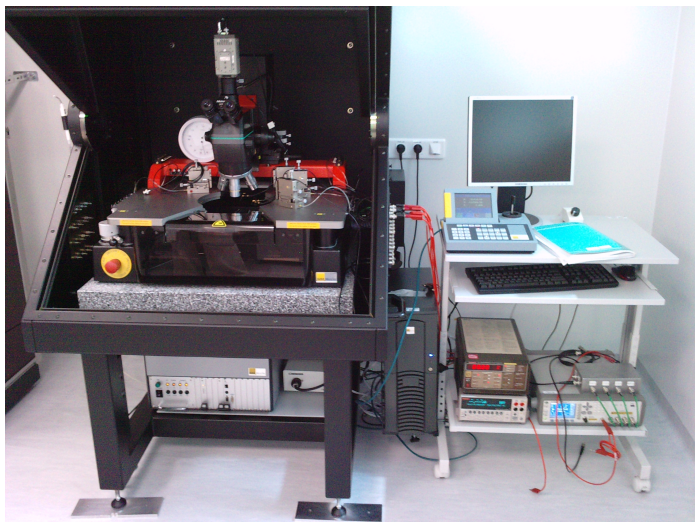








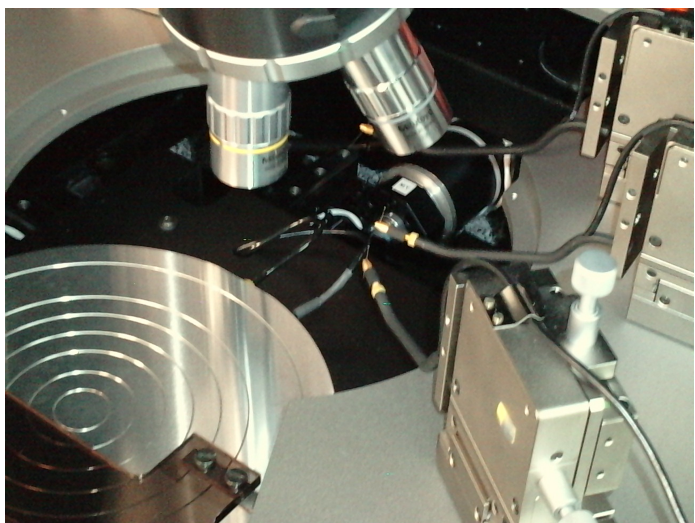
## Wafers characterisation



Some electrical tests on the sensors during the R&D phase and for the series production

Using the probe system of the lab PA200 and the expertise of the sLHC group:

A fully equipped probe system (chuck stage, microscope, probe-head) in a clean room (ISO7)



Measurements:

Leakage current, typical  $I(V)$  response curves;  
Overall capacitance of the sensor and individual pads,  $C(V)$ ;

Depletion voltage;

Guard rings behaviour: coupling capacitance, remaining potentials

## Budget 2011 et demande 2012

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Budget 2011: 14 000 Euros

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Demande 2012:

Robot cartésien comprenant un ensemble RoboCylinder IA, 1 Kit de communication PC ref RCM-101-USB, un ensemble de contrôle

Coût total = 22 500 Euros

Missions, déplacements et petits matériels = 12 500 Euros

- Calice collaboration meetings - ILD meetings - SiW working group meetings
- Colle, petits outillages mécaniques, petits appareillages électroniques

Total de la demande 2012 = 35 000 Euros

## Conclusion

SiW Electromagnetic calorimeter for the ILD detector:  
main ILC activity at IN2P3 and in the labs of « Ile de France »

Two topics in Paris, focused on the silicon sensors:

-Mechanics:

gluing of the sensors onto the PCB with a controlled technique;  
expertise of D. Imbault, experience of P. Ghislain

*1 stage de deux mois, DUT/BTS mesures physiques (janvier - février)*

- Electronics:

Characterisation tests of the wafers;  
under the responsibility of J. David, expertise of L. Lavergne

*- Un IE en informatique pour automatiser des bancs de tests (0.2 FTE)*

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These activities:

- ✓ meet needs of Calice collaboration
- ✓ use the infrastructures and experiences of the lab
- ✓ develop the local competences
- ✓ develop the relationships with the Silicon manufacturers