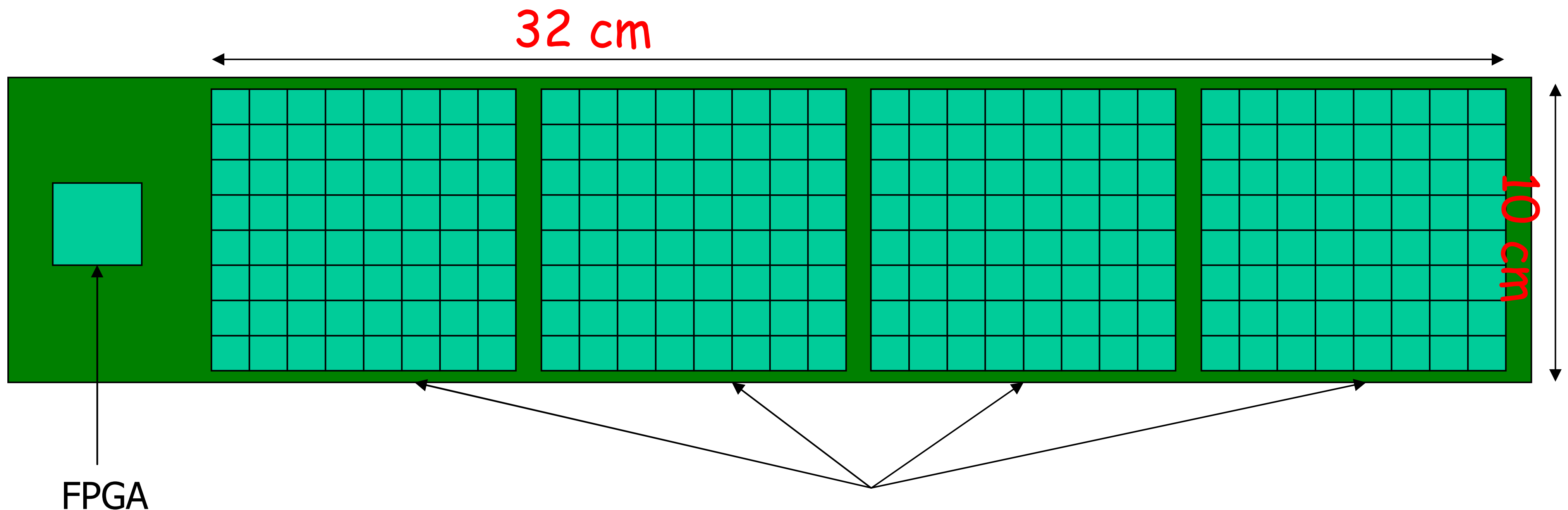
DHCAL PCB STUDY for RPC and MicroMegas

William TROMEUR, Hervé MATHEZ, Renaud GAGLIONE, Imad LAKTINEH
(CNRS IN2P3 IPNL)
Collaboration with LLR and LAL

LAYOUT DESIGN

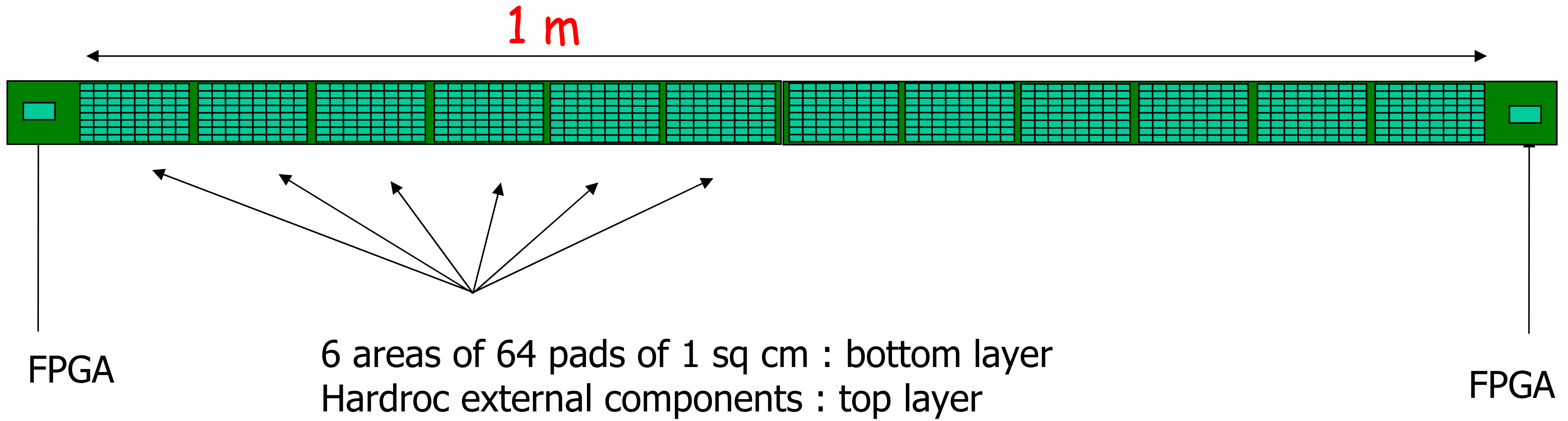
Design RPC PCB front end board prototype

- 4x64 1 sq cm pads
- 4 Hardroc Asics chained
- 1 FPGA to concentrate and send data using USB

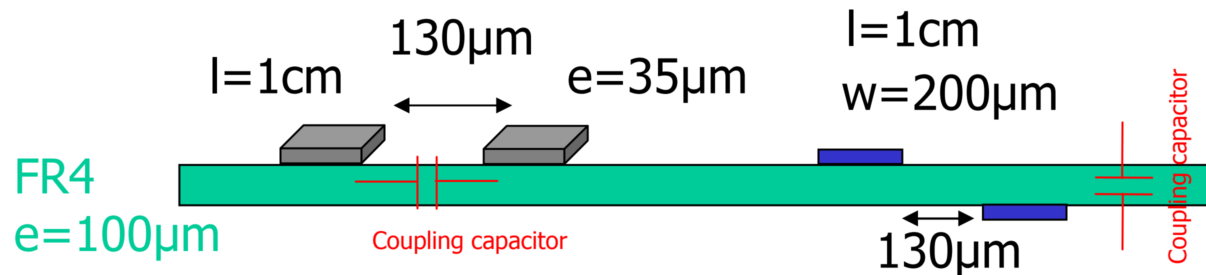


4 areas of 64 pads of 1 sq cm : bottom layer
Hardroc external components : top layer

LAYOUT DESIGN



Cross-talk



Cross-talk depends on coupling capacitor values

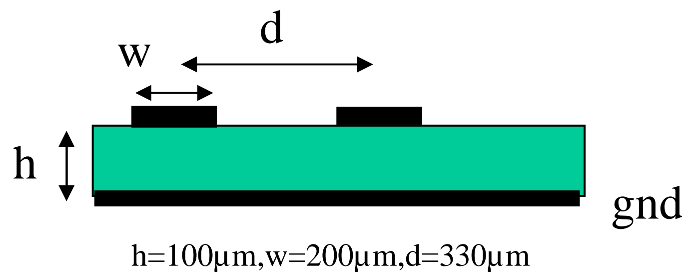
C=Er*E0*S/e   Er (FR4)=4.5   C=800fF/cm abacus gives 1 pF/cm for 2 path face to face

C is less than 1pF/cm in all other cases

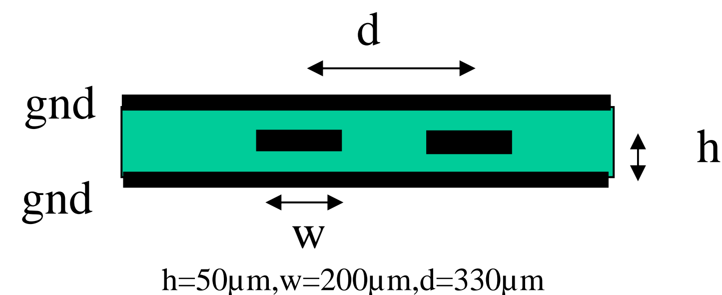
Er (glue between 2 level of PCB)=4.5 C=100fF/cm first approximation

But the real calculation is more complicated (with abacus C = 500fF/cm)

Cross-talk increase as C increase and depends on PCB achitecture



C = 150 fF/cm



C = 50 fF/cm

LAYOUT DESIGN

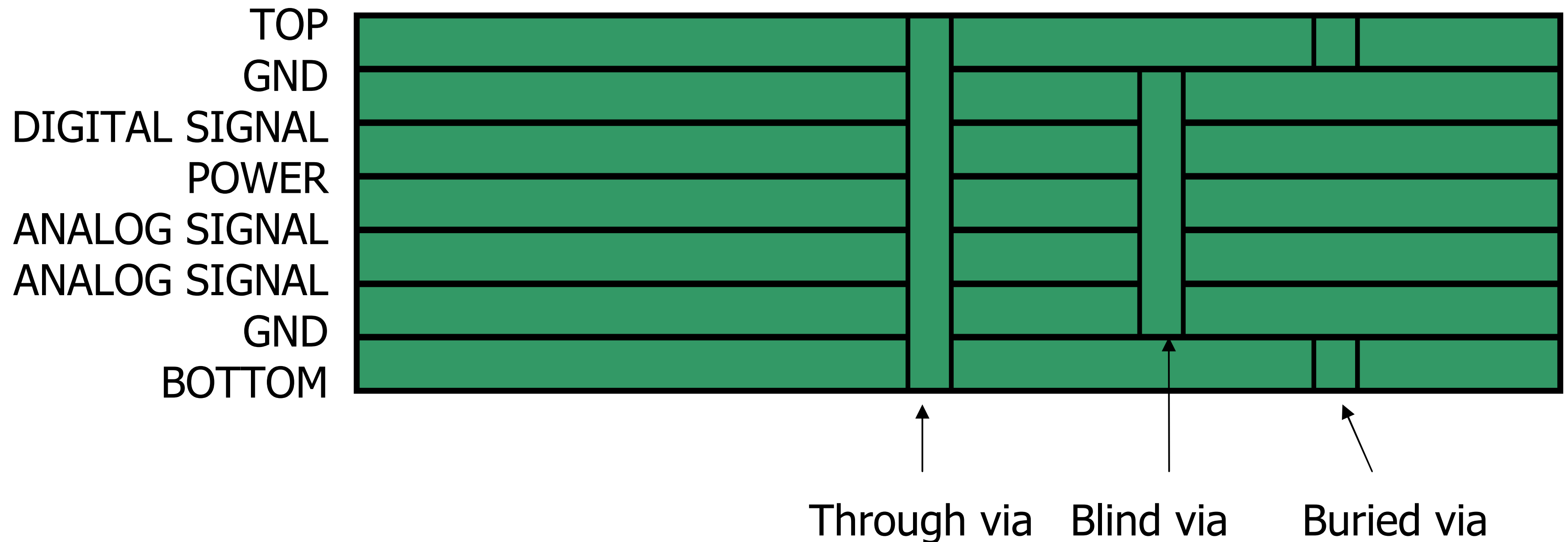
Prototype Design :

- PCB 8 layers for 2 blocks of 64 pads
- PCB 7 layers for 2 blocks of 64 pads (if we reduce Asics external components we can probably use 6 layers)
- PCB 8 layers with 2 GND layers added : not possible for this design

Prototype Design :

- PCB extra thin (0.8 mm in 8 layers and 0.6 mm in 6 layers)
- Special PCB with blind and buried vias
    - Bottom layer is free to accept RPC pads without constraints
- Passive Component extra flat (0.3mm max except Hardroc in cqfp package)
- Total thickness 1.1mm

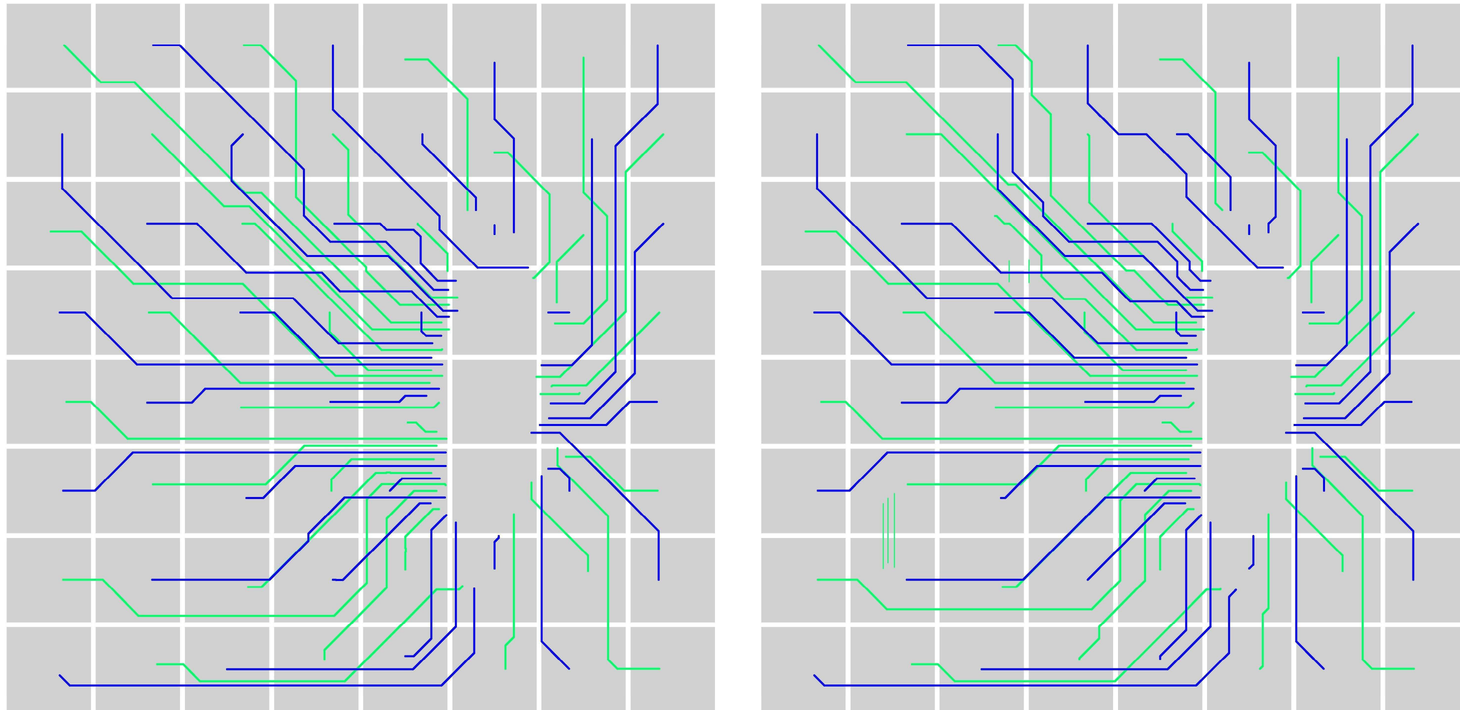
Layout in 8 layers (solution1)



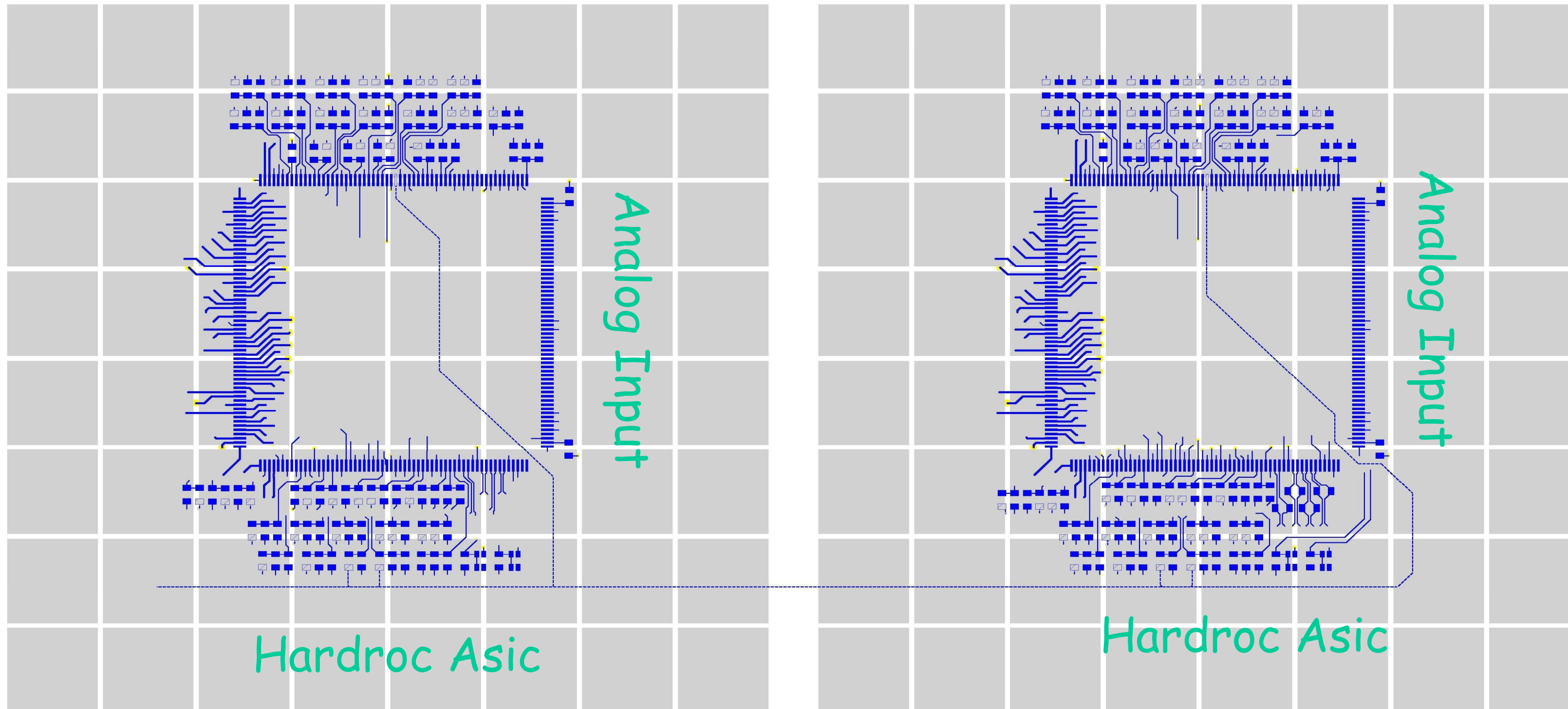
Layer definition (except FPGA area)

TOP LAYER	: Component layer
GND	: Ground layer and access to internal layers
DIGITAL SIGNAL	: Layer to interconnect between hardroc and FPGA
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

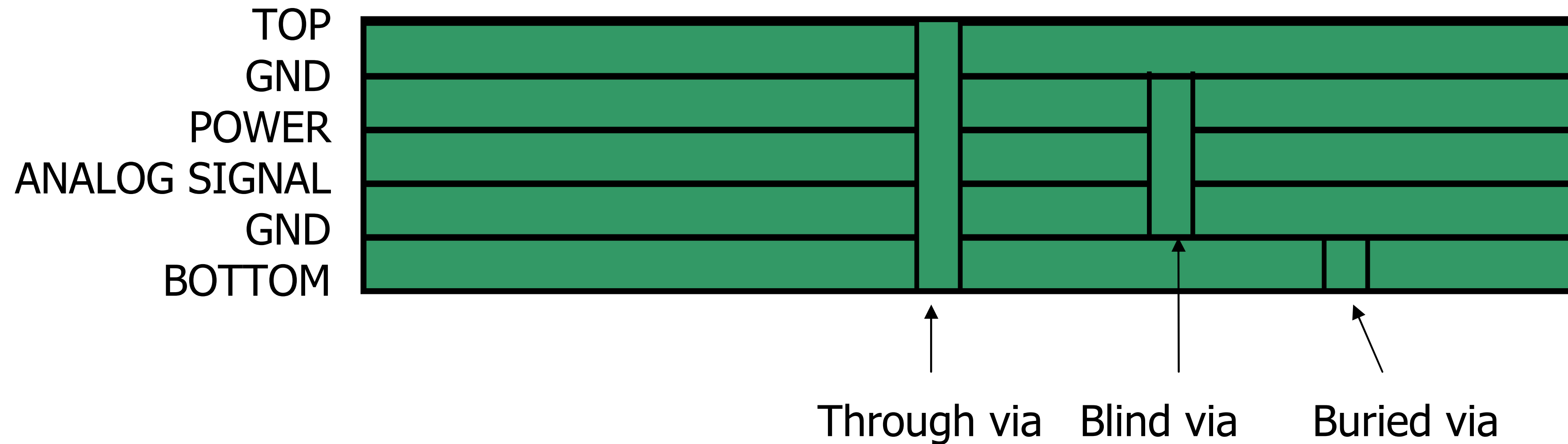
Analog input and Pads (8 layers)



Top layer and Pads (8 layers)



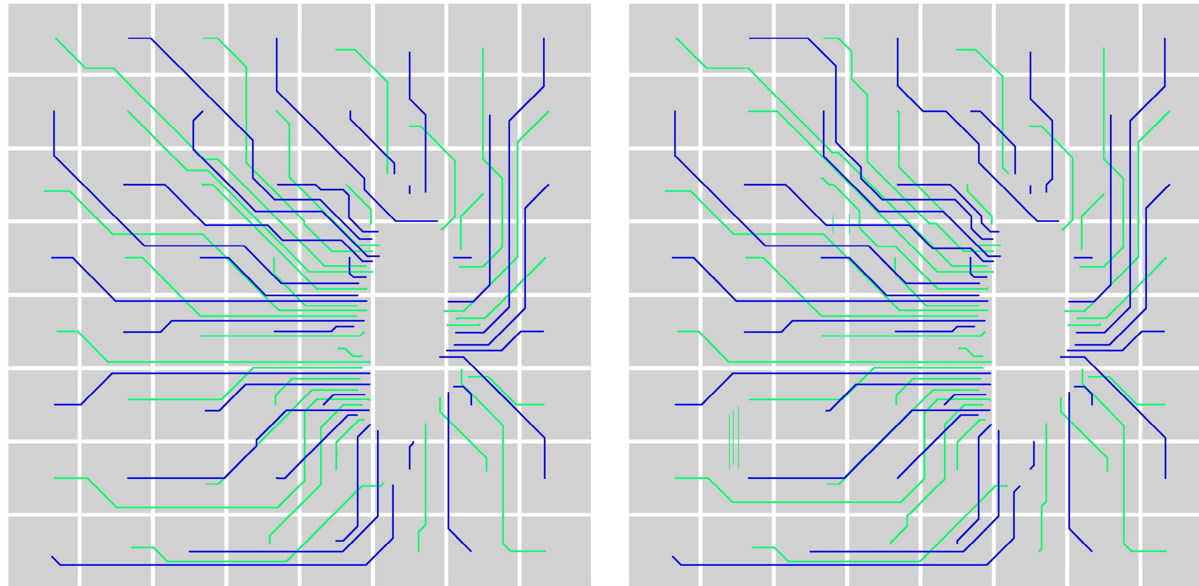
Layout in 6 layers (solution2)



Layer definition (except FPGA area)

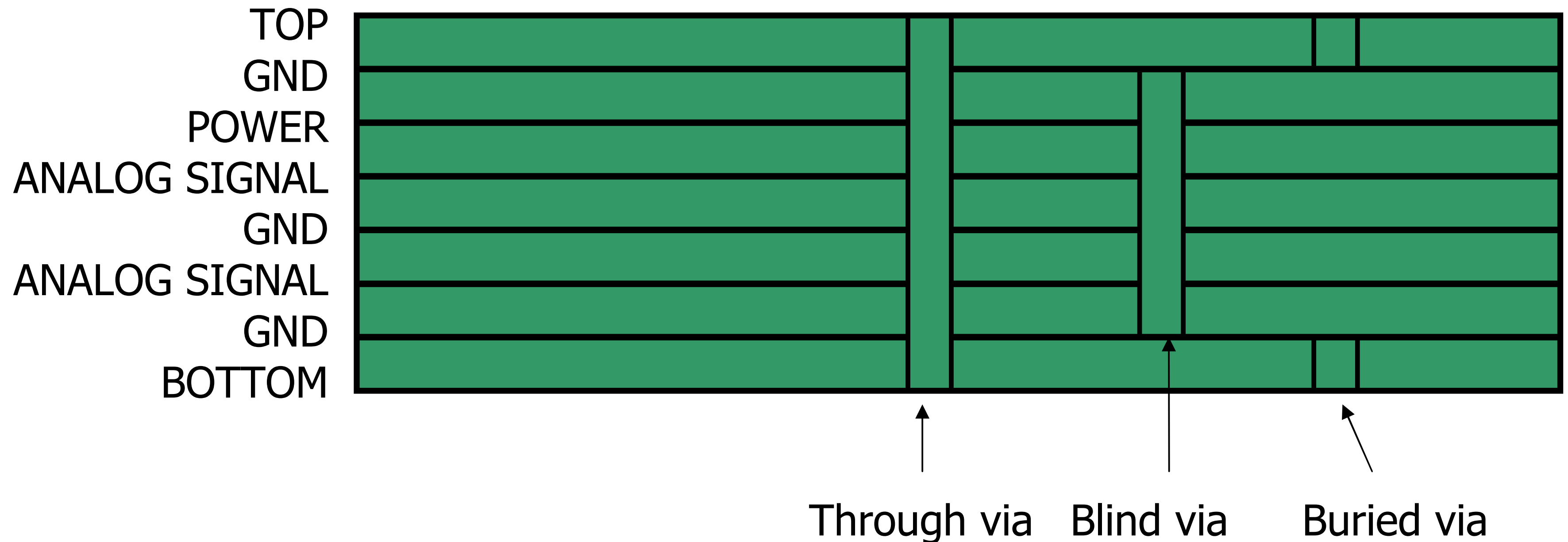
TOP LAYER	: Component layer+interconnect between hardroc and FPGA
GND	: Ground layer and access to internal layers
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

Analog input and Pads (7 layers)



Under work, need to rearrange input assignment and use 1 layer for analog input

Layout in 8 layers (solution3)



Layer definition (except FPGA area)

TOP LAYER	: Component layer+interconnect between hardroc and FPGA
GND	: Ground layer and access to internal layers
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

Tests

Try to measure the cross talk for solution 1 and solution 2

If the results are close, solution 2 (6 layers) could be the solution

Back up version with solution 3 and 8 layers