DAQ overview

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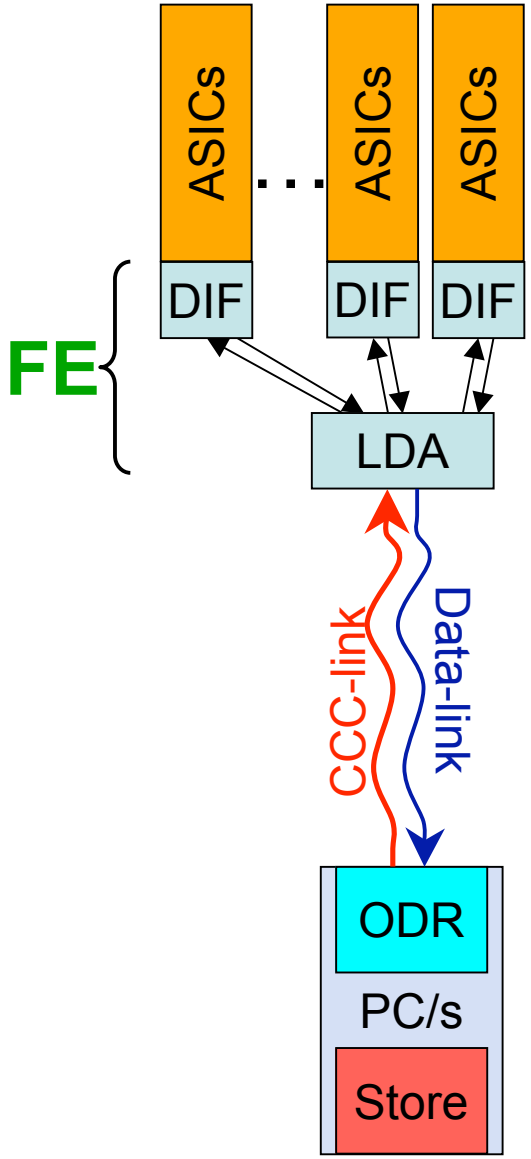
- DAQ structure and responsibility
- Short-term results and plans
- Deliverables and milestones (PPARC and EUDET)
- Status
- Longer-term plans

Ideal DAQ Structural Overview

- Detector ASICs on e.g. ECAL slab
- Front-End (FE)
  - FE-Interface (DIF): Detector specific
  - FE Link/Data Aggregator (LDA): Generic
- Data-link (FE to Off-Detector Receiver)
- CCC-link (Clock+Control+Config to FE)
- DAQ PC
  - Off-Detector Receiver/s (ODR)
  - Drives CCC-link
  - Data Store



FE Structure Detail

- We have 2+ types of detector to readout.
- Divide the FE into a 2 part, tiered system
- Detector Interface module (DIF)
  - Detector specific interface
  - Includes power connectors
  - ‘Local’ systems (e.g. stand-alone clock)
  - Debug connectors
- Link/Data Aggregator module (LDA)
  - Collects data from many ‘DIF’s
  - Drives data Off detector link
  - Receives and distributes C+C
  - FPGA Development board
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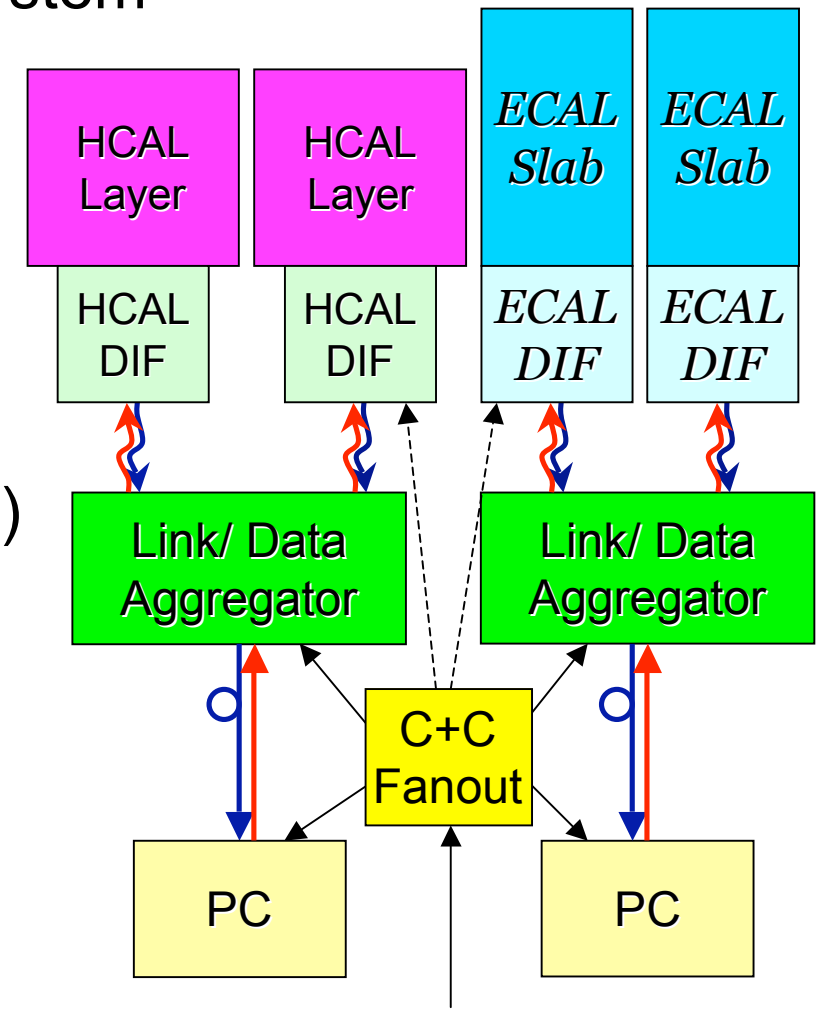
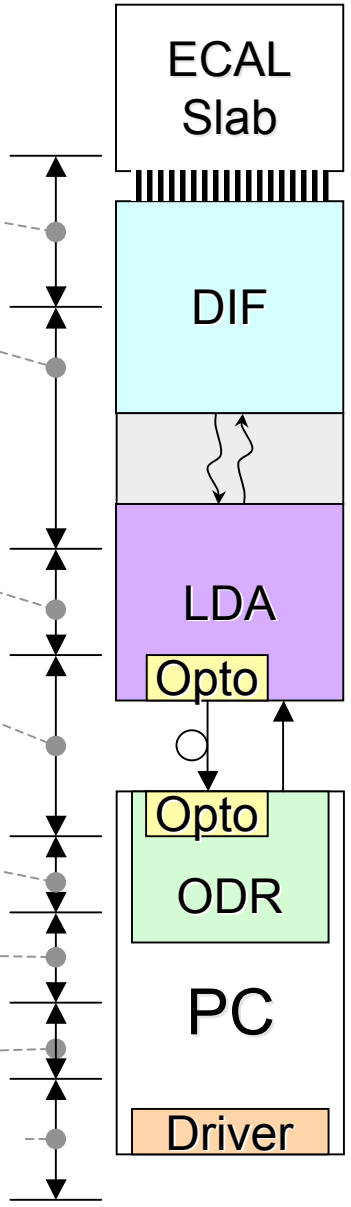


- **BUT:**
- We might like to read-out slabs individually first…

UK Read-out work (ECAL FE)

- Detector Interface (Cam, IC)
  - Spec + hardware
- DIF to Link/Data Aggregator (Cam/Man)
  - Spec + hardware
- Data aggregate, format (Man)
  - Hardware + firmware
- LDA to ODR opto-link (Man, UCL)
  - Hardware + firmware
- ODR (RHUL, UCL, Cam)
  - firmware
- ODR to disk (RHUL)
  - Driver software
- Local Software DAQ (RHUL)
- Full blown Software DAQ (RHUL, UCL, [IC])



Short-term results and plans

- Tests of new ASIC. At Imperial, results to come.
- Model slab almost ready for testing in Cambridge:
  - Information on data transfer: speeds, efficiency, volume
  - Number, configuration of data lines
  - Some information on mechanical structure
  - Definition of FE, end-of-slab electronics/interface

- Feedback on chip design/performance
- Above results from model and definition and pledge to build ECAL FE electronics: DIF+LDA
- Assistance in designing other DIFs

Deliverables and milestones

- PPARC programme (October 2005-March 2009)
  - Tests of ASICs in 2007 and 2008
  - Test results on model slab (2007)
  - Prototype ODR (March 2007)
  - Initial ODR (December 2007)
  - Full-scale DAQ system (2008/9)
  - Much more which you don’t (necessarily) know about - networks, c&c&c
- EUDET programme (January 2006-December 2009)
  - PCI prototype available (June 2007)
  - DAQ system prototype available (September 2008)
  - DAQ system available (June 2009)

Status

- Tests of new ASIC ongoing and ready to test new ASICs
- Model slab almost ready and to provide lots of vital information
- Prototype ODR is complete - milestone ✓
  - Have hardware with firmware
  - Can transport data
  - Know speed of transmission and working on optimisation
  - Further improvements and tests to be done by end 2007
- This does not include
  - DAQ software
  - Clock, control and configuration up to detector
- Although they are both being (starting to be worked) on

Longer-term plans

- R&D into commercial systems to investigate a flexible DAQ, with measured limits and assessment of applicability
- To provide a working and 100% efficient DAQ system for future prototypes, specifically the EUDET modules
- Other DAQ within EUDET proving useful and may speed up development by borrowing from each other
  - Fast control - TLU from JRA1
  - DAQ software - XDAQ, JRA1-DAQ, our own. Start work next week.
- We will be ready for a test-beam programme in 2009

Summary

- From our perspective, work is proceeding on schedule
- Both our PPARC and EUDET commitments point to 2009
- DAQ systems provided for test-bench, ECAL, AHCAL

- The DHCAL is now an issue:
  - This was not part of our original remit
  - This would precipitate focused action on our part: +ive & -ive
  - We have to discuss