ATLAS activities for the HL-LHC upgrade at LPNHE Paris and LAL Orsay

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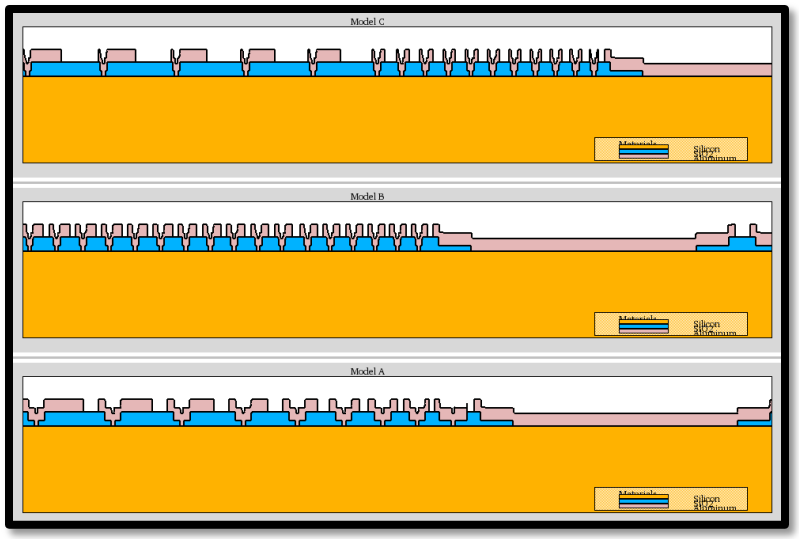
cnrs

General picture of R&D activities

- **Sensors**
  - Device Simulations
  - Sensor Production
  - Characterization
  - Irradiations
  - Testbeam evaluation
- **Edgeless sensors**
  - Active edge sensors
- **Track trigger**
  - FastTrack project
- **FE electronics**
  - Development of 3D OmegaPix prototype chip
  - On-beam characterization
  - Participation to RD53 (ATLAS/CMS) project
- **Mechanics**
  - Thermal simulations
  - Thermal characterization
  - Mechanical design
  - Material budget evaluation

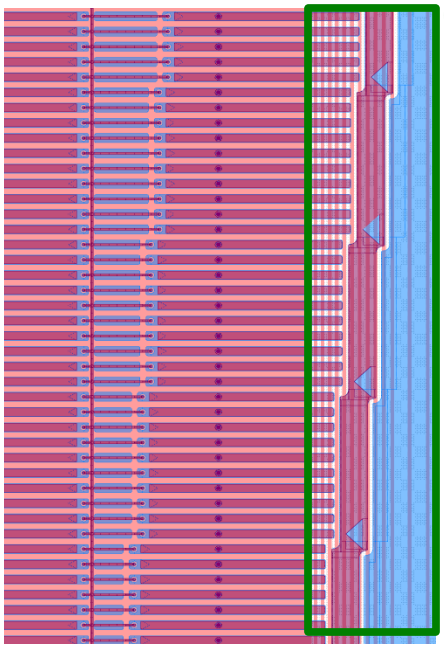
In the following, I'll concentrate on activities on which the collaboration with Ukraine groups has already progressed

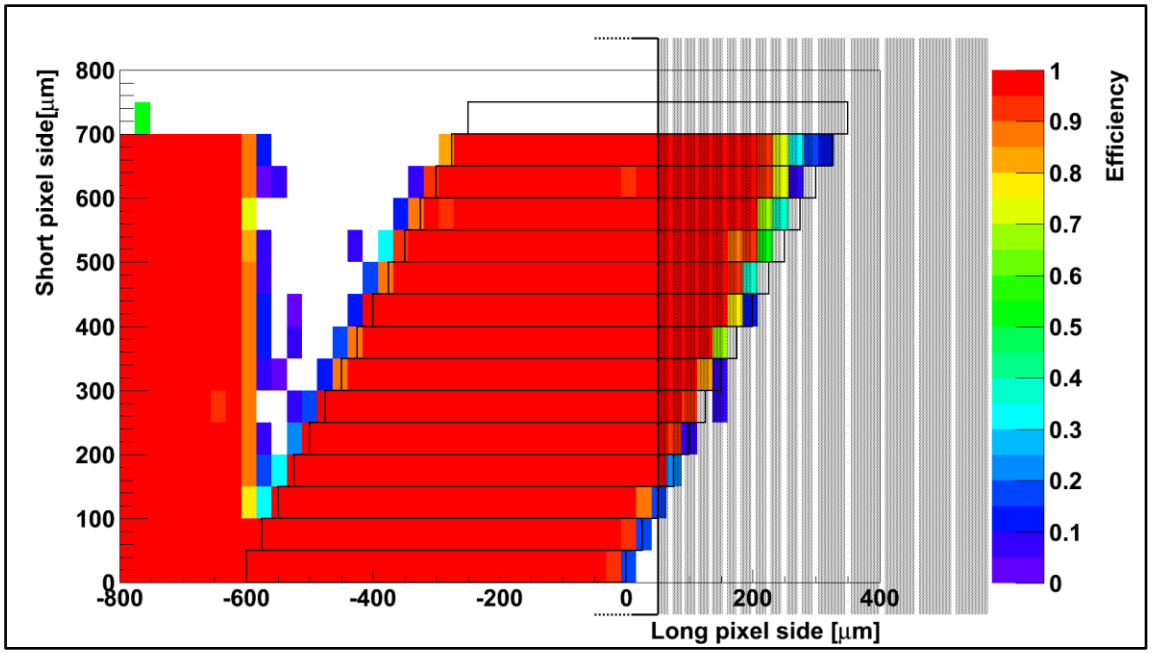
Since many years the LPNHE and LAL groups have developed experience in Si sensors simulation and design

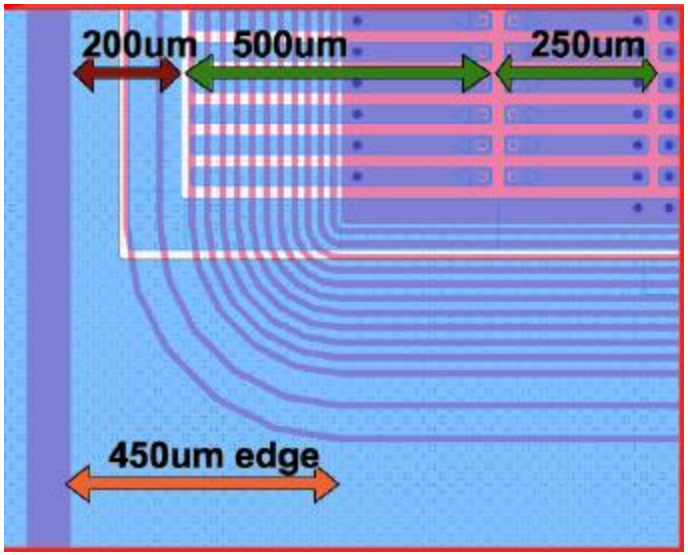


Major role in the design of the ATLAS IBL layer, installed now during the 2014 shutdown

Guard ring optimization, pixels inside guard-ring region to maximise active area





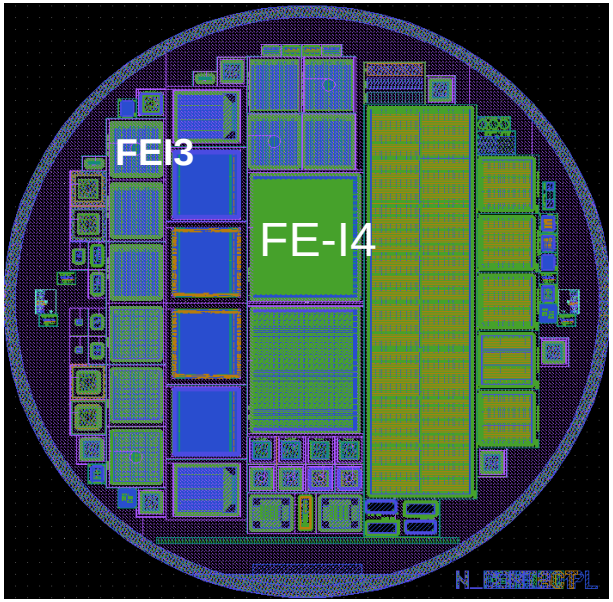


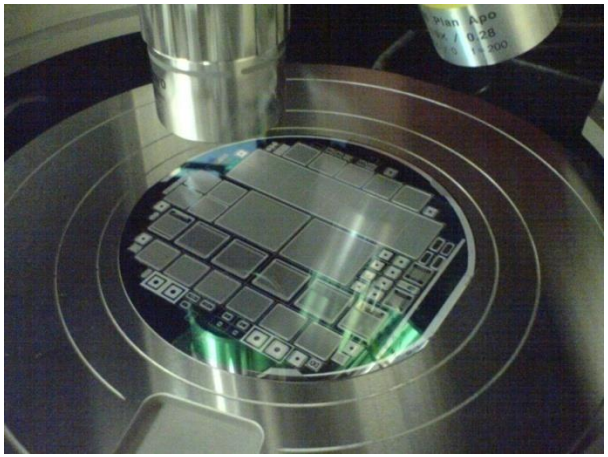
Pixels now very close to the cut region, choice possible thanks to simulations

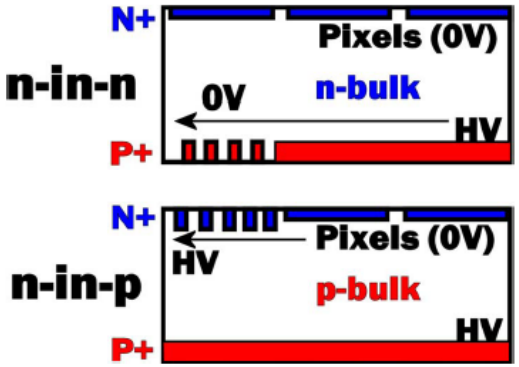
Many production of prototype sensors at Cis (Germany), FBK (Italy), VTT (Finland) by the LAL and LPNHE groups

Tested at the laboratories and put on testbeams

Both n-in-n and n-in-p prototype productions

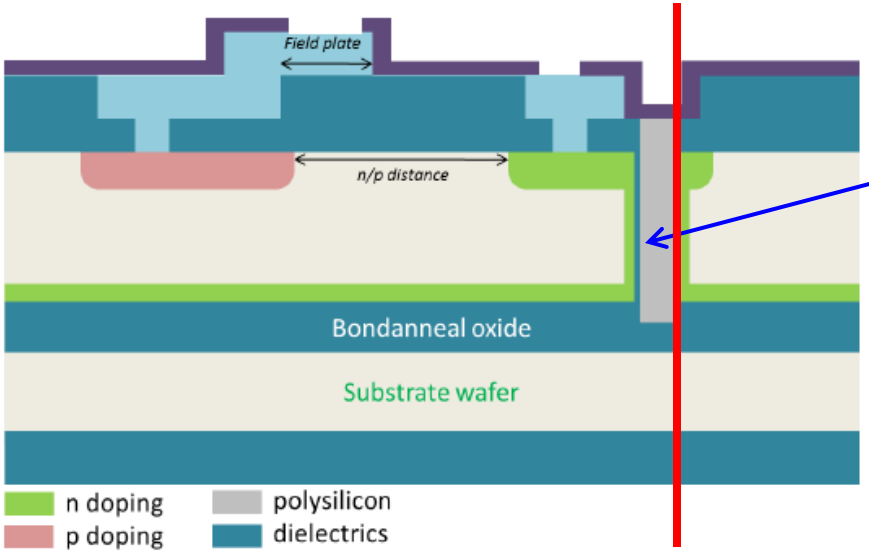






Additional long-term sensor development

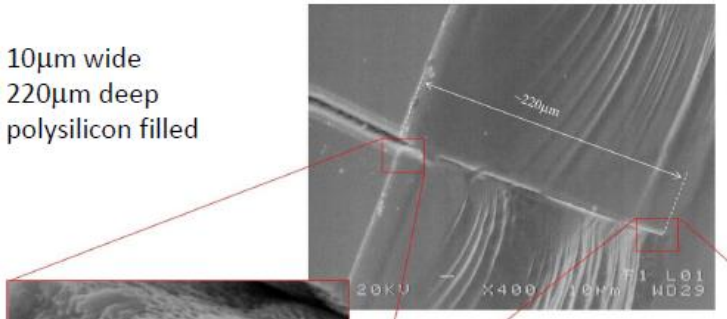
Active-edge detectors for sensor tiling

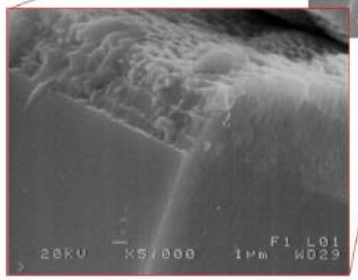


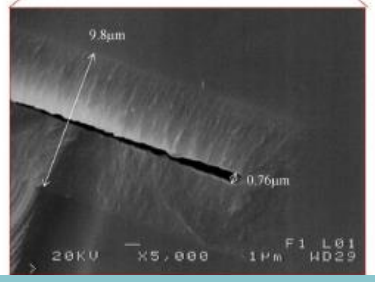
Deep trench diffusion (to prevent electrical field on the damaged cut)

Cut line

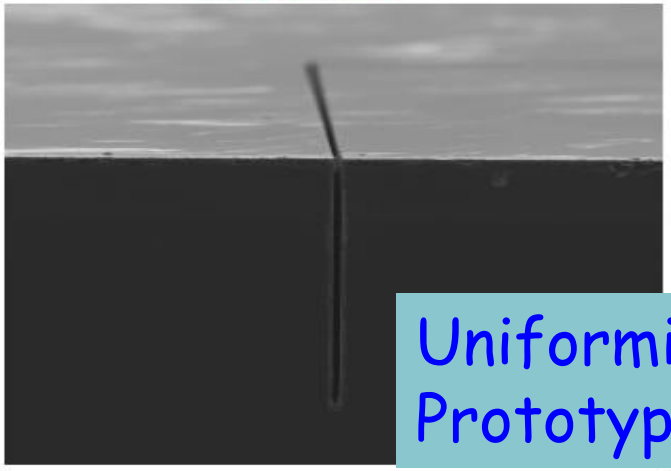
- 10µm wide
- 220µm deep
- polysilicon filled







4,5µm wide
220µm deep



Uniformity of trench filling is critical.
Prototypes production under way, good results

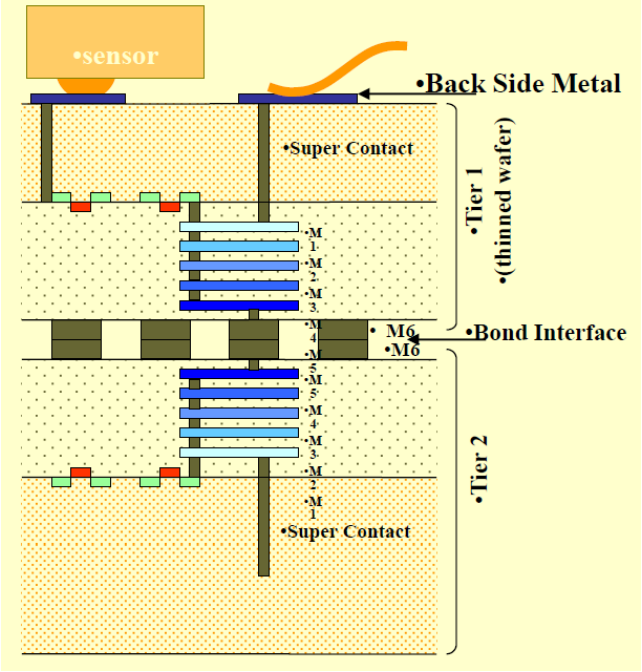
Electronics

- 3D/Vertical Integration R&D (LAL, LPNHE, CPPM)

Tezzaron/Chartered 130 nm

- Deep N-well,MiM capacitors – 1 fF/um^2 Single poly, 6 (8) levels of metal available,
- Vias 1.6x1.6 x10um, pitch 3.2 um
- Bond points Cu 1.7x1.7 um, pitch 2.4 um
- Wafer bonding at 375 deg C

Significant support from IN2P3, ANR, AIDA



OmegaPix and MemDyn chips (LAL, LPNHE)

- Exploratory OmegaPix chip (LAL, LPNHE) with small pixel size 50x50 um, matrix of 24 columns x 64 rows
- Goals: low threshold (1000 e), low noise 100 e) low consumption (3 uW/pixel)
- Reduced power voltage (1.2 V analog, 1.0 digital), feedback by parasitic capacitance

Participation to RD53, ATLAS/CMS common project (65nm)

Track trigger (FastTrack)

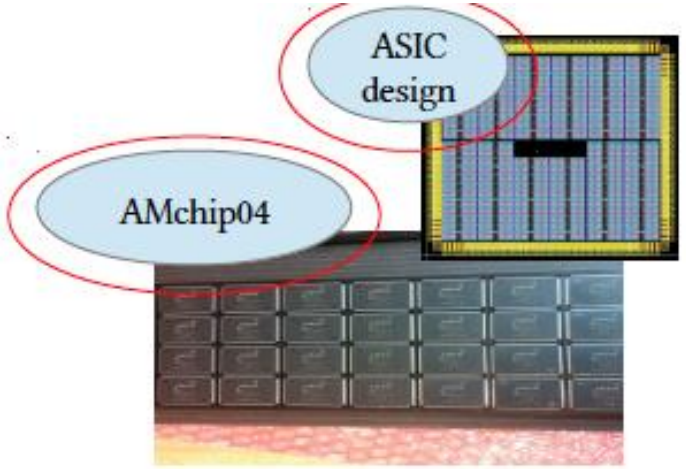
Increase in luminosity will oblige to improve trigger performance

Some event topologies involve reconstructed track information (example: impact parameter)

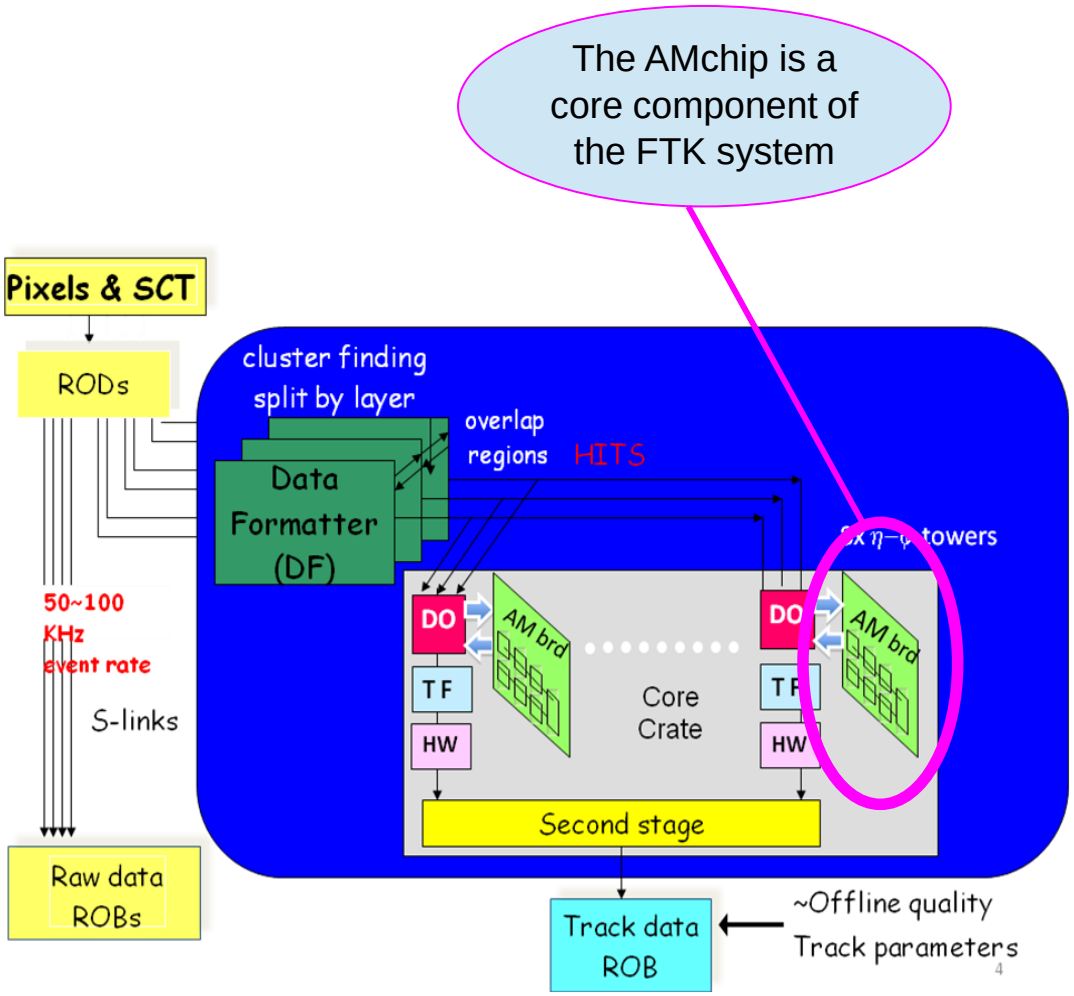
At present the full information from the tracker cannot be used in early trigger decision (algorithms of hit association and track fitting not fast enough for that, especially at high pile-up)

Associative Memory (AM) chip developed to do pattern recognition

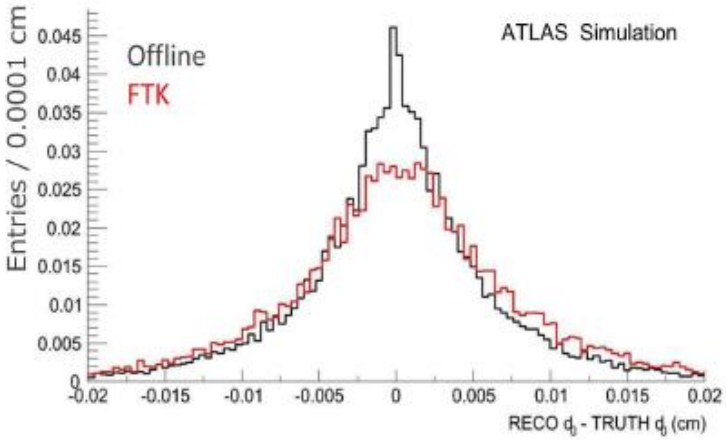
Fast. All stocked patterns tested at the same time
Comparison time does not depend on the number of patterns !



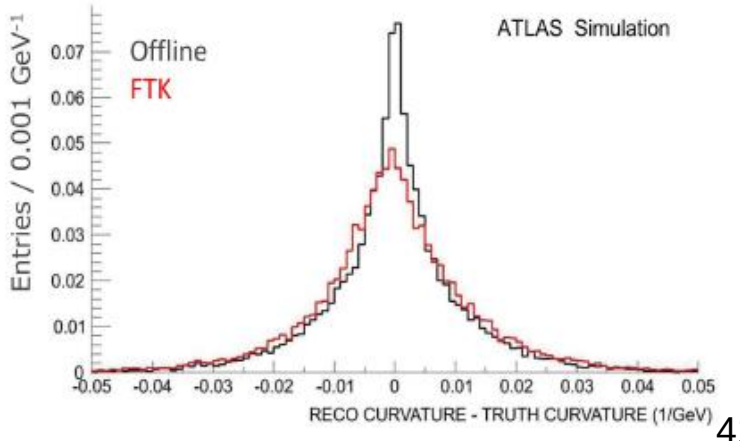
Hardware: many different boards, each with FPGAs with specific firmware and control software



Impact parameter resolution (FTK vs offline)



Curvature resolution (FTK vs offline)



We believe this is a highly strategic development in research

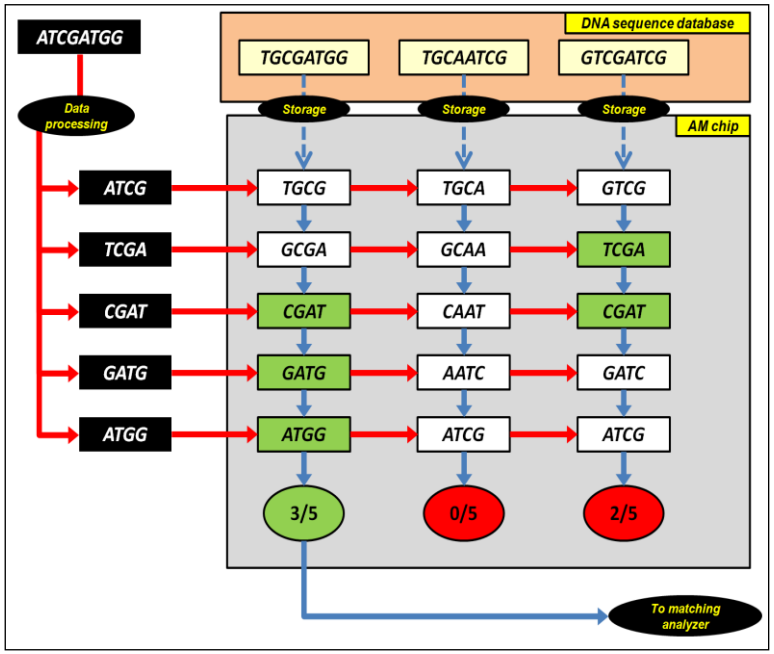
This high-speed processing/comparison has infinite ways of application in several domains

Flexible / easily scalable with the number of AM chips

For example:
image processing/comparison with unprecedented speed

traffic control
security
image-based web search
medical applications

Other example:
pattern identification in DNA sequencing



Link with CNAG (Centre Nacional d'Anàlisi Genòmica) in Barcelona who is proposing to use our board for this application

Three Ukranian students have already done (or are scheduled to do) periods in Paris to work with the LAL and LPNHE groups on :

- Sensor design and test
- Design and implementation of test benches and cards in the framework of 65nm electronics development
- FastTrack applications for track trigger

Yurii Piadyk (LPNHE, first part of 2014)
already scheduled to come again beginning 2015

Dmytro Hohov (LAL, first part of 2014)

Mykyta Haranko (LPNHE, Autumn 2014)

I found this collaboration an excellent experience
Students of very high quality, very motivated !