

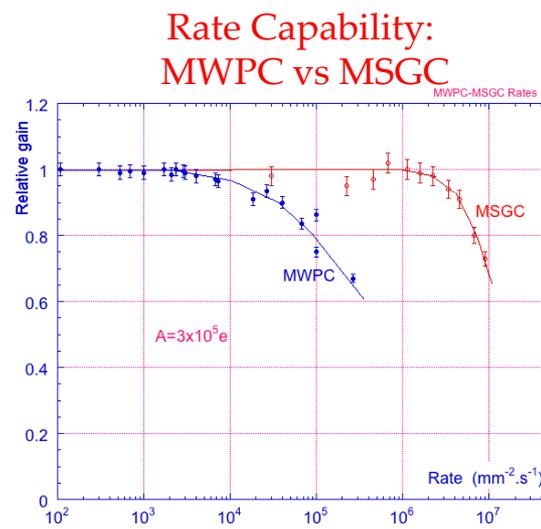
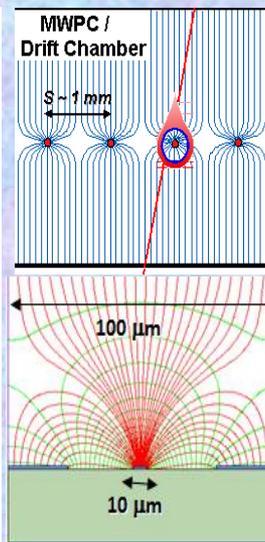
Pixel Readout for the ILC TPC in the Framework of the RD51

Maxim Titov
CEA Saclay, France

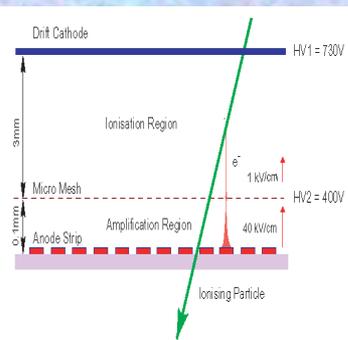
- University of Bonn: Y. Bilevych, C. Brezina, K. Desch, J. Kaminski, T. Krautscheid, C. Krieger, M. Lupberger
- NIKHEF: Jan Timmermann
- CEA Saclay: David Attie, Xavier Coppolani, Andrii Chau, Paul Colas, Maxim Titov
- LAL Orsay (S. Barsuk)
- Kyiv University (O. Bezshyyko group)

Micro-Pattern Gaseous Detector Technologies for Future Physics Projects

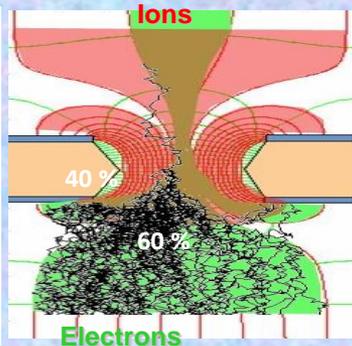
- Micromegas
- GEM
- Thick-GEM, Hole-Type and RETGEM
- MPDG with CMOS pixel ASICs (“InGrid”)
- Micro-Pixel Chamber (μ PIC)



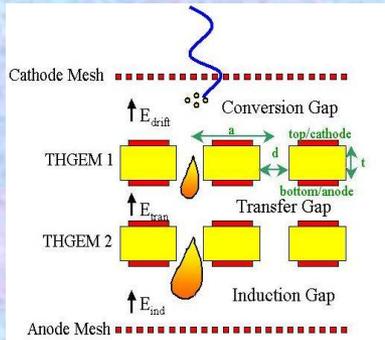
Micromegas



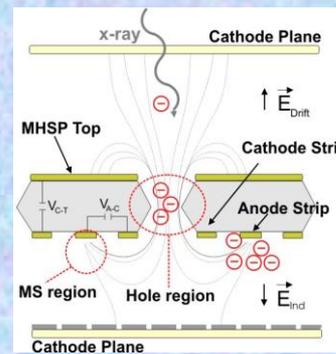
GEM



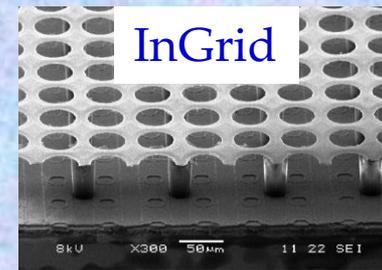
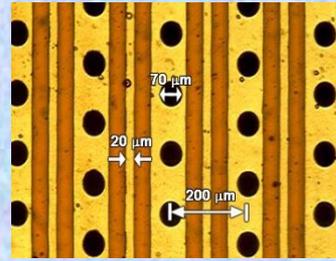
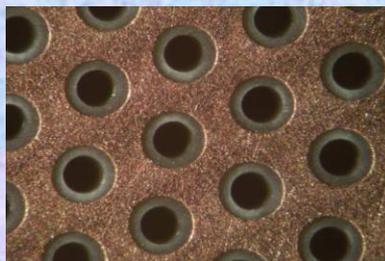
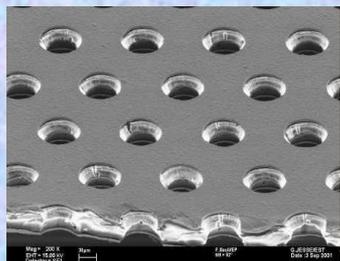
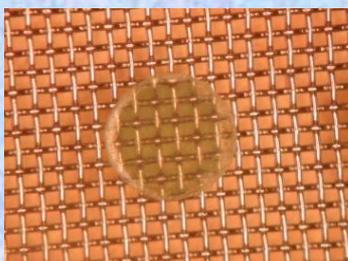
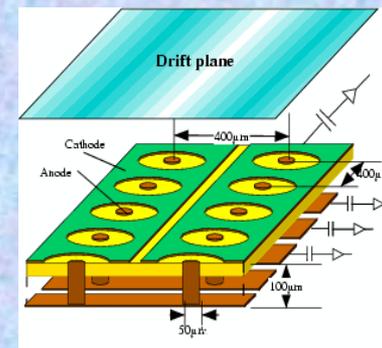
THGEM



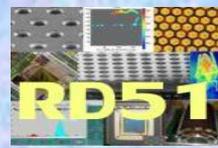
MHSP



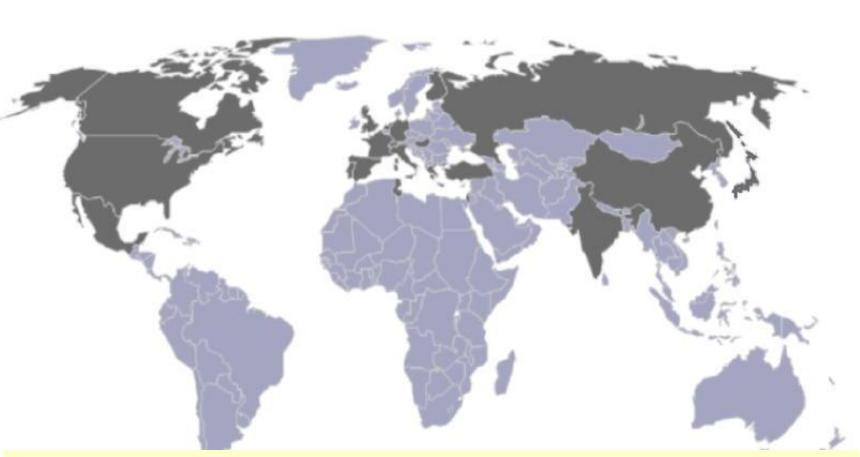
μ PIC



RD51 – Development of Micro-Pattern Gaseous Detector Technologies



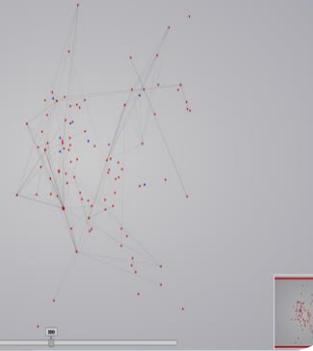
The **main objective** is to advance **MPGD technological development** and associated electronic-readout systems, for applications in basic and applied research”



<http://rd51-public.web.cern.ch/rd51-public>

A **fundamental boost** is offered **by RD51**: from isolate MPGD developers to a world-wide net

1998



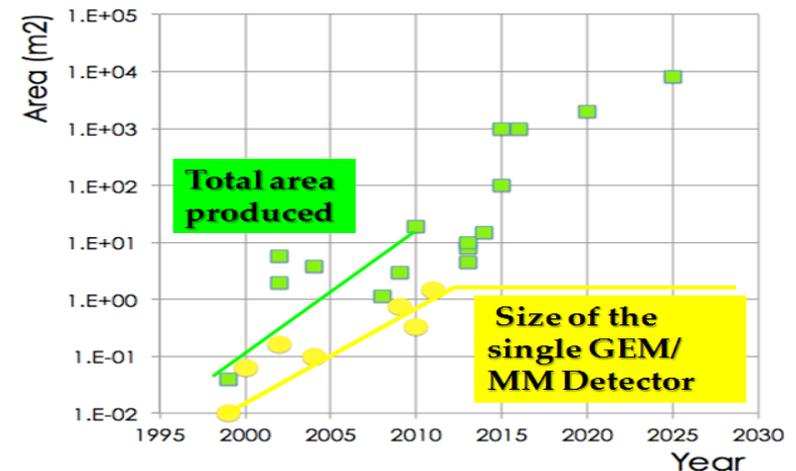
2014



World-wide Collaboration for the MPGD Developments → RD51 (91 institute, > 500 people):

- ❖ Large Scale R&D program to advance MPGD Technologies
- ❖ Access to the MPGD “know-how”
- ❖ Foster Industrial Production

Advances in photolithography → Large Area MPGDs (~ m² unit size)



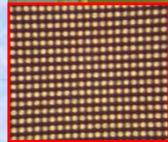
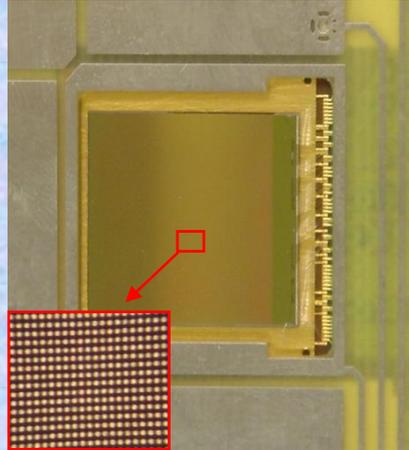
Integrated Electronics: Pixel Readout of Micro-Pattern Gas Detectors

3D Gaseous Pixel Detector → 2D (CMOS pixel chip readout) × 1D (drift time)

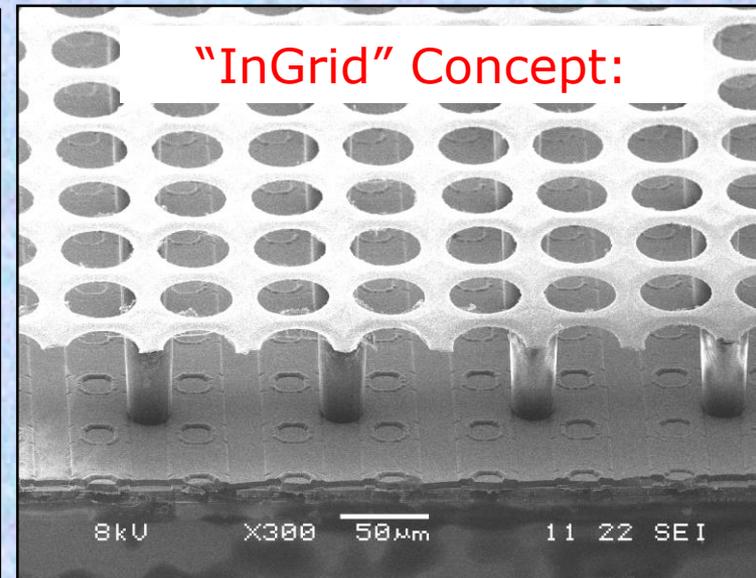
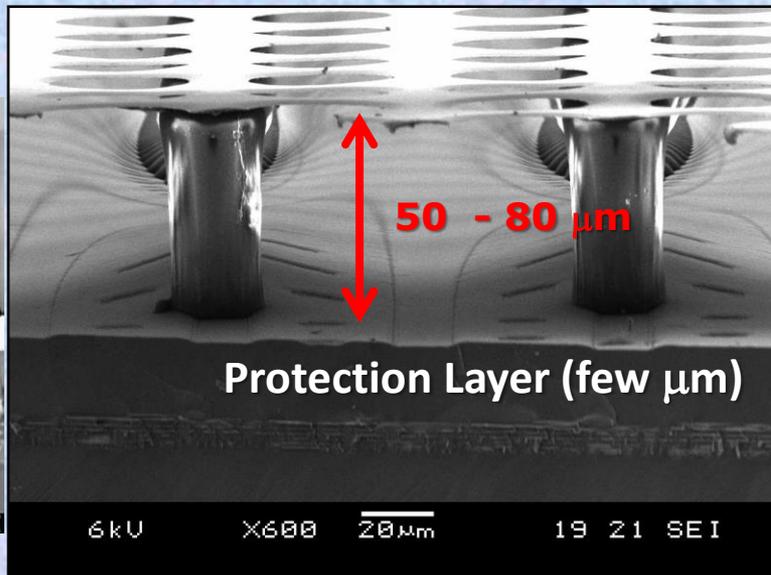
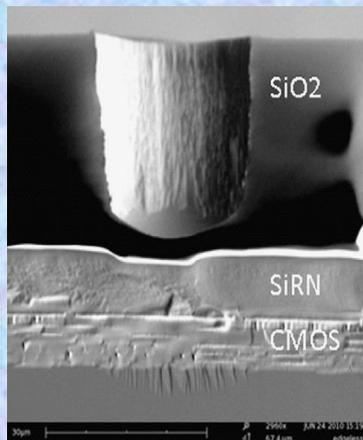
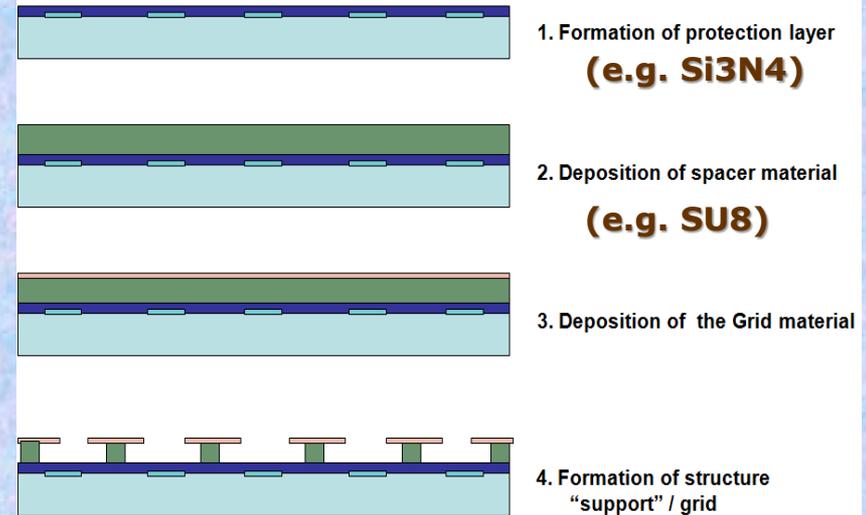
Bump bond pads for Si-pixel Detectors - Timepix or Medipix2 (256 × 256 pixels of size 55 × 55 μm²) serve as charge collection pads.

Each pixel can be set to:

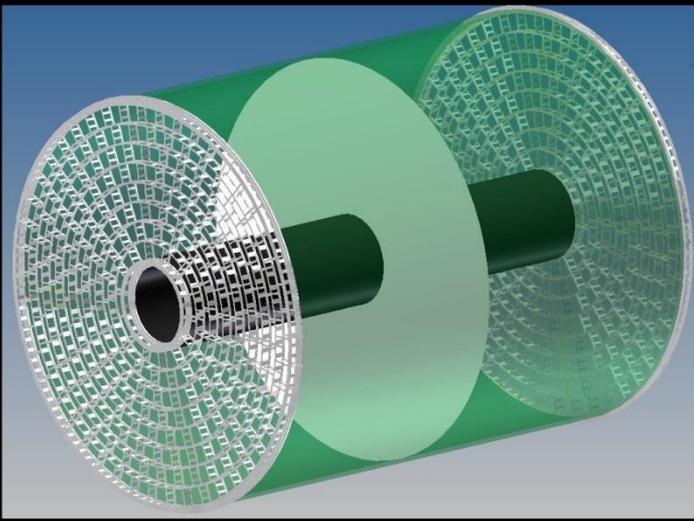
- TOT ≈ integrated charge
- TIME = Time between hit and shutter end



Through POST-PROCESSING **INTEGRATE MICROME GAS** directly on top of CMOS chip



Pixel Readout for Time Projection Chamber at the ILC or CLIC



MPGDs are foreseen as TPC readout for ILC or CLIC (size of endcaps of $\sim 10 \text{ m}^2$):

- **Standard pads ($1 \times 6 \text{ mm}^2$):** 8 rows of detector modules ($17 \times 23 \text{ cm}^2$); 240 modules per endcap
- **Pixel ($55 \times 55 \mu\text{m}^2$):** ~ 100 - 120 chips per module
→ 25000-30000 per endcap

Potential advantages of pixel TPC ($55 \times 55 \mu\text{m}^2$):

- very good point + momentum resolution
- dE/dx via cluster counting
- frontend electronics automatically integrated ('active endplate')

Potential concerns:

- diffusion will limit resolution (gas!):
how small is necessary?
- cost ?
- stable operation possible ?

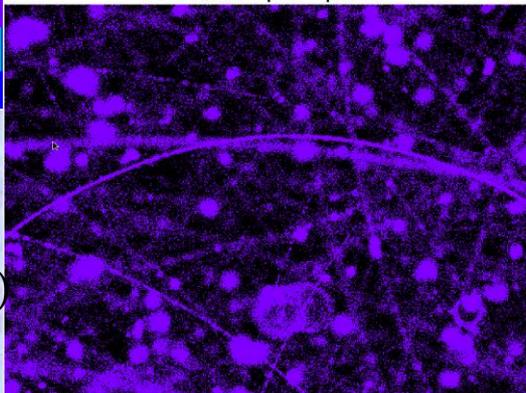
- **Demonstrate operability of the concept;**
Measure & understand (details of) charge cloud

$1 \times 6 \text{ mm}^2$ pads

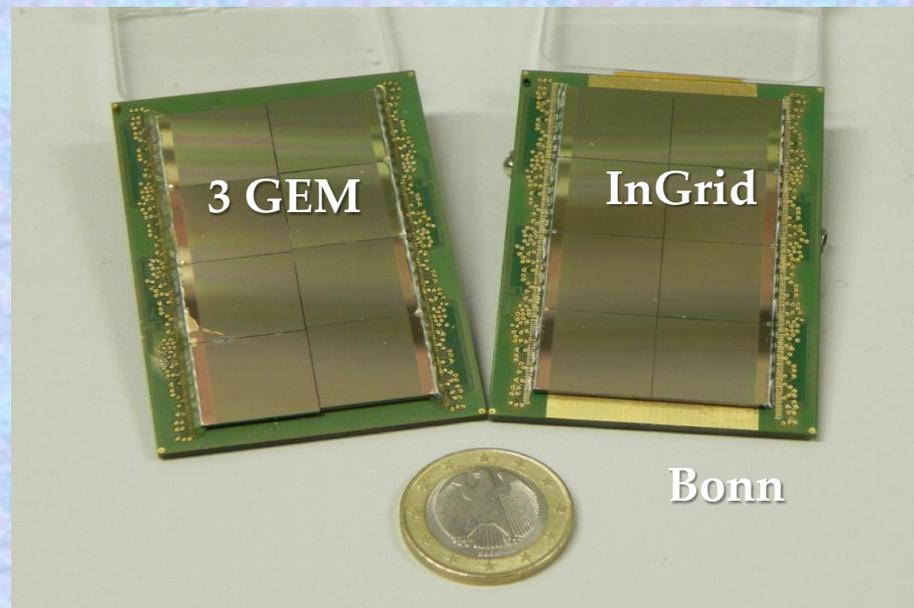
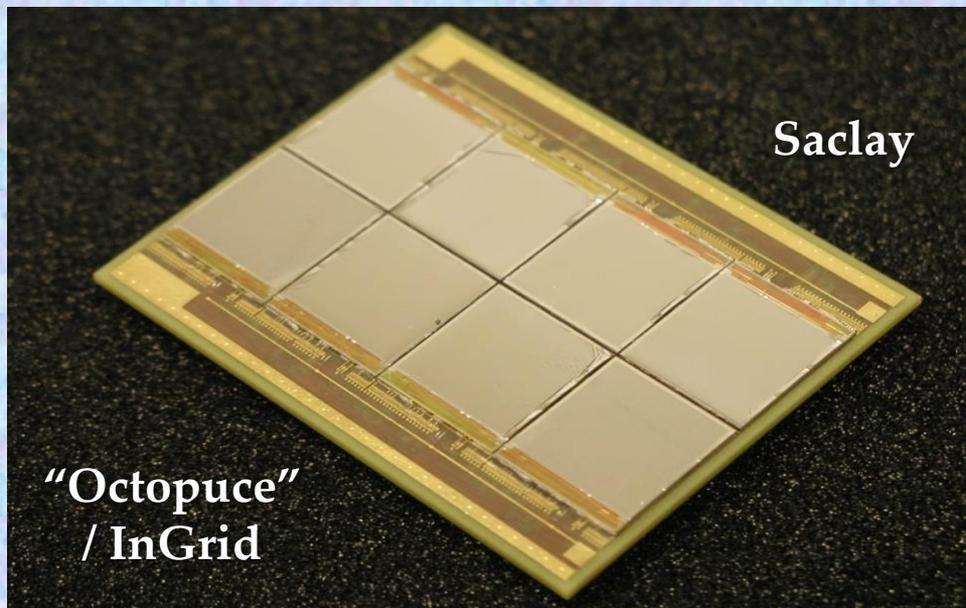
Backgrounds in CLIC TPC requires very small pixels ($< 1 \times 1 \text{ mm}^2$)

$100 \times 100 \mu\text{m}^2$ pixels

CLIC TPC
Simulation
(M. Killenberg)



Going to Larger Areas: "Octopuce" Modules based on the 2 x 4 Timepix ASICs



- ❖ 2010: Saclay / NIKHEF "Octopuce" (InGrid): studies with X-Rays and at DESY e- beam
- ❖ 2012-2013 : 2 Saclay / NIKHEF "Octopuce" (InGrid): 1 - some issues with readout; 2 - OK
- ❖ 2013: 2 Bonn "Octoboards" (InGrid & 3-GEM): studies with RD51 SRS at DESY e- beam

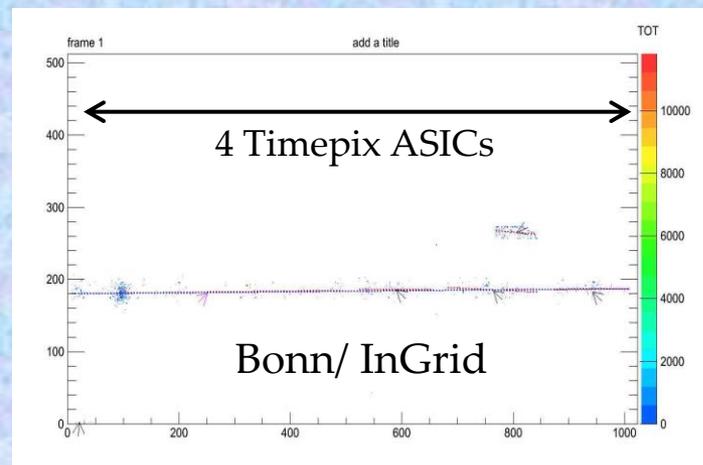
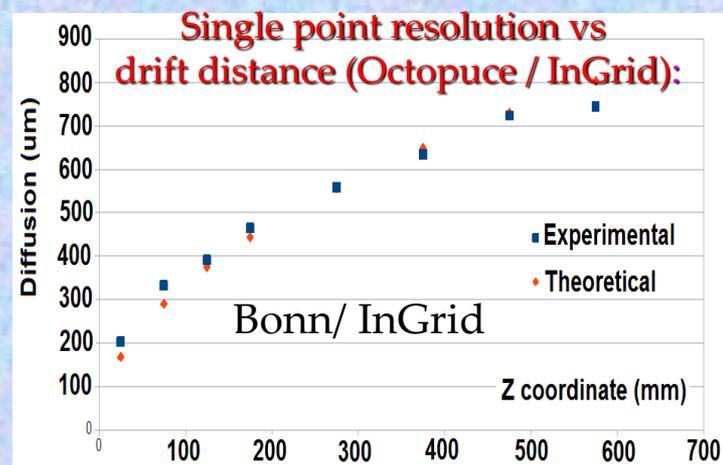
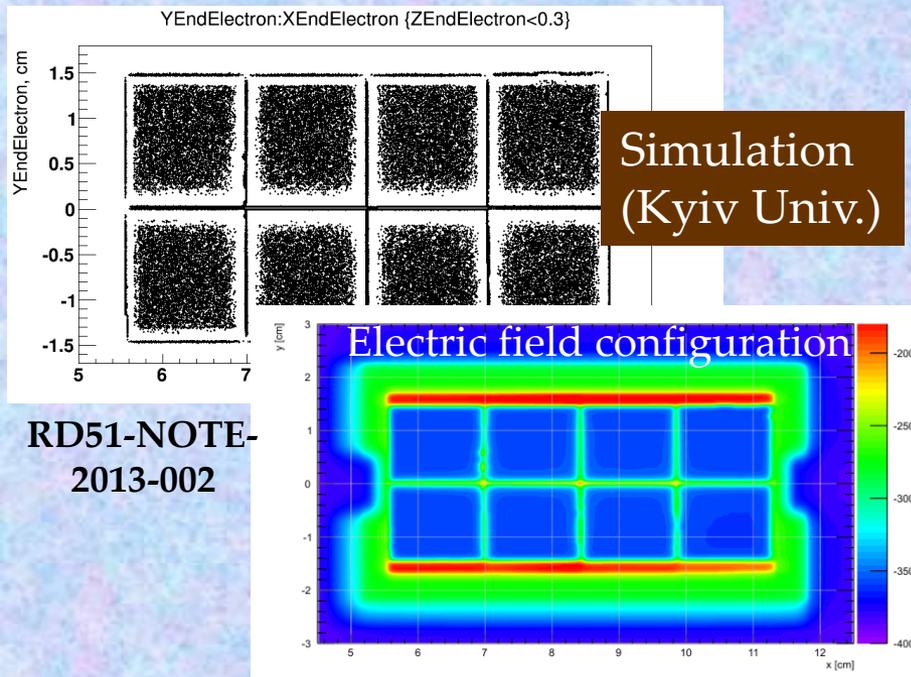
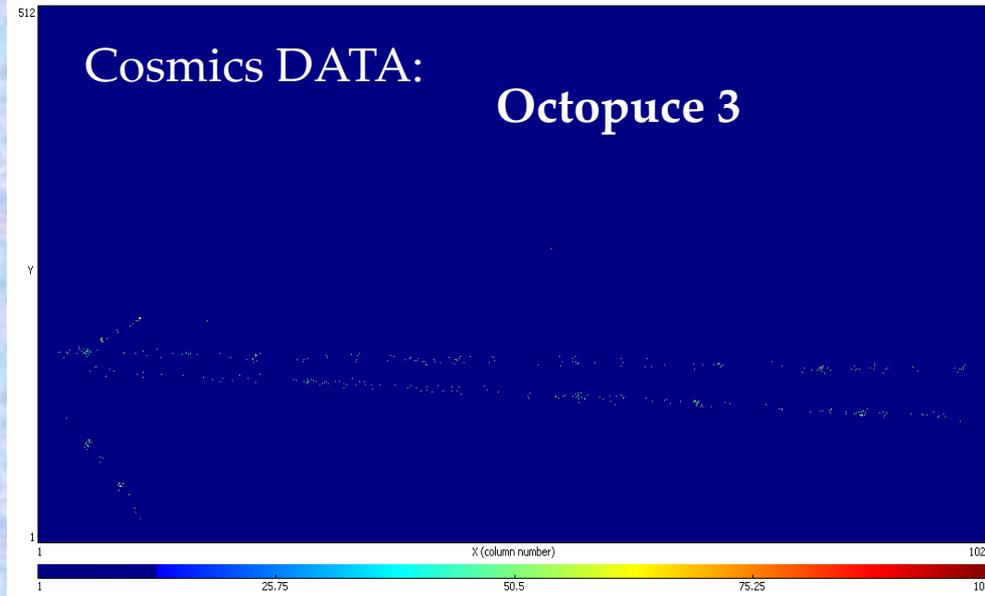
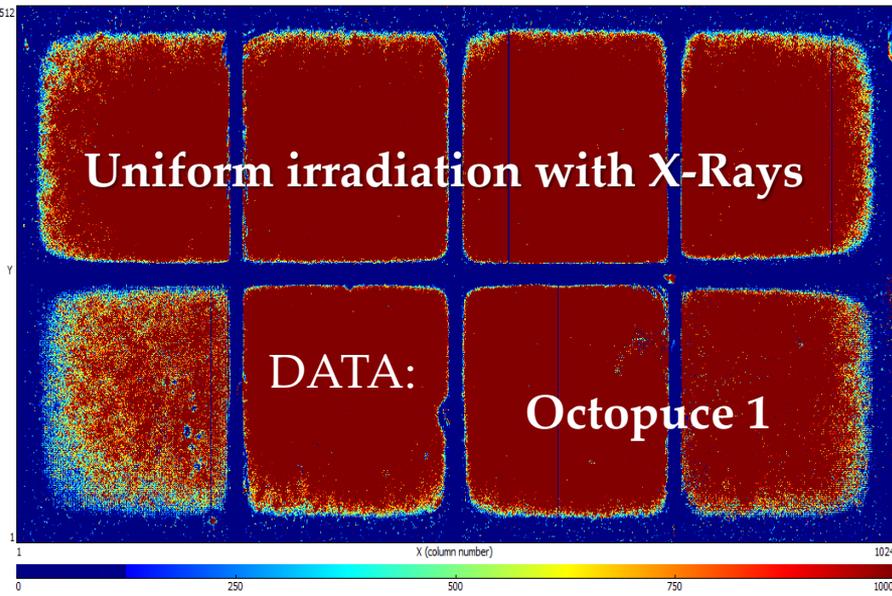


Image from
Bonn/"Octoboard"
(5 GeV e-):

InGrid: each electron
avalanche
corresponds to
single pixel hit

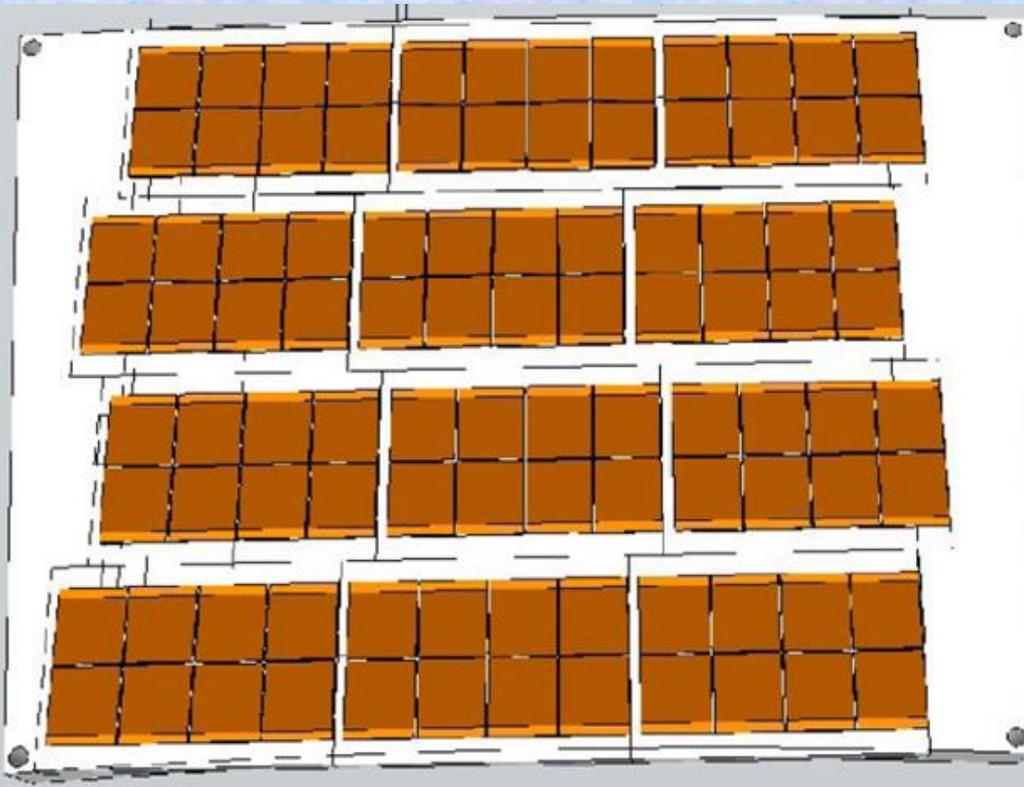


Saclay "Octopuce's": Study of Uniformity with X-Rays & Cosmics



- Single electron sensitivity ~ 100 % (in the central areas of the chips)
- Work is ongoing to better understand & improve field distortions in-between and at the borders of "InGrid's (based on simulation)

Future Plans: Pixel Readout of MPGD - Proof-of-Principle of Si-TPC



Mid-term plan (3 years):

Develop and equip a full LCTPC module (~100 chips) with “InGrid”s, using “Octopuce” module as the basic building block

Pixel LC-TPC Consortium:
Bonn, Saclay, NIKHEF, DESY,
LAL, Kyiv University

- Improved mass production of “InGrid”s (less dead area, higher yield, protection)
- Minimize field distortions in the « Octopuce » plane; work on more realistic cooling and power pulsing
- Develop simulation chain to compare momentum resolution, double track resolution, dE/dx and pattern recognition to pad-based readout and to optimize the geometry
- Experimental dE/dx study by cluster counting using InGrid at the LAL/PHIL facility

Pixel Readout for LC TPC: Next Steps

Short-Term Plans:

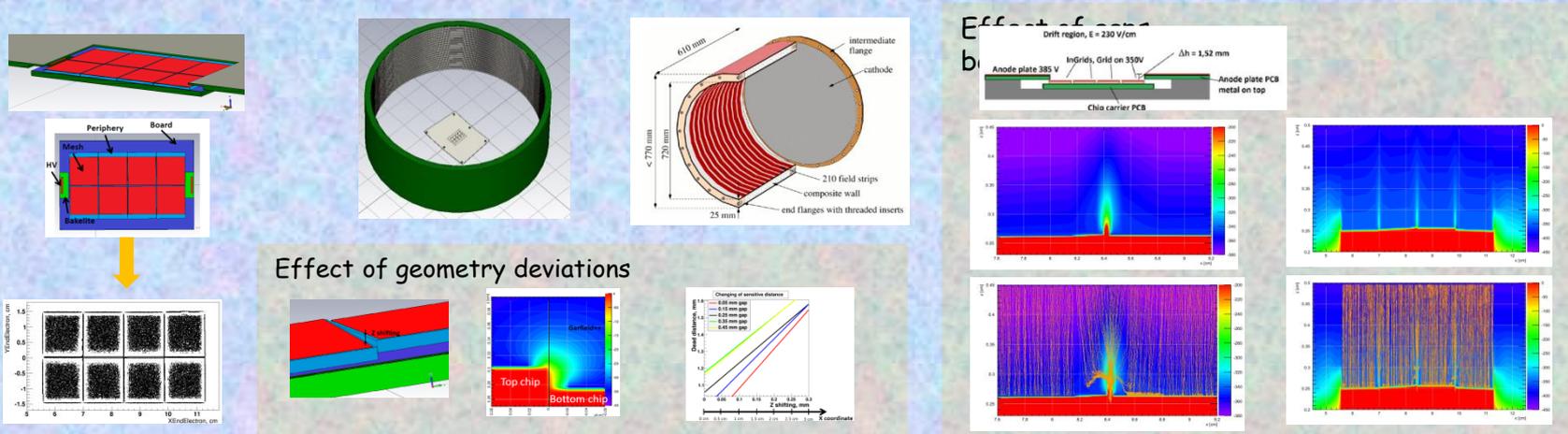
- Improve SU8-based « InGrid » structure (less dead area, higher yield, protection)
- Better understand and improve field distortion issues at the « InGrid » plane (in between chips and at the borders of the Octopuce);
- Develop simulation chain to compare momentum resolution, double track resolution, dE/dx and pattern recognition to pad-based readout and to optimize the geometry (e.g. minimize the needed chip coverage)

Long-Term Plans:

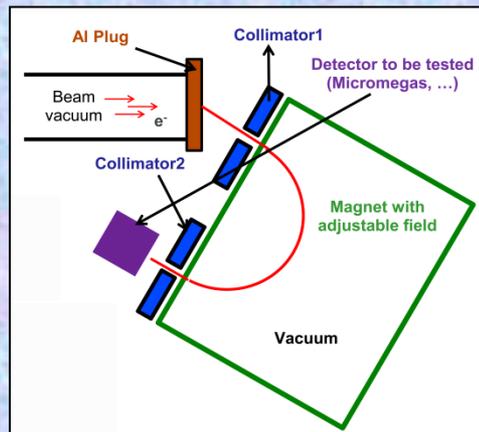
- Improved chip functionality → Timepix3 → transfer InGrid process to Timepix3
- Adapted readout system → high-speed SRS readout for Timepix(3)(8 & 100 chips);
- Improved mass production of InGrids → in collaboration with IZM, Berlin
- Work on more realistic cooling and power pulsing;
- Develop a backside connection technology both for LV/data and for the HV;

Irfu – LAL – Kyiv Cooperation: Present and Future

- ❖ Kyiv University made a major contributions towards optimization of geometry of large-area “InGrid” Detectors (Garfield ++ simulations) within the ILCTPC-Pixel Collaboration:



- ❖ LAL/Kyiv U/IRFU/CERN Cooperation on LEETECH Platform / PHIL @ LAL: Magnet (CERN) + Collimators (Kyiv University)



- ❖ Ultimate goal is to develop experimental setup with “InGrid” Detectors @ Kyiv university (optimization of detector characteristics and educational setup)