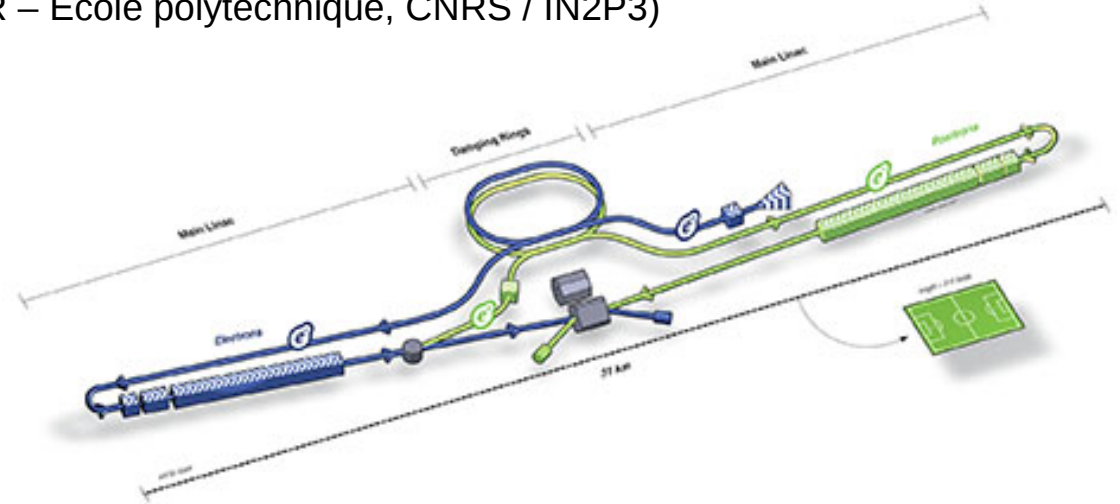


ILD SiW ECAL project

French-Ukrainian Workshop, LAL, Oct 2014
Vladislav BALAGURA (LLR – Ecole polytechnique, CNRS / IN2P3)

International Linear Collider



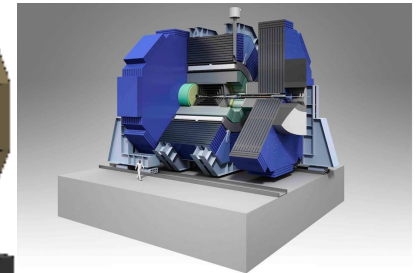
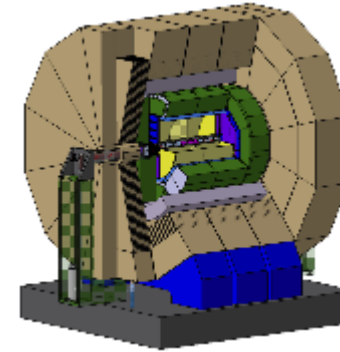
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two detectors proposed:

- ILD (International Large Detector) and
- SiD (Silicon Detector)



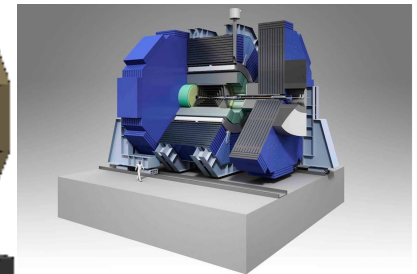
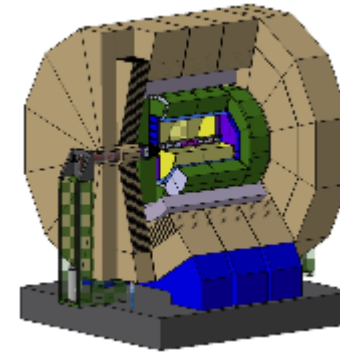
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International Linear Collider

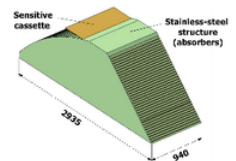
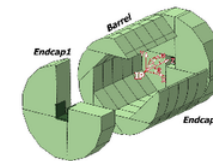
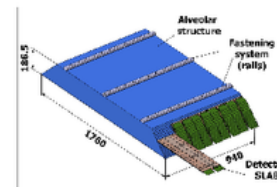
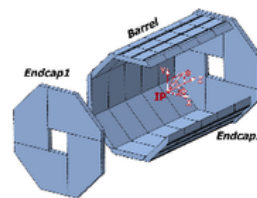
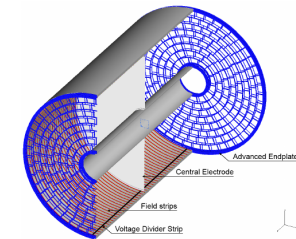
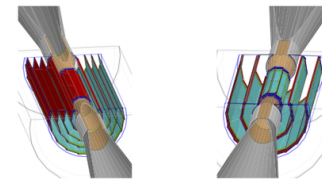
two detectors proposed:

- ILD (International Large Detector) and
- SiD (Silicon Detector)



8 French labs participate in ILD:

- vertex detector,
- TPC,
- Silicon-W ECAL and
- Semi-Digital HCAL
(plus accelerator R&D)



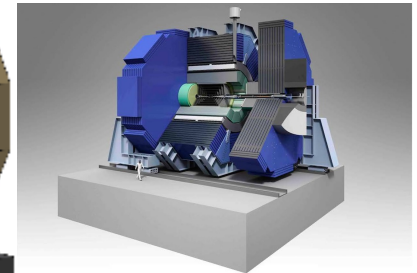
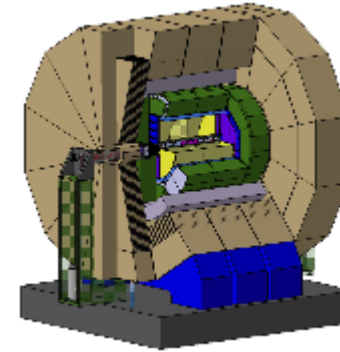
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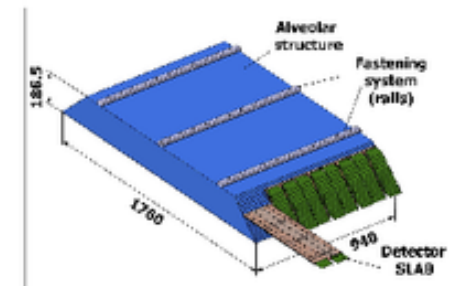
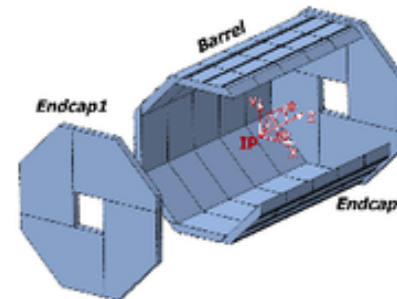
two detectors proposed:

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8 French labs participate in ILD:

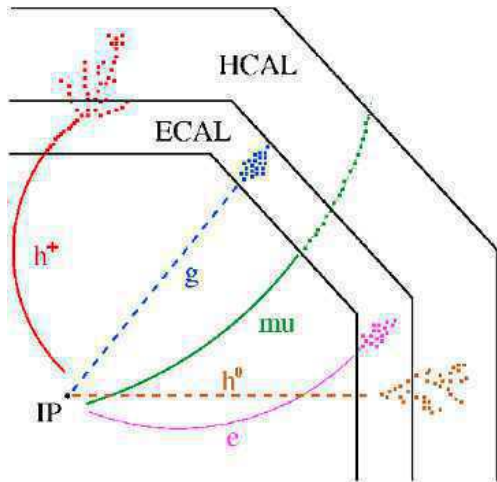
- vertex detector,
- TPC,
- Silicon-W ECAL and
- Semi-Digital HCAL
(plus accelerator R&D)



SiW ILD ECAL:

- Omega group, LLR, LAL, LPNHE and LPSC in France
- Tokyo and Kyushu Universities in Japan

Particle Flow Algorithm (PFA) in calorimetry

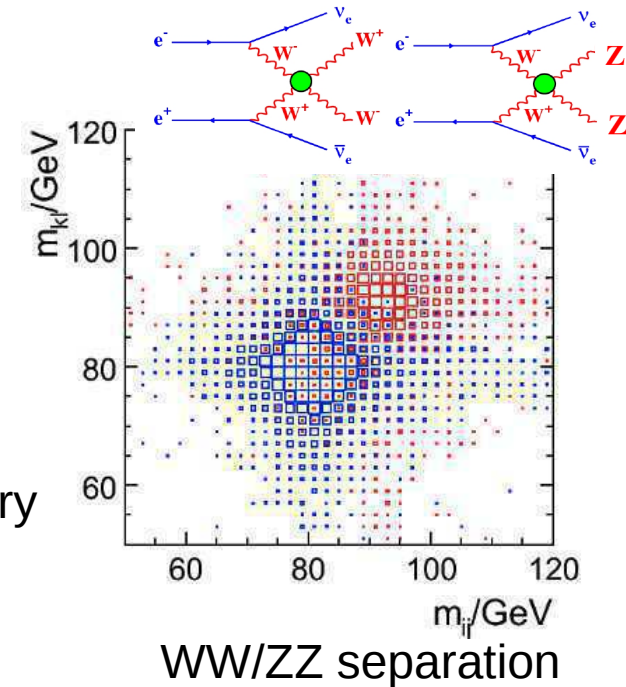


Particle Flow Algorithm:

Jet = 65% charged + 25% γ + 10% h_0
 Tracker ECAL HCAL

$$\sigma E/E (\text{jet}) = 3\text{...}4\%$$

about **twice better** than traditional calorimetry



– High granularity “imaging” calorimetry is needed to match CAL clusters to tracks. Especially important in ECAL (resolve narrow e-m showers and distinguish them from hadron interactions)

Best granularity with silicon detector (eg. 5x5 mm² pixels, 100 M channels). Also: perfect linearity, easy calibration, time stability, robustness, thus low systematics.

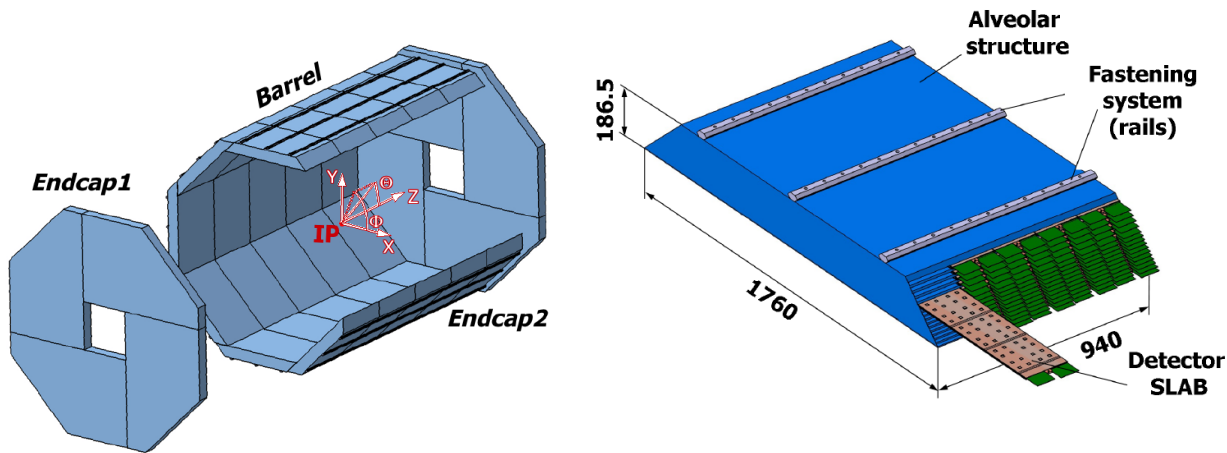
– To avoid overlaps of electromagnetic showers with themselves or with hadronic showers: small Moliere radius and large interaction / radiation length ratio, select tungsten (W) as absorber (140 t)

Moderate energy resolution $\sigma E/E = 0.17/\sqrt{E} \oplus 0.01$ is sufficient for jets, since HCAL uncertainty dominates.

Silicon-tungsten calorimetry

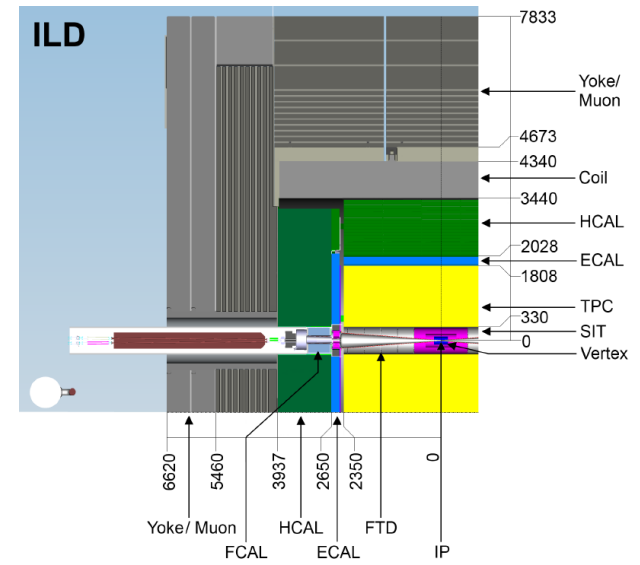
SiW ECAL in ILD:

- TDR: 2600 m² of Si, 140 t W, ≈20 cm thickness
- modular design (eg. barrel = 8x5 modules, each with 5x15 slabs), no projective cracks
- power pulsing (ON during ILC bunch trains, 1%)

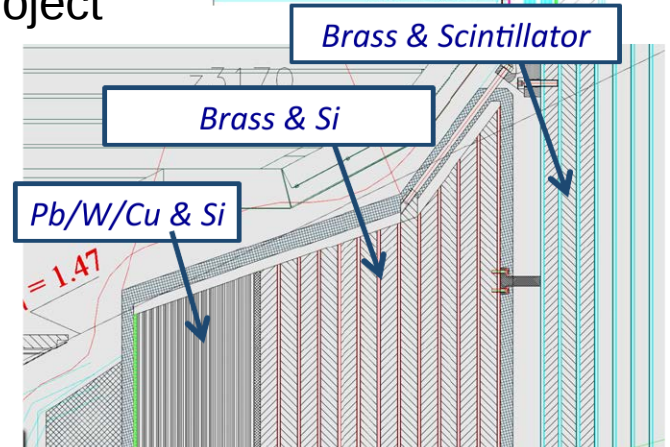
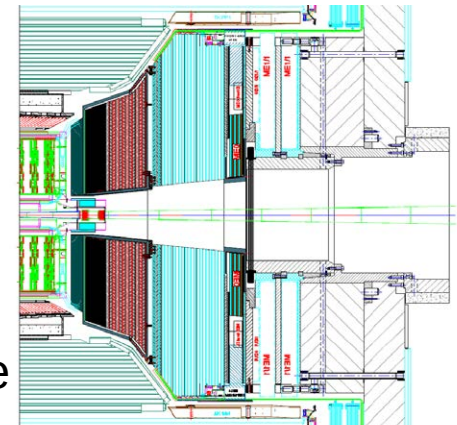


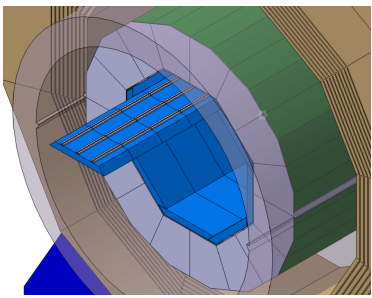
Recent interest to Si-W(Pb) technology for CMS endcap Phase 2 upgrade (HGCal) and for circular collider projects (TLEP, CEPC).

Technology choice between HGCal and shashlyk in CMS in spring 2015. Operation starts around 2025.

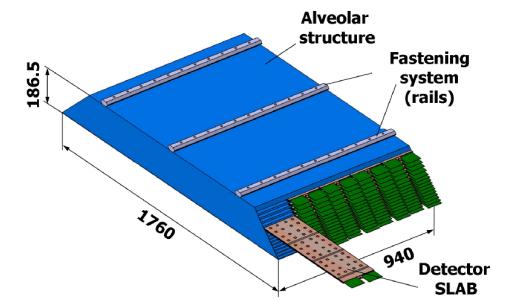


CMS HGCal endcap upgrade project



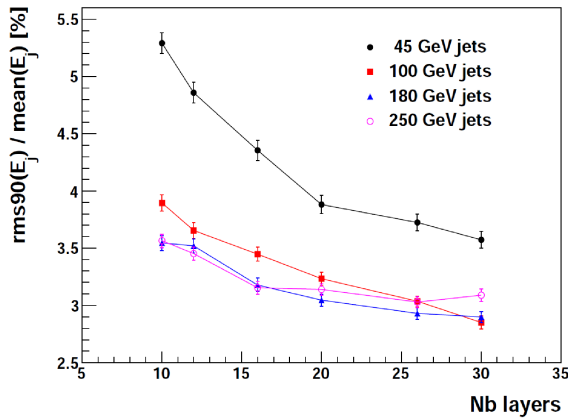


On-going cost / performance optimization of ILD ECAL

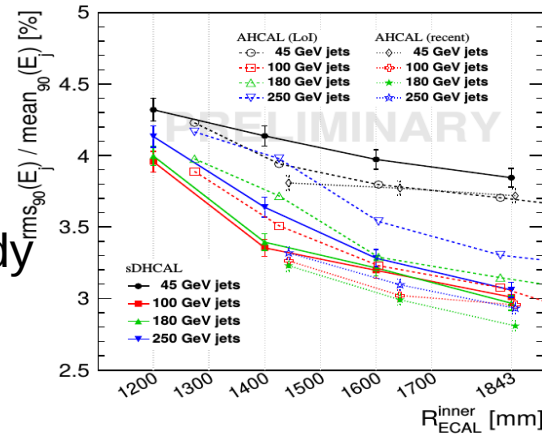


– Jet energy resolution dependence on N ECAL layers,

dimensions



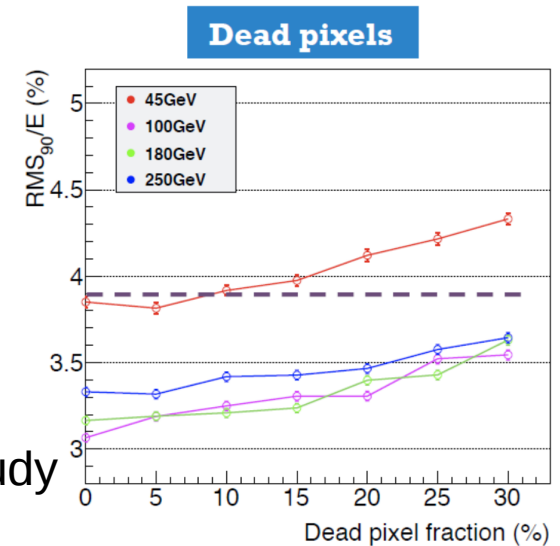
LLR study



eg. $R=1843 \rightarrow 1500$, N layers = 29 \rightarrow 25 reduces the ECAL cost by about 40%

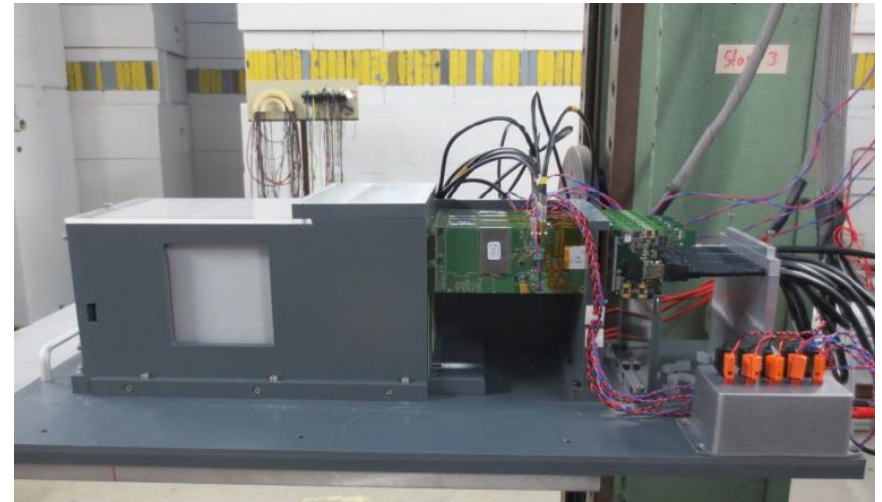
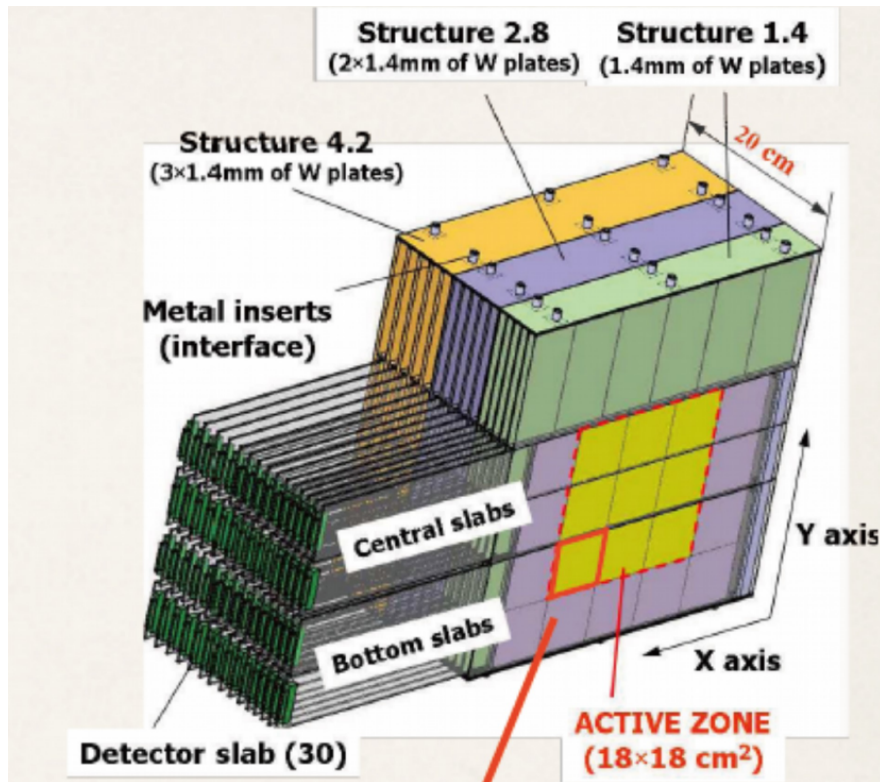
– 10% of bad pixels is affordable (not tracker device), lower price

Tokyo study



Physical prototype: 2005-2011

Technological prototype: present



Conceptual proof of PFA,
verification of MC

10x10 mm², 30 layers
Electronics outside

$\sigma E/E = 16.6\%/\sqrt{E} \oplus 1.1\%$,
linearity within 1%.

Embedded electronics

Assess feasibility, choose and finalize
design, prepare mass production

SKIROC 2 chip: autotrigger, power pulsed
(gives higher noises at acceptable level)
channel-wise zero suppression is planned
for SKIROC 3.

Charge injection + cosmic + laser tests,
4 TB @DESY 1-5 GeV e⁻ in 2012-2013.

Silicon sensors

Hamamatsu (HPK) offer in 2013: 31000 Yen per 98x98 mm² sensor or 2.54 EUR/cm², full ILD ECAL production.

This price is the same as in DBD (3 ILCU/cm²)

Silicon contributes ≈45% to SiW ECAL price

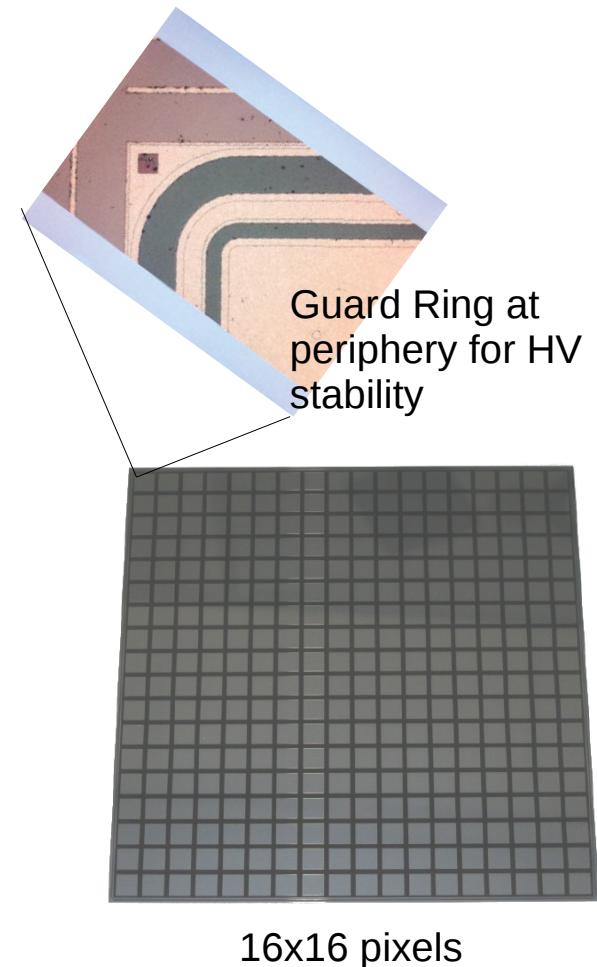
Sensor is made from 6" raw wafers, for sensor thicknesses 300 – 500 μm the price is the same (but 500 μm gives 8% better resolution), for 650 μm it is 10-15% higher

Lfoundry in Europe: 8" wafers, 700 μm, first test production is planned to evaluate quality.

Constraint on ECAL dimensions, optimally:

$N * \text{sensor length} + \text{all inter-wafer gaps}$

Guard Ring(s) (GR) at periphery ensures HV stability and low dark currents. R&D is on-going to reduce capacitive x-talk between GR and boundary pixels. HPK produced sensors with different GR designs with 0,1,2,4 segments.

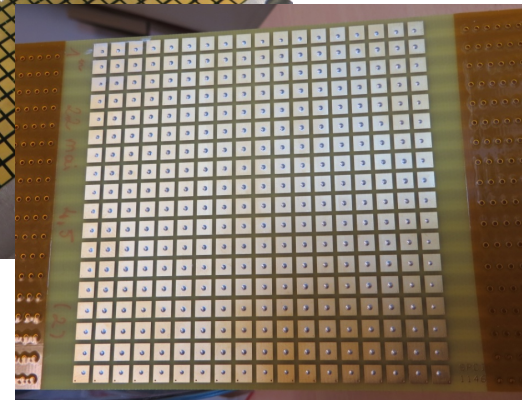
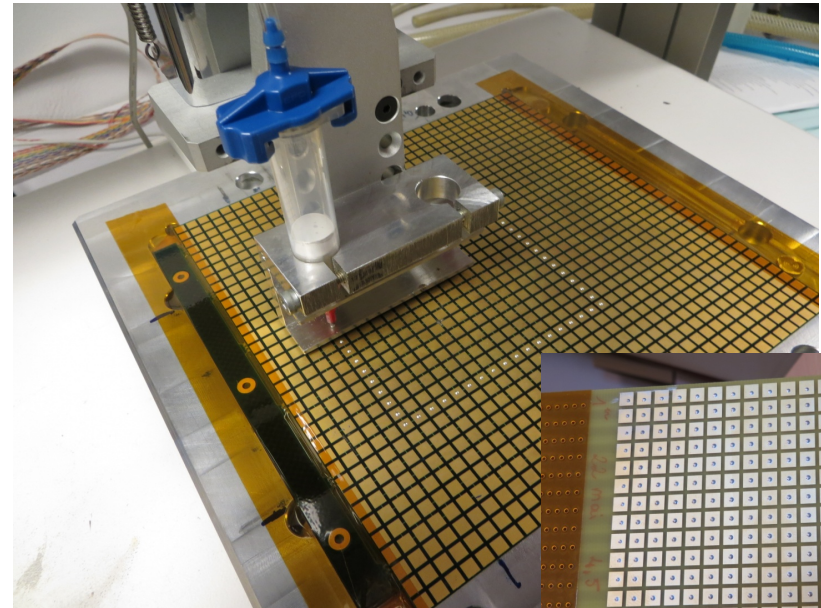


Gluing silicon sensors to FEV PCB at LPNHE

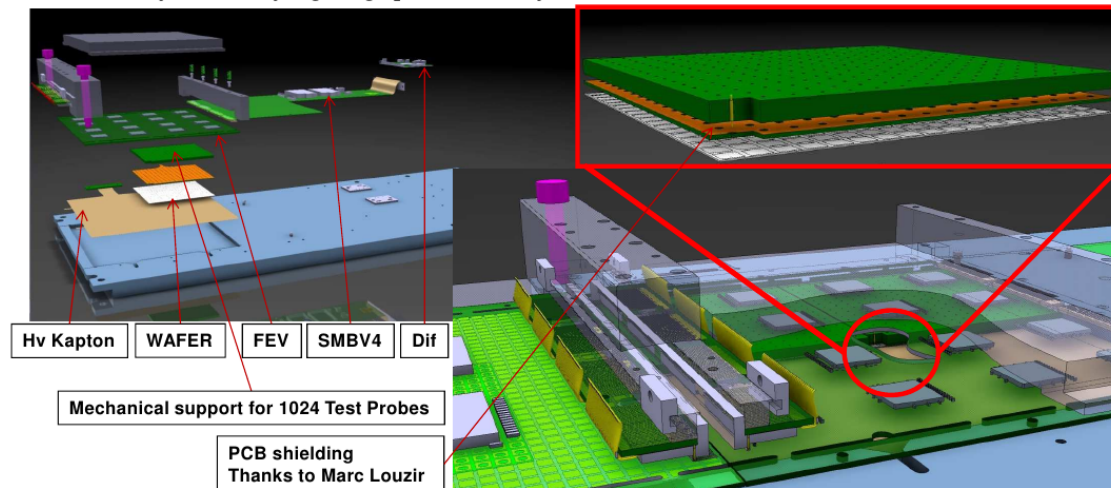
Gluing robot was successfully used to glue 9 sensors to 9 PCBs of technological prototype.

Next steps:

- combine gluing and positioning robots,
- glue 4 sensors to one PCB (already tested with 4 glass plates instead of sensors)
- move to clean room
- formalize all procedures (transportation, verification tests) for mass production

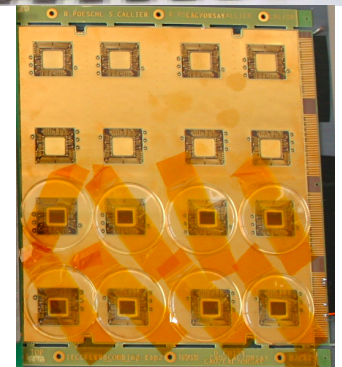
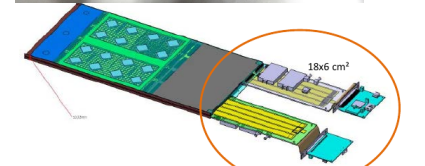
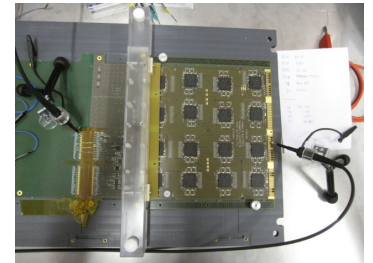
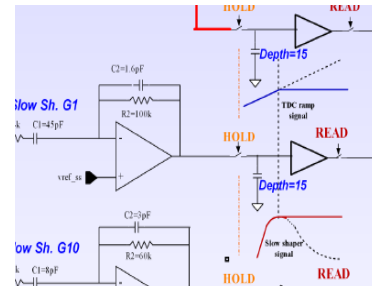


To test sensors before gluing: new setup with 1024 spring contacts (without neither glue nor soldering)



DAQ electronics

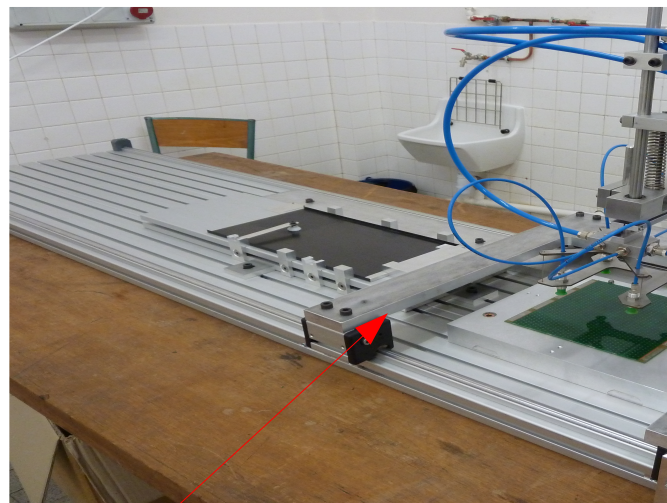
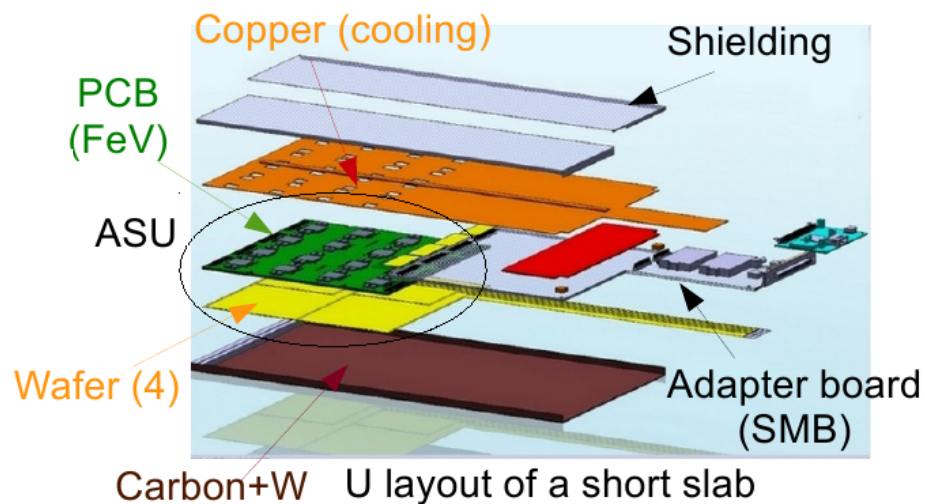
1. **FE chip SKIROC2** developed by Omega (Ecole polytechnique)
1-1500 MIPs, S/N=10–20 (@ MIP).
Power pulsing successfully tested in 2013
New BGA packaging, 1.1 mm thick + 1.6mm PCB
New chip production with bug fixes in fall 2014
2.
 - a) **PCB with sensors and FE chips** (FEV9,10,11)
New design, QFP->BGA chip packaging, x4 channels (as in ILD), many improvements this year, goal: industrial mass production. FEV9-11 are produced. Readout of all channels in FEV9 is tested.
 - b) **clock + voltage distribution** (SMB4), serves 1 -> 8 FEVs
Designed, produced, not yet tested
 - c) **Detector Interface (DIF) board**, improved firmware
 - d) **Gigabit Data Concentrator Card (GDCC)** sending data to PC
Working version in spring'13, continuously improved.
No packet losses any more.
3. **Chip-on-board PCB (FEV8)** version (very thin: 1.2–1.5 mm incl. chip), Korean SKKU/EOS company. Flatness is not yet sufficient for gluing Si. May be improved: new production in Jul'14
4. **Omega SKIROC test board** (Kyushu) with analog+digi outputs; summer 2014: QFP->BGA packaging, possibility to connect DIF or old FPGA



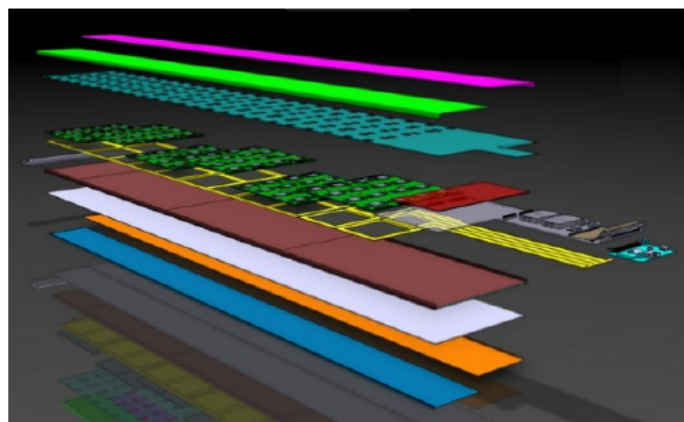
Putting all together: slab assembly

ILD goal: mount several interconnected square FE PCBs (up to 8 in barrel), each with 4 sensors, along long slab. First short slab(s) with 1 PCB: in the end of this year.

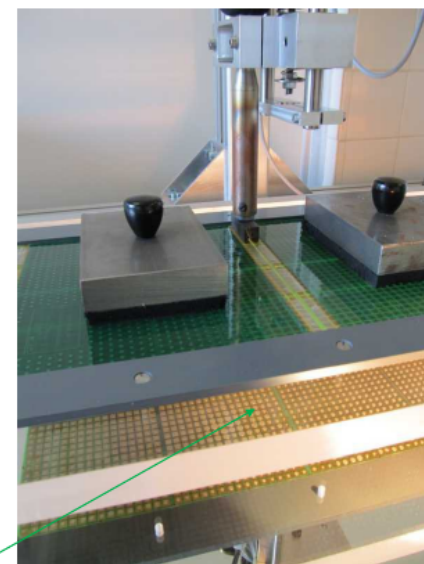
Several assembly benches are built or will be improved



Flexible suspension for exact PCB positioning



Pressure test

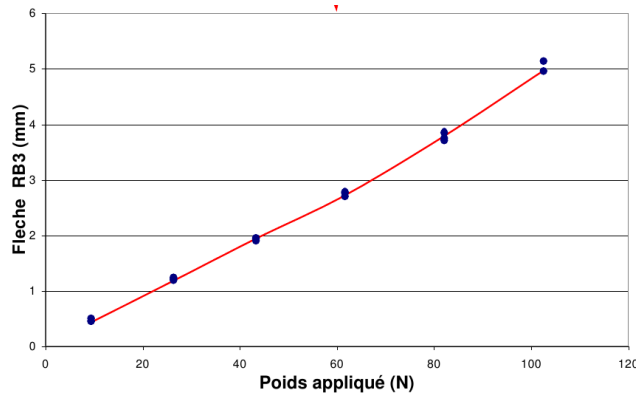
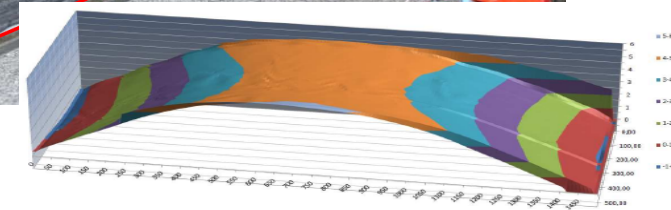
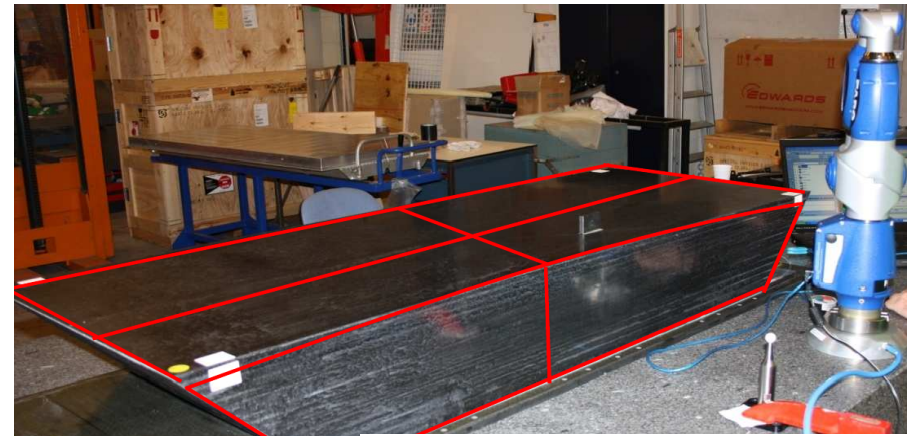


Mirrored PCB image

Mechanical modules with alveoli (common to Si and Sc)

Big prototype with 15 alveoli has been built:
3/5 of one ILD barrel module, ~600 kg.
Separately built layers of carbon fiber + W
“cooked” together.
Simulated mechanically & thermally.

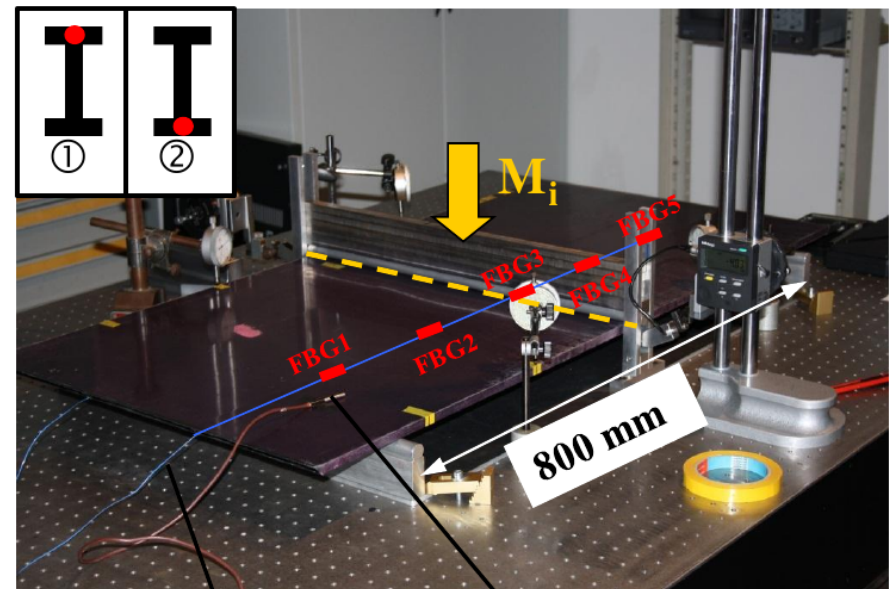
Another prototype with **molded Bragg grating fibers**, 2013. Detailed verification of simulated elongations under loads (by monitoring frequency shift of light reflected by fiber).



Vérification des paramètres du modèle en comparant la flèche FBG3 mesurée et simulée

Similar studies for **endcap and fastening rails**.
According to **thermal simulations**, only passive cooling is required inside alveoli.

Plan: produce H-shaped slab with W



Optical fiber

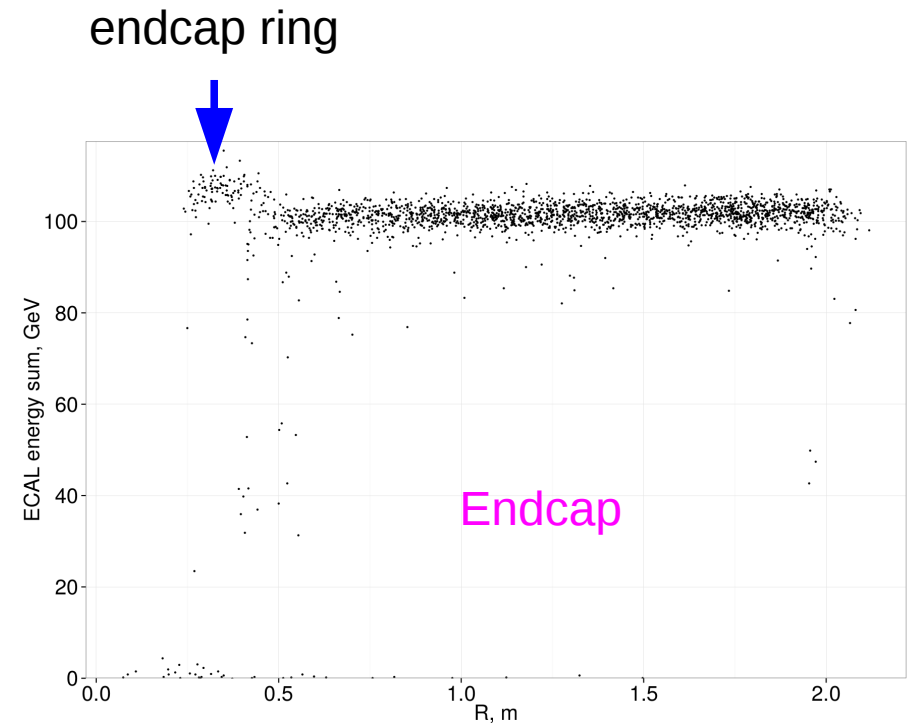
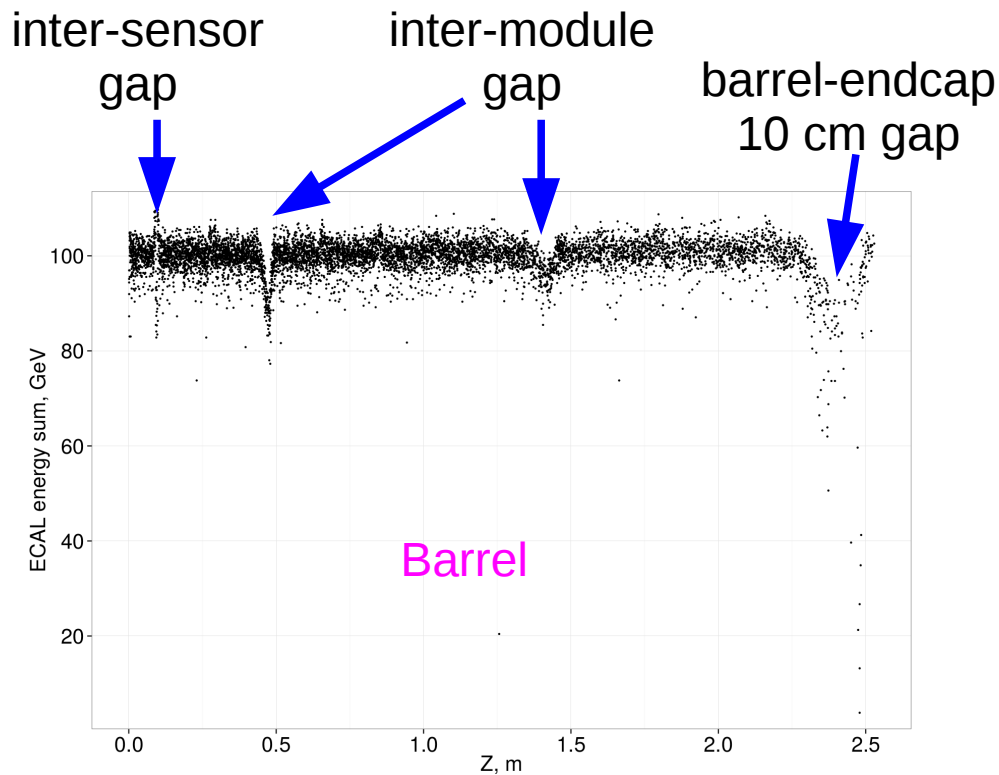
Thermal sensor

Participation of Ukrainian students

Iaroslava Bezshyiko – internship student from Kiev, 3 months in LLR in 2013,
Kostiantyn Shpak – PhD student in LLR (Ecole polytechnique + Kharkiv Uni), started
in beginning of 2014

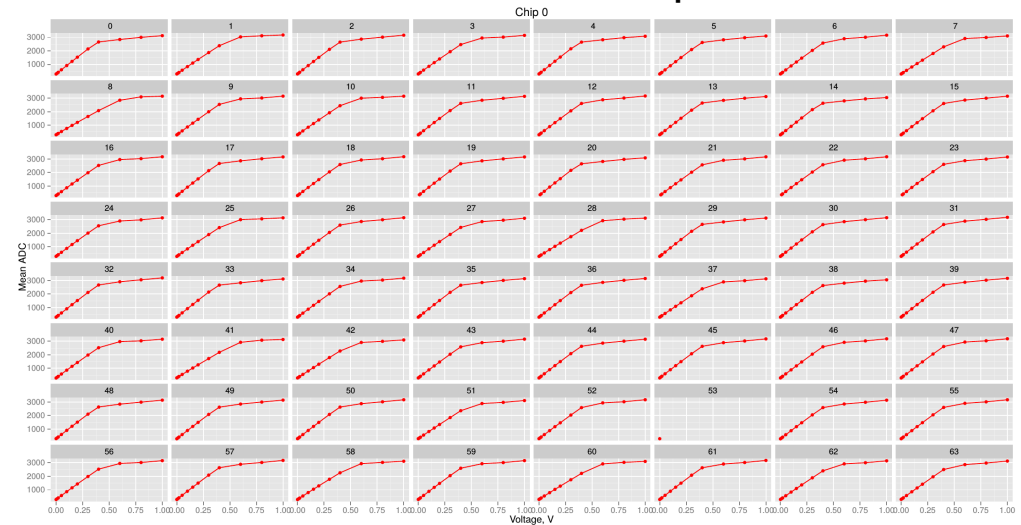
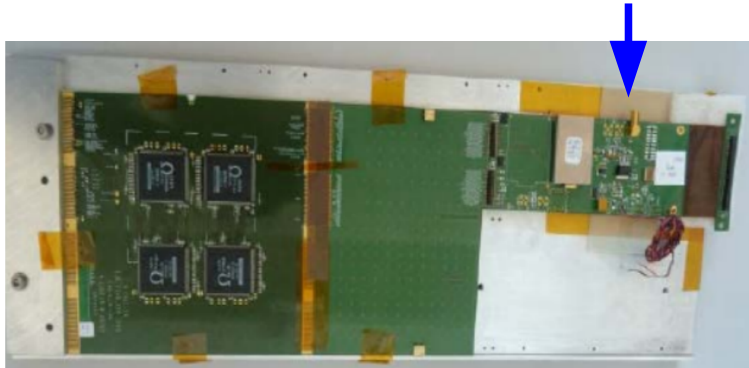
Iaroslava Bezshyiko (Kiev), analysis of ECAL photon energy resolution

Energy sum of all hits (below) or PFA Pandora program results, 1-100 GeV photons



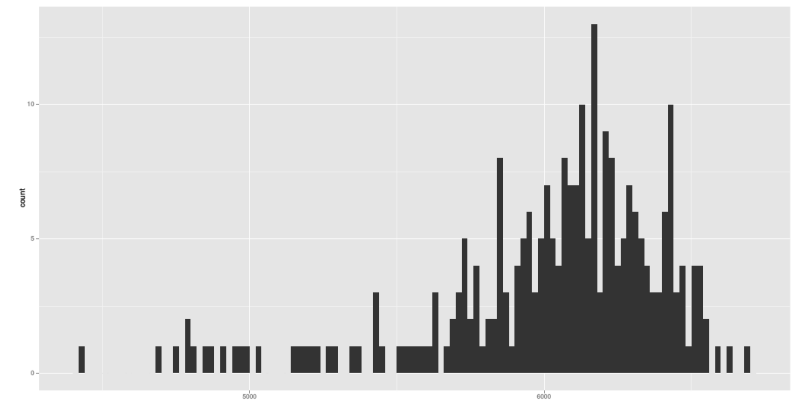
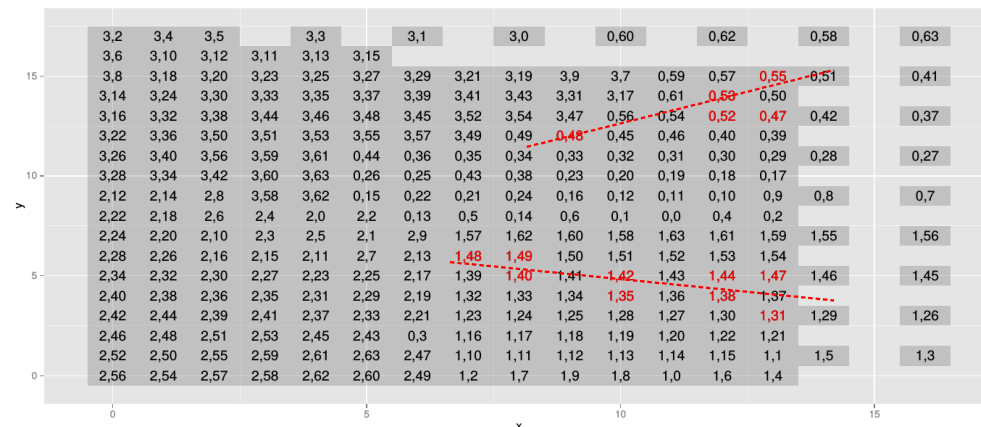
Kostiantyn Shpak (Kharkiv-Ecole polytechnique), analysis of Si technological prototype

Charge injection into front-end chips, 3 slabs X 256 channels X 11 amplitudes



RMS of linear slopes within chips 2,3	2...4%
RMS at saturation within chip	1...2%
Bad channels	5%

One chip example

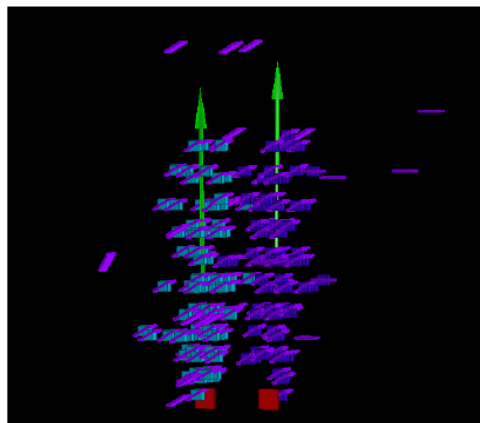


Linear slopes, tails due to chips 0,1 with bad areas

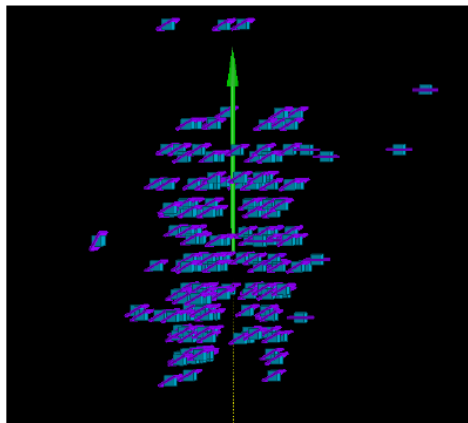
(chip, channel): X-Y position on PCB, red is bad

K. Shpak (Ecole polytechnique-Kharkiv), physical prototype capability to separate showers

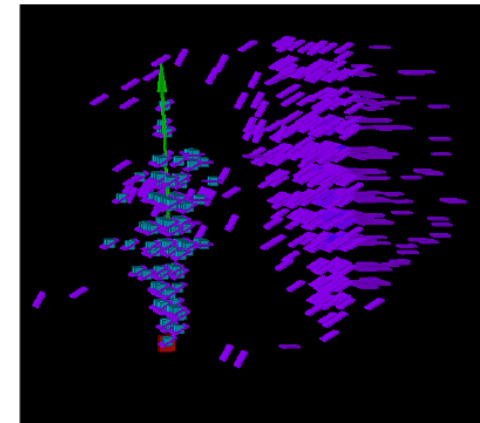
FNAL'2011 data, overlay two single-positron events or positron – hadron and study separation power of several programs: Garlic, Pandora, Arbor. Crucial for PFA.



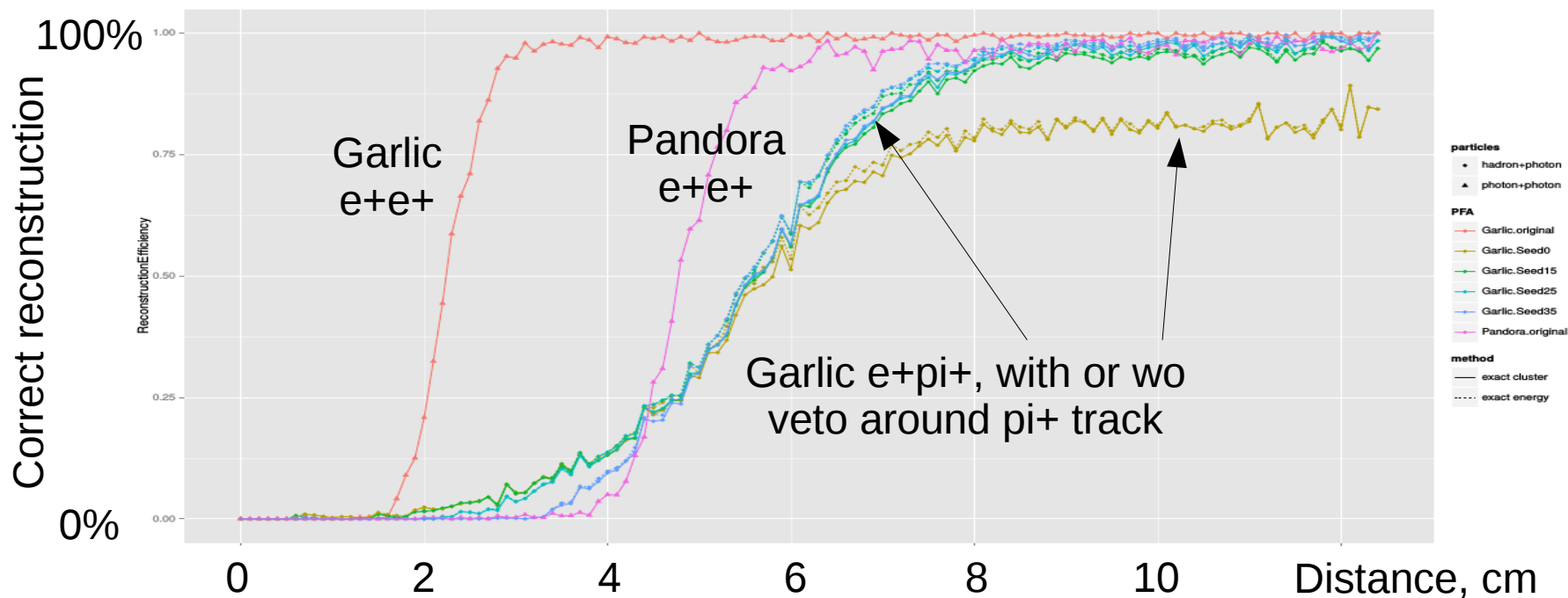
Two e^+ reconstructed showers in GARLIC



Merged e^+e^+ shower in Pandora



EM (left) and hadron (right) showers in GARLIC



Conclusions

Status: Silicon-Tungsten ECAL for ILD is well advanced.

Advantages: the best granularity (5x5 mm²) for PFA, perfect linearity, easy calibration, time stability, robustness, so low systematics.

Plans:

1. Finalize **optimization** (geometry, Si sensor, GR, electronics, mechanics, cooling)
2.
 - a) Test **new electronics** (FEV11 / SMB4 / GDCC) and software
 - b) Produce short and long slabs
 - c) Extend technological processes towards mass production
3. Recent significant reduction of Si sensor price: 2.5 EUR / cm² offer from Hamamatsu.

Recent interest to Si ECAL technology from **future circular colliders** TLEP/CEPC and **CMS endcap calorimetry** Phase 2 upgrade project, HGICAL. Decision on HGICAL or shashlyk by spring 2015.

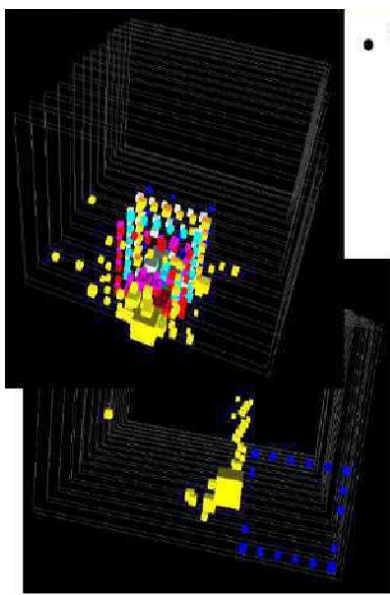
Backup slides

DAQ software

1. Version 2 of PYRAME, generic DAQ framework, is released this month
 - multiple acquisition PCs
 - hierarchical configuration, dumped at each run (XML)
 - C++ or python
 - many improvements

Previous version with specialized SiW ECAL drivers has been used to take all technological prototype data since Jan'2013.

2. Kyushu team develops
 - combined DAQ for Si and Sc ECAL based on EUDAQ
 - online monitor

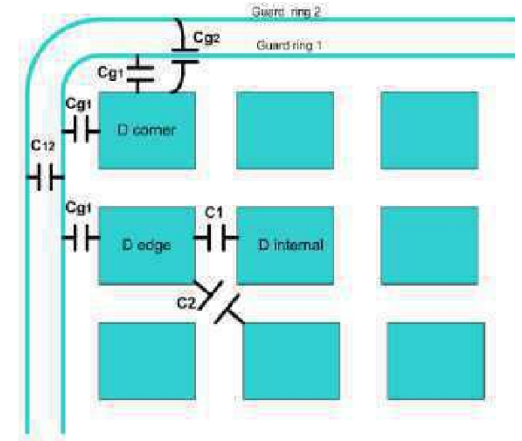


Physical prototype TB "square" event display

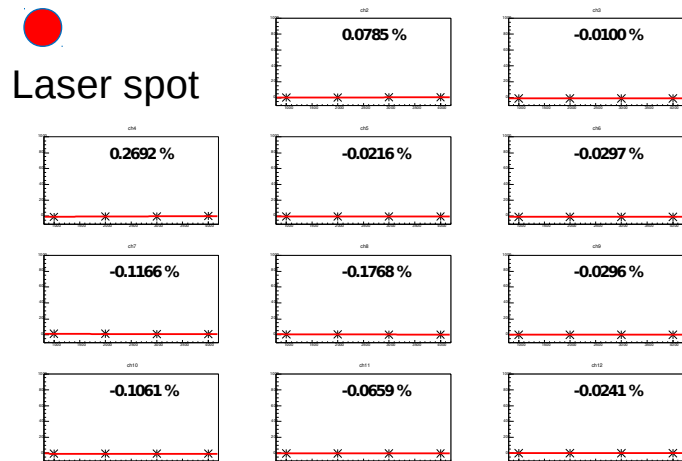
"Square" events

... explained by capacitive coupling of boundary pixels to guard ring

Capacitive coupling is minimized either by segmenting GR or avoiding it.



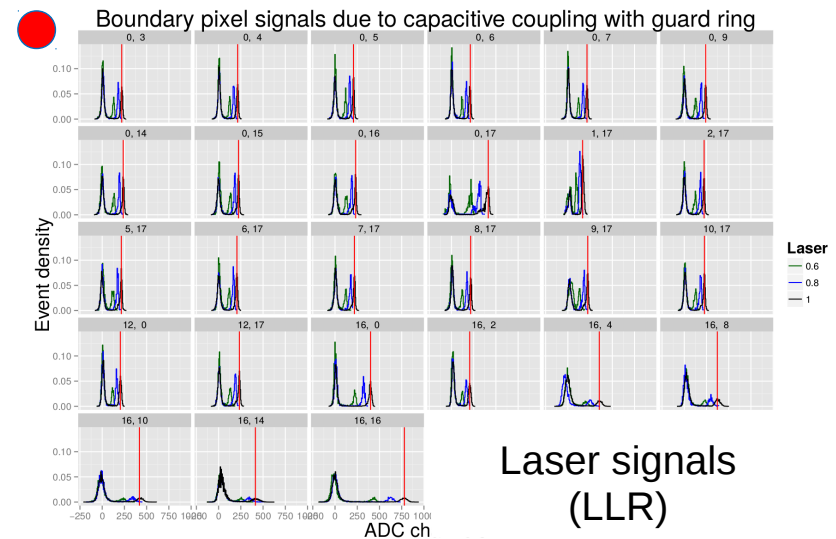
Preliminary results of recent studies using high signals at GR induced by **infrared laser light**: GR segmentation or no GR design significantly reduces xtalk, it remains at the level $O(1e-3)$.



no GR, small 4x4 pixels sensor, xtalk $\leq 0.1\%$ except one pixel

HPK also produced sensors with meshed electrodes which allow laser light injection inside pixels.

Plan: test more sensors with various designs, possibly using upgraded DAQ electronics



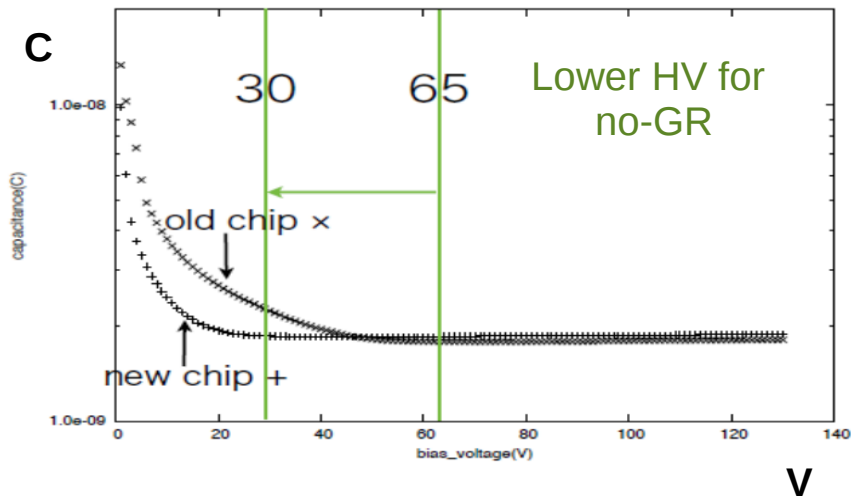
2 segments GR, xtalk = 0.4-0.5% per outer pixel side.

Silicon sensor tests

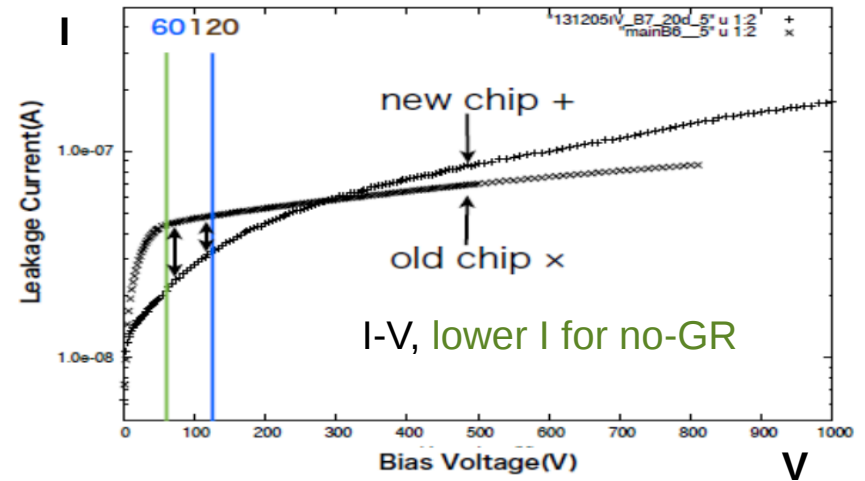
I-V and C-V tests (current and capacitance vs HV) of different Hamamatsu designs with 0,1,2,4 GR.

Recently: no-GR design is very promising

Plan: test more sensors



The leakage current at 120 V is 31nA (old : 48nA),
at 60 V is 21nA.



Irradiation tests at nuclear reactor are planned for sensors and super-capacitors (used for power-pulsing LV electronics)