

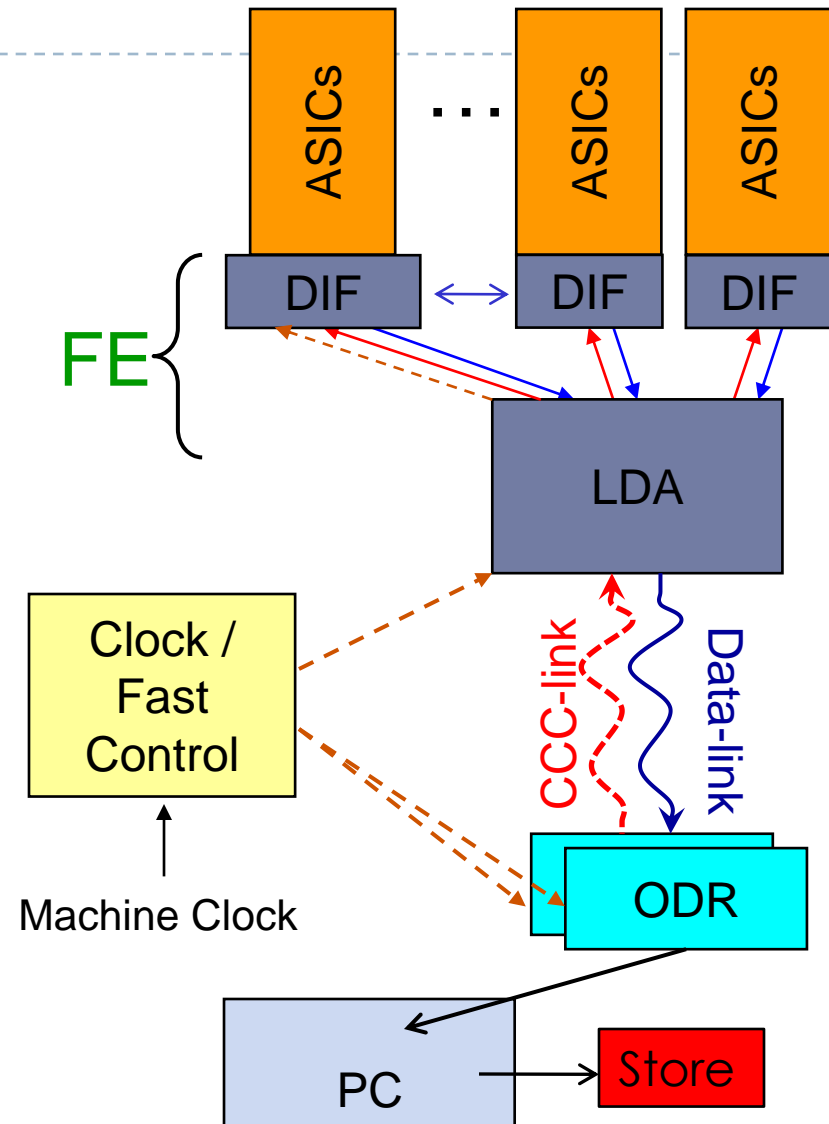
DIF → LDA Interface

David Bailey

Current Architecture

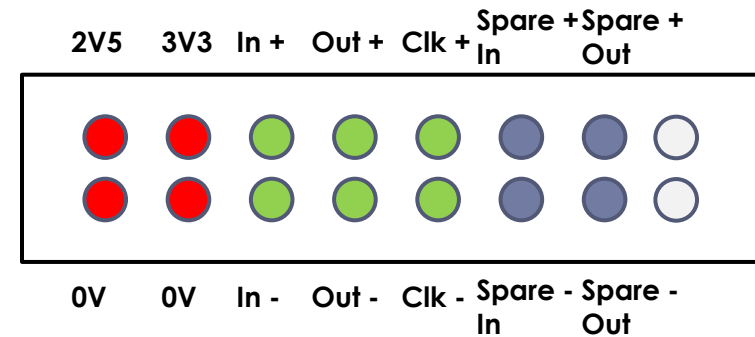
▶ DIF

- ▶ Supplied with low jitter clock from LDA
 - ▶ 50MHz with $\frac{1}{2}$ ns jitter (for now)
 - ▶ All detector-specific clocks are derived from input master clock on the DIF
- ▶ Bi-directional serial links to LDA
 - ▶ Would like these to be “generic” – driven by highest bandwidth requirement
 - ▶ Require fixed latency links if clock and control encoded across them
- ▶ Clock feed through and redundant data links to neighbouring DIF for readout and clock redundancy
- ▶ Standard firmware to talk to DAQ



Current Architecture

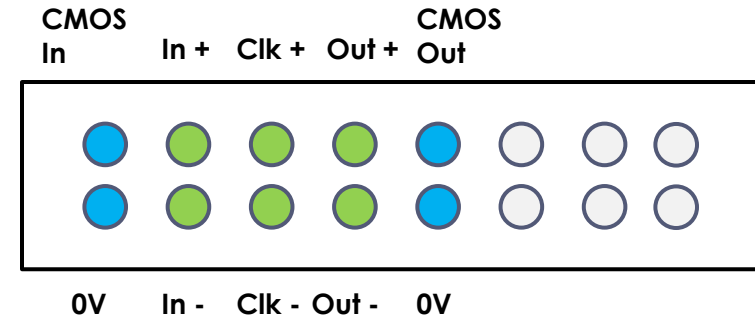
- ▶ DIF → LDA Interface
 - ▶ Keep it simple
 - ▶ Standard 10/16 pin IDC format connector
 - ▶ Power from DIF for link SERDES if required (3V3 and 2V5 at 250mA)
 - ▶ Input from/to LDA
 - Serial In
 - Serial Out
 - Clock In (may be recovered from link)
 - 2 spares (sync signal?)
 - All LVDS 2V5
 - 8B10B encoding (or Manchester)



HDMI might be another option for this connector. We lose one of the spare pairs but get more control lines and connector is compact.

Current Architecture

- ▶ **DIF→DIF**
 - ▶ Same format as LDA interface
 - ▶ Used for redundant communications and clock between DIFs in case primary link to LDA fails
 - ▶ Require 2 extra single ended lines to specify link and clock direction
 - ▶ Master/Slave signal to define clock master
 - ▶ CMOS 2V5 suggested
 - ▶ Maybe use a single 3-state line later



Aim to make this a simple crossover cable connection if possible

Document

- ▶ Discussion document available
 - ▶ No final – might have been by next week but no time to finalise it this week...
 - ▶ Please read it!
 - ▶ Comments welcome
 - ▶ We will have to iterate again anyway to think about HDMI and possible opto/magneto isolation schemes on the LDA
 - ▶ Have some quotes from a company (Enterpoint) who could make the LVDS interface/drivers for LDA with or without isolation (arrived this morning)
 - ▶ Turnaround time is ~weeks, so (in principle) can get samples on short timescales