Questions to the setup of the SPIROC in the final ILC environment (+ DIF board concept)

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RamFull or SCAsat?: Do we need the RamFull Signal as DIF input for the SPIROC (AHCAL), or is the SCAsat sufficient? (What is the RamFull needed for?)

CK_40M?: How is the 40MHz clock used by the SPIROC? According to the manual, the 5MHz clock is used for acquisition and readout.

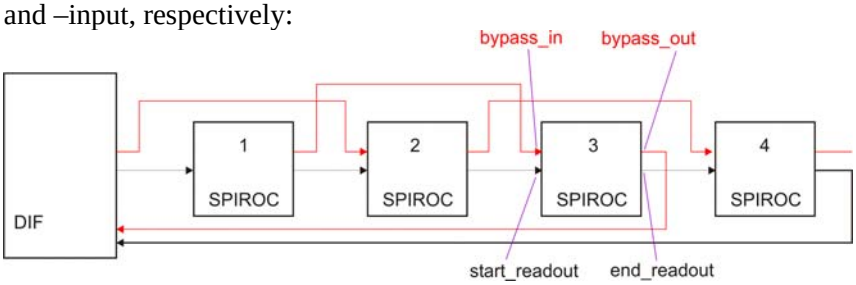
Power supply pins and (analogue) bias signals: There are a lot of ASIC Pins dedicated to power supply and analogue bias of the different stages. How many of these can be omitted in the final ASIC version? The aim could be to fit the number of pins to a smaller chip package, as the TQFP100.

Debug Signals: Which of these digital inputs (debug signals) should be accessible in the final setup from DIF?
Pin 115: hold_ext
Pin 116: trig_ext
Pin 159: digital_probe1
Pin 160: digital_probe2
Pin 179: holdb_backup
Pin 184: flag_tdc_ext
Pin 185: start_rampb_adc_ext
Pin 186: start_ramp_tdc_ext
Pin 235: sw_c15p

Combine Reset Signals: Is it ok to connect the reset signals to one global line ‘reset’ from the DIF? Or (better) will these be connected chip-internally in the final version?:
Pin 117: resetb_delay
Pin 118: resetb_read
Pin 118: resetb_read
Pin 152: resetb
Pin 164: resetb_probe
Pin 166: resetb_sc
Pin 180: resetb_pa

Combine Power-Down Signals: Is it ok to connect the power-on signals to one global line ‘pwr_on’ from the DIF? Or (better) will these be connected chip-internally in the final version?:
Pin 136: pwr_on_dac
Pin 137: pwr_on_adc
Pin 138: pwr_on_sca
Pin 139: pwr_on_a
Pin 142: pwr_on_d

Bypass of one SPIROC for the readout token: There is the possibility to bypass a SPIROC during a readout process by setting one bit in the slow-control (configuration) data. I am not sure if this is a sufficient protection against a broken readout chain, because I think one has to assume that it is impossible to load data into a broken chip. Therefore, we could consider the HELIX failsafe setup again, in which the chips before and behind the broken ASIC are programmed to use the bypass output and –input, respectively:



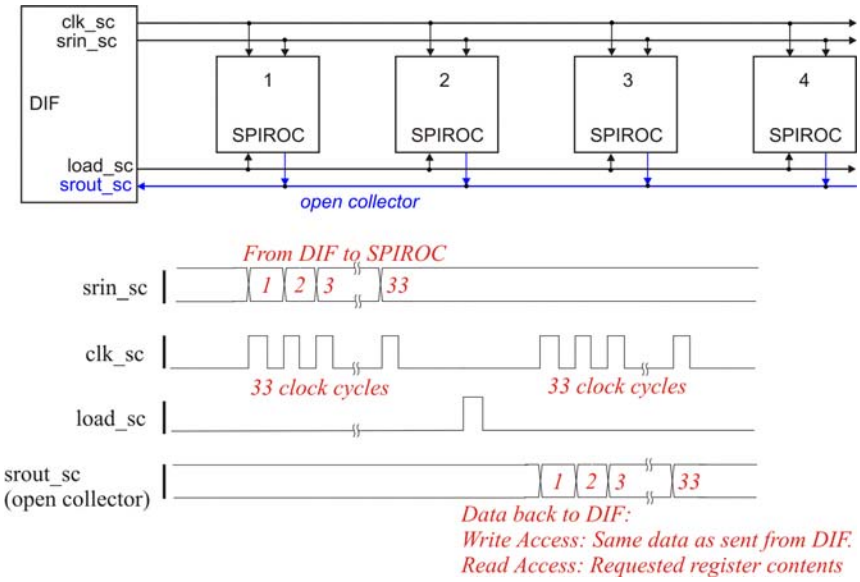
SRIN_READ for analog multiplexer only?: What is the task of the srin_read (Pin 120) and the respective output srout_read (Pin 133)? Is it used as for the current VFE ASIC to operate the analogue output multiplexer (now in front of the ADC inside the ASIC)? Do we need the srout_read pin connected to the DIF? This would be a lot ….

Slow-Control and Probe registers (+Chip-ID):
This question arose during the work on the DIF concept. At first, Bart Hommels and Maurice Goodrick asked on the CERN electronics meeting for a unique address of each VFE chip. Additionally, the configuration sequence is quite long (703 bits of slow control data and 939 probe bits per SPIROC). With up to 128 SPIROCs for the largest AHCAL layer, we don't have enough signal lines to connect each SPIROC with 3 separate lines to the DIF. So the SPIROCs would be in a slow-control chain with typically 24 chips length, resulting in almost 17k data for writing and 22.5k for reading. Reading back the data with the dedicated output would double the amount of data. With 1MHz clock rate only the readout would be 22.5ms (probe data), during which the SPIROC can not be powered down. In order to change single configuration bits, one would have to send the full sequence each time. Additionally, there is no possibility to verify if the bits arrive at all the SPIROCs correctly (only directly after the write access).

Therefore, I suggest thinking about an alternative setup with data frames and addresses for the slow-control data (again quite similar to the HELIX setup). Each SPIROC can have a 8-bit hardwired address, realized on the PCB by jumpers. Then the data could be sent to all SPIROCs in parallel in Slow Control Data Frames with e.g. a length of 33-bit:

<1-bit always '1'>< 8-bit ASIC identifier> <8-bit register identifier> <16-bit data>

On a rising load_sc signal, the ASIC interprets the identifiers and accepts the data if it is addressed. The first bit of the register identifier could define if it is a read- or write-access. See figure for the setup:



After a slow-control access, the addressed SPIROC sends back the data in additional 33 clock cycles to the DIF for verification, or for reading the requested data (read- or write access from DIF). In case of a write access, the SPIROC simply sends back the data it has received. The advantages of this setup are:

- one address could be used to send data to all SPIROCs, which allows a very quick configuration. E.g. the gain could be changed for all SPIROCs in a single access (66 clock cycles of clk_sc)
- configuration data can be read out at any time for verification, or if radiation induced bit-flips are suspected. This might be useful not only for debugging.
- accesses are small, so the SPIROCs can be changed in configuration every time between bunch trains (e.g. for calibration) without touching the DAC settings. The ASIC has to be switched on only for a short time, improving the power pulsing behaviour.

Of course, the setup also works with the long shift register chain, also concerning write time and read time for the probe registers. This is just an alternative, about I would like to ask you if it is worth to think about.