SOI Monolithic Pixel Detector Technology

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Le Laboratoire de l’Accélérateur Linéaire (LAL)@Orsay

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Outline

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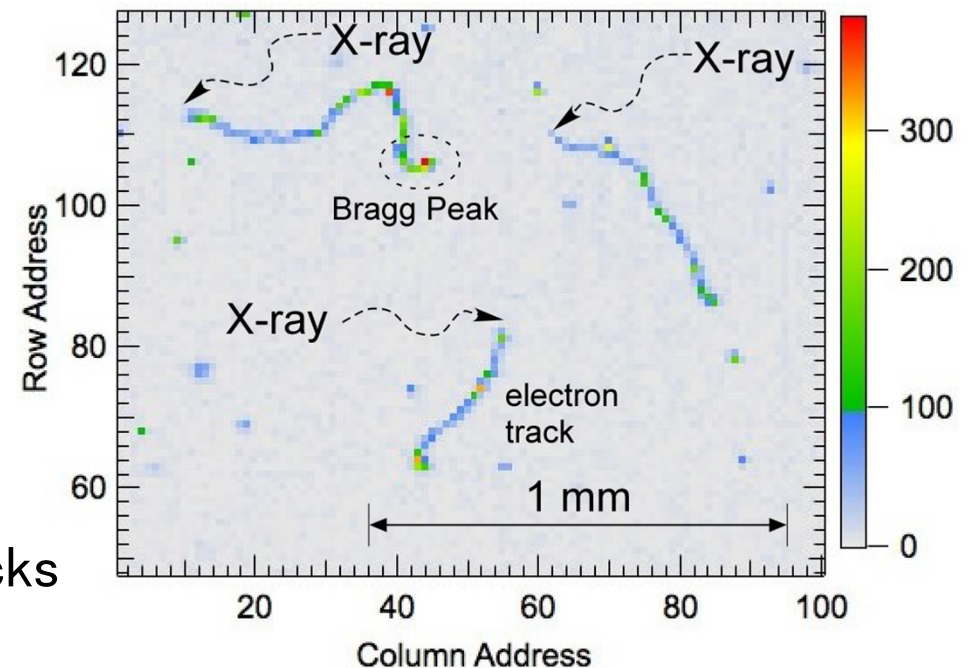
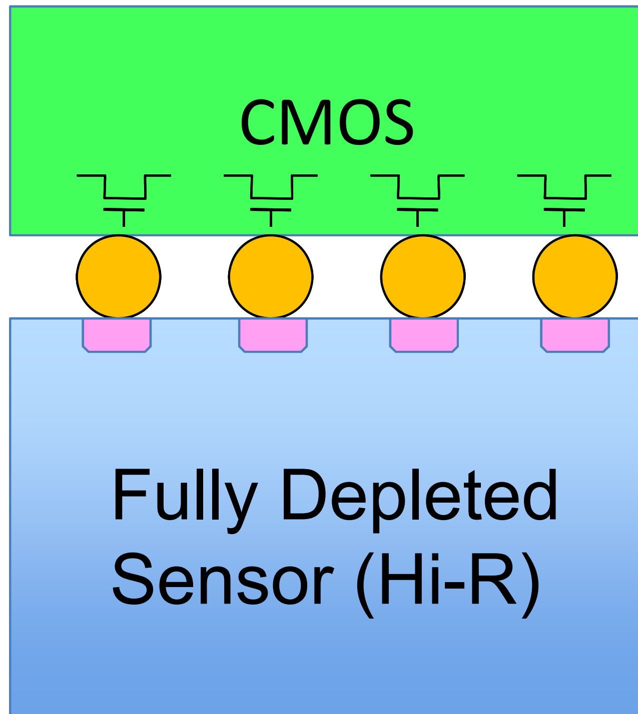
II. SOI Pixel Process
III. Detector Examples
IV. Summary



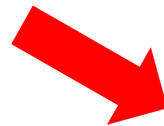
Compton Electrons Tracks

I. Introduction

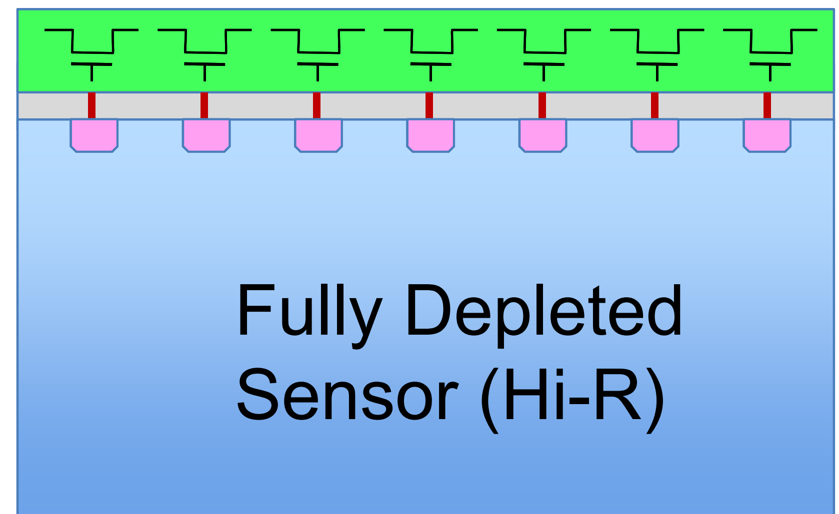
Hybrid Detector



Monolithic

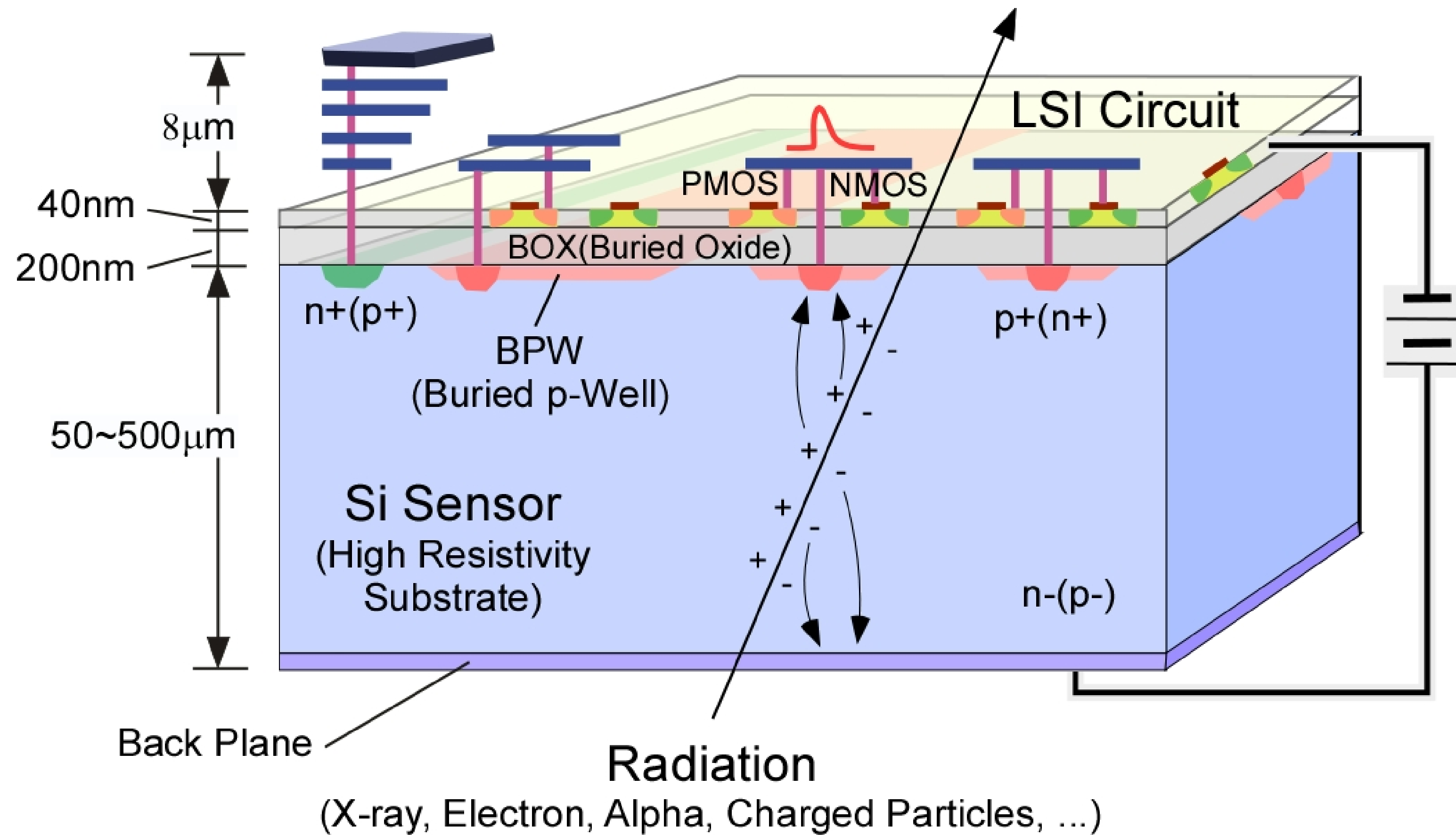


Silicon-On-Insulator (SOI)



SOI technology is a natural solution in the evolution of radiation pixel sensor.

Silicon-On-Insulator Pixel Detector (SOIPIX)



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.

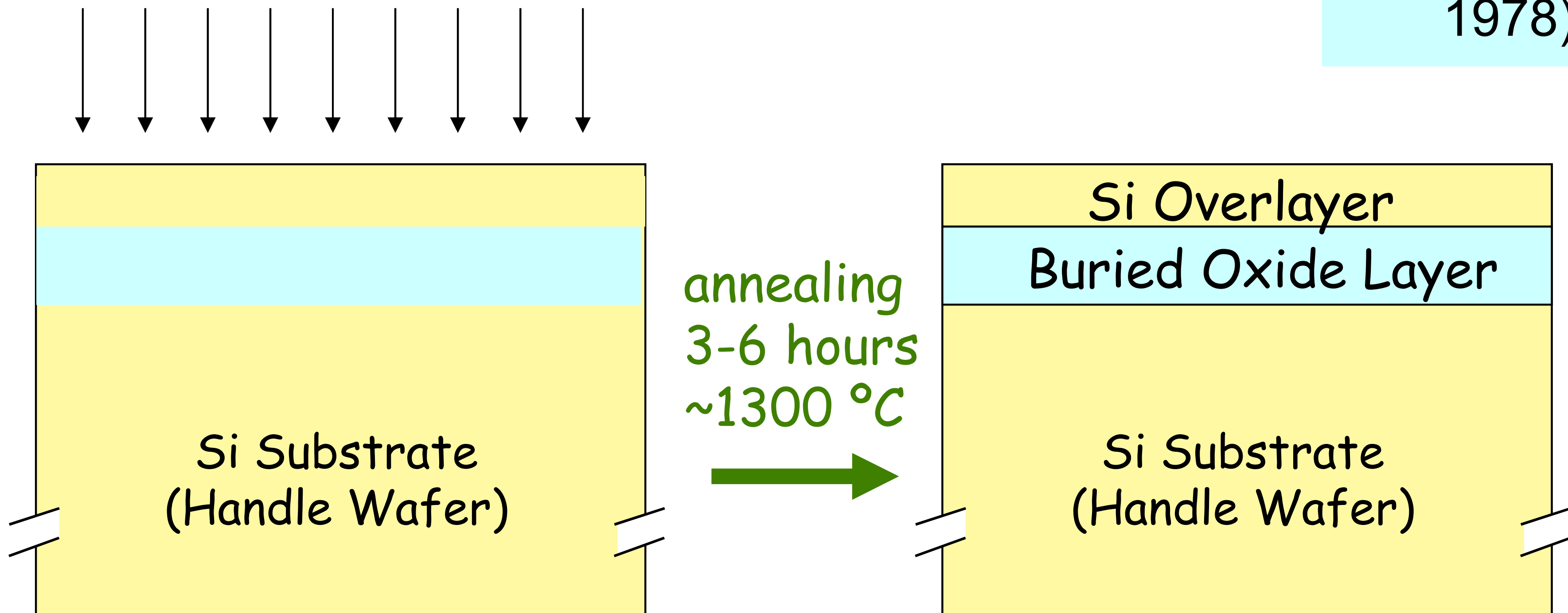
First SOI Wafer (SIMOX)

First good quality SOI wafer

SIMOX (Separation by Implanted Oxygen)

This took long implantation time of Oxygen, so the production cost was very high and applications are limited.

K. Izumi (NTT Japan, 1978)



Pesent SOI Wafer (SmartCut™)

Become popular after 2000. soitec

Michel. Bruel (Leti, 1991)

1_Initial silicon

2_Oxidation

3_Implantation

4_Cleaning and bonding

5_Splitting

6_Annealing and CMP touch polishing

7_Donor wafer becomes new wafer A

Layer Transfer

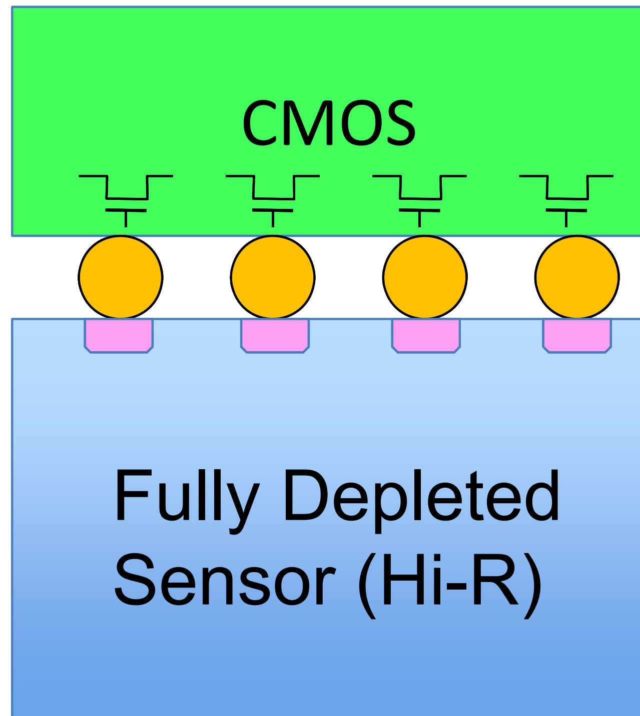
SOI wafer

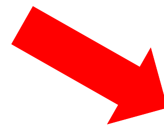
CMOS(Low R)

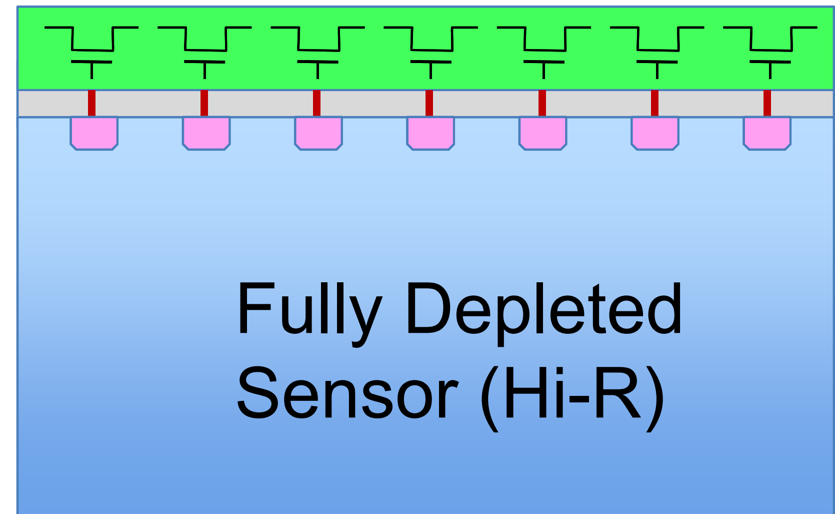
Sensor(High R)

(from SOITEC Web)

II. SOI Pixel Process



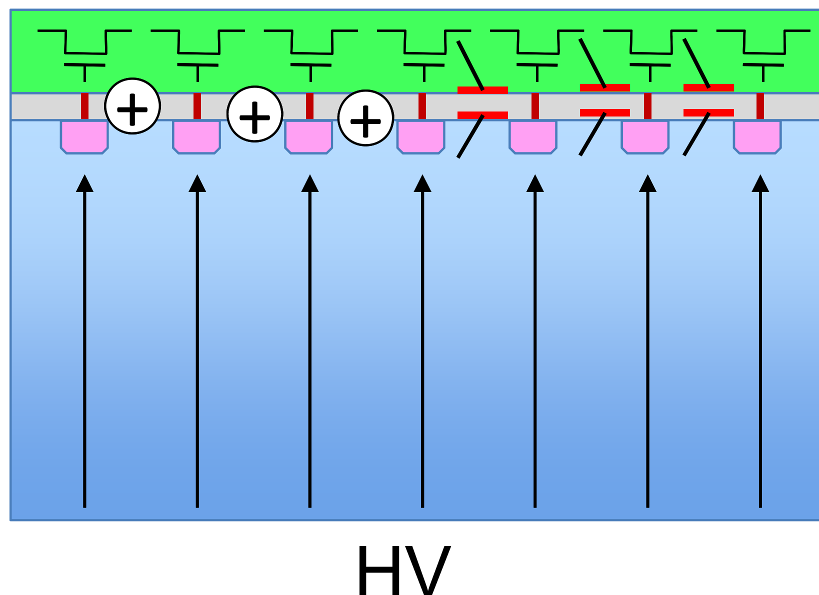




To use SOI technology for pixel detector is already discussed in 1990(*).

(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

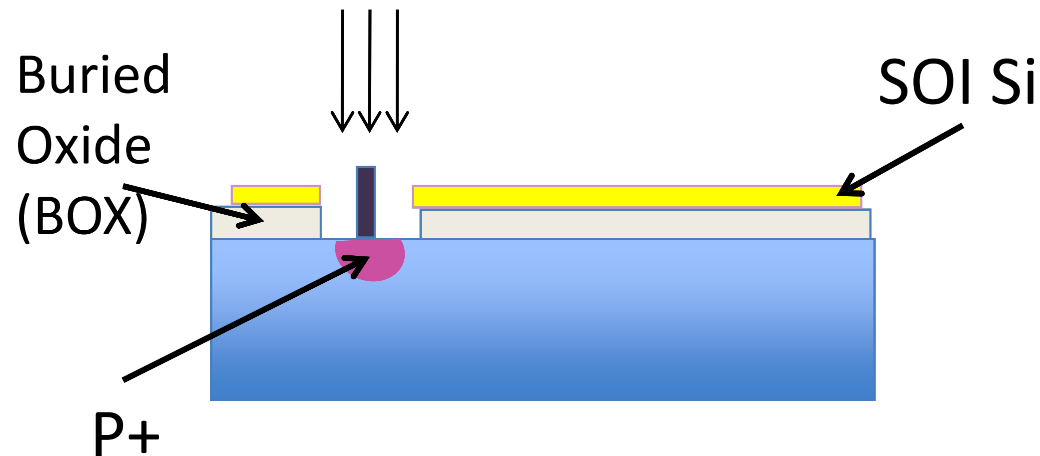
Issues in SOI Pixel

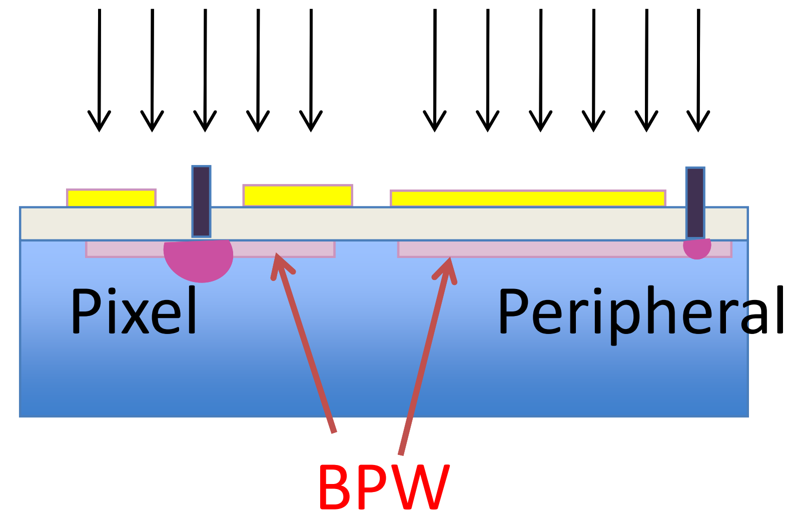


- Transistors does not work with Detector High Voltage.
  (Back-Gate Effect)
- Circuit signal and sense node couples.
  (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage.
  (Radiation Tolerance)

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc. , many SOI sensor R&D projects were stopped.

Buried p-Well (BPW)





- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

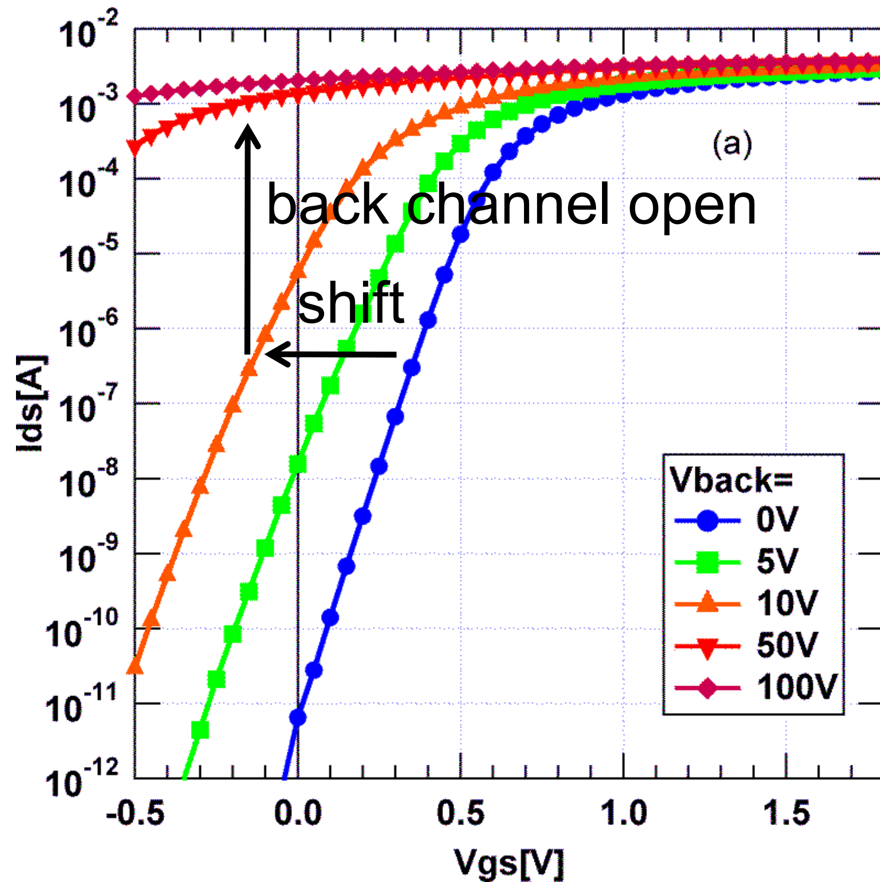
- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Reduce electric field in the BOX which improve radiation hardness.

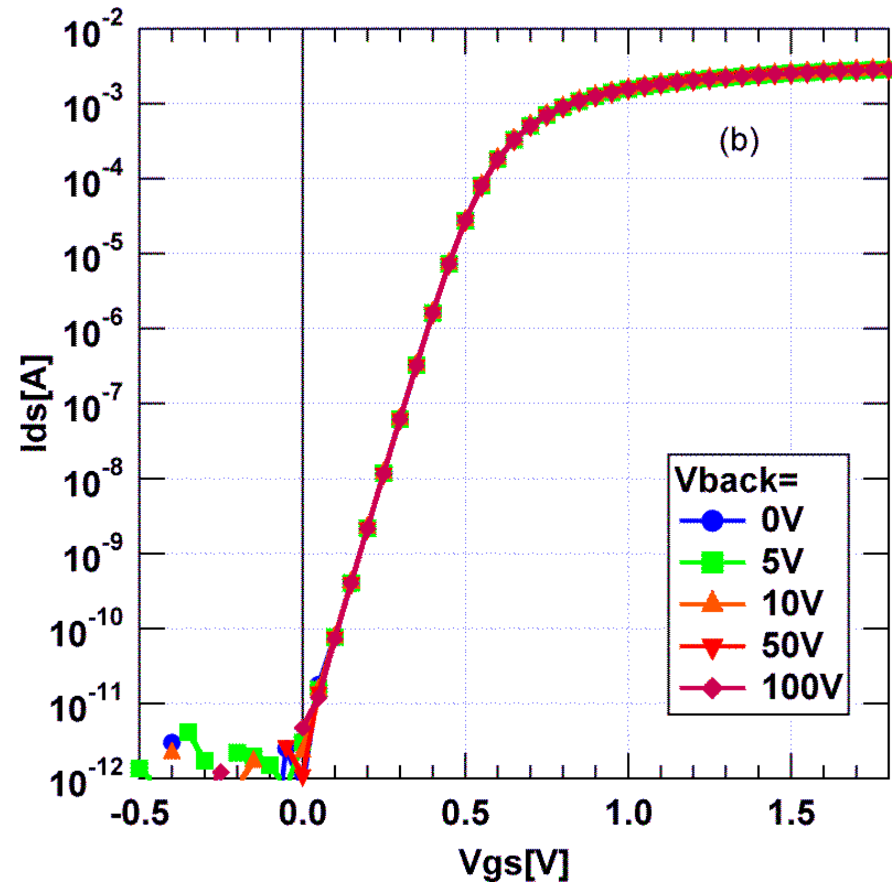
I_{ds}-V_{gs} and BPW

w/o BPW

with BPW=0V

NMOS





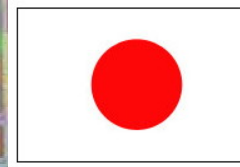
Back-gate effect is completely suppressed by the BPW.

Lapis Semi.(*) 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.

We operate Multi-Project Wafer (MPW) run. (1~2 times/year)



KEK

Shizuoka U.

JAXA/ISAS

RIKEN

Tohoku U.

Osaka U.

Hokkaido U.

Kyoto U.

Tsukuba U.

Kanazawa I.T.

AIST

IHEP China

AGH & IFJ, Krakow

Lawrence Berkeley Nat'l Lab.
Fermi Nat'l Accl. Lab.

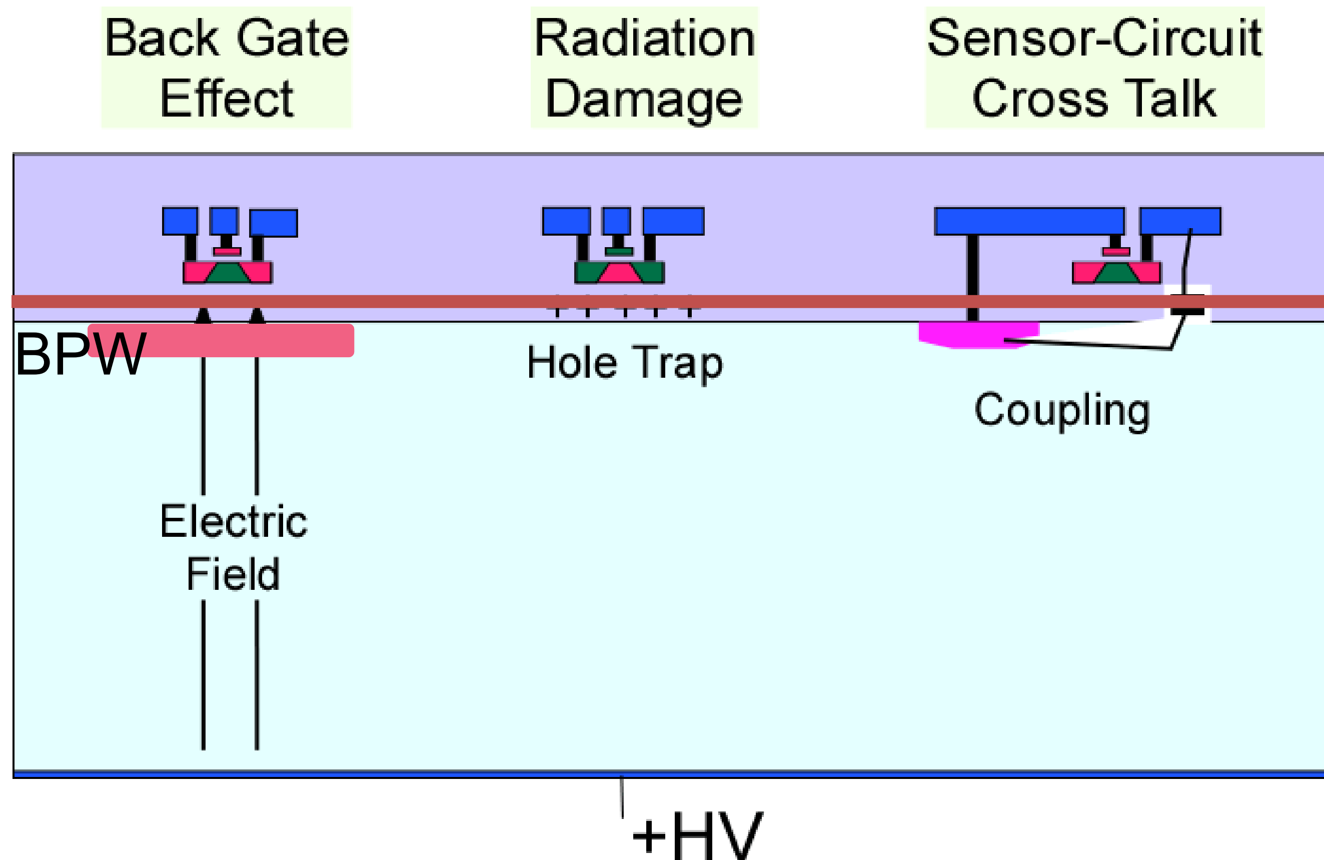
Louvain Univ.

U. Heidelberg

Only one SOI radiation pixel process in the world!

Issues in SOI detector

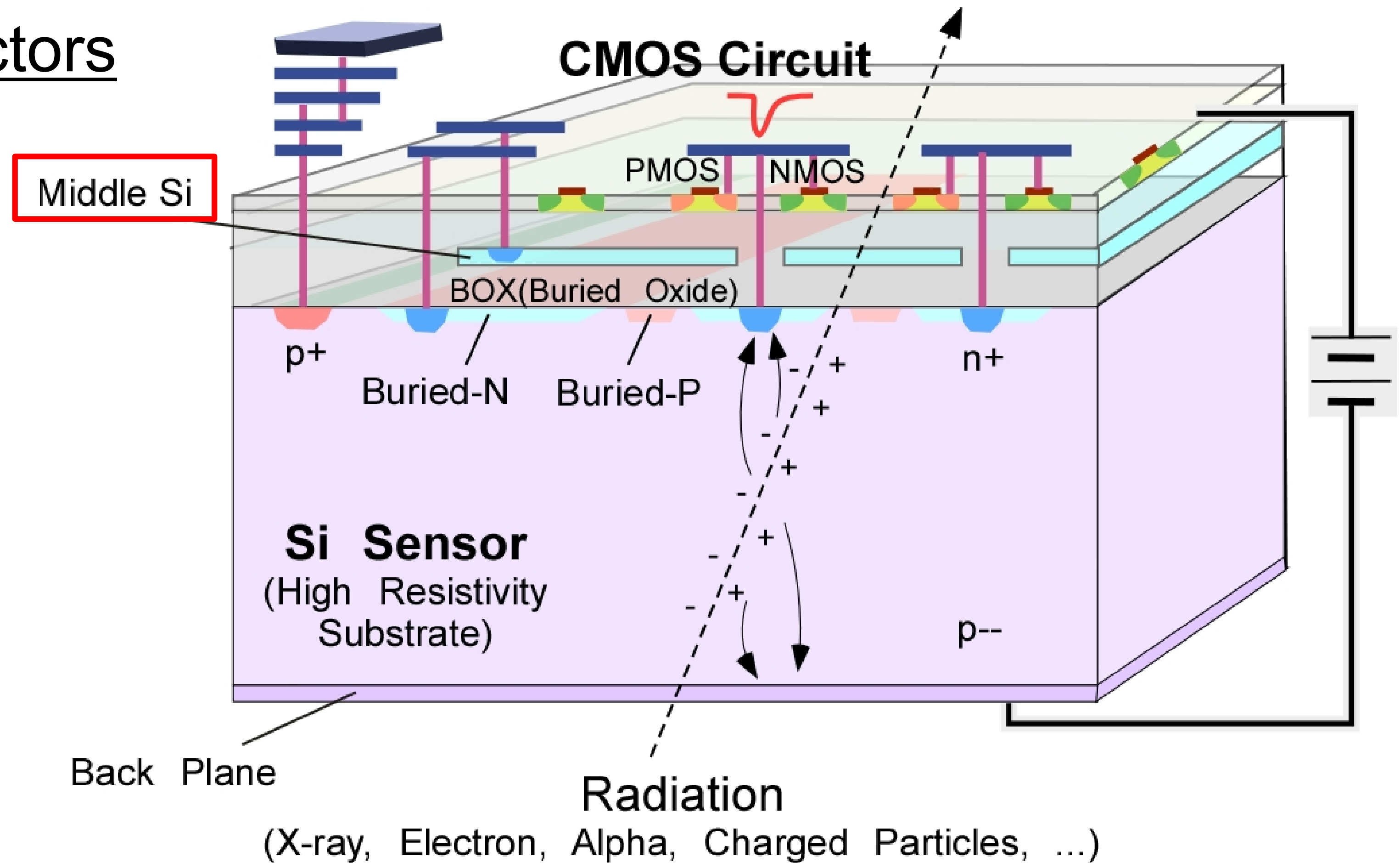
Sensor and Electronics are located very near. This cause ..



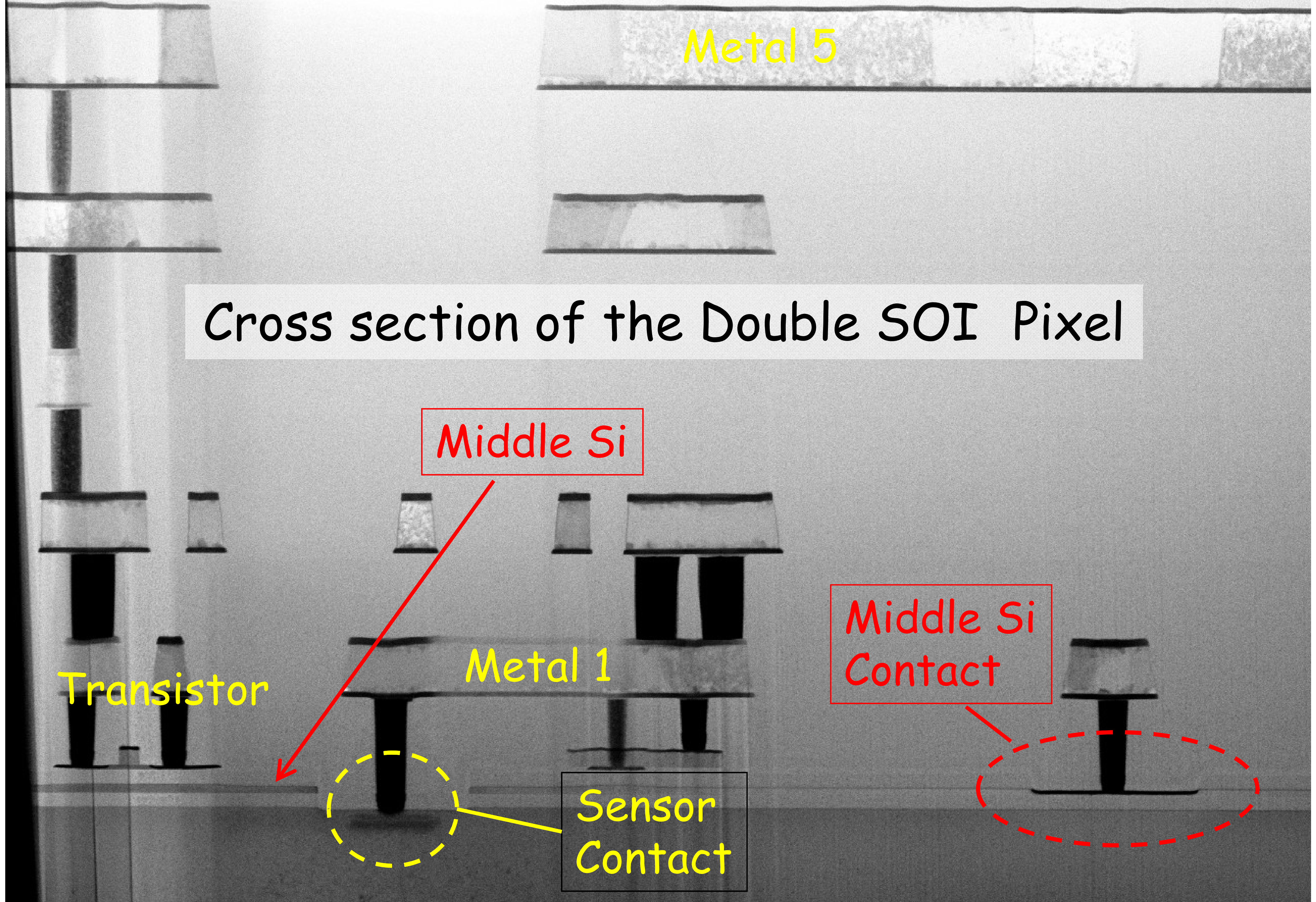
The BPW layer solved the back gate issue, but other issues are not yet solved.

Then we introduced additional conductive layer under the transistors (→ Double SOI).

SOIPIX Detectors (Double)

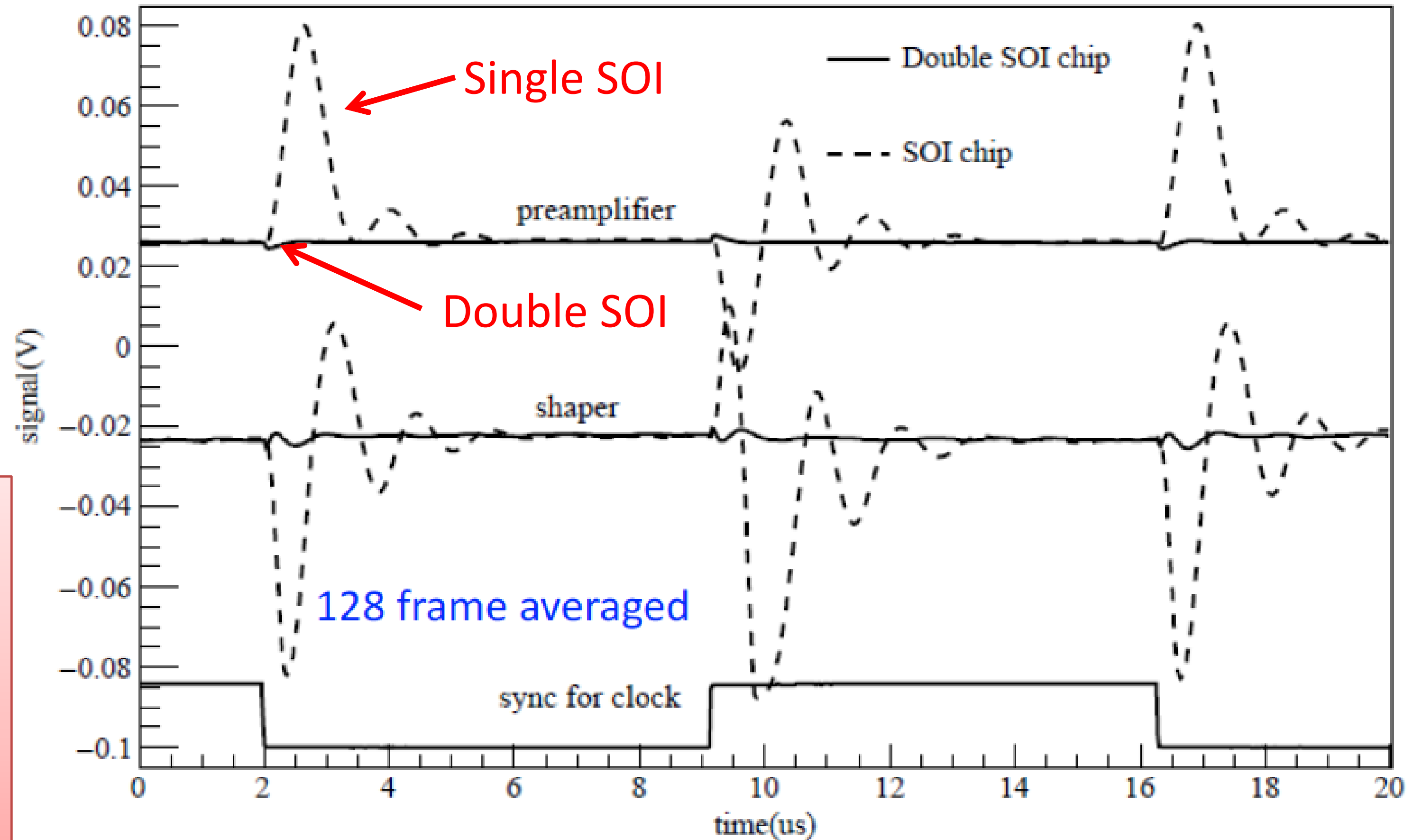


Double SOI Detector
- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.


Metal 5
Cross section of the Double SOI Pixel
Middle Si
Middle Si Contact
Metal 1
Transistor
Sensor Contact
x9.0k TE 12/10/16
3.00μm

Effect of Double SOI

Cross Talk from Clock line



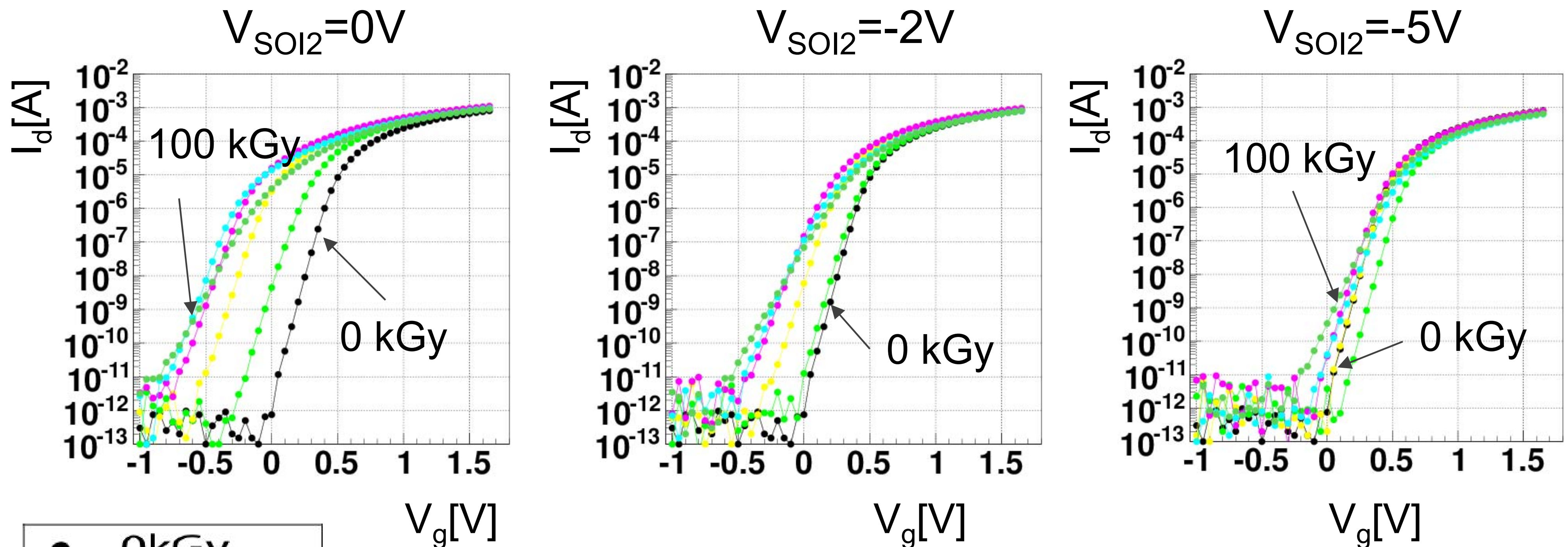
Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

(by Lu Yunpeng (IHEP))

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



0kGy
0.5kGy
1kGy
2kGy
5kGy
10kGy
20kGy
100kGy

By setting Middle Si potential (Vsoi2）to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(by U. of Tsukuba)

Variation of Id-Vg Characteristics and Effect of SOI2 Potential

PMOS

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

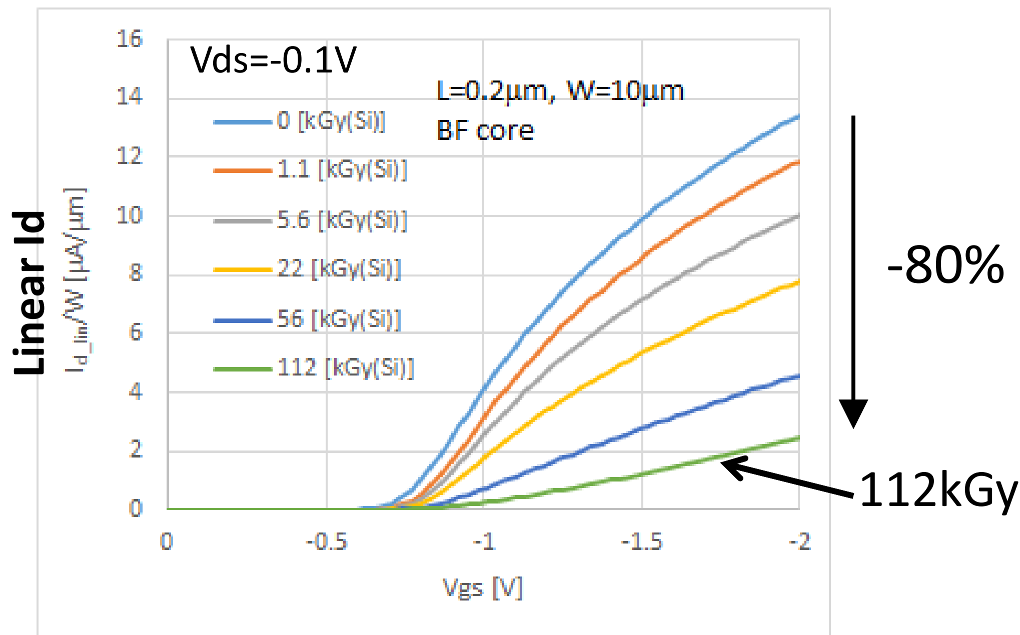
V_{SOI2}=0V V_{SOI2}=-2V V_{SOI2}=-5V

I_d[A]

0 kGy

100kGy

V_g[V]



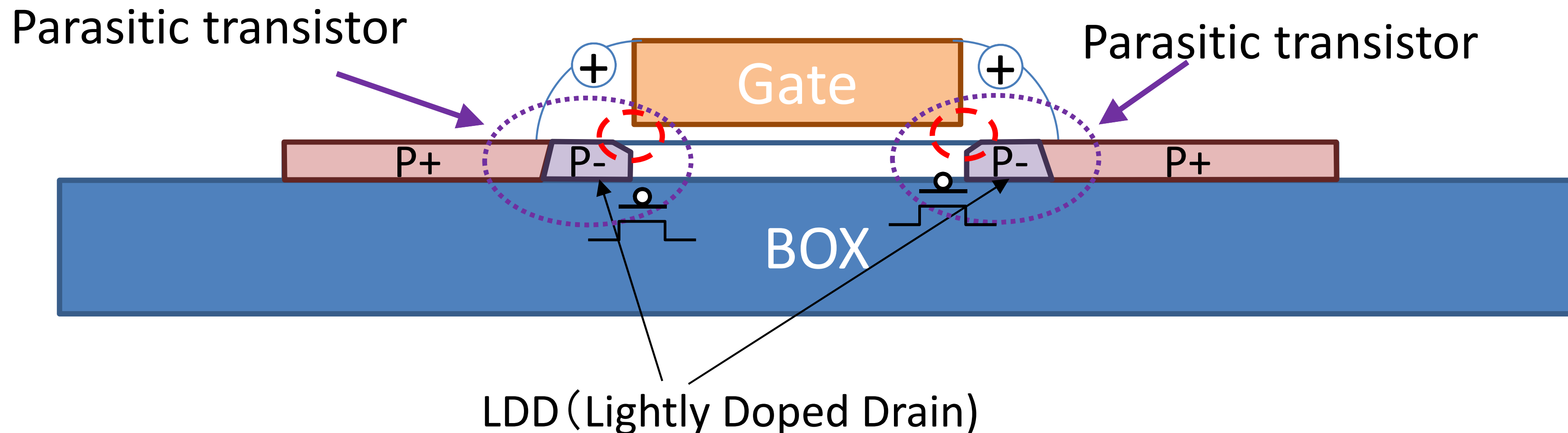
-80%

112kGy

Threshold voltage shift is not so large in PMOS, but Drain Current decreases much .

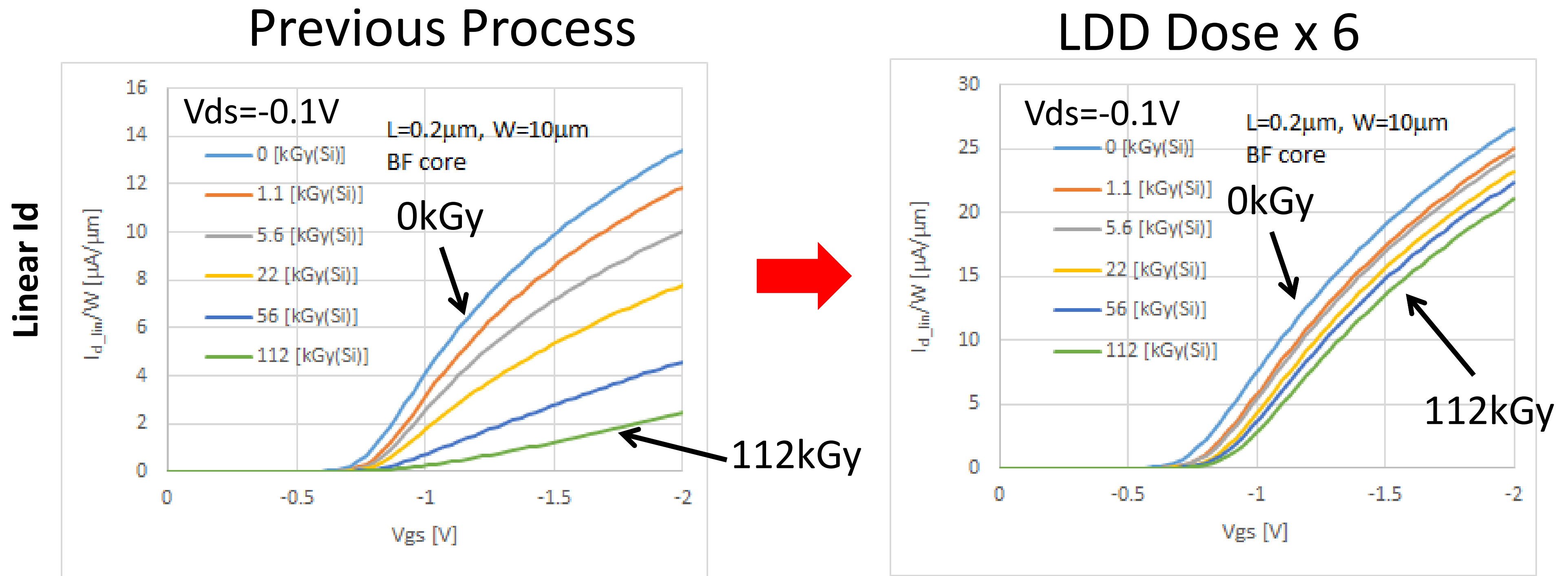
Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation by radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



(by I. Kurachi)

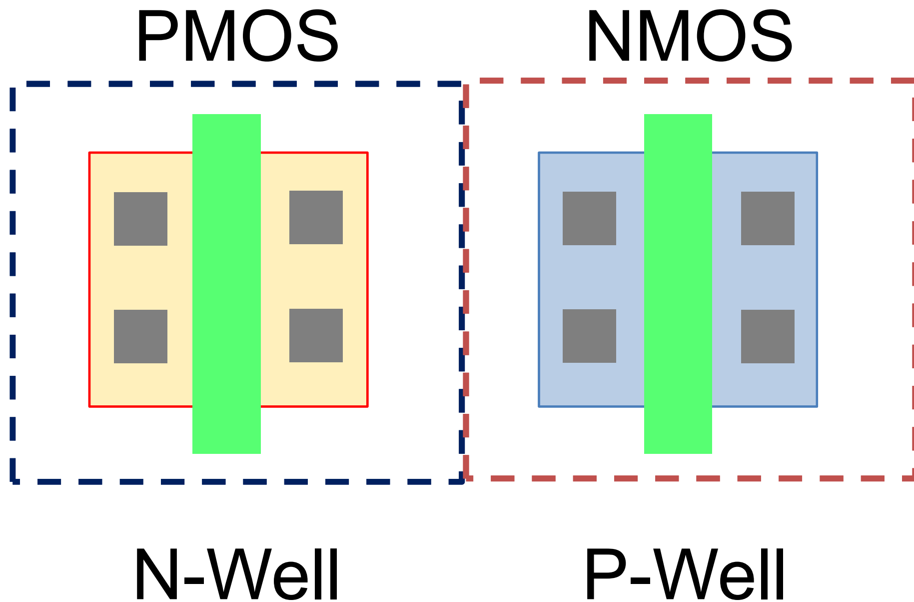
Id-Vg Characteristics in Triode Region

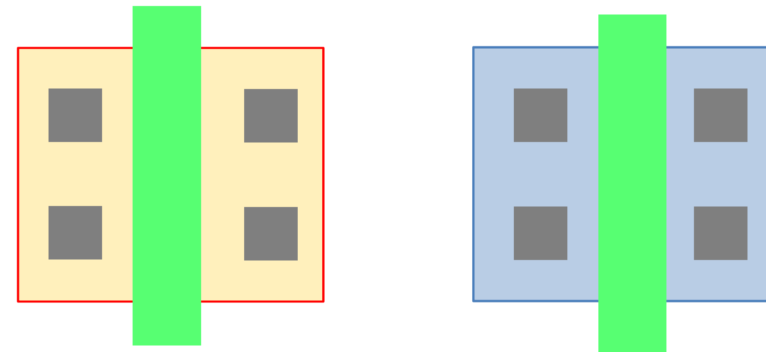


With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

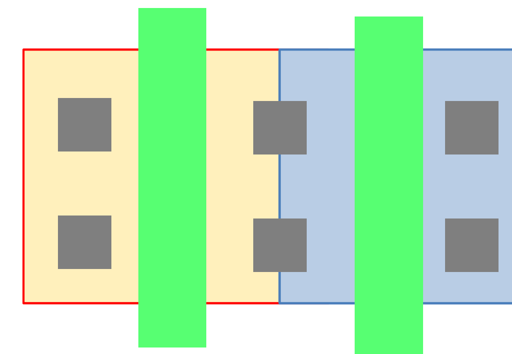
Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

Layout Shrink（Active Merge)

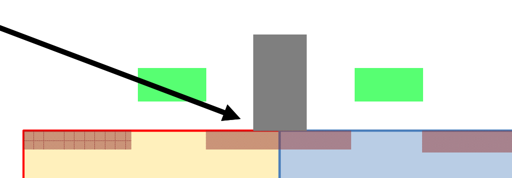




Share Contacts

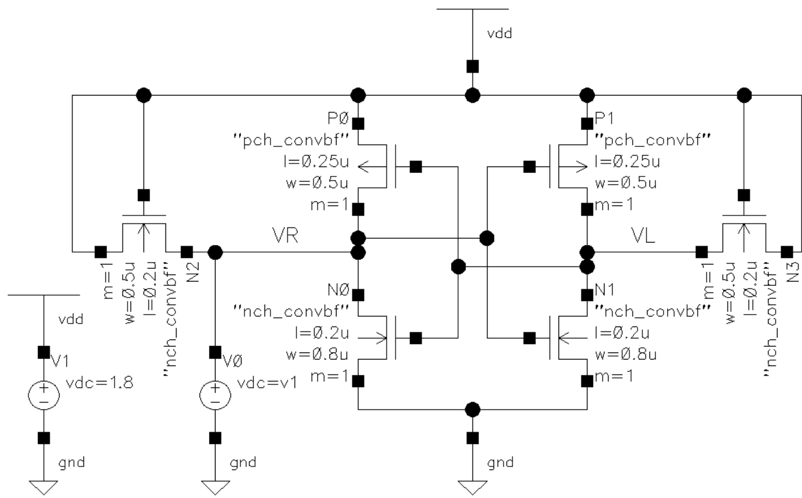


Salicide Connection

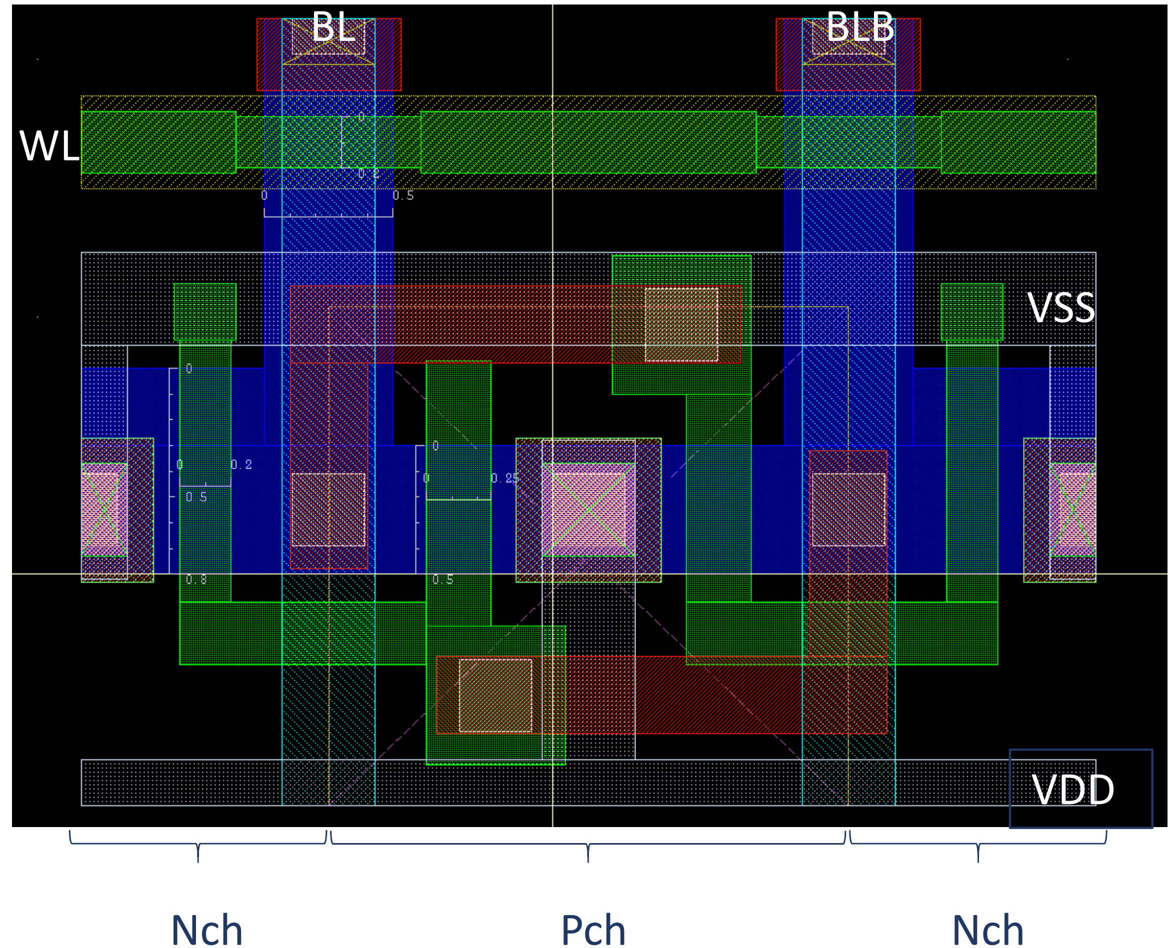


In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Single Port SRAM Bit Cell



Only 1 Active region



Cell Size : 3.94μm X 3.06μm = 12.06μm^2

Hexagonal Counting-type Pixel (under development)

CNPIX1

45um

52um

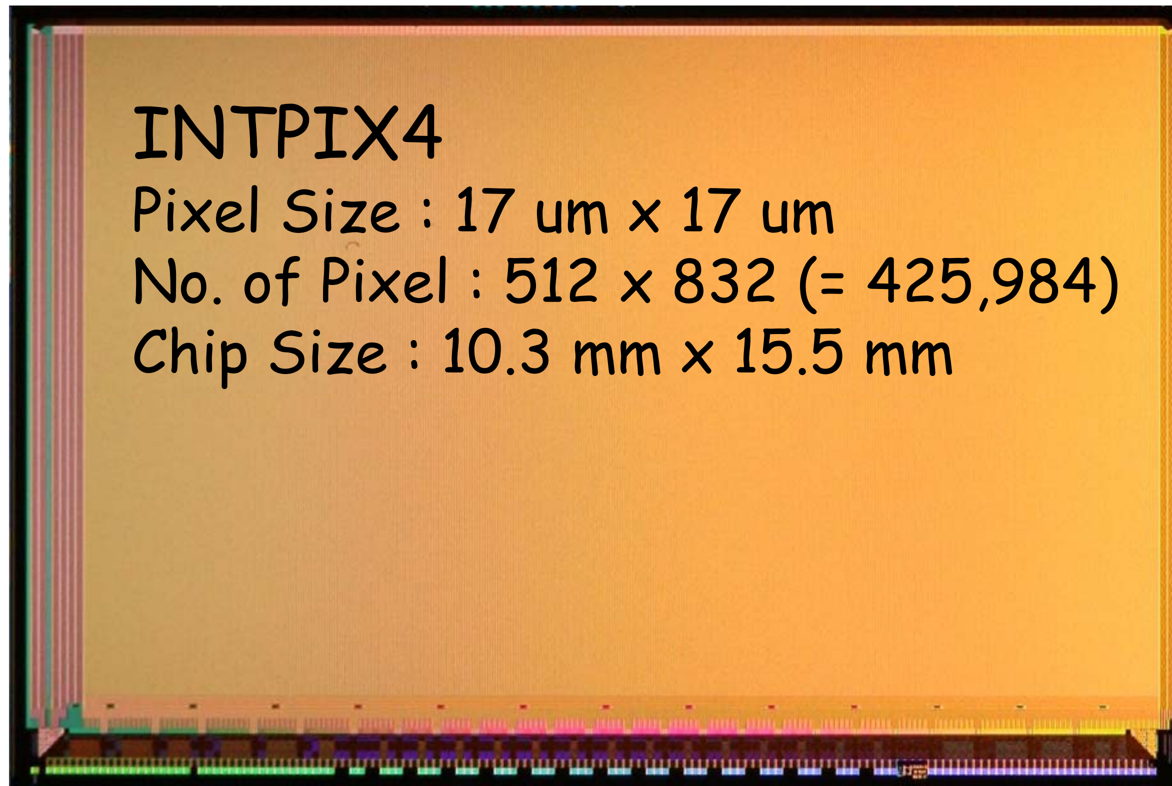
Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

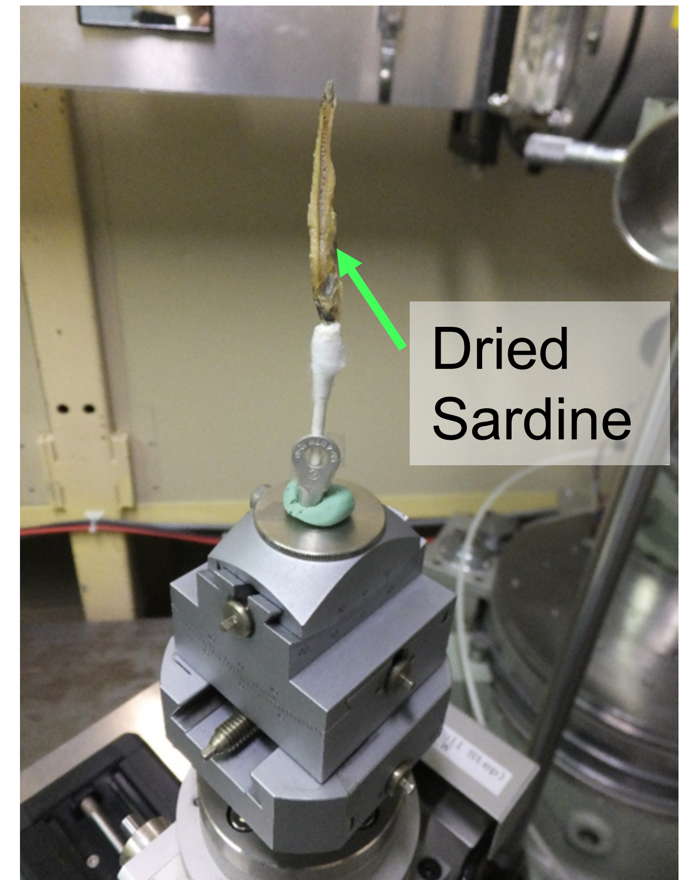
(in 2,340 um^2)

Smallest Counting-type Pixel of this kind.
(much smaller than designed in 0.13um process)

III. Detector Examples

Integration type detector & 3D CT

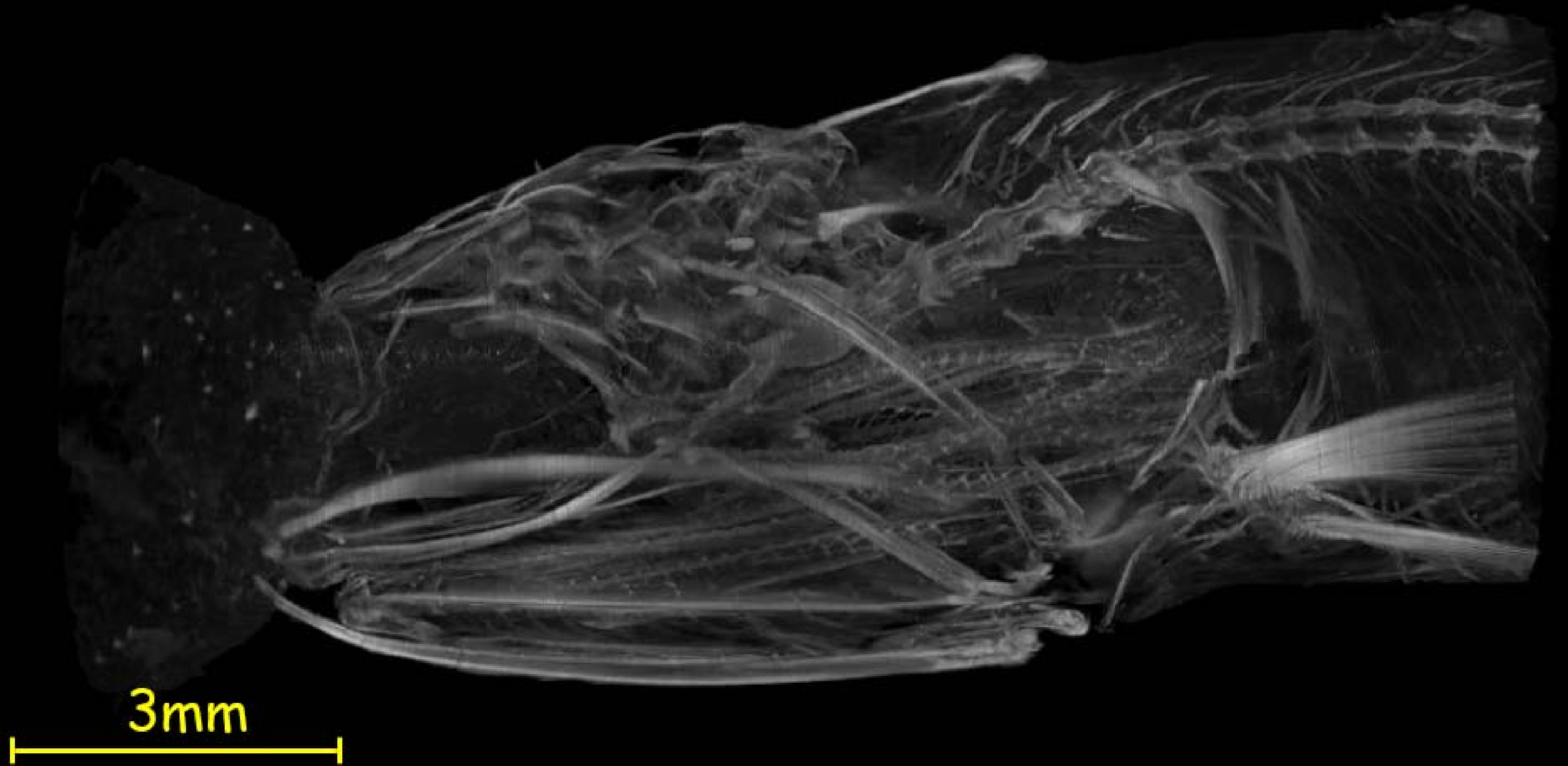




- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

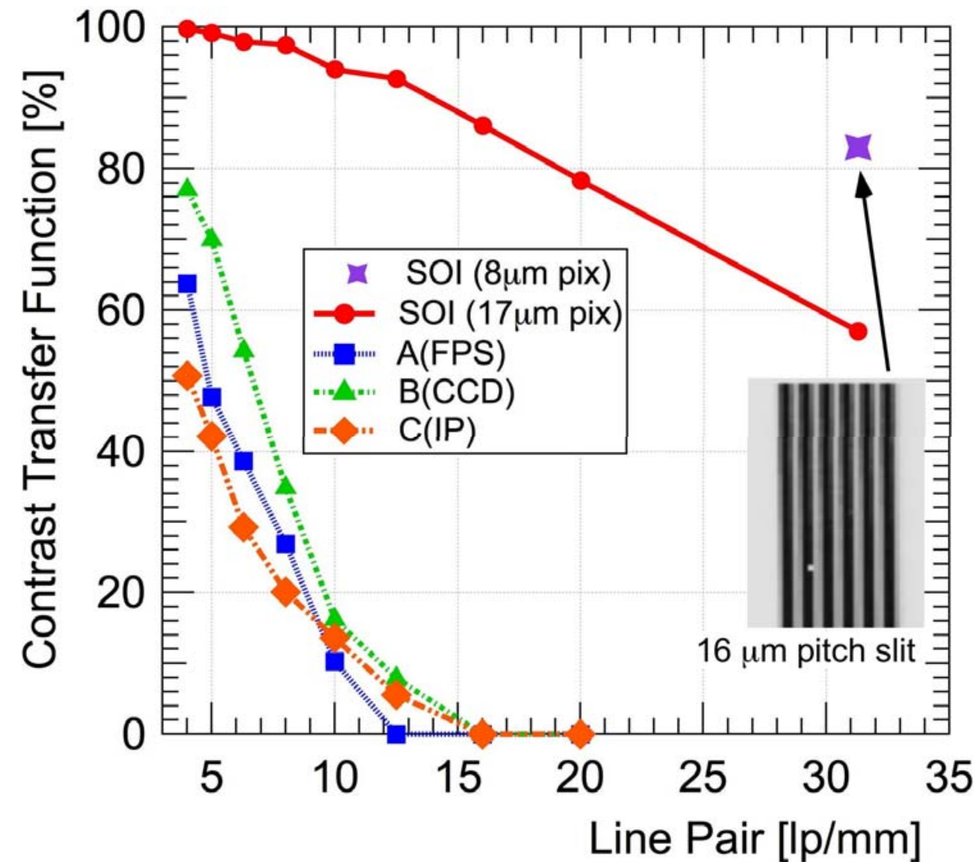
(by R. Nishimura, K. Hirano (KEK)

INTPIX4: Computed Tomography with Syncrotron X-ray

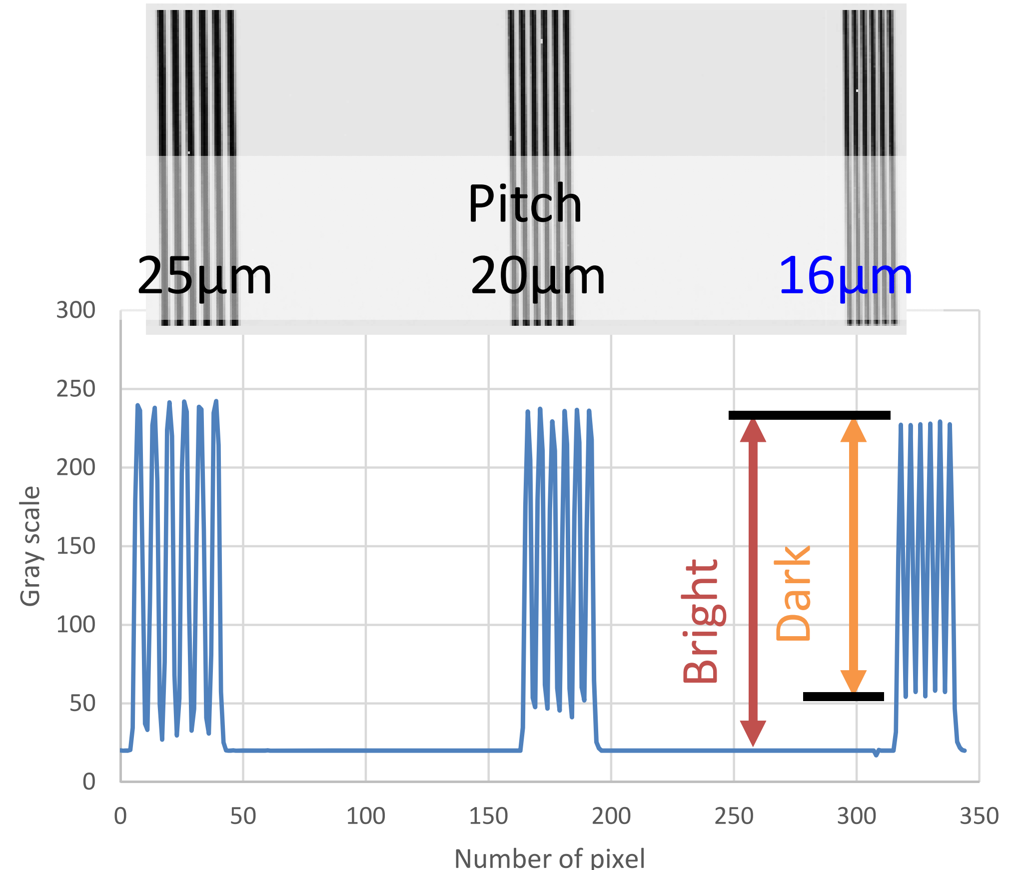


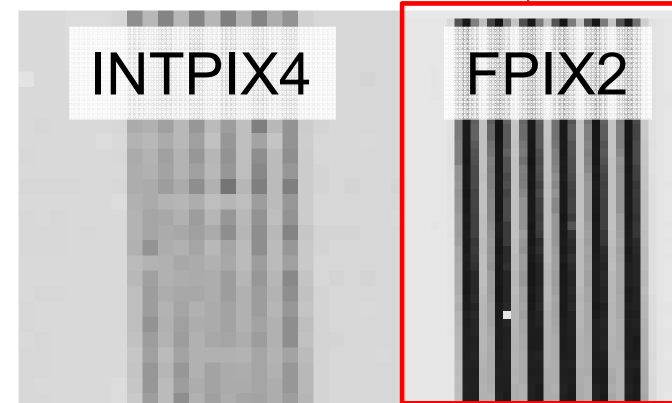
(by R. Nishimura, K. Hirano (KEK)

Contrast Transfer Function



FPIX2 FZn, 8um pixel





16 μm pitch slit

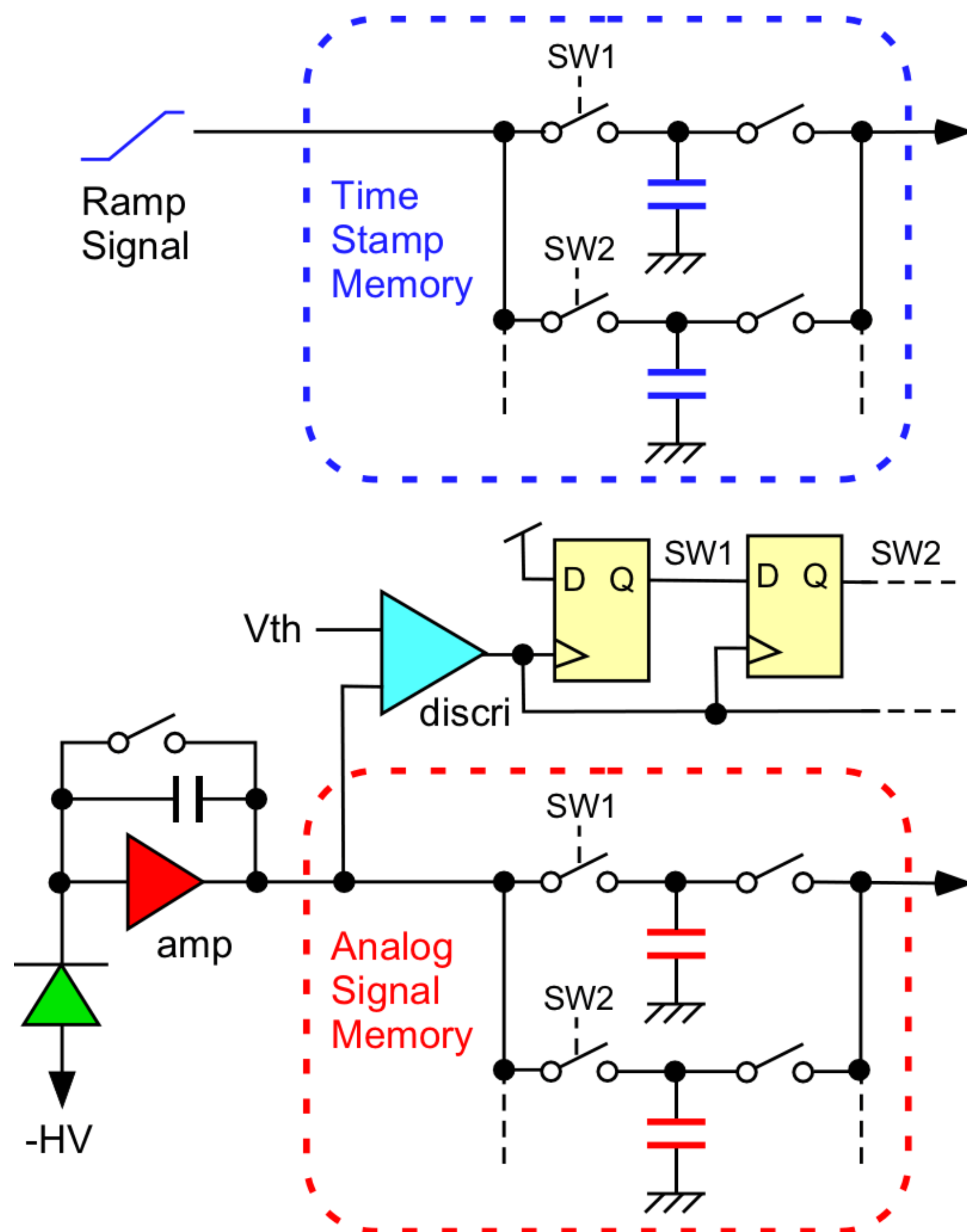
Contrast of 16μm Pitch Slit

INTPIX4(17μm pix) : 0.57、

FPIX(8μm pix) : 0.83

ILC Vertex Detector R&D : SOFIST

(SOI sensor for Fine measurement of Space & Time)



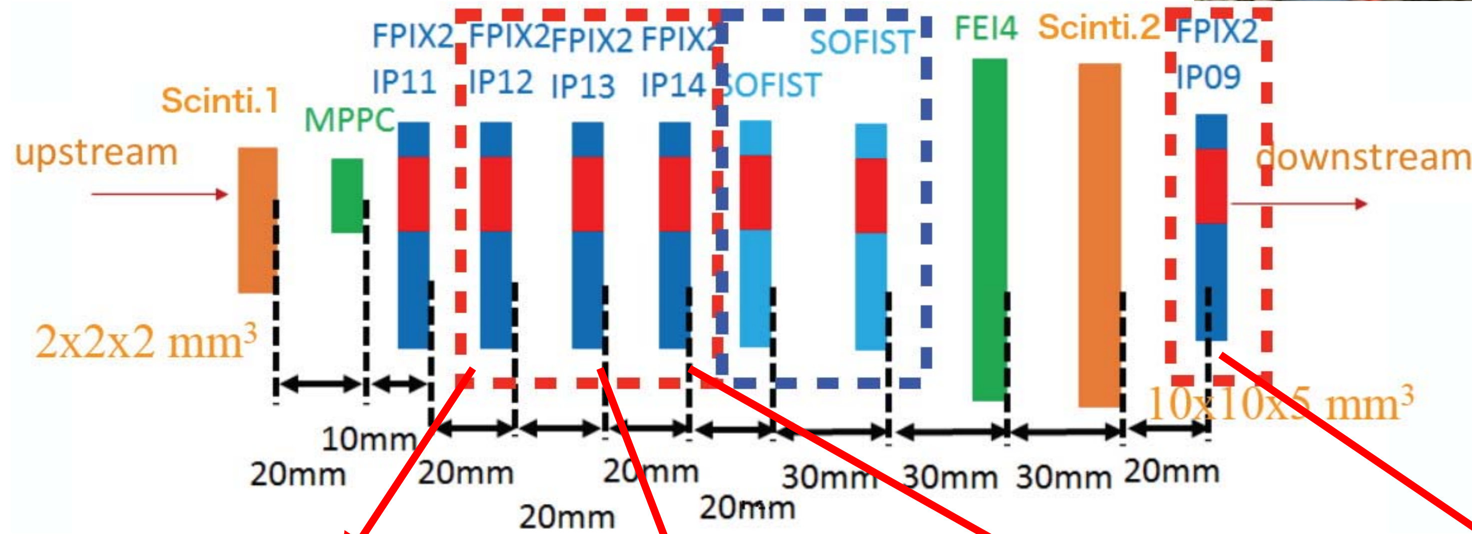
Test Chip Spec.

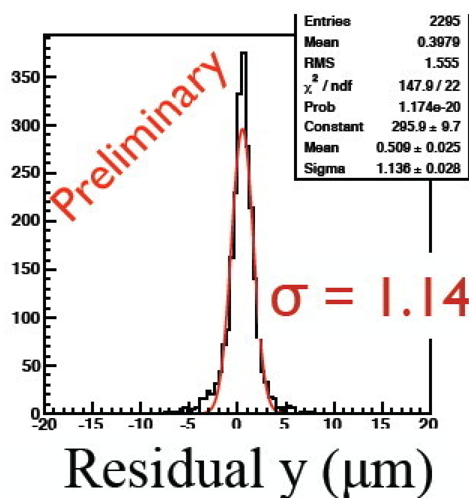
- Chip size: 2.9 × 2.9 mm2
- Substrate (FZ n-type, 2 kΩ•cm)
- Pixel size: 20~25 μm
- No. of Pixel: 50 × 50 pixels
- Gain: 32 mV/ke- (@Cf=5fF)
- Analog signal memories: 2 for signal or 2 for time
- Column-ADC: 8 bit
- Zero Suppression Logic

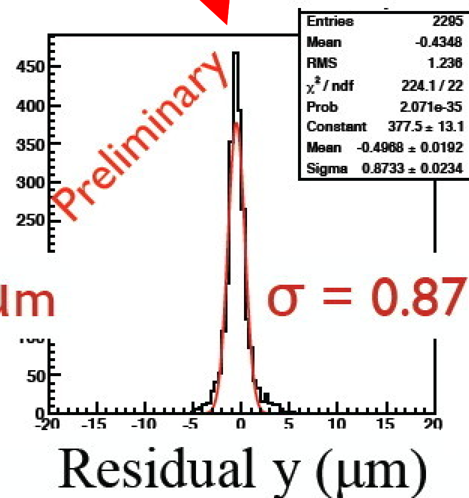
R&D for 3D integration is also progressing.

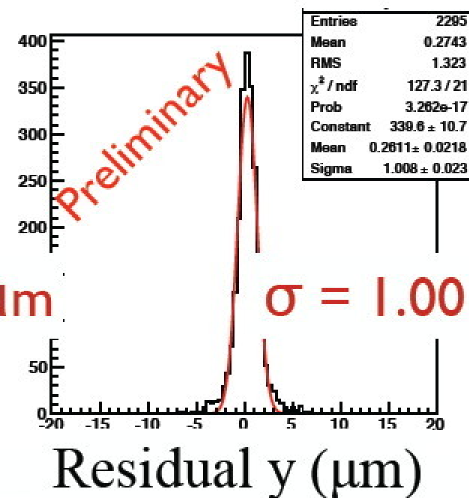
120GeV/c Proton Beam test at FNAL

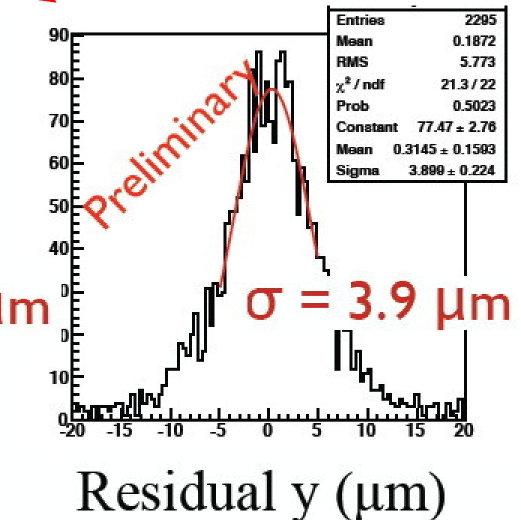
FPIX2 (8 μm pixel) x 4
SOFIST_v1 (20 μm pixel) x 2







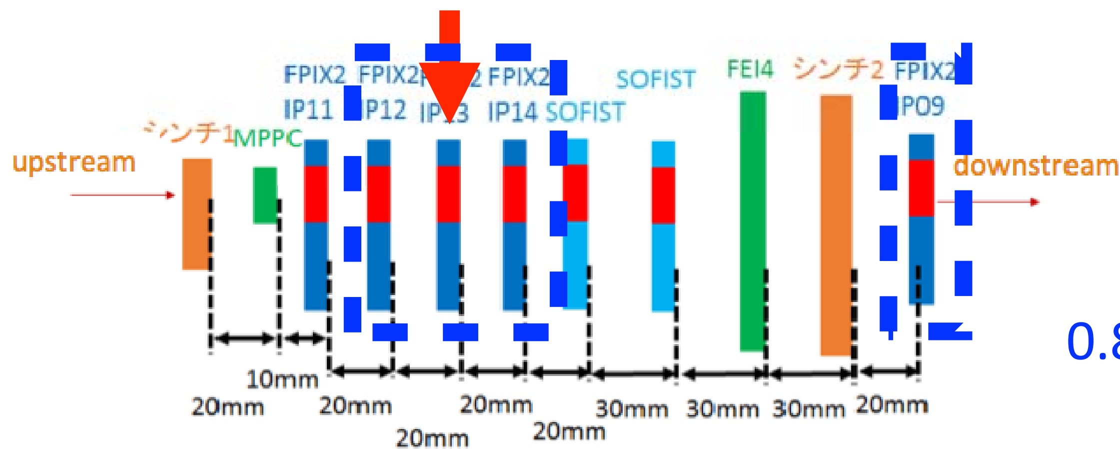


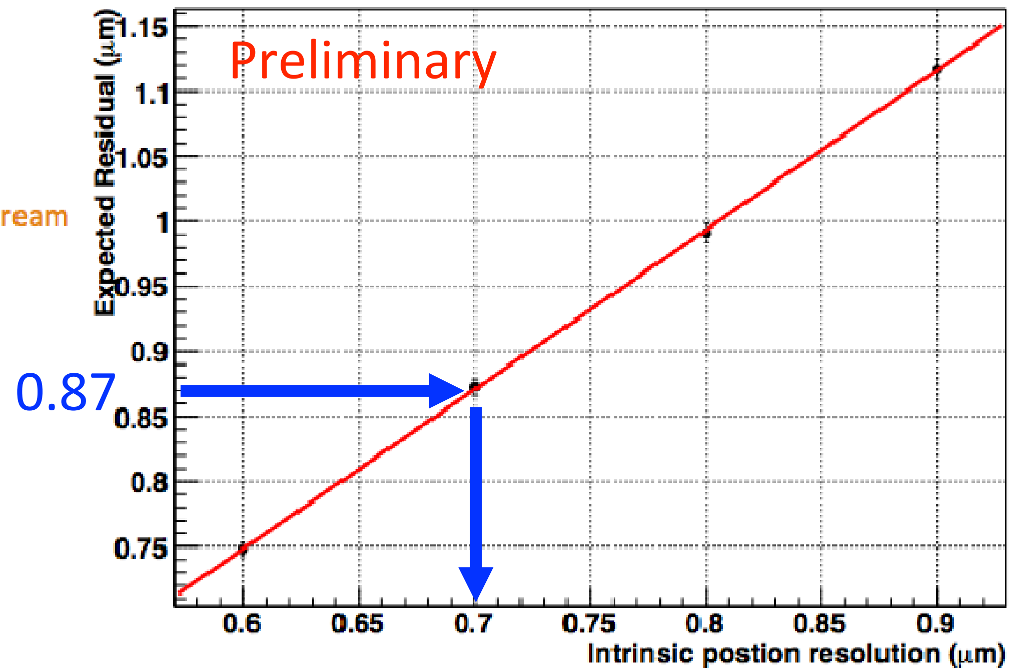


FPIX

The position resolution of FPIX2 demonstrated by MC

Evaluated by center sensor

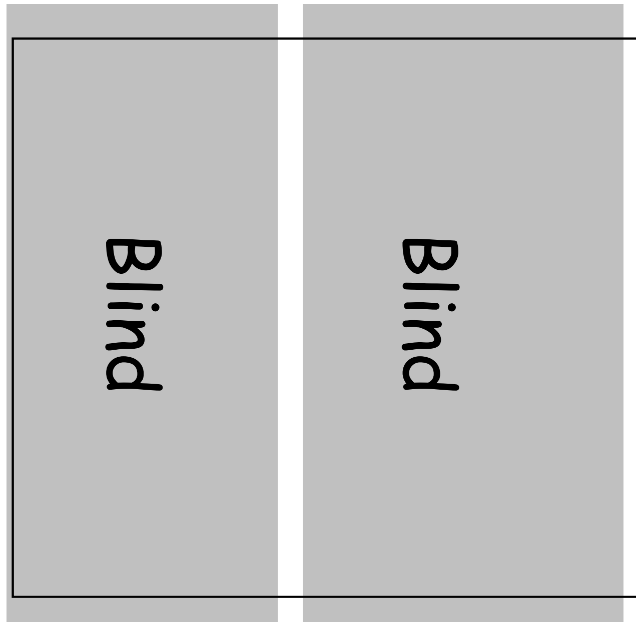


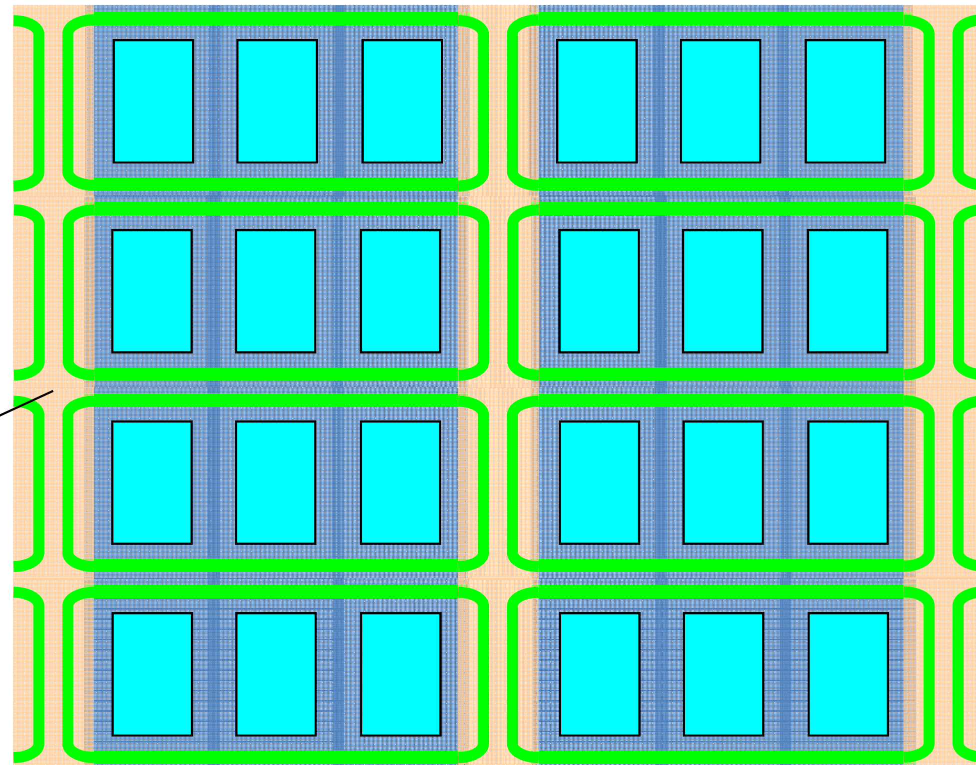


- Intrinsic position resolution is expected to be **~0.7 μm !**
- No evaluation systematic error yet
- Tracking resolution is ~0.5 μm

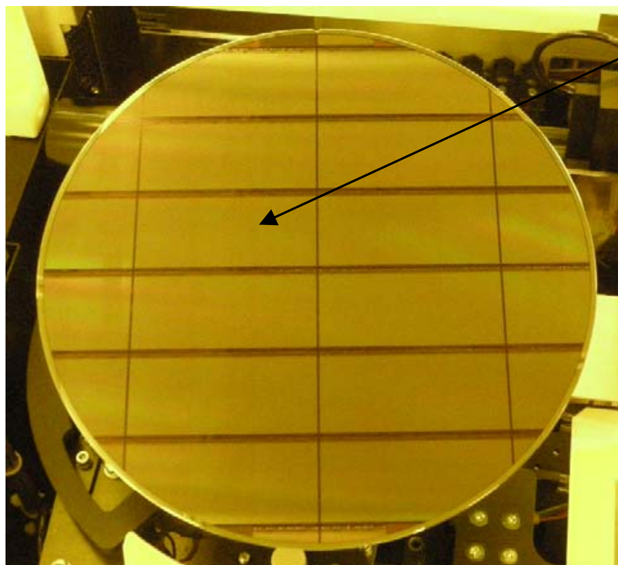
Stitching Exposure for Large Sensor

Mask Layout





Exposed Layout

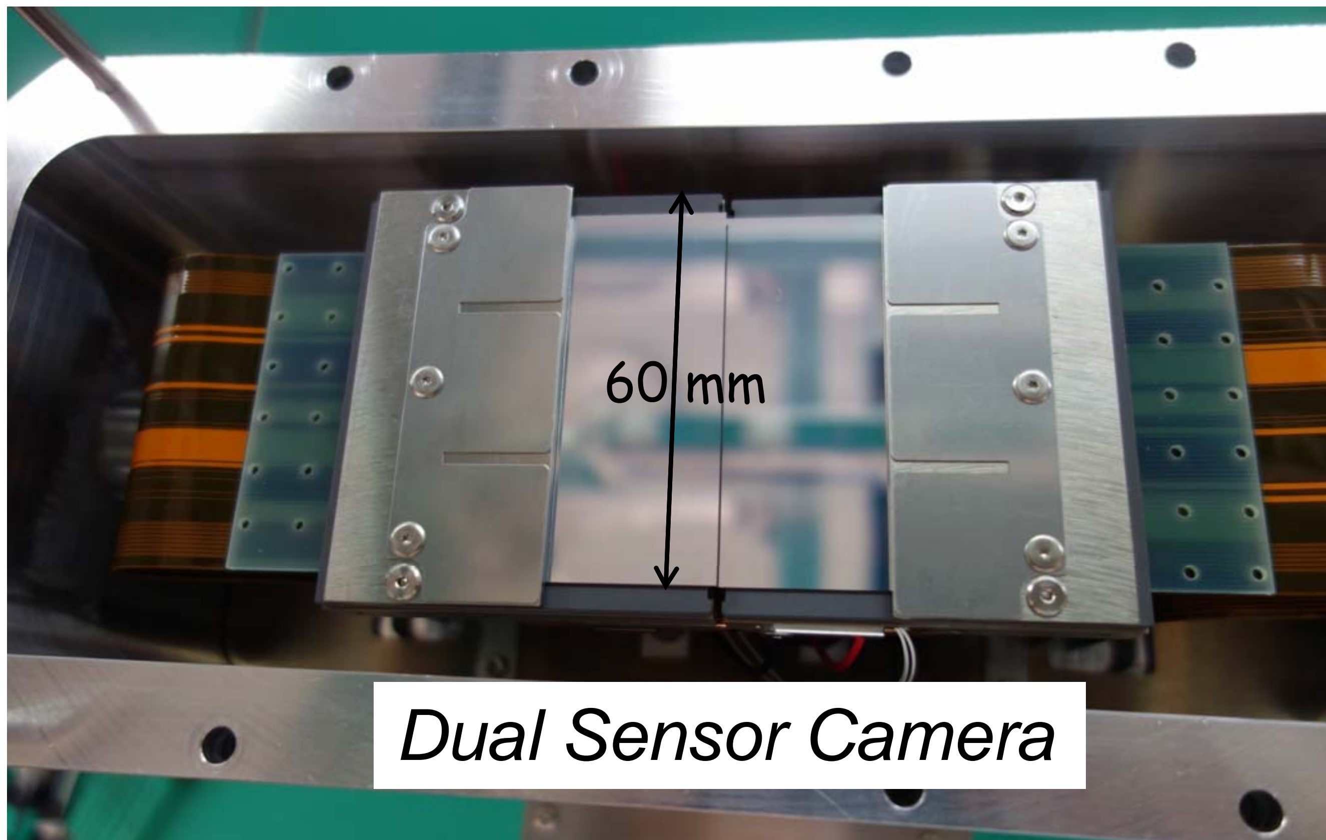


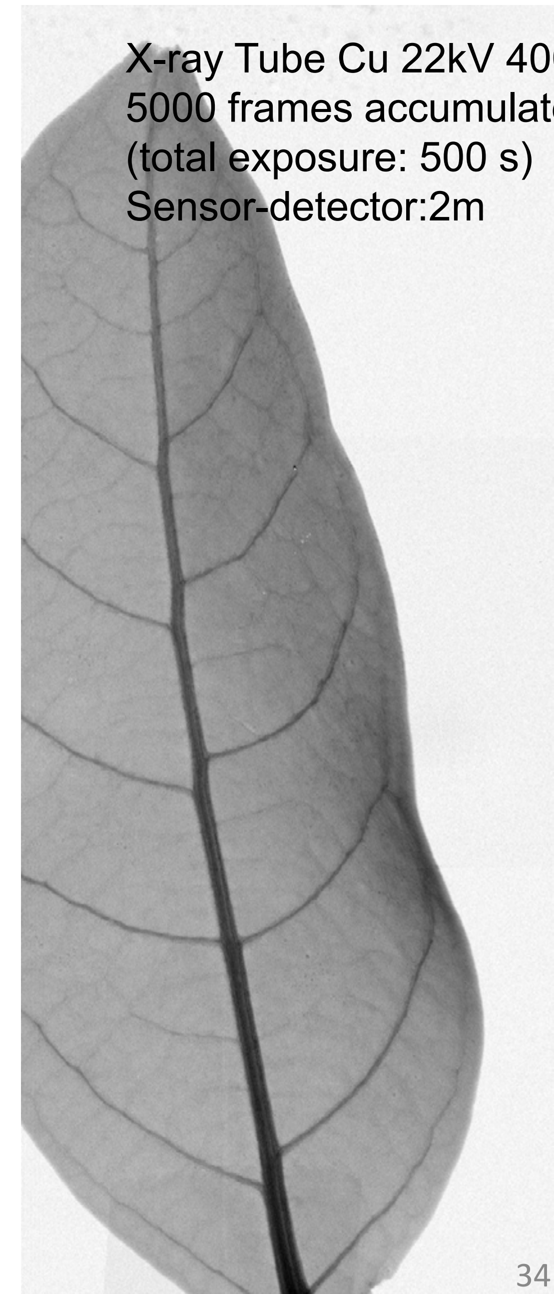
SOI Photon-Imaging Array Sensor (*SOPHIAS)*
for X-ray Free Electron Laser (XFEL) SACLA

SPring-8 SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.

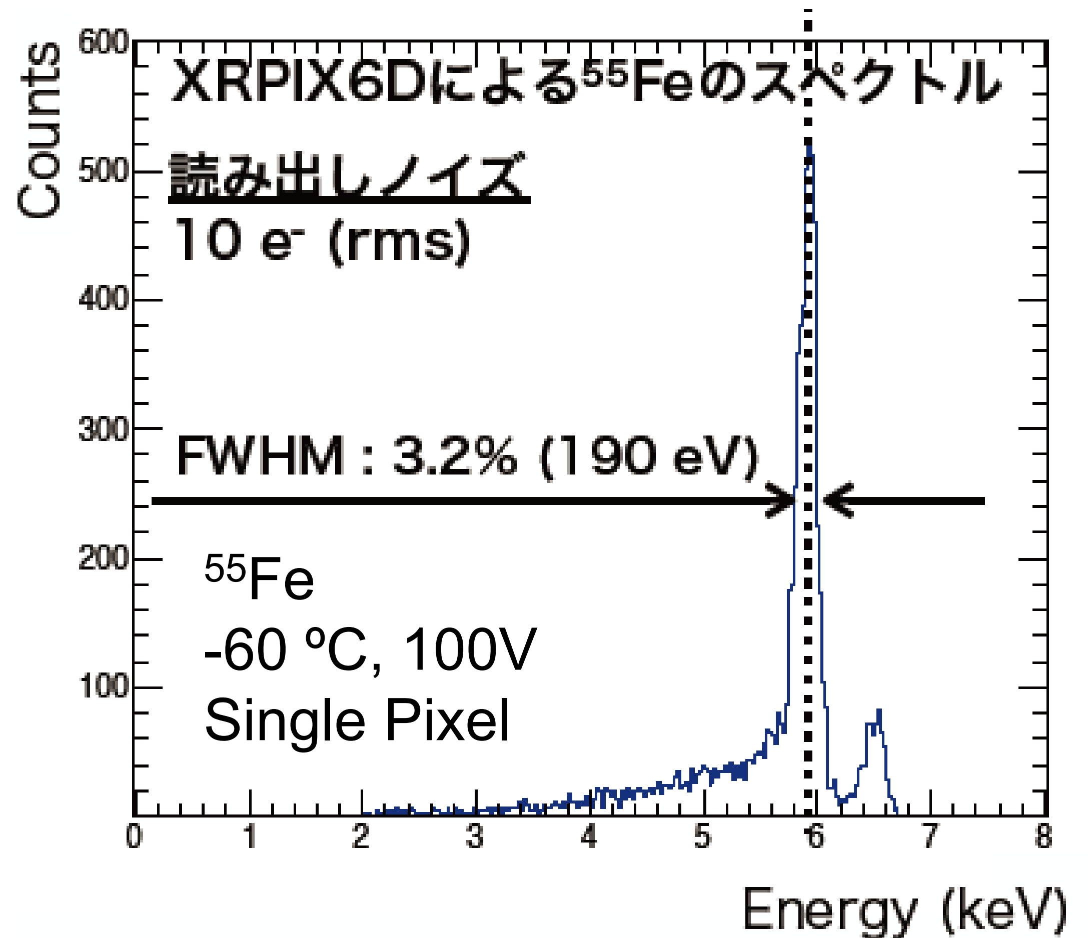




XRPIX: Event Driven X-ray Astronomy Detector

→ Tsuru's Talk

- Chip size : 24.6 mm x 15.3 mm
- Pixel size : 36 μm sq.
- # of pixel : 608 x 384 (= ~233k)
- Thickness of sensor layer : 310 μm (CZ wafer)
  500 μm (FZ wafer)



IV. Summary

- SOI pixel technology becomes mature. Back-gate and sensor-circuit coupling issues are solved by introducing double SOI wafer.
- Radiation tolerance is improved to more than 10 Mrad by biasing middle Si of the Double SOI.
- NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping analog voltage of 0.2um process (1.8V/3.3V).
- Many kinds of SOI X-ray detectors are developed (or under development) so far.
- Our SOI Pixel process run is open to academic people. Please join the run.

11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking detectors (HSTD11)

in conjunction with

2nd Workshop on SOI Pixel Detector (SOIPIX2017)

OIST, Okinawa, Japan, Dec. 11-15, 2017.

TOPICS:

- Simulations
- Technologies
- Pixel and Strip Sensors
- Radiation Tolerant Materials
- ASICs
- Large Scale Applications
- Applications in Biology, Astrophysics, Medical, ...
- New Ideas and Future Applications
- SOI Detectors

KEY DATES:

Abstract submission: 10 July - 28 Aug.

Registration: 10 July – 20 Nov.

https://indico.cern.ch/event/577879/

For further information – email: hstd@ml.post.kek.jp

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