

Sampling the signal from timing detectors for TOTEM at LHC



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CERN and INFN-Pisa
(on behalf of the TOTEM collaboration)



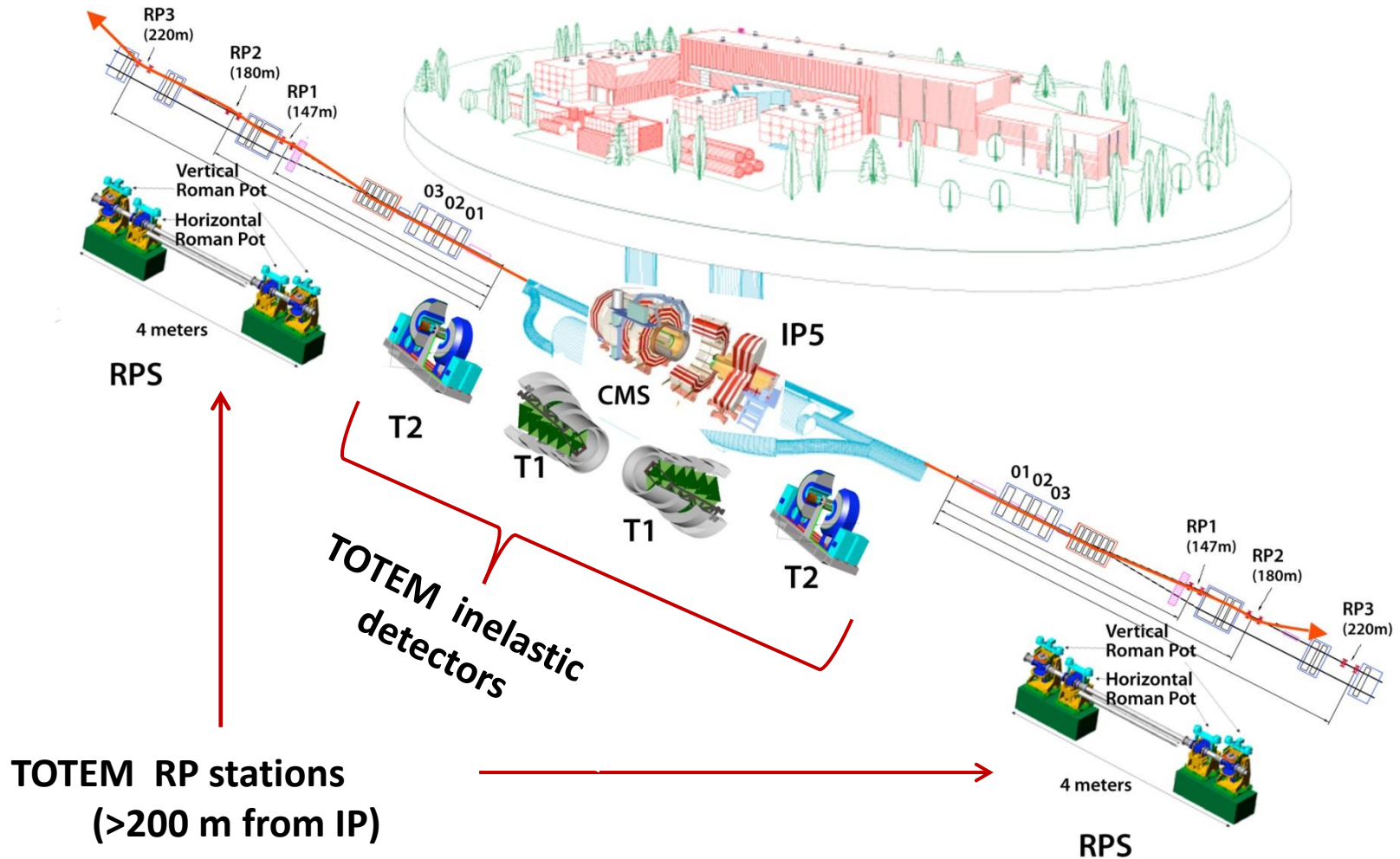
WaveCatcher and SAMPIC International Workshop
Orsay, 7 February 2018



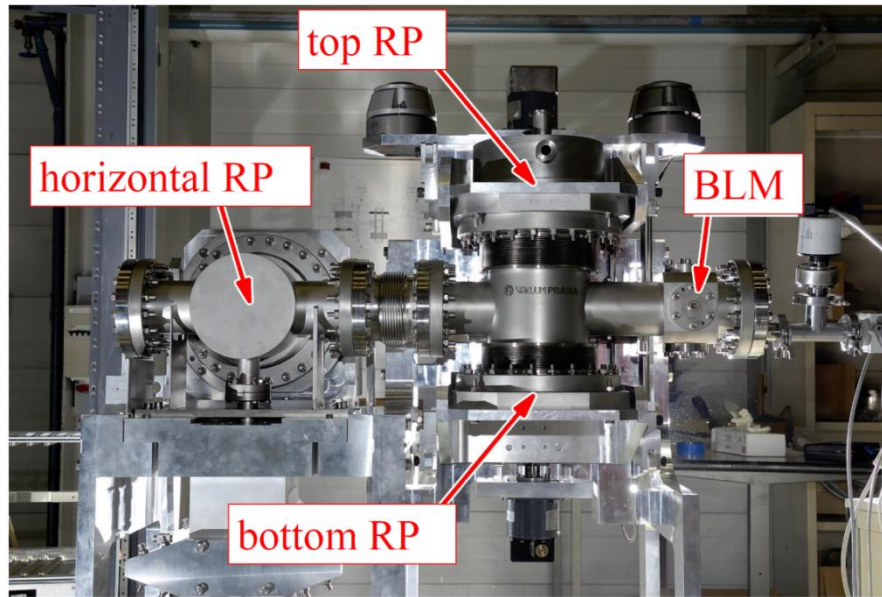
OUTLINE:

- Experiment overview
- Physics program
- Timing detectors
- Firmware for SAMPIC chip
- Future needs in HEP

TOTEM experiment

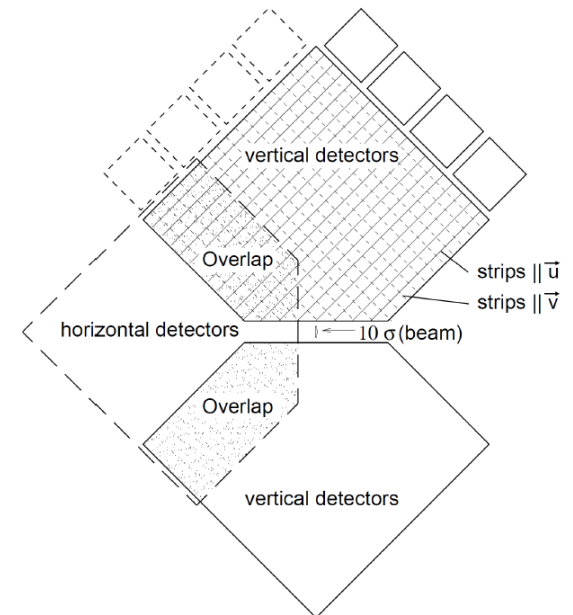
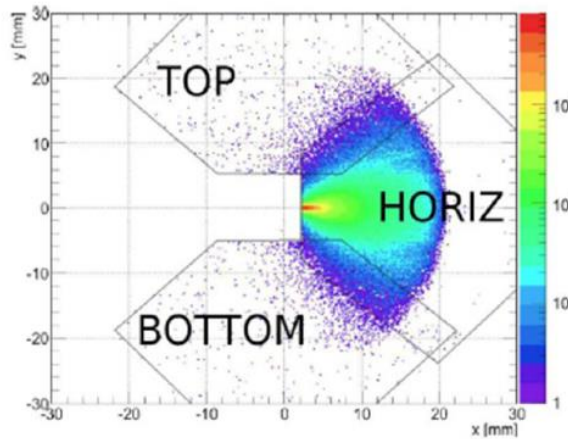
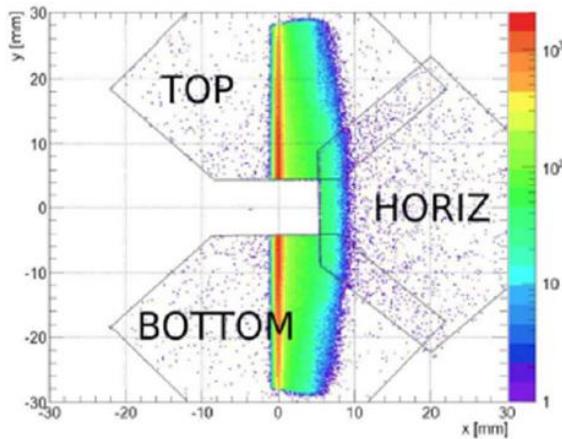


Roman Pots stations



- Vacuum vessel entering the beam pipe, can be equipped with many types of detectors.
- Scattered protons with very-low $|t|$ can be detected
- Standard units composed of 3 RP (2 vertical, 1 horizontal)

Distance from IP5 200-220 m

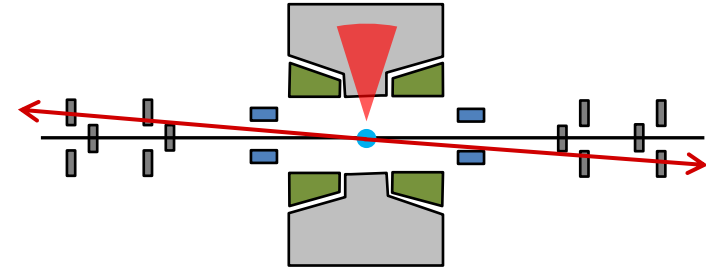
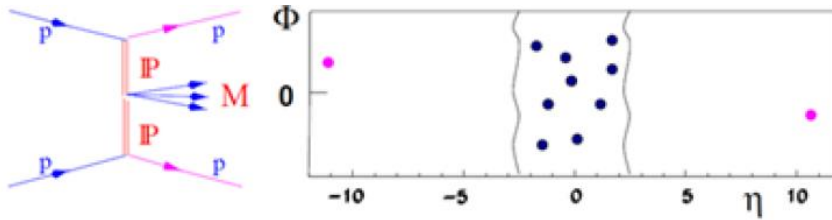


Central Exclusive Production



CMS and TOTEM works together to performs CEP studies. trigger information are exchanged and data can be offline merged.

Double
Pomeron
Exchange
(DPE)



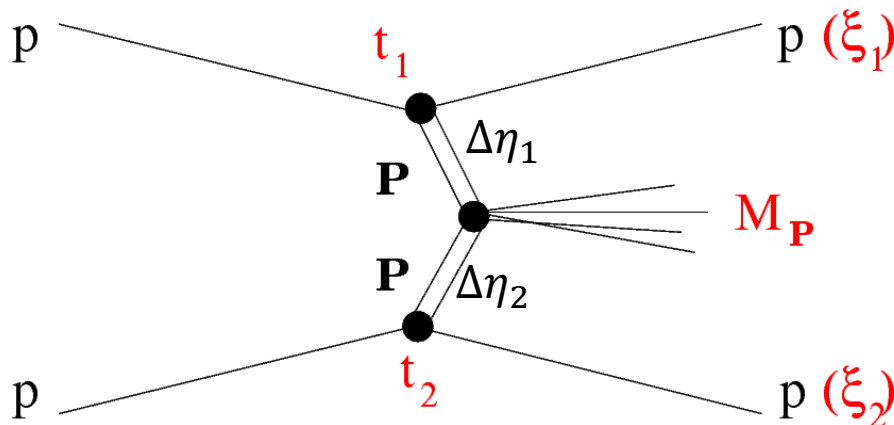
- Comparison/prediction from forward (TOTEM) to central (CMS) system:

M_{PP} , $p_{T,z}$, vertex

Proton
tracking

$$M_{PP} \sim \sqrt{\xi_1 \xi_2 S}$$

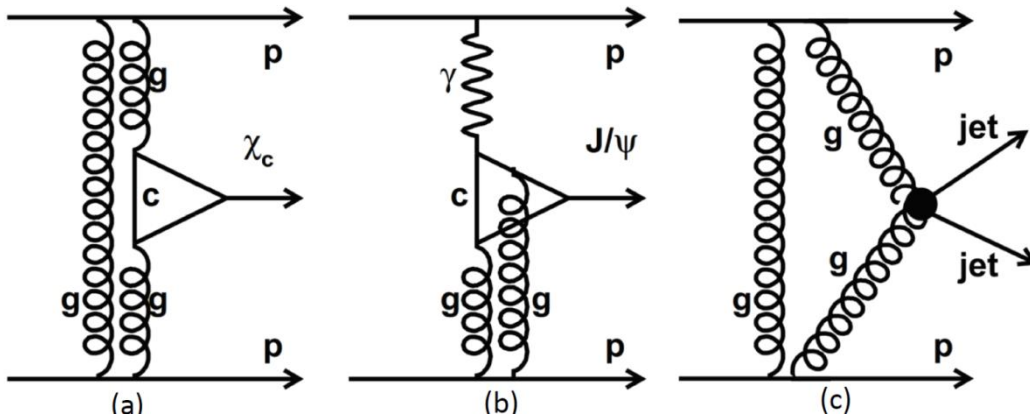
$$\Delta\eta_{1,2} = -\ln \xi_{1,2}$$



With CMS data central exclusive production can be investigated with strong BG rejection

For CEP studies in standard LHC condition the CT-PPS detector (based on TOTEM RP system) has been developed, fully integrated in CMS

TOTEM-CMS Physics program



Unprecedented low- $\xi \rightarrow$ almost pure gluon-gluon production



LHC as a gluon-gluon collider

➤ selection rules for system X: $J^{PC} = 0^{++}, 2^{++}$

➤ Glueball searches (f_0 tensorial states)

➤ Low mass resonances/meson pair

($\pi\pi$, KK , $\rho\rho$, $\eta\eta$):

- Spin
- Decay modes
- Branching ratios

➤ Exclusive $c\bar{c}$ states production (χ_c) with different states resolved

➤ Exclusive J/ψ and (ψ_{2S}) production:

- Direct DDIS HERA confrontation

$J_z = 0$ selection rule \Rightarrow pure gluon jets

➤ Cross-sections extremely sensitive to important & subtle QCD effects:

- generalized gluon PDFs
- rapidity gap survival probabilities
- “Sudakov” factors.

BSM search:

- Missing mass/momentum
- Rapidity gap violation

Timing detectors



Higher the LHC luminosity, higher the probability to have more than one simultaneous pp interaction (with mean μ)

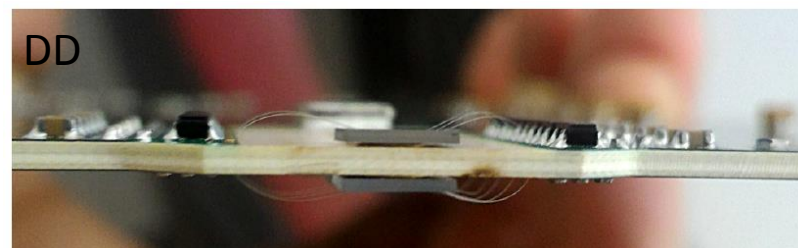
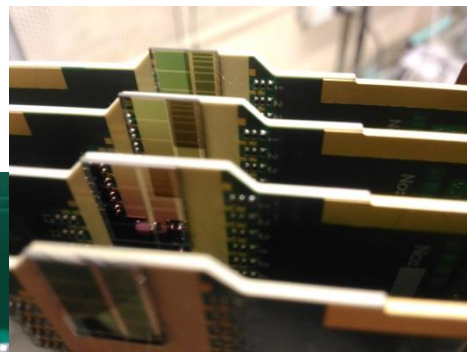
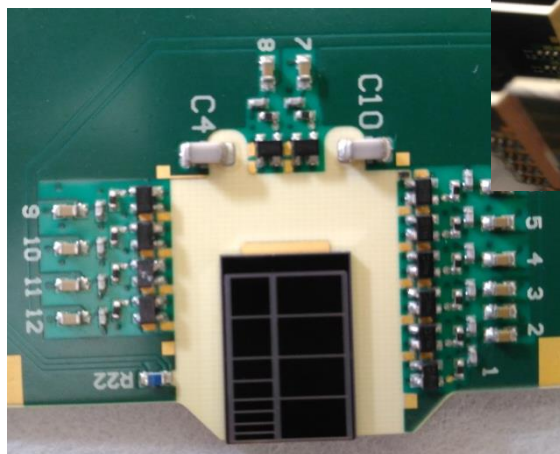
Reconstruction of primary vertex of detected protons with TOTEM Roman Pots (RPs) limited
→ difficult if $\mu > 0.1$

Max luminosity mandatory to access low cross-sections ($\mu \sim 1$ for 90 m run, much higher in standard runs)

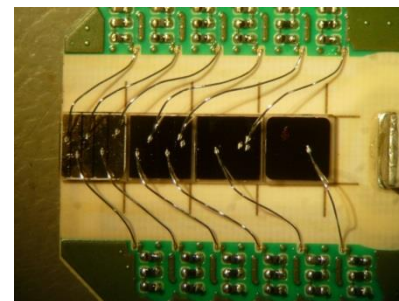
Measure of the proton time of flight in the two arms:

$$\triangleright Z_{PP} = c\Delta t/2$$

With few tens of ps resolution (for MIP)



Diamond[1] and UFSD[2] detectors developed.
Both technologies actually used in the RP



Readout



Both technologies have similar characteristics of the output signal

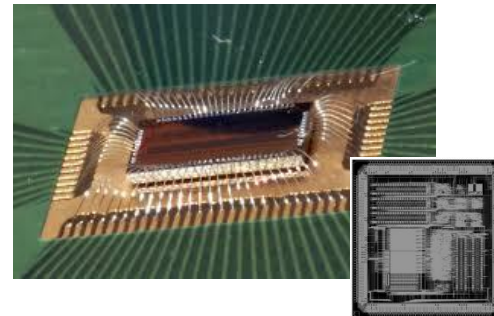
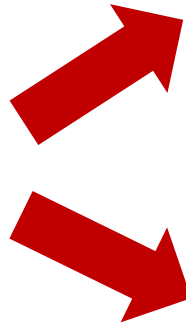
Rise time $\sim 0.5 - 1.5$ ns

SNR $\sim 30 - 50$

Amplitude $\sim 300-600$ mV



Fast sampler



ToT
Discriminator +
TDC
(NINO+HPTDC)



Why SAMPIC:

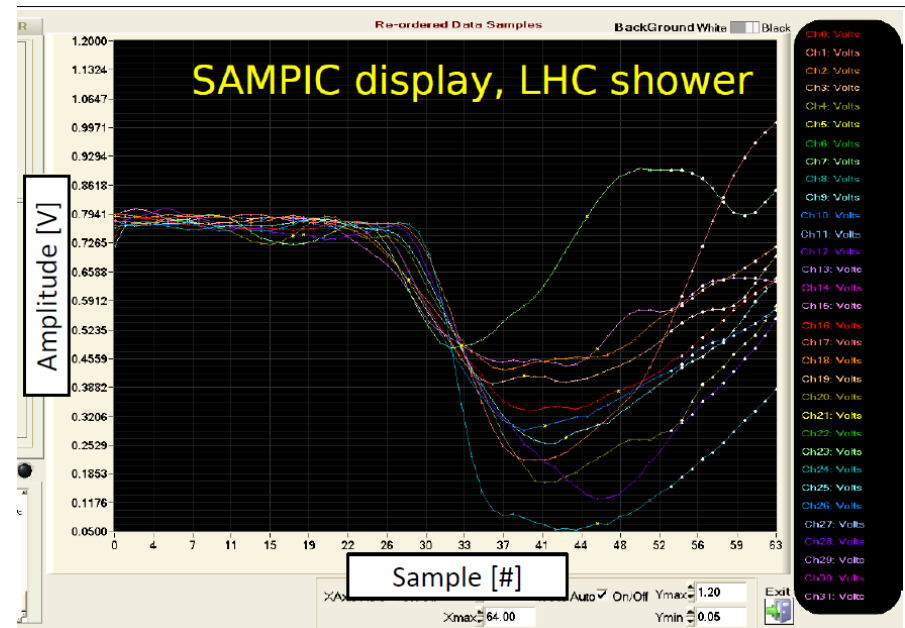
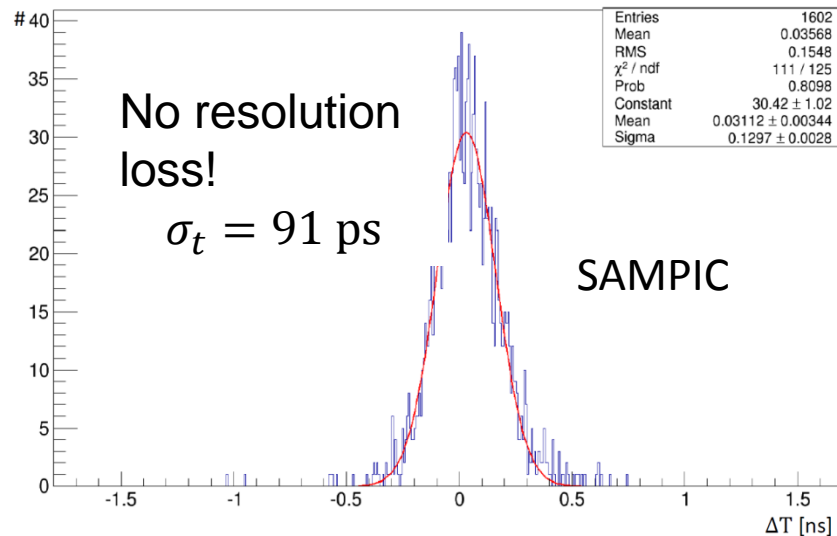
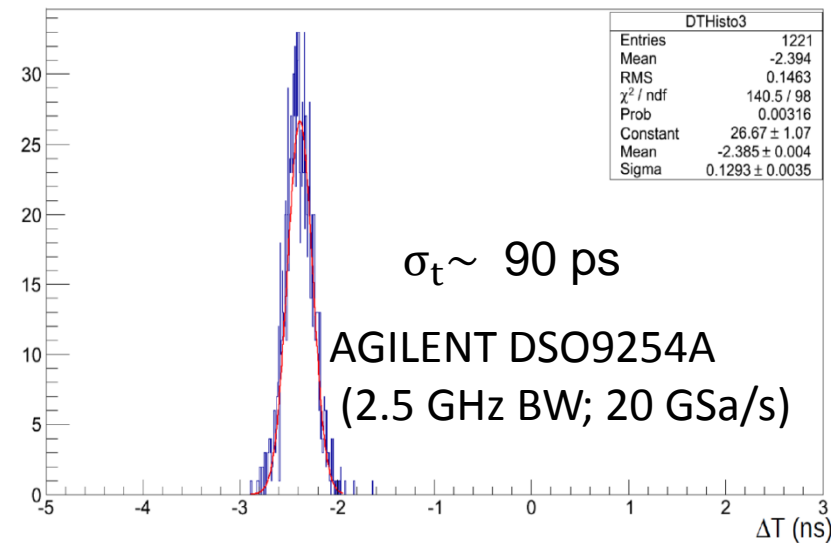
- ✓ To achieve maximum resolution a fast sampling (5-10 Gsa/s) of the signal is mandatory.
- ✓ Low channel dead time and high input rate are also needed , even for $\mu \sim 1$.
- ✓ Low cost/channel (~ 200)

Used in CT-PPS due to the input rate (~ 1 MHz/channel).
Loss in performance expected to be around 30%.

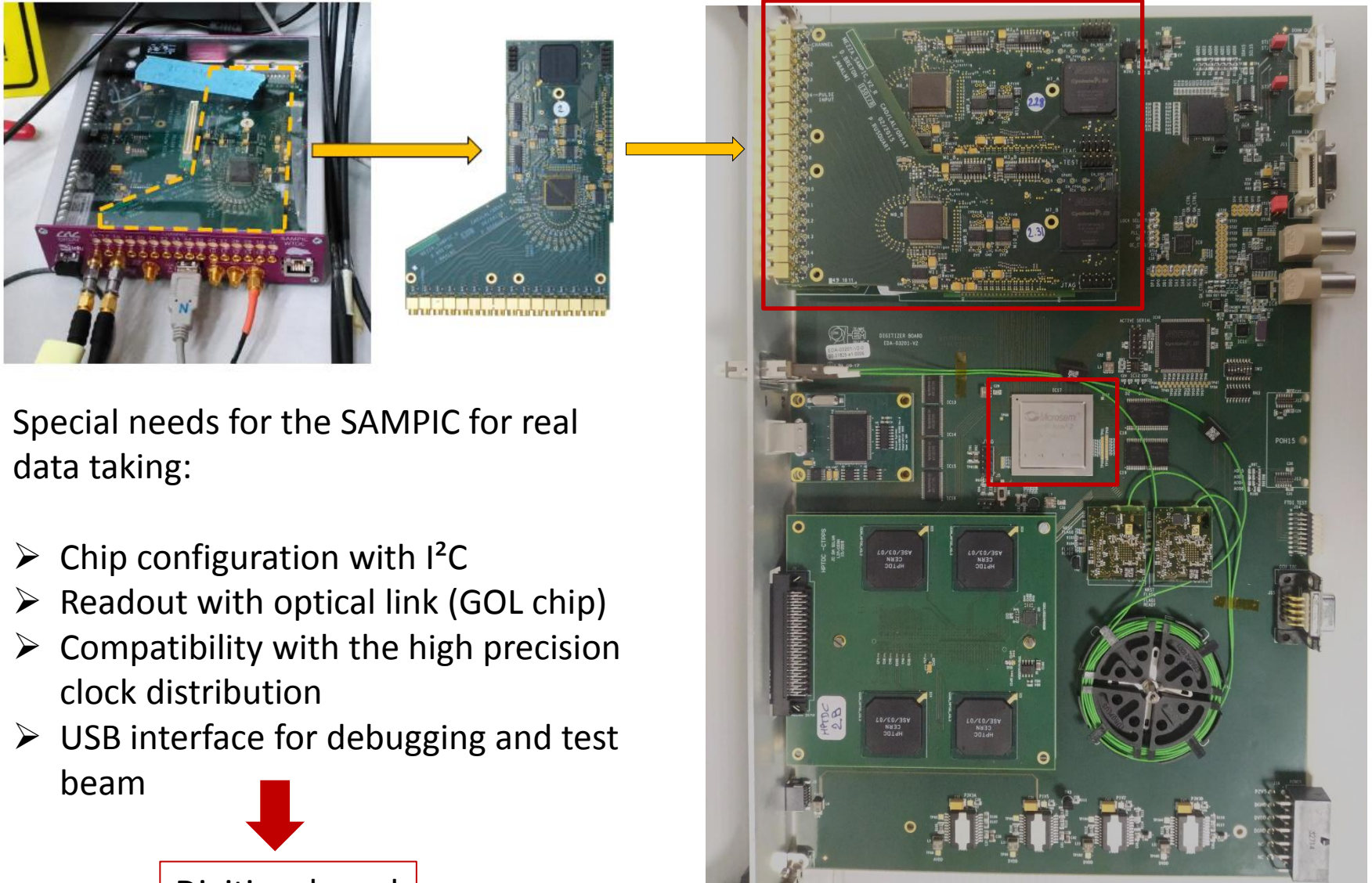
LHC test

Tested in the LHC tunnel in 2015:

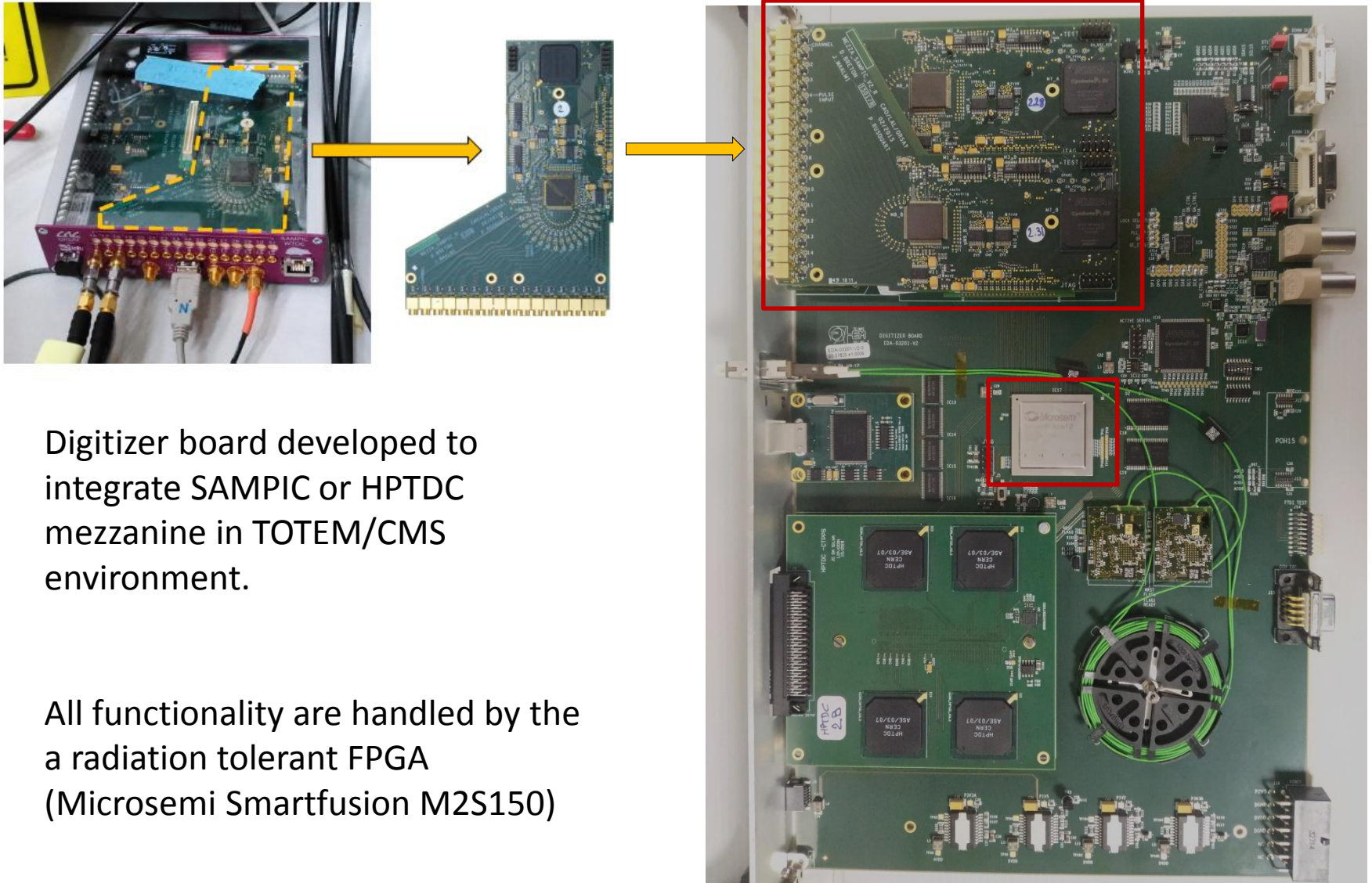
- sCVD diamond detector with ~ 90 ps intrinsic resolution[3] (sensor + amplifier)
- Standard module from LAL
- 6.4 GSa/s with 11 bit ADC resolution
- No loss of resolution compared to oscilloscope!



Mezzanine integration



Mezzanine integration

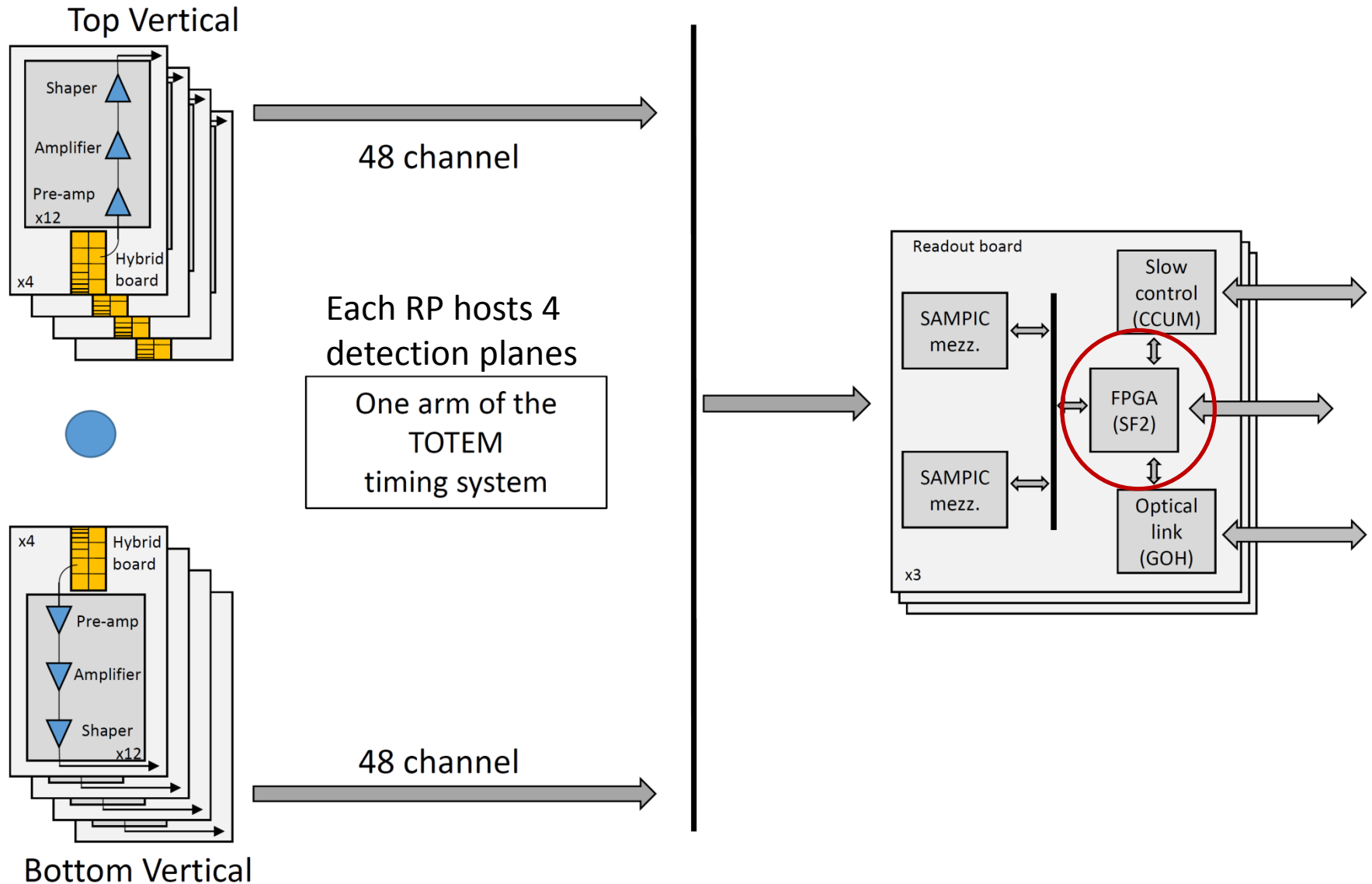


Digitizer board developed to integrate SAMPIC or HPTDC mezzanine in TOTEM/CMS environment.

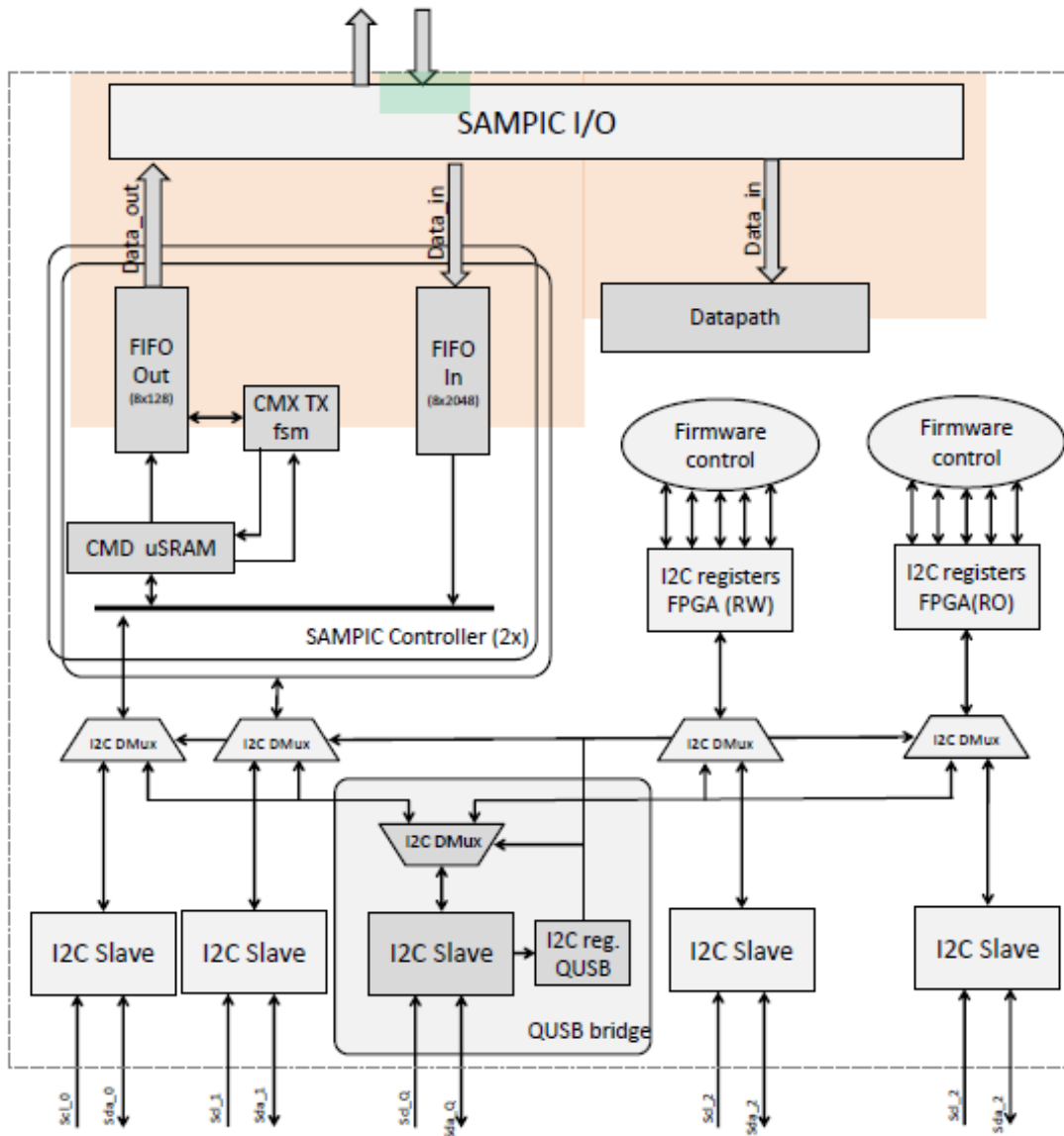
All functionality are handled by the a radiation tolerant FPGA (Microsemi Smartfusion M2S150)

More details in G.Antchev talk!

TOTEM TOF system

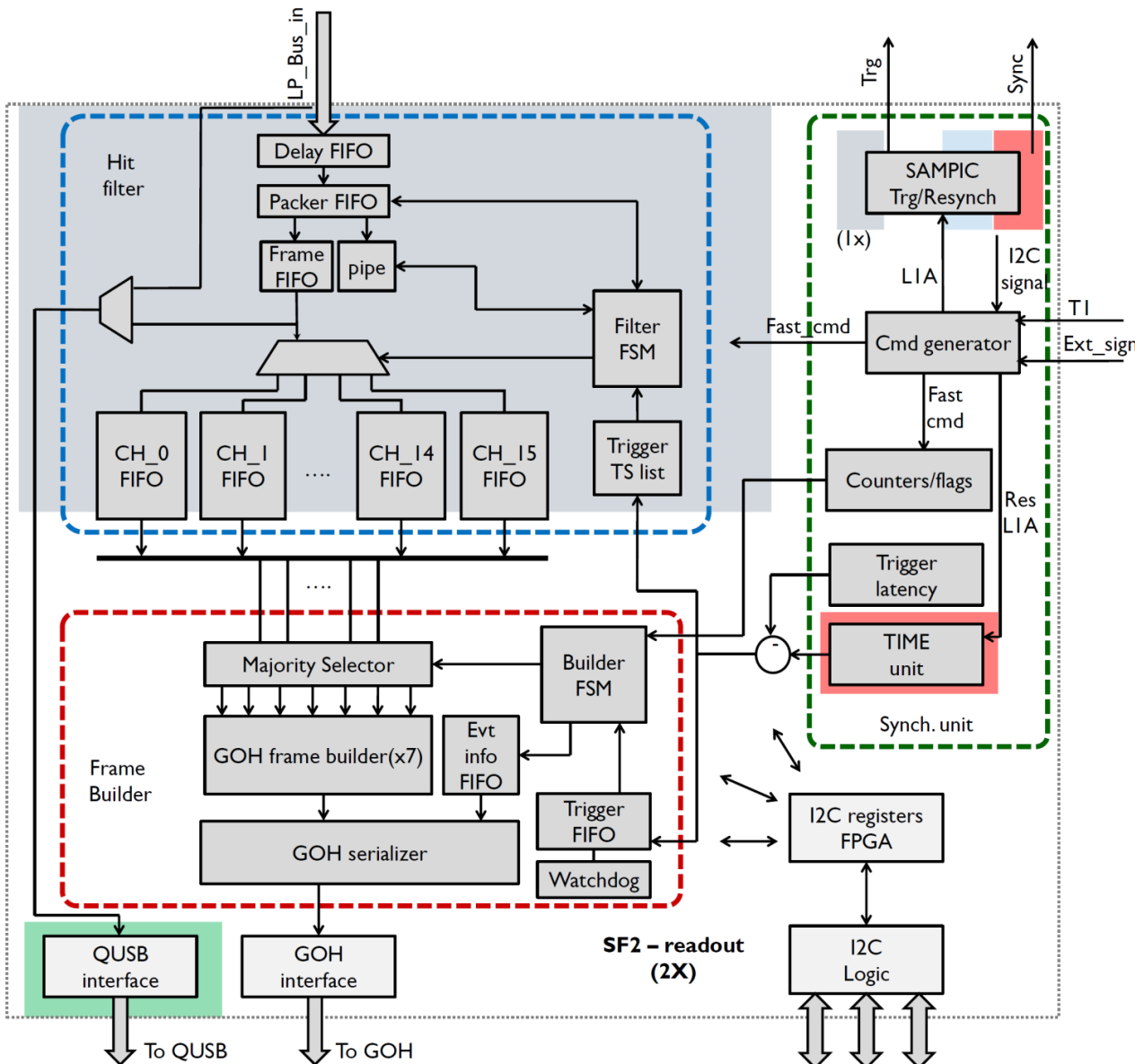


Control firmware



- 4 slave I2C:
 - FPGA register
 - 2xSAMPIC config
 - 1 QUSB
- Control system shared by QUSB and TOTEM control system to allow maximum testability
- Firmware builds LPBUS data packet compatible with SAMPIC mezzanine
- Check of SAMPIC configuration packet available

Readout firmware



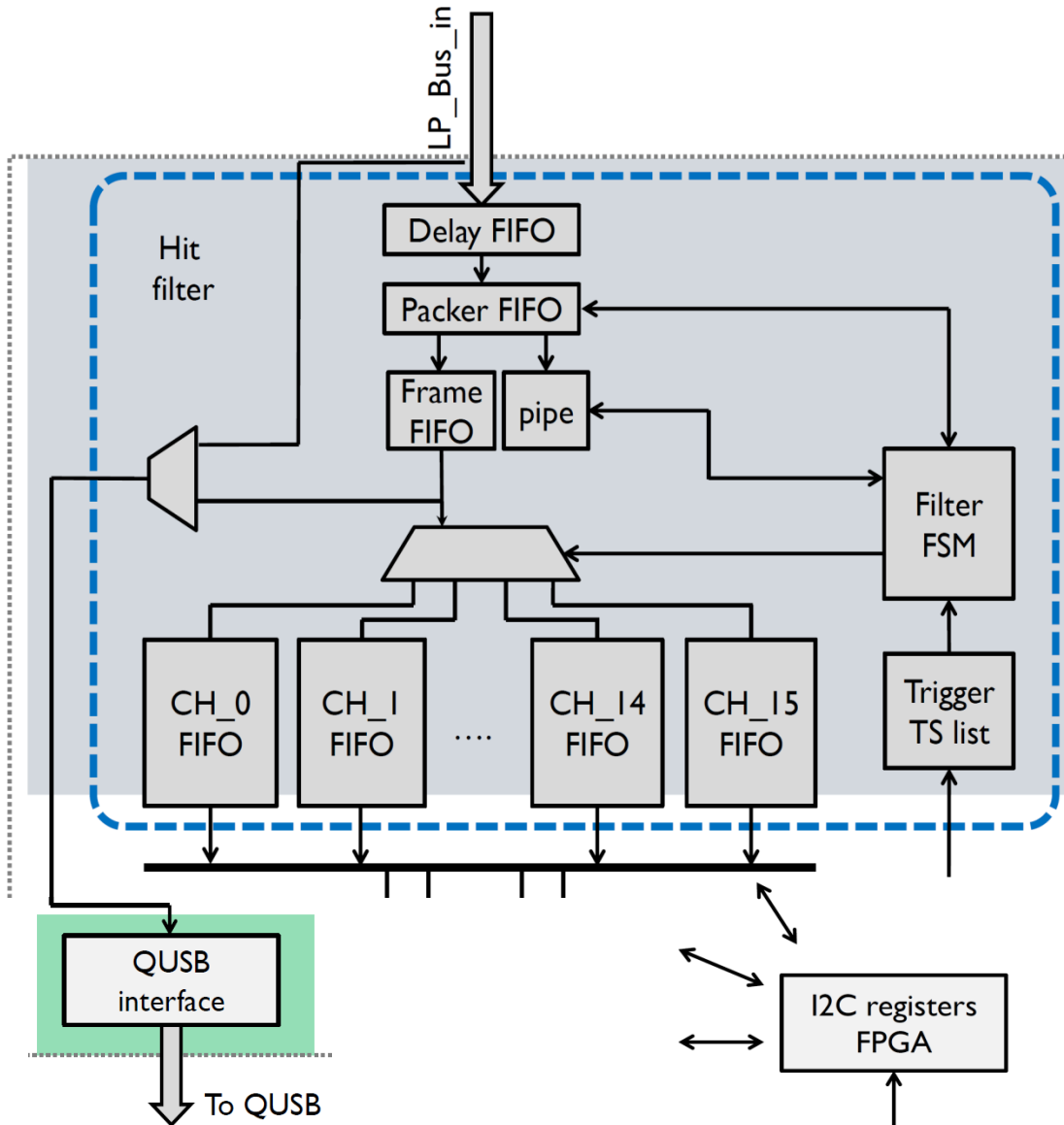
Trigger latency ~ 6 us
 1 Frame for each trigger
 No frame if no trigger
 Max frame size ~ 350 B
 Trigger rate up to 100kHz



Hit selection, frame building and data reduction to be done inside Digitizer central FPGA (Microsemi SF2)

SF2 - readout (2X)

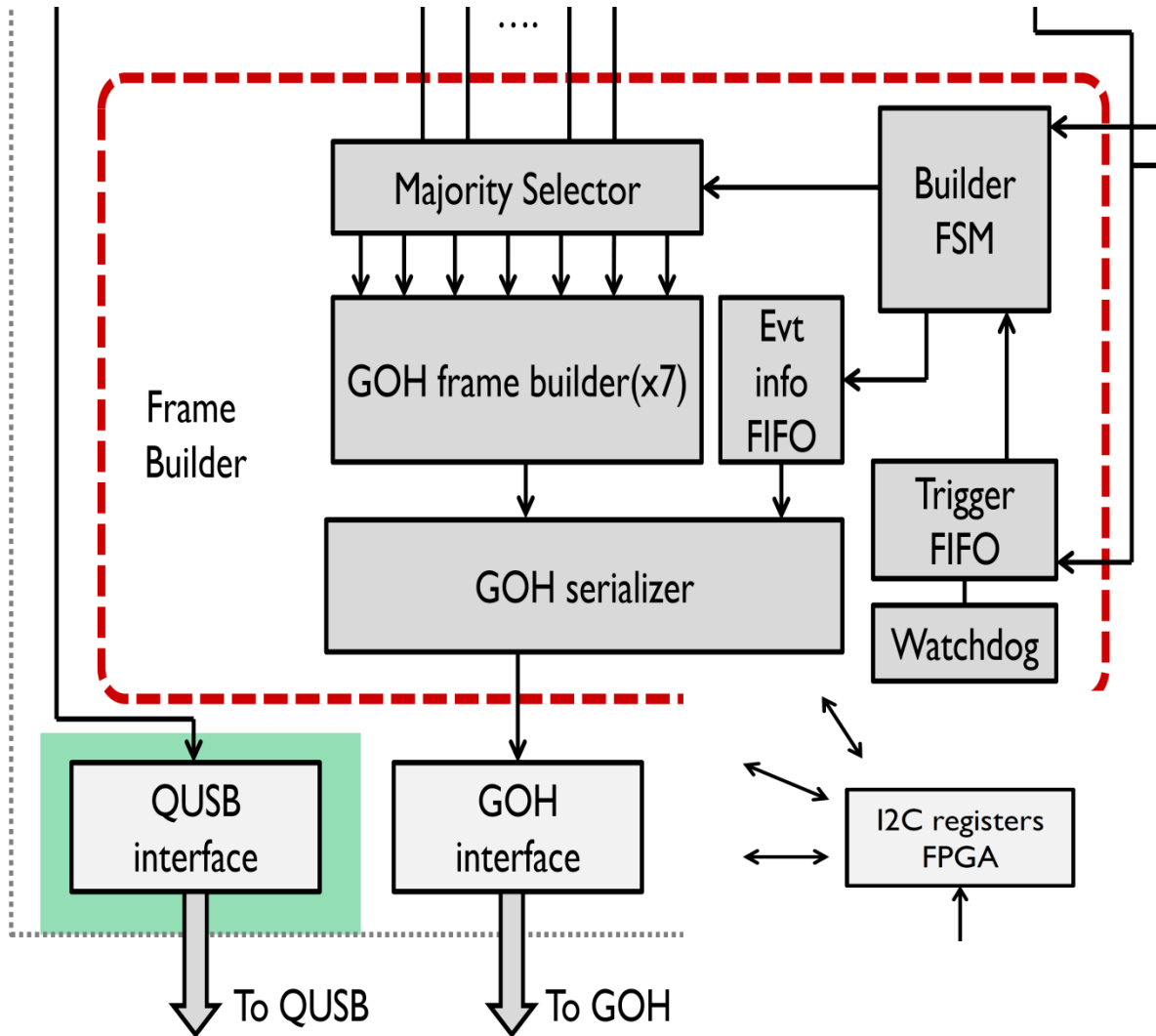
SAMPIC hit filter



Frame Filter

- Delay of incoming frames
- Check frame integrity (header, trailer, WC)
- Timestamp reconstruction and matching with trigger list
- Event rejected or send to channel FIFO
- USB readout available

DAQ frame builder



Event builder

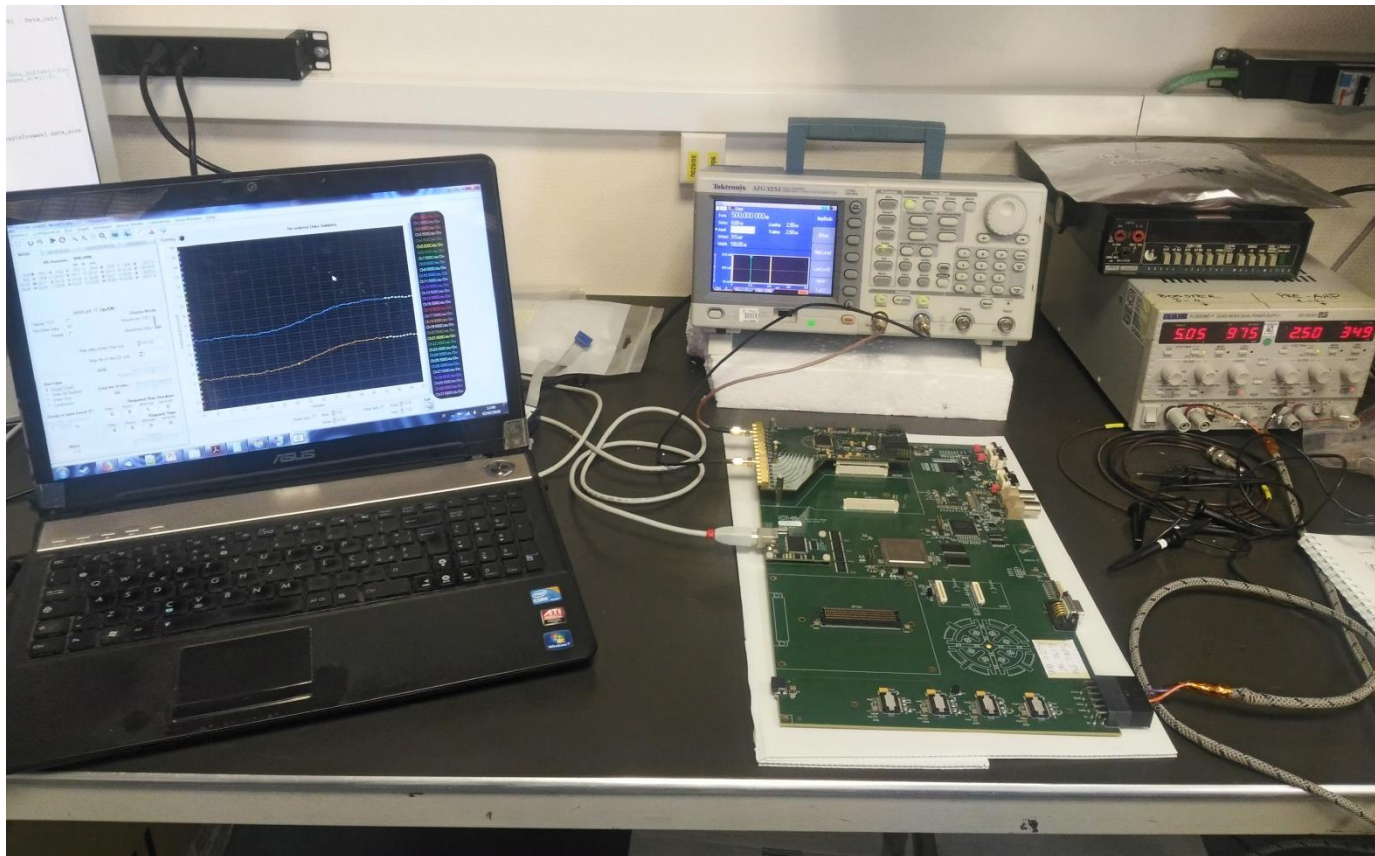
- Selection of up to 7 matching channels
- Event built after ~100 us from trigger arrival to collect all frames
- Assembly of global event info
- Data reduction (factor ~ 0.5)
- Serialization of the event stream
- GOH output (16 bit data bus)

Actual SAMPIC configuration:

7.8 Gsa/s @ 8 bit resolution
24 samples

Project status

- Full system under test in Lab.
- All board functionalities successfully tested. Readout chain fully working.
- Expected to be installed in the tunnel in 4 weeks from now



Future needs in HEP

Even more challenging for LHC phase II with expected rates up to 3/4 MHz for each channel:

- Present Sarpic bottleneck (Self-triggering mode needed) in data transfer out from the chip. Can be improved by integrating the SAMPIC chip in the motherboard, allowing to profit of the 12 bit LVDS connection, but still not enough.
- Only a fraction of the hits must be readout (L1 trigger rate $\sim 100\text{KHz}$)



Need internal buffer to give the time from the L1 to reach back the chip (up to 6 us)

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Thank you for your attention

References:

- [1] G.Antchev et al. (TOTEM collaboration), JINST 12 P03007 (2017)
- [2] R.Arcidiano et al., JINST 12 no.03, P03024 (2017)
- [3] M.Berretti et al. JINST 12 P03007 (2017)

Diffractive physics

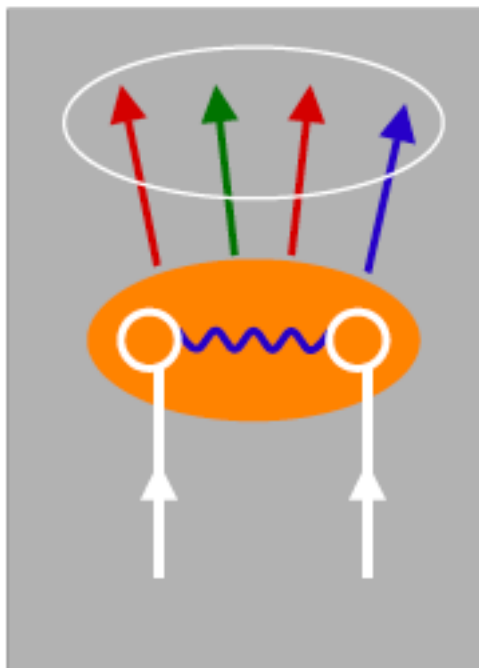


Non-diffractive

- Exchange of quantum numbers possible
- Rapidity gaps exponentially suppressed

$$dN/d\Delta\eta \sim e^{-\Delta\eta}$$

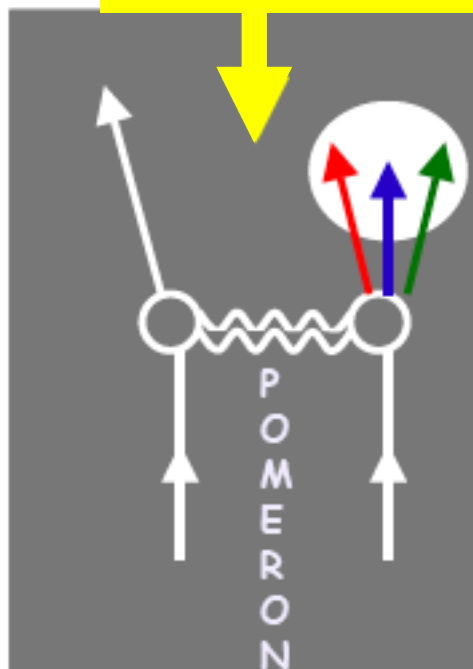
Incident hadrons acquire color and break apart



Diffractive

- No exchange of quantum number
→ no color exchange
- Rapidity gaps constant
 $dN/d\Delta\eta \sim \text{const}$

Rapidity gap



Well described by the Regge phenomenological model.

Diffraction is modeled as an exchange of one or more "objects" with vacuum quantum number, the Pomeron

One or both hadrons can survive the interaction.