WaveCacher and Sampic Workshop

Experience form the HGTD timing application on laboratory and test beam environment

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•Overview

Introduction

- ATLAS HGTD
  - Upgrades: Towards HL-LHC
  - Geometry and integration
  - Sensor technology and design

Sensor testing

- Time resolution & lab testing
  - Test-bench setup – Oscilloscope vs SAMPIC
  - Rise time, pulse shapes and time resolution
  - Sampic trigger time correction
  - Beta run results

Test beam case

- Testbeams
  - Typical Setup
  - Sampic Trigger time and integration

Conclusions

- Suggestions and outlook

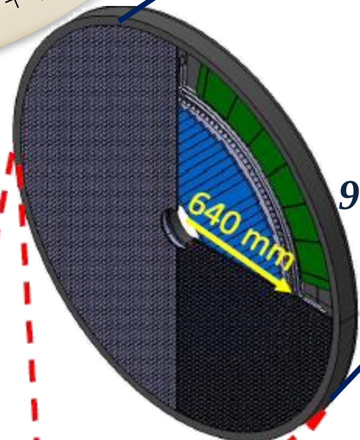
• Phase 2 Upgrade, towards HL-LHC

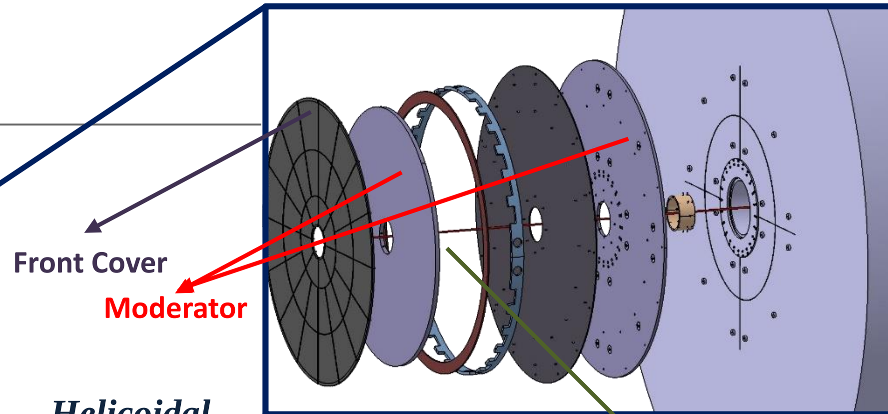
•HGTD System

Geometry

Specifications for 2023	
Coverage	$2.4 < \eta < 4.0$
R_{min}	12 cm
R_{max}	64 cm
Δz	~ 3.5 cm
Δt	< 50 ps
Cell Size	1.7 mm^2

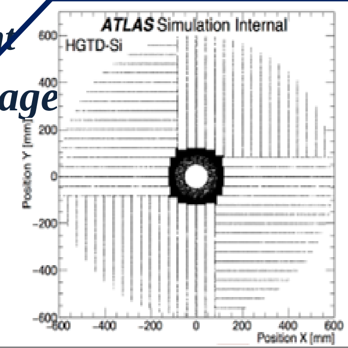
High Granularity Timing Detector
2 + 1 Si layers

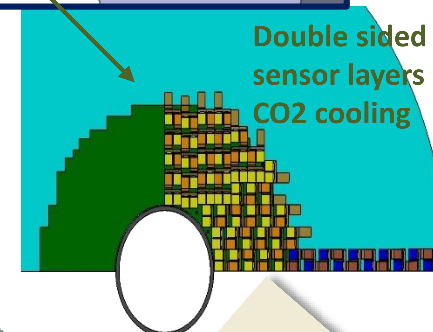


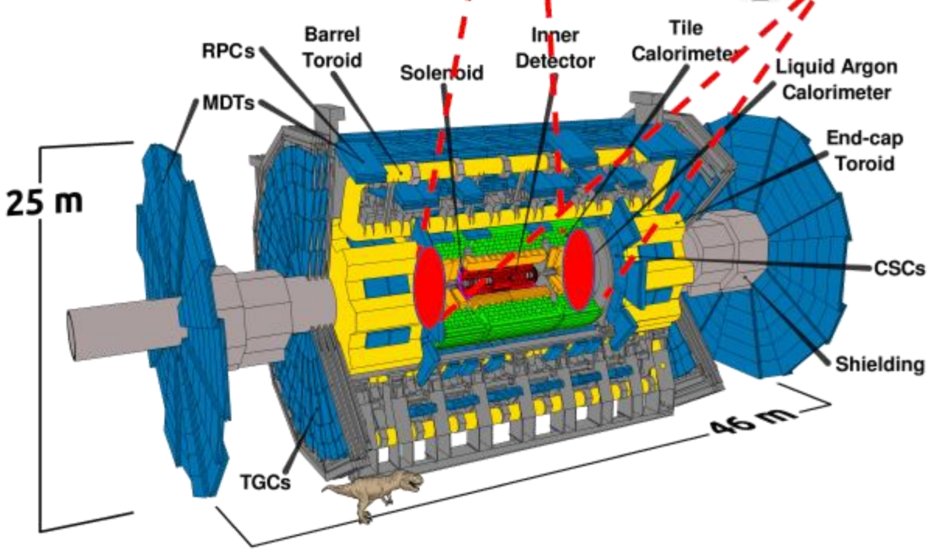


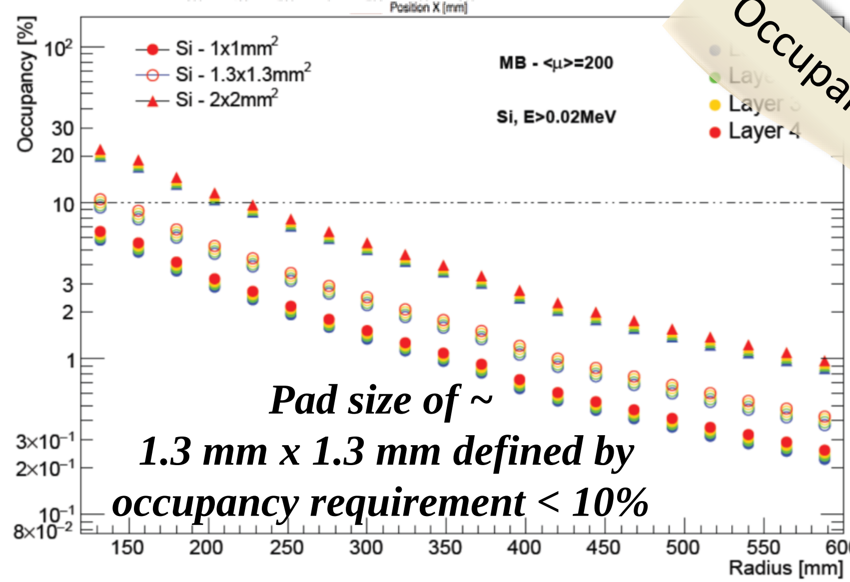
Helicoidal arrangement

91.8 % coverage







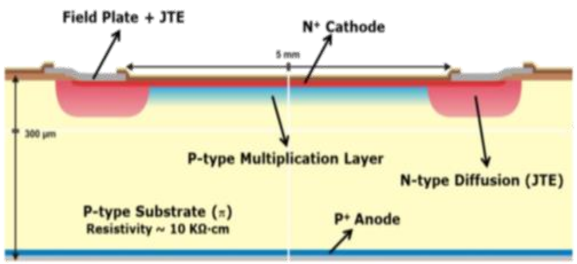


Occupancy

Pad size of ~ 1.3 mm x 1.3 mm defined by occupancy requirement < 10%

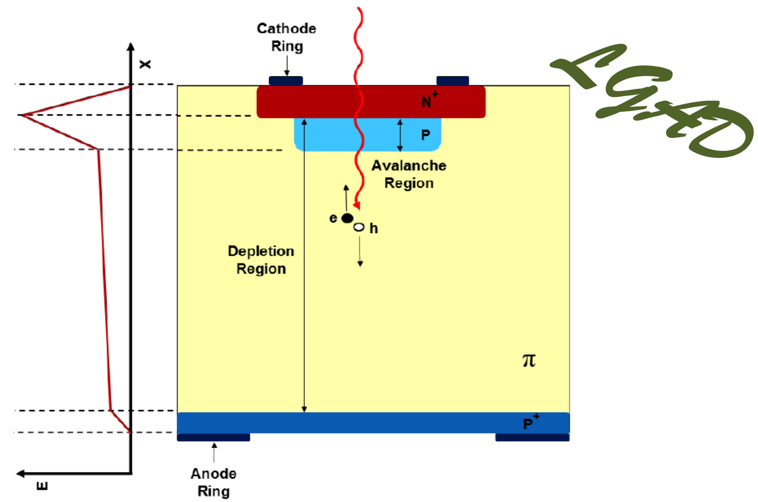
• Sensors

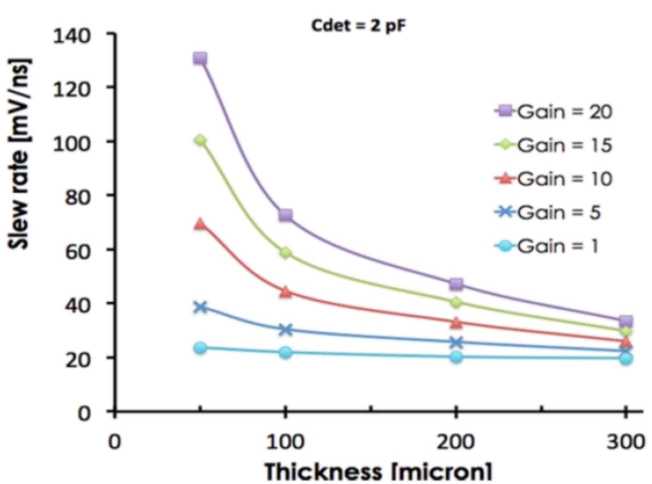
LGADs



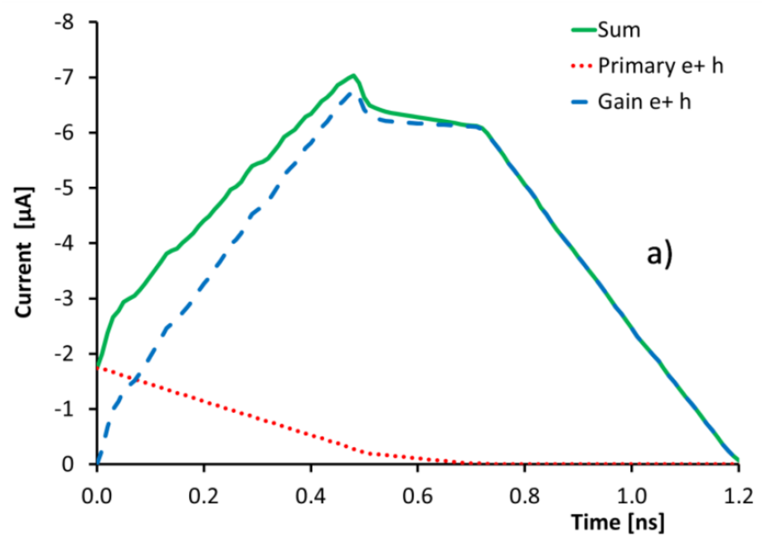
Low Gain Avalanche Diodes (LGAD)

- ✓ Primary technology for ATLAS - CMS
- ✓ Secondary implant introducing moderate gain
- ✓ HPK, CNM, FBK & Micron producing





H.-W. Sadrozinski, A. Seiden and N. Cartiglia, 2817 4-Dimensional Tracking with Ultra-Fast Silicon Detectors, arXiv: 1704.08666.



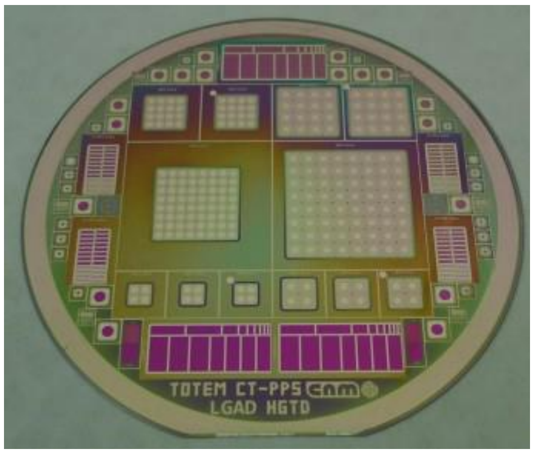
F. Cenna et al., Weightfield2: A fast simulator for silicon and diamond solid state detector, 2822 Nucl. Instrum. Meth. A796 (2015) 149.

• Sensors

Fabrication

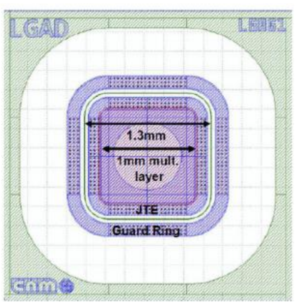
Technology development and initial productions for R&D done at **CNM (Barcelona)**

- Productions in collaboration with Totem (CMS) and RD50
- Now FBK (Italy) and HPK (Japan) also producing LGAD sensors

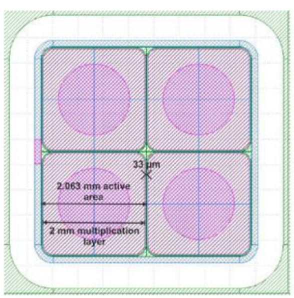


First production

- 4” SOI wafers
- 50 µm thickness on 300 µm support wafer
- Different implantation doses
- Various structures including:
  - Pad diodes of 1.3x1.3 mm^2
  - 2x2 arrays of 2x2 and 3x3 mm^2 pads
  - Larger structures for different applications



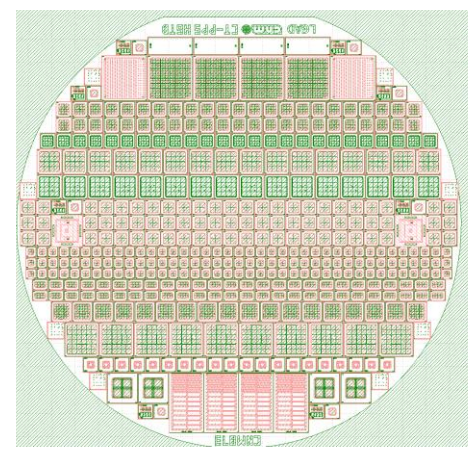
Single Diode



2x2 array

Specific HGTD wafers

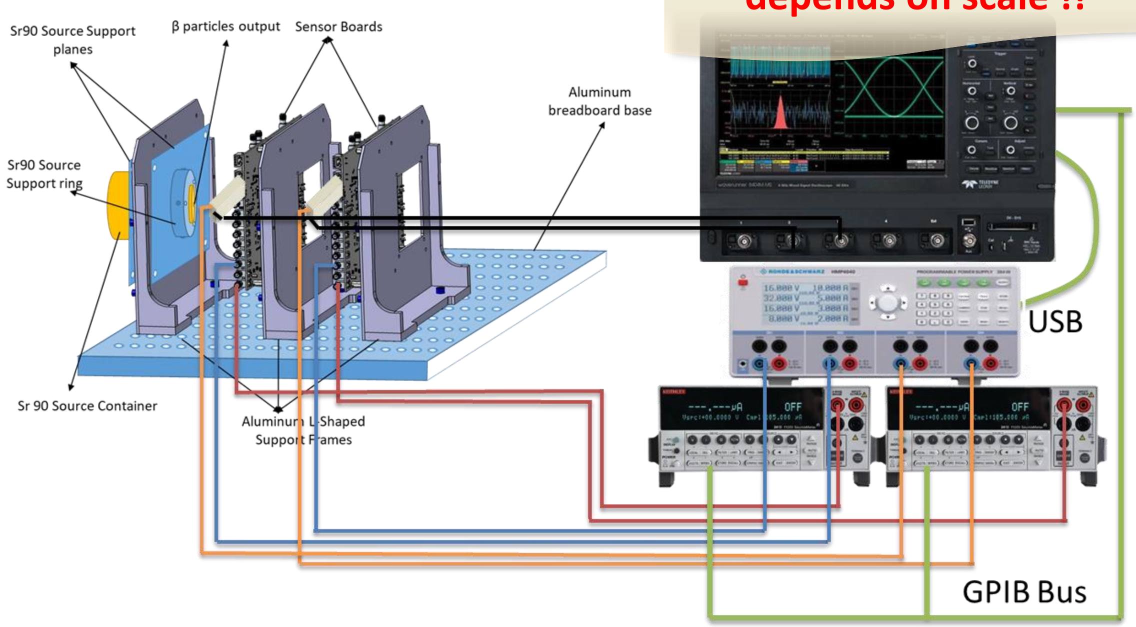
- 6” Si-on-Si wafers
- 50 µm thickness on 250 µm support wafer
- Different implantation doses including Gallium and Carbon
- Various structures including:
  - Pad diodes of 1.3 x 1.3 mm
  - 2x2 arrays of 1 x 1 mm pads
  - **5 x 5 arrays of 1 x 1 mm pads**



• Lab tests

Sr^{90} Timing Setup

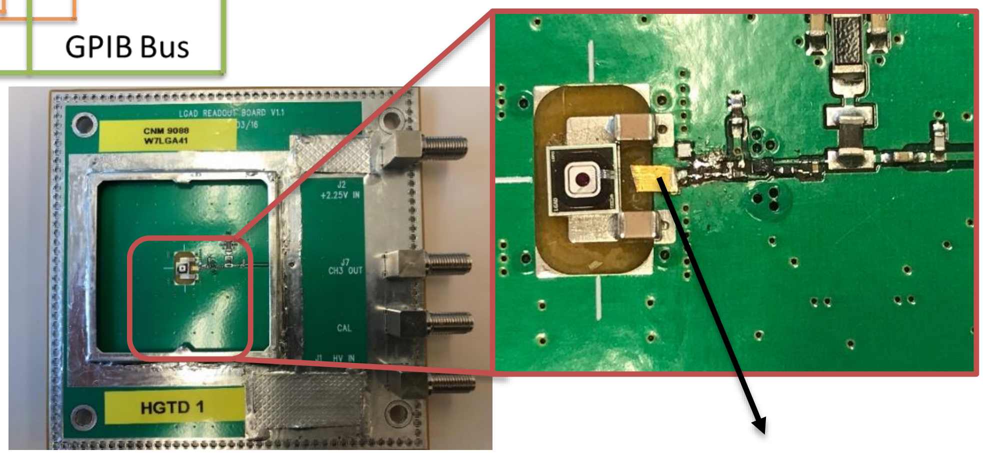
Minimum ToT to trigger depends on scale !!



Minimum Configuration

Board type	Sampic	LeCroy WR
Channels	16	4
Sampling Rate	8.4Gs/sec	20 Gs/sec
Impedance	50 Ω	50 Ω
Connectors	MCX, SMA, USB, Ethernet	BNC, USB, GPIB slave
Bandwidth	1.6GHz	5GHz
Resolution	8 – 11 bit	8 bit (11 tough fit)
Dynamic Range	1V	Scale dependent

- High frequency SiGe (~2GHz) common emitter first stage charge amplifier (470 Ohm transimpedance)
- Integrated commercial second stage GaAs microwave voltage amplifier (gain of 10, 50Ohm line)
- Mean sensor + amplifier noise < 2.5 mV
- Use of identical sensors for calibration and comparison (Run 9088, W5LGAxx – 1.3mm)

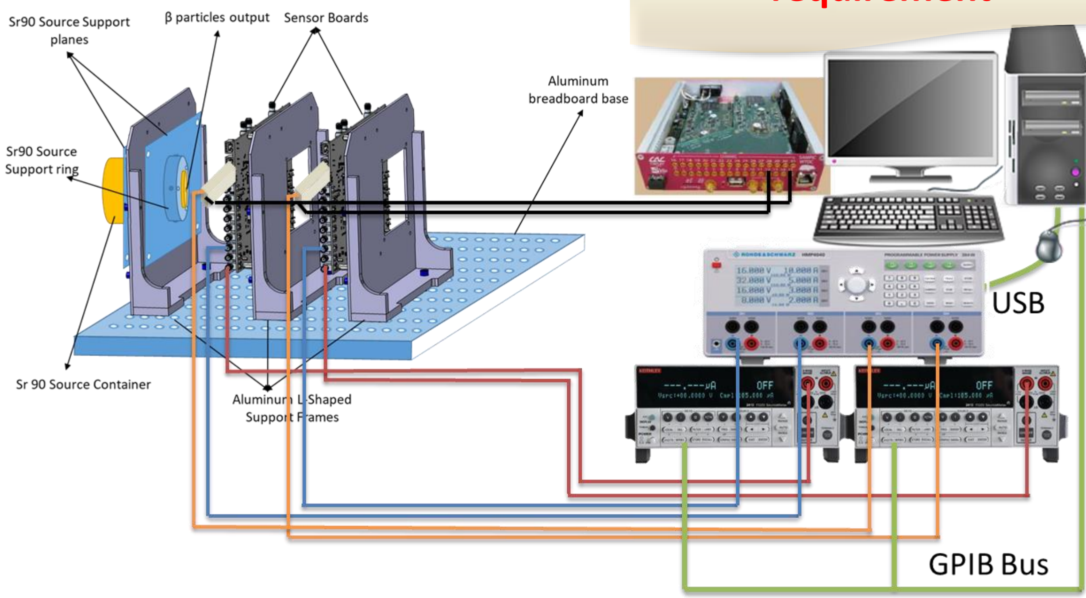


Multiple wires for low inductance
0201 smd components for low parasitic

• Lab tests

Sr^{90} Timing Setup

No minimum ToT requirement



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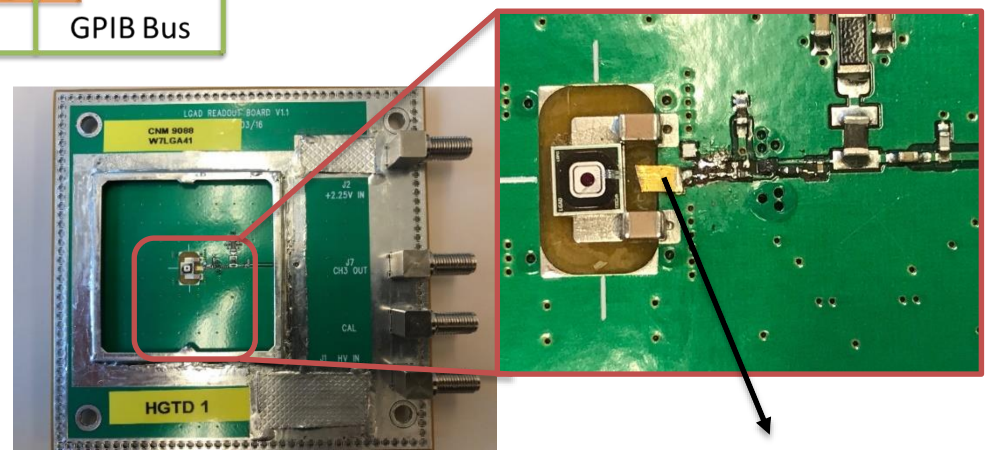
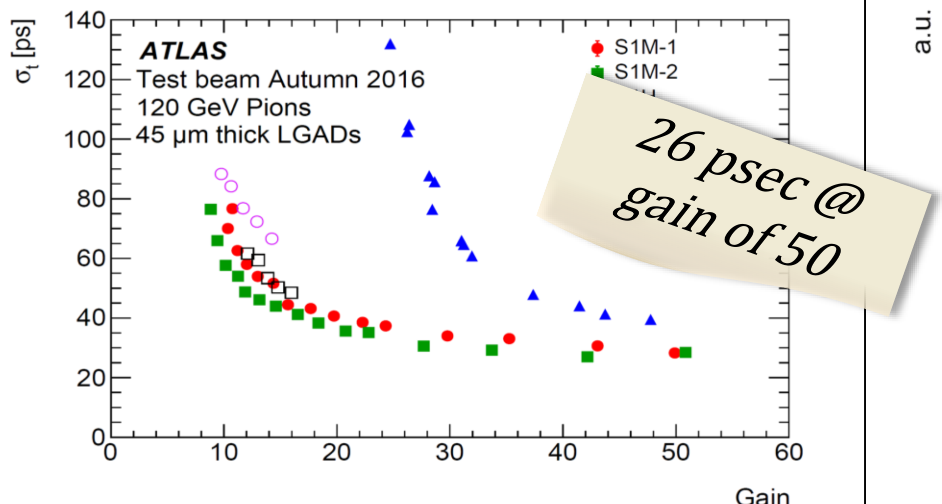


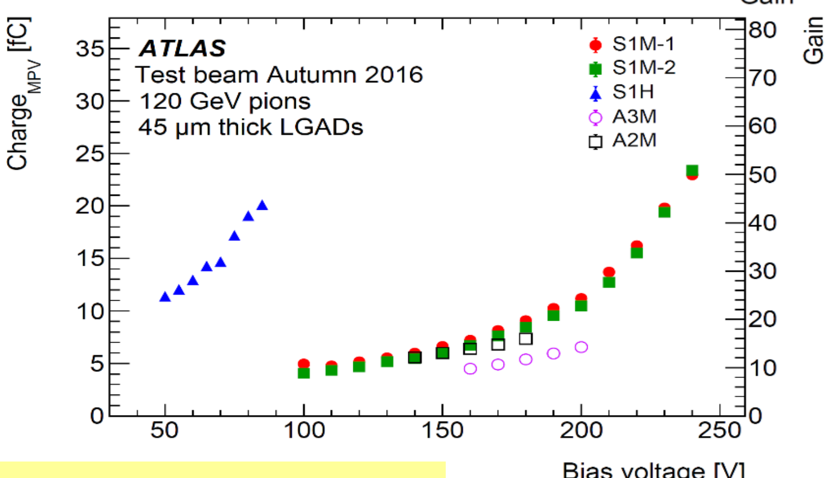
Multiple wires for low inductance
0201 smd components for low parasitic

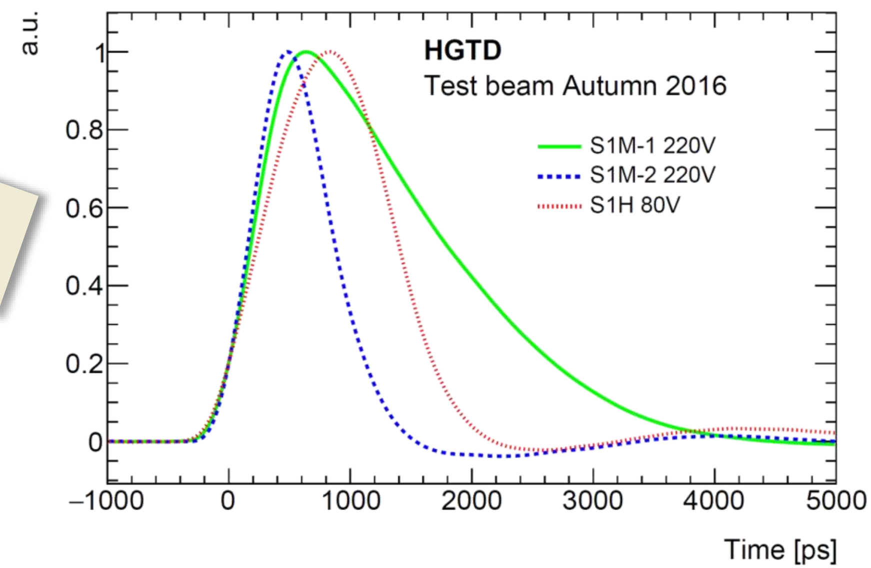
•Expected Results

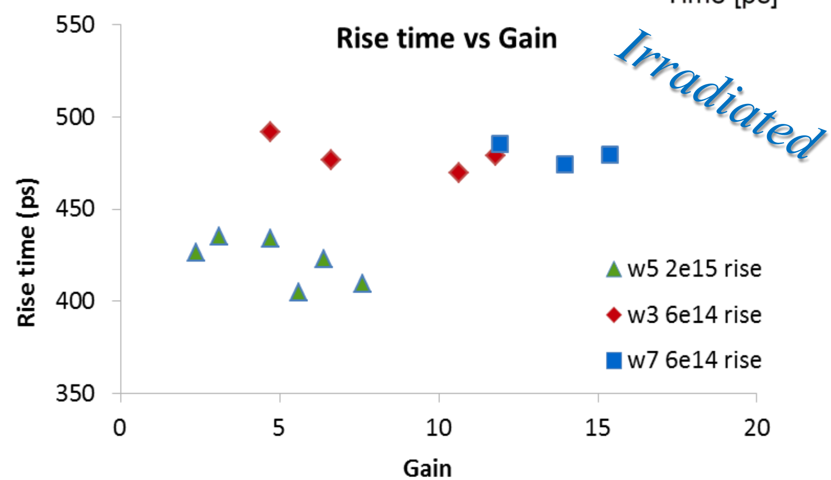
Pulse specifications

Non Irradiated









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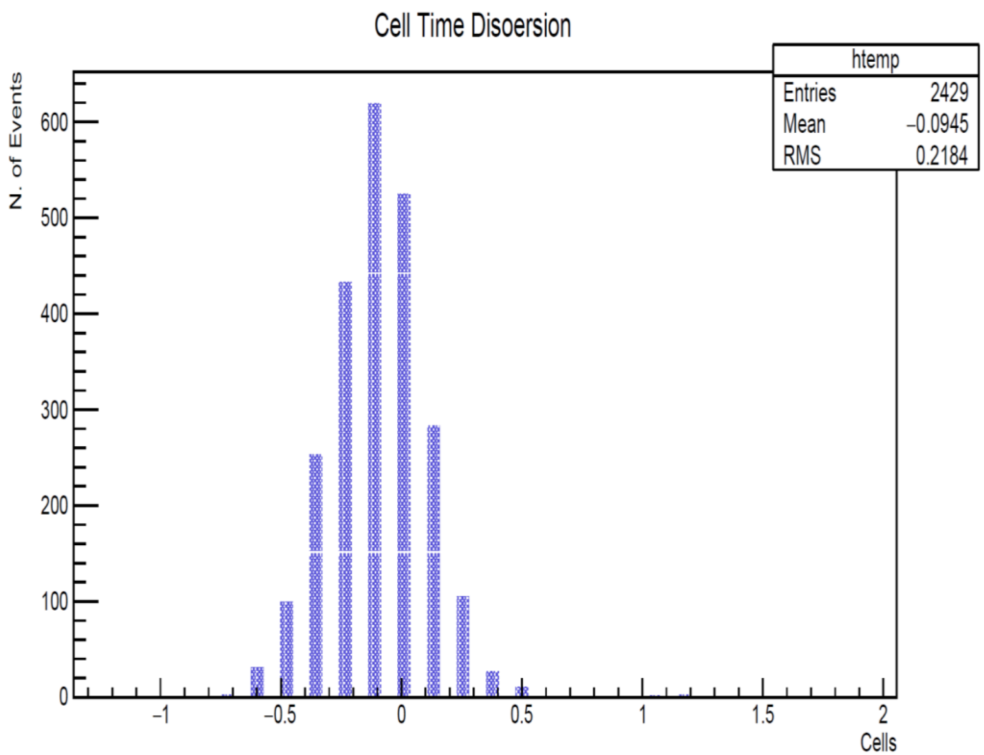
•Sampic Runs

Trigger time correction



2 LGAD Run	
Channels	2
Sampling Rate	8512 MS/s
Sampling time	117 psec
Acquisition window	7.52 nsec

- *Time bin of 117 psec too large to see trigger delays*
- *Both channels should trigger simultaneously*
- *Trigger time between the two channels presents a Gaussian peeked at 0*

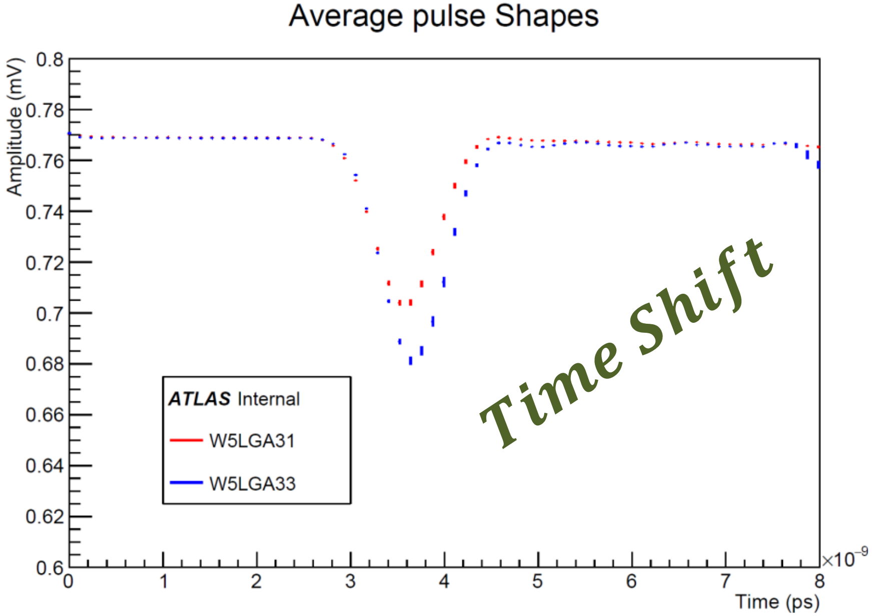
Correction

Time for each channel needs to be recalibrated with respect to a channel of reference

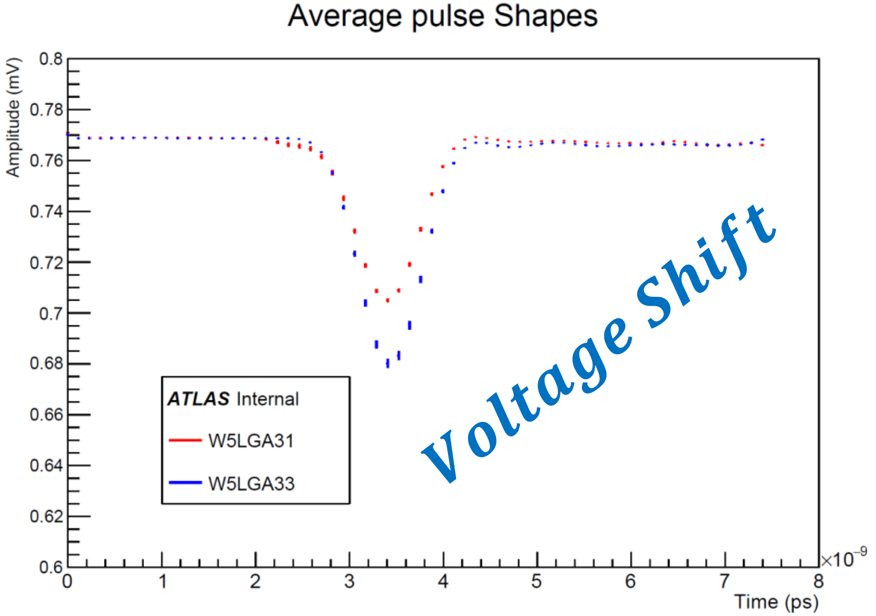
•Sampic Runs

Trigger Time Corection

Tow possible correction methods



- Assume that reference channel start always at 0
- Adjust the start time of additional channels to compensate trigger time mismatch



- Assume all channels start at 0
- Shift voltage values to any of the channels to the end of the waveform to compensate for trigger mismatch
- Works for small mismatches

•Sampic Runs

Time resolution results

Both methods give similar results:

- Linear fit 20% - 80% analysis on rising edge
- Results may be improved by global fit on pulse shape
- Not more than 10 % - 20 % improvement

2 LGAD Run	
Time resolution	40 psec (26 psec with oscilloscope)
Jitter	34 psec

Trigger:

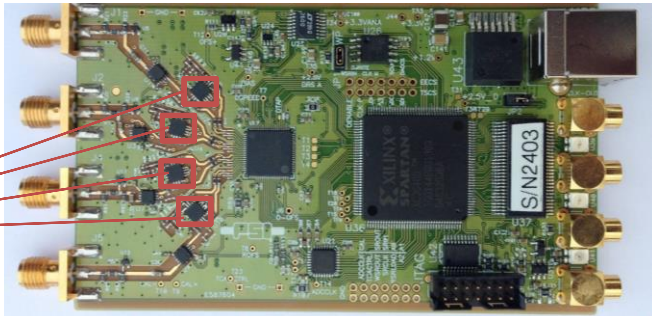
- Self trigger on either channels
- No coincidence implementation
- No internal buffer, no opportunity for combined trigger with tracker
- Only independent operation possible

2 LGAD Run	
Registered Events	2452860
Coincidences	2429
Efficiency	0.1 %
Thresholds	20 mV
Trigger Mode	Self Trigger

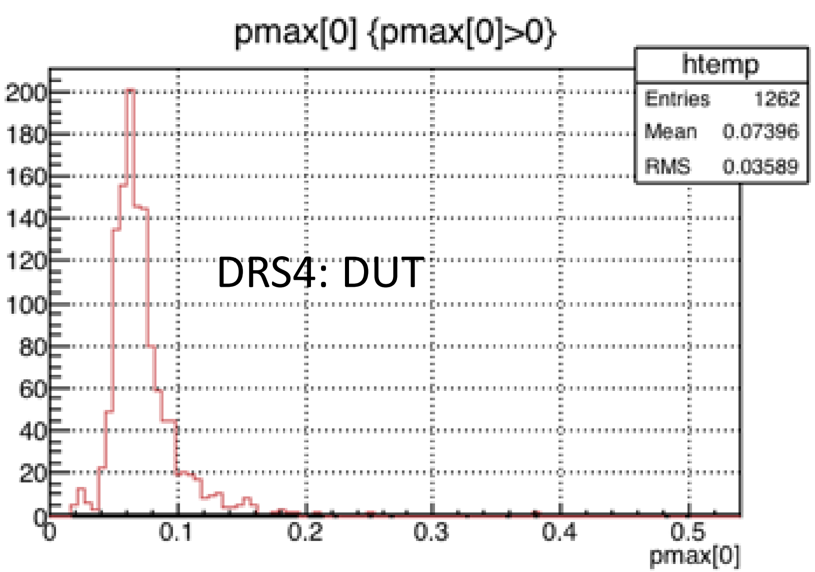
•Other Solutions

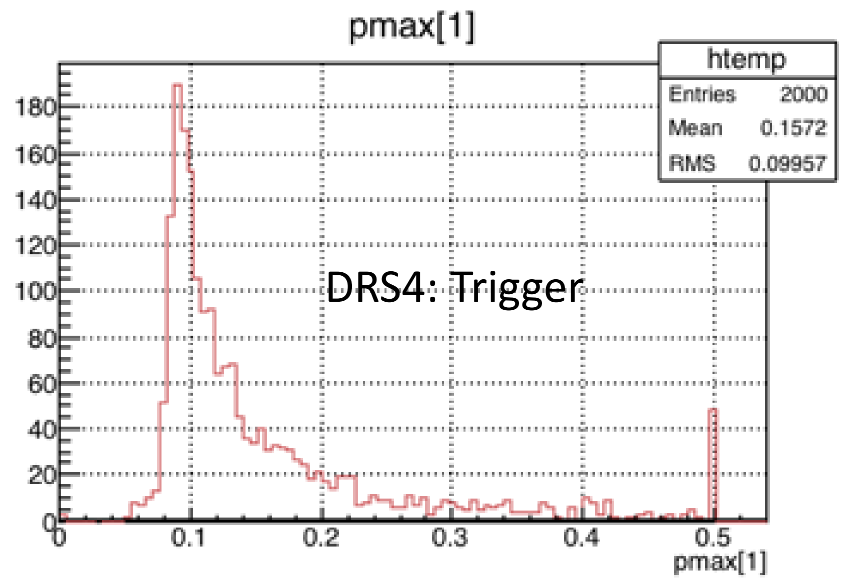
DRS4 – Capacitor arrays

Ti discriminator with a 1.2 nsec minimum ToT requirement



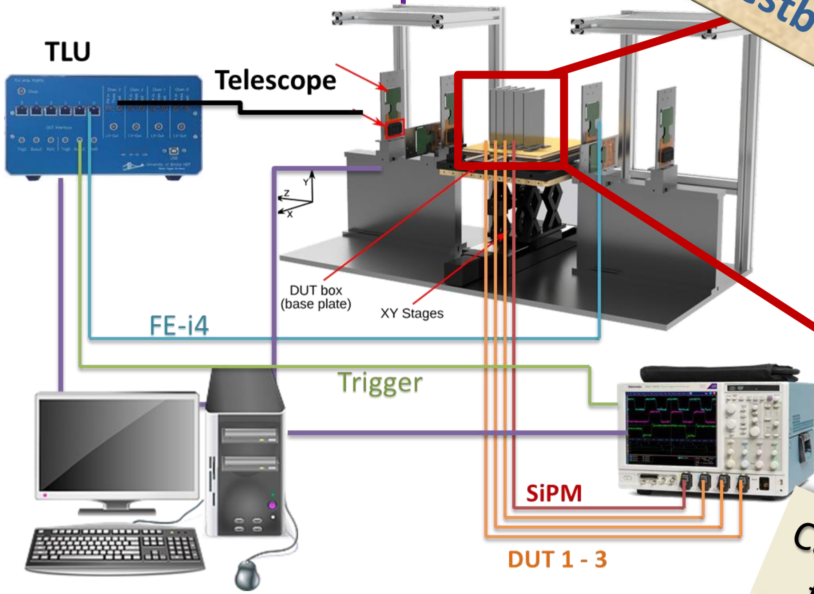
- For the DRS4 the set-up time is 1.2 ns, i.e. 6 time bins. So the data we took at 20 mV threshold gave only pulses with pulse height above 80mV: can't evaluate the timing resolution of DRS4 for our present amp which minimizes the pulse width.



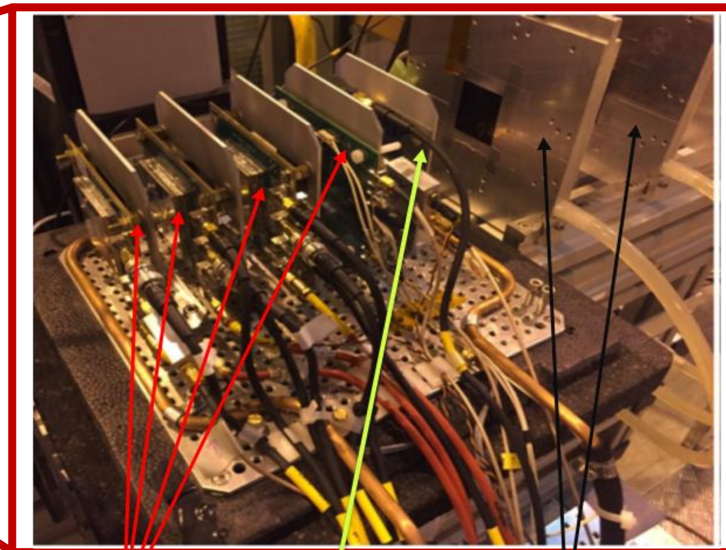


• Test beam case

Current Setup



Testbeam



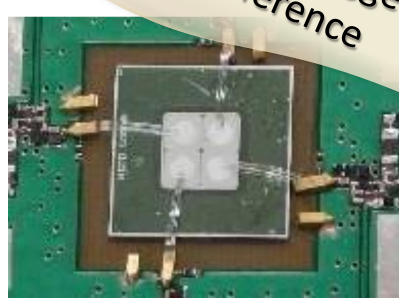
CERN HGTD Testbeams (120 GeV pions)

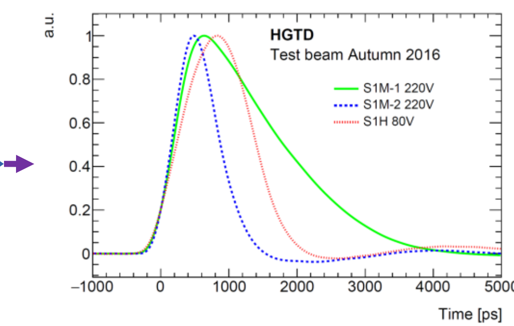
- ✓ Trigger form FE-i4 plane (25nsec timing)
- ✓ Tracking with MIMOSA planes (200nsec)
- ✓ Trigger distribution from ALU (30nsec decision time)
- ✓ Oscilloscope only accepts trigger, does not do coincidences

Requirements

- ✓ Able to support the 55nsec delay
- ✓ Implement busy (veto) for MIMOSA redout

Can include trigger time reference





Sensor   Amplification   Oscilloscope

• Test beam case

Sampic integration requirements

- ✓ Tow possible trigger scenarios
  - ✓ Have a 60 nsec buffer to wait for trigger decision from EUDAQ
  - ✓ Do a first level coincidence trigger and have a hold-off time of 60 nsec to wait a TLU decision
  - ✓ Since no minimum ToT requirement, second case more promising
- ✓ Need a Veto function to wait for the MIMOSA readout time
- ✓ Develop C/C++ libraries for integration with EUDAQ framework and universal data acquisition and monitoring
- ✓ Implement the time trigger correction within the EUDAQ framework and applied before data store on the fly
- ✓ Increase rate to 10Gs/sec to avoid degrading time resolution, current state may be corrected via signal fit

• Conclusions

Suggestions and Outlook

- ✓ Need a multi-channel fast read-out for future test beam and lab measurements
- ✓ Sampic initial results demonstrate 40psec resolution with possibility of 10-20% improvement
- ✓ In lab implementations need coincidence trigger and 10Gs/s rate
- ✓ Testbeam implementation requires hold-off time, veto and coincidence implementation, C/C++ libraries
- ✓ Very promising multichannel solution because of no minimum ToT for trigger