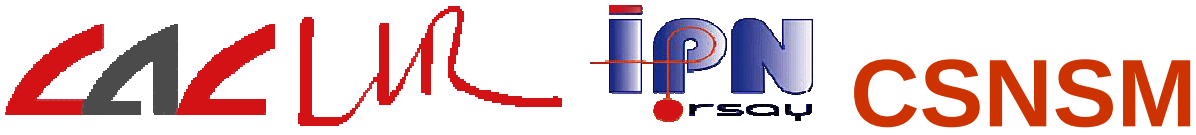
First Annual Report to the Administration Council

July 4th 2008



1. Introduction

The Omega convention has been officially signed in October 2007. The first months of Omega activity have been useful to point the advantages and limits of the structure.

1.1. Productivity increase

Having a critical mass of designer closer from each other in a well defined structure in which experience and knowledge can easily be shared improve noticeably the productivity and the capability to handle complex projects. Having several engineers working together on many experiments or R&D designs involves a very strong emulation conducting to a very efficient team work.

1.2. Transversal design

Reuse of building blocks from one chip to another allows much faster and efficient design with proved and tested features.

1.3. Communication improvement

Single name and logo for all external communication, own website with chip description, firmware and datasheets

1.4. Cold start up

- Omega borderlines definition inside the electronics group is not clear enough. It involves constraint on projects especially for the test and characterization of ASICs.
- The Integration in the LAL electronic unit is not easy since what should be an interlab structure is less than a unit for administration
- No budget in 2007 and 2008

1.5. Staff

The pole comprises 9 permanent research engineers, 1 CDD Eudet and 1 PhD student and 1 visitor from China (6 months)

- Gisèle Martin Chassard (IR1)
- Nathalie Seguin-Moreau (IR1)
- Christophe de La Taille (IR0), Director
- Vanessa Tocut (IR2)
- Julien Fleury (IR2), Deputy Director
- Ludovic Raux (IR2)
- Sylvie Blin (IR2)
- Frederic Dulucq (IR2)
- Pierre Barrillon (IR2)
- Stephane Callier (CDD IR2 EUDET)
- Selma Conforti di Lorenzo (PhD student ANR PMm2)
- Wei Wei (visitor from IHEP Beijing)

1.6. Teaching

• Gisèle Martin Chassard	Supelec, analogue microelectronics, labs, 16h
• Nathalie Seguin-Moreau	Master MIP, analogue electronics, lectures and training, ups, 9h
• Vanessa Tocut	ISEP, mixed electronics, lectures and training, 60h
• Julien Fleury	ENSTA, digital electronics, training, 24h
• Ludovic Raux	ENSTA, digital electronics, training, 24h
• Sylvie Blin	ISEP, mixed electronics, training, 60h
• Christophe de La Taille	Supelec, analogue electronics, lectures, training and labs, 40h
• Stephane Callier	ESIEE, RF&HF measurement, labs, 16h
	EFREI, mixed microelectronics, lectures and training, 30h

2. Manpower commitment

%	ANR			EU	IN2P3			TOTAL		
	2006 PMm²	DHCAL 2007	VITESSE2008	EUDET 2006	LSST	SuperNemo	ATLAS Lumi	ANR+EU	IN2P3	GRAND
Pierre Barrillon	30						70	30	70	100
Sylvie Blin	30						70	30	50	100
Stéphane Callier				100				100		100
Selma Conforti	100							100		100
Frederic Dulucq		50		50				100		100
Julien Fleury				100				100		100
Christophe de La Taille	15	25	25	25	10			100		100
Gisèle Martin	25		30	20		25		100		100
Ludovic Raux				100				100		100
Nathalie Seguin		50	25	25				100		100
Vanessa Tocut					60	30			90	90
Wei Wei	25					25		25	50	50
TOTAL FTE	2.25	1.25	0.8	4.2	0.7	0.8	1.45	8.6	2.8	11.4

ANR/EU project commited ratio:		**74%**	i.e.	8,5 FTE
IN2P3 not commited project ratio :		**25%**	i.e.	2,9 FTE
Permanent positions :	9 engineers	i.e.	**78%**	of total FTE

3. Financial report

Omega manages four budget lines. Three of these lines are for self operating and the fourth is managed by omega but is used by all the microelectronics group of IN2P3 to design building blocks and conduct generic R&D on microelectronics features. The building block group has been nicely working in IN2P3 since 2004 and has provided a necessary uniformity in the microelectronics technology used inside IN2P3. That line has been correctly funded to ensure 2008 needs for IN2P3 generic R&D. The Omega operating budget has been left to zero in 2007 and 2008 precluded the new structure to work as it is aimed for. That budget should be used to improve the Omega visibility and its capability to handle new projects especially for promoting trade of public research. It is still not possible for omega to easily provide on the shelf electronics for non-collaborating experiments due to the non-funding of its own activities.

3.1. Omega operating budget

That line is twofold. It funds Omega for its general operating needs (internal testboard, additional packaging, bonding, internal store covering, etc.) and it covers the equipment requirements (Die storage, computers, furniture, etc.)

2008 operating credits needed:	10 000 €
2008 operating credits granted:	0 €
2008 equipment credits needed:	15 000€
2008 equipment credits granted:	0€

3.2. External services budget

That line is used to embank invoices from products sold by Omega. It is also used to pay for the test boards and ASICs sold. It allows providing test boards for labs to test our ASICs and eventually start a collaboration if the ASICs correctly fit the experiment requirements.

2008 credits needed:	5 000 €
2008 credits granted:	0 €
2008 external resources	30 000€
2008 spent (1/7/08)	25 000€

3.3. Travel budget

The travel assignment line is used to expense travels operated for pole aim, such as pole presentation or technical mission assignment for research promoting trade essentially for medical imaging.

2008 credits needed:	15 000€
2008 credits granted:	0€
2008 spent (1/7/08)	5 000€

3.4. External contracts

3.4.1. European contract EUDET (2006-2010)

R&D for detectors at the ILC. Calorimetry : design of chips for ECAL, AHCAL and DHCAL.
36 ppm engineer + 130k€ chip foundries.
JRA3 : coordination of JRA with Felix Sefkow (DESY)
Responsible at LAL for ECAL : R. Poeschl
Responsible at LAL for FEE : C. de La Taille

3.4.2. ANR PMm2 (2006-2009)

R&D for large arrays of photomyultipliers (“square meter PM”).

36 ppm engineer + 130k€ chip foundries.
Responsible for LAL : JE Campagne

3.4.3. ANR DHCAL (2007-2010)

R&D for a cubic meter digital hadron calorimeter at the ILC. 140k€ chip foundry for production of 5000 hardroc ASICs.
Responsible for LAL : N. Seguin-Moreau

3.4.4. ANR vitesse (2008-2012)

3D electronics for trackers. R&D for ATLAS at SLHC.
Responsible for LAL : A. Lounis

4. Collaboration report

4.1. LSST (2006-2010)

Omega is part of the LSST collaboration. It is designing the CCD camera front-end ASIC 'ASPIC' in collaboration with LPNHE Paris.

4.2. ILC Si-W ECAL (2003-2020!)

The Si-W ECAL prototypes designed within the CALICE/EUDET collaboration is read out with Omega ASICs ('FLC_PHY3' and 'SKIROC' in collaboration with LPC Clermont).Prototypes funded by EUDET FP6 program. Production of 1000 ASICs in 2009

4.3. ILC RPC-Fe DHCAL (2006-)

Omega is designing a read-out ASIC for the RPC digital HCAL ('HARDROC') within the CALICE collaboration. Collaboration with IPNL, LLR & LAPP. Production of 5000 chips in 2009.

4.4. ILC Scintillator (SiPM)-Fe AHCAL (2003-)

Omega is designing a read-out ASIC for the Scintillator SiPM Analogue HCAL ('SPIROC') within the CALICE/EUDET collaboration. Collaboration with DESY. Production of 1000 chips in 2009.

4.5. ILC Scintillator (SiPM)-W ECAL(2005-)

Front-end electronics designed for ILC AHCAL is reused to read-out the Sci-Fe ECAL designed by the KEK group within the CALICE collaboration. Collaboration with KEK. Omega is providing technical support on that detector electronics.

4.6. ATLAS luminometer ALFA (2003-2009)

Omega is part of the ALFA luminometer collaboration and has designed the MA-PM read-out ASIC ('MAROC2'). Collaboration with CERN.

4.7. ATLAS luminometer LUCID (2005-2009)

Omega is part of the LUCID luminometer collaboration and has designed the MA-PM read-out ASIC ('MAROC3'). 1000 ASICs produced in 2008.

4.8. ATLAS tracker (2007-)

Omega is part of the collaboration on 3D electronics R&D for ATLAS tracker with CPPM.

4.9. Double Chooz (2007-2008)

Omega has provided a small production of MAROC2 chips to readout the muon veto tagger. Collaboration with NEVIS labs. 250 ASICs produced in 2008

4.10. PMm² (2007-2010)

Omega is part of the generic research program PMm² (funded by ANR) aimed to reduce cost on high area of PM detectors. An ASIC ('PARISROC') has been designed for that program. Collaboration with IPNO, LAPP.

4.11. SuperNemo Front-end (2008-)

A readout ASIC (PARISROC) has been adapted to read out the supernemo calorimeter.

4.12. SuperNemo SNATS (2008-)

Omega has designed a time stamper in collaboration with LPC Caen for supernemo calorimeter.

4.13. SymbolX (2008-)

A Maroc test board has been provided by Omega to perform irradiation tests for the spatial experiment. SymbolX by APC lab.

4.14. North Auger (2004-2007)

Omega has designed a set of current-feedback operational amplifiers prototypes to read out PM for the north auger proposal. Collaboration with IPNO.

4.15. Medical imaging ISS Roma (2007-)

Omega provides chips and test boards to Roma lab for medical imaging applications (PET cameras)

4.16. Medical imaging INFN Pisa (2007-)

Omega provides chips and testboards to INFN Pisa lab for medical imaging applications (PET cameras).

4.17. Medical imaging IMNC (2007-2009)

Omega provides HARDROC chips and support for PCB design of the TRECAM camera to IMNC for medical imaging applications.

4.18. Balloon experiment Aachen (2008-)

Omega provides HARDROC chips and testboards to Aachen lab for balloon experiment applications.

4.19. Generic detector R&D (2007-)

Omega provides electronics for SiPM R&D to readout SiPM matrices (LAL Detector group)

4.20. Space telescope for EECR measurement (2006-)

Omega provides MAROC chips to Korean EWHA physics group to read out MAPMT for a space telescope aimed to EECR measurement.

4.21. FJPPL (2006-)

Collaboration with KEK group (M Tanaka) on ASIC R&D for megaton-like experiment linked to PMm². One Maroc test board supplied.

4.22. FCPPL (2007-)

Collaboration with IHEP (Beijing). One Chinese visitor for 6 months (1/2/08 →31/7/08) on photomultiplier readout design. Collaboration on Parisroc and Building blocks.
One Chinese PhD student (1/9/08→1/9/09).

4.23. New requests

4.23.1. CLAS12 with IPNO.

SiPM readout for sub nanosecond time measurement

4.23.2. Hardroc CSNSM

4.23.3. FP7 Medical imaging Pisa

5. Communication report

5.1. Talks and poster in conferences June 07-June 08

5.1.1. Photo Detector '07, Kobe

June, 29th, 2007 – Invited Talk - Integrated electronics for SiPM, J. Fleury

5.1.2. TWEPP '07, Prague

September, 5th, 2007 – Poster – Digital part of Spiroc, F. Dulucq

5.1.3. TWEPP '07, Prague

September, 5th, 2007 – Poster – Analogue part of Spiroc, L.Raux

5.1.4. TWEPP '07, Prague

September, 5th, 2007 – Poster – Skiroc presentation, J. Fleury

5.1.5. TWEPP '07, Prague

September, 5th, 2007 – Talk – Hardroc presentation, N. Seguin Moreau

5.1.6. TWEPP '07, Prague

September, 5th, 2007 – Talk – MAROC presentation, P. Barrillon

5.1.7. IEEE – Nuclear Science Symposium, Honolulu

October, 31st, 2007 – Talk - A front-end chip to read out the imaging Si-W calorimeter for ILC, J. Fleury

5.1.8. IEEE – Nuclear Science Symposium, Honolulu

October, 31st, 2007 – Talk - Hardroc, N. Seguin-Moreau

5.1.9. IEEE – Nuclear Science Symposium, Honolulu

October, 31st, 2007 – Talk - Spiroc, C. de la Taille

5.1.10. IEEE – Nuclear Science Symposium, Honolulu

October, 31st, 2007 – Poster – ROC chip, digital, F. Dulucq

5.1.11. IEEE – Nuclear Science Symposium, Honolulu

October, 31st, 2007 – Poster – MAROC chip, P. Barrillon

5.1.12. ASPERA R&D and astroparticle physics meeting, Lisbon

January, 8th, 2008 – Talk - Integrated front-end electronics for astroparticle, J. Fleury

5.1.13. CALOR '08, Pisa

May, 28th, 2008 – Talk – Second generation ASICs for CALICE/EUDET calorimeters, C. de La Taille

5.1.14. NDIP '08, Aix-les-bains

June, 4th, 2008 – Tutorial – Tutorial on readout electronics for photodetectors, C. de La Taille
June, 6th, 2008 – Talk – SPIROC : Readout ASIC for Silicon PM, C. de La Taille

6. Technical report

6.1. Introduction

This section describes the ASICs currently in R&D, test or production at Omega. Due to recent programmable features, most of ASICs have multiple applications.
A goal of Omega creation was to be able to create emulation from a critical mass of human resources, thus increase the design speed using common building blocks for several ASICs. The June prototyping run has shown how efficient that organization is since 3 complex ASICs (SPIROC2, HARDROC2, PARISROC) has been submitted at the same time.
The following ASICs have been designed during the June 07 – June 08 period:

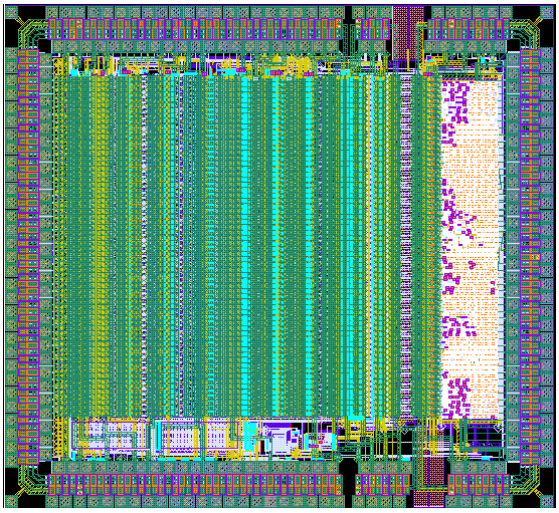
- June 07 : SPIROC1
- November 07 : MAROC3, ASPIC
- June 08 : SPIROC2, HARDROC2, PARISROC

6.2. Maroc

6.2.1. MAROC description

The MAROC chip is a 64-channel input front end circuit developed to read out PMTMA outputs. For each one of the 64 channels, the PM signal is first amplified thanks to a variable gain preamplifier which has low noise and low input impedance to minimise crosstalk. It allows compensating for the PM gain dispersion up to a factor 4 to an accuracy of 6% with 6 bits.
The amplified current feeds then a slow shaper combined with a Sample and Hold buffer to store the charge in 2pF and provide a multiplexed charge output up to 30 pe^-. A 64-channel 12-bit Wilkinson ADC is embedded to provide a digital information of the 64 charge measurement.
In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by a discriminator. The discriminator threshold is set by an internal 10 bit DAC.

6.2.2. MAROC die snapshot



Chip size	4x4=16 mm^2
Contact names	Sylvie Blin, blin@omega.in2p3.fr
	Pierre Barrillon, Barrillon@omega.in2p3.fr

6.3. Hardroc

6.3.1. HARDROC description

HARDROC (HAdronic Rpc Detector ReadOut Chip) is the first prototype of the very front end chip designed for the readout of the RPC or GEM foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider.

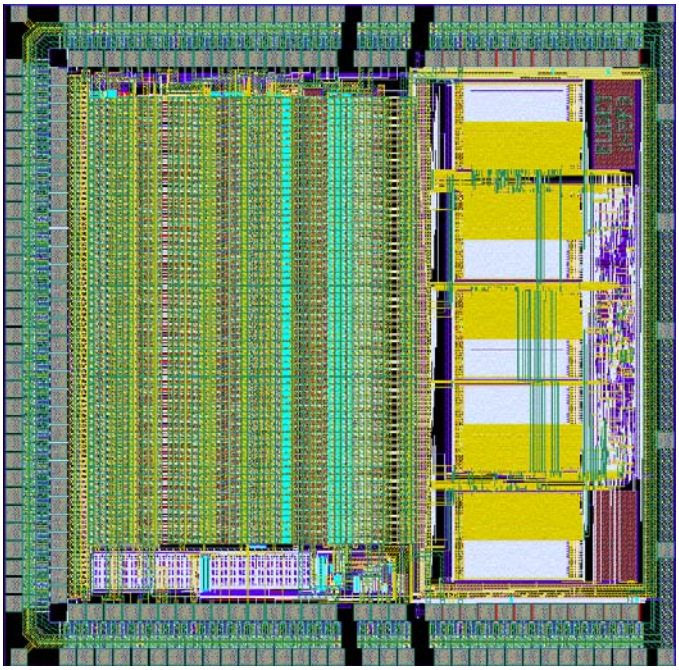
The very fine granularity of the ILC hadronic calorimeters (1cm² pads) implies a huge number of electronics channels (4 10^5 /m³) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption to 10 μWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).

HARDROC readout is a semi-digital readout with two thresholds (2 bits readout) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

The 64 channels of the ASIC are made of a fast low impedance preamplifier with 6bits variable gain (tuneable between 0 and 4), a variable shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC,.a variable gain fast shaper (15ns) followed by two low offset discriminators to autotrig down to10 fC. The thresholds are loaded by two internal 10 bit- DACs. A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

6.3.2. HARDROC die snapshot



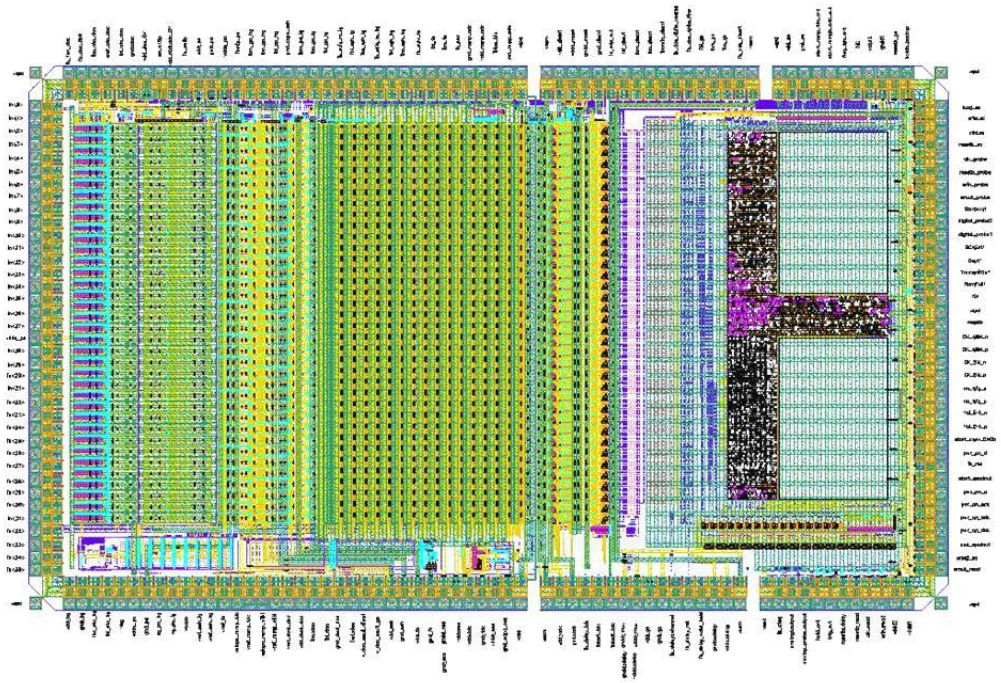
Chip size	4x4=16 mm²
Contact name	Nathalie Seguin-Moreau, seguin@omega.in2p3.fr

6.4. Spiroc

6.4.1. SPIROC Description

SPIROC is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC. An analogue memory array with a depth of 16 for each is used to store the time information and the charge measurement.
A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory contents (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A high-level state machine has been integrated to manage all these features automatically and control the data transfer data to the DAQ.

6.4.2. SPIROC die snapshot



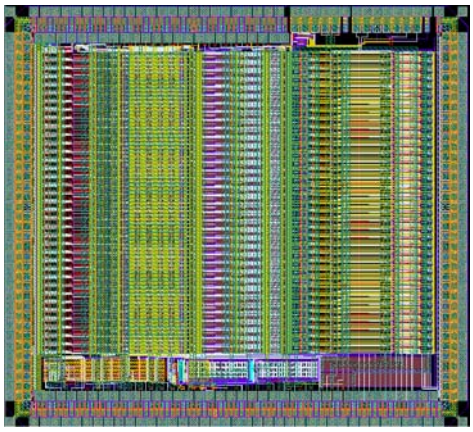
Chip size	4.27x7.2=32 mm², 400 000 transistors
Contact name	Ludovic Raux, raux@omega.in2p3.fr

6.5. Skiroc

6.5.1. SKIROC Description

SKIROC is a 36-channel front-end chip designed to read-out silicon PIN diodes for calorimetry application. It has been designed in a general framework ensuring consistent back-end of different front-end ASIC for several calorimeters (HaRDROC to read out the digital RPC HCAL prototype and SPIROC to read out the SiPM and Sci tiles HCAL prototype are the two others chip existing on that framework).
Each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator. The measured charge is stored in a 5-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12 bit Wilkinson ADC. Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level. A bandgap ensures the stability versus supply voltage and temperature for all the requested reference in the analogue core.

6.5.2. SKIROC die snapshot



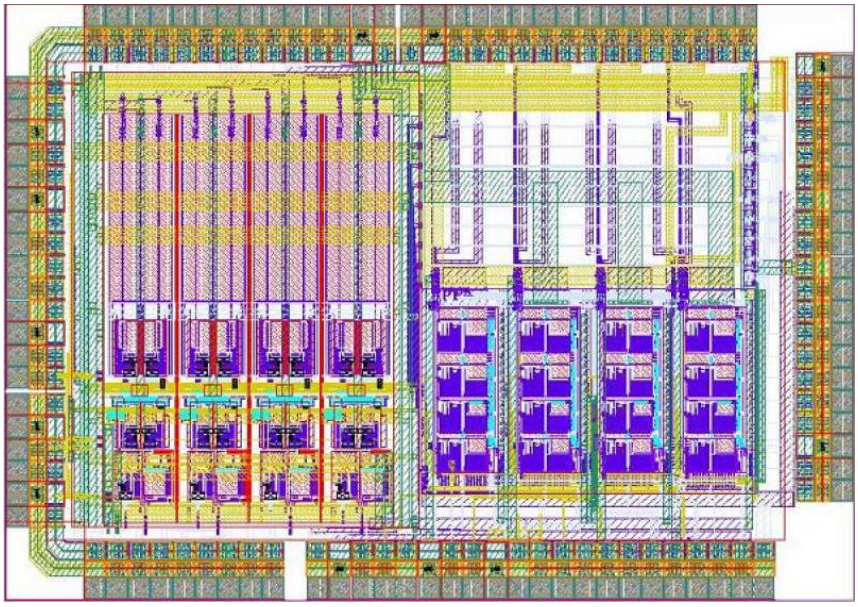
Chip size	4x5=20mm²
Contact name	Julien Fleury, fleury@omega.in2p3.fr

6.6. Aspic

6.6.1. ASPIC Description

The LSST camera will have more than 3000 video-processing channels to readout its large and highly segmented focal plane, requiring a compact readout chain. The standard technique for analogue signal processing of CCDs is "Correlated Double Sampling," which can be implemented either with "Dual Slope Integration" or "Clamp and Sample" architecture.
ASPIC has been designed to directly compare the strengths and weaknesses of these methods on a working device. 4 channels of each method have been implemented on the same ASIC to perform direct comparisons and fine crosstalk measurements. Video channel to video channel crosstalk due to electronics (cables, boards, chips) has to be no more than 0.05% (1::2000) with a 0.01% goal (1::10000) at 500 kHz readout frequency. The other requirements on this readout chain are extreme low readout noise (< 5 e^-), high dynamic range (16 bits), low power consumption (below 25mW/channel) and cryogenic working temperature (173 K)

6.6.2. ASPIC die snapshot



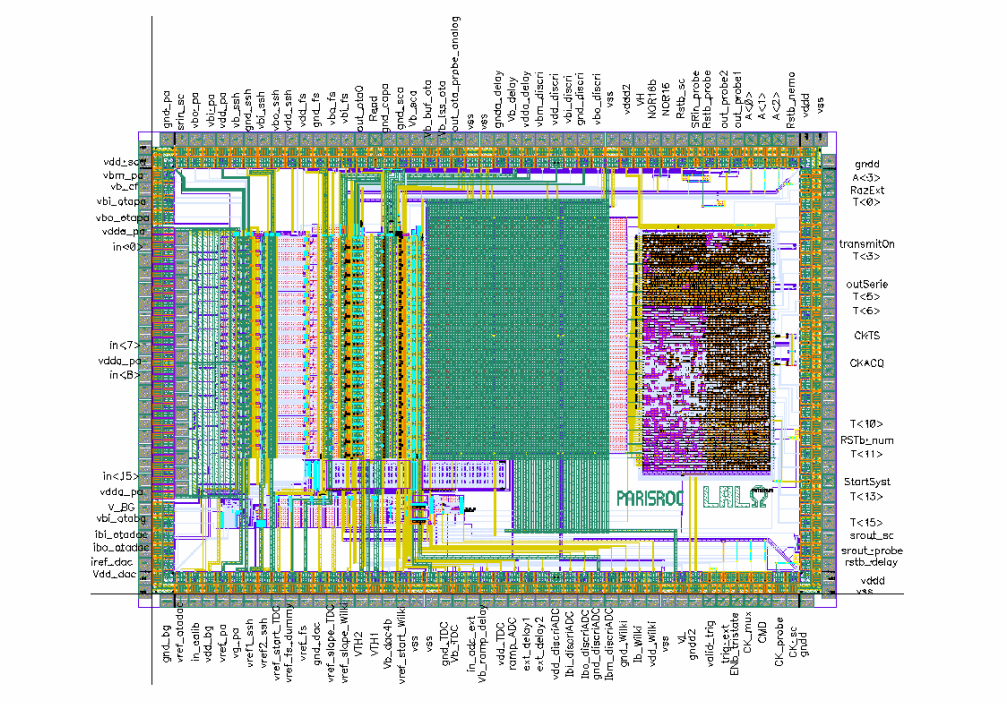
Chip size	9.5mm²
Contact name	Vanessa Tocut, tocut@omega.in2p3.fr

6.7. Parisroc

6.7.1. PARISROC Description

The PARISROC chip integrates 16 channels totally independents. Each channel
contains: a low noise preamplifier with 8 bits variable gain (tuneable by a factor 4) to adjust the PMTs gain variation. a variable slow shaper (50-200ns) followed by an analogue memory with depth of 2 to provide a charge measurement up to 50pC. a second analogue memory with same depth to sample fine time measurement with precision of 1ns. a 12-bit Wilkinson ADC to convert the charge and fine time measures. a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs. A digital part manages all the acquisition, the conversion and the readout and provides by a 24-bit counter the coarse time measurement or timestamp.

6.7.2. PARISROC die snapshot



Chip size	5.1x3.5=18 mm²
Contact name	Gisèle Martin Chassard, chassard@omega.in2p3.fr