R&D for a Vertex Detector suited to the ILC250 Scientific Goals & Running Conditions

M. Winter (IJCLab-Orsay, IPHC-Strasbourg)

8th France-Ukraine Workshop / IJCLab / 22 Octobre 2020

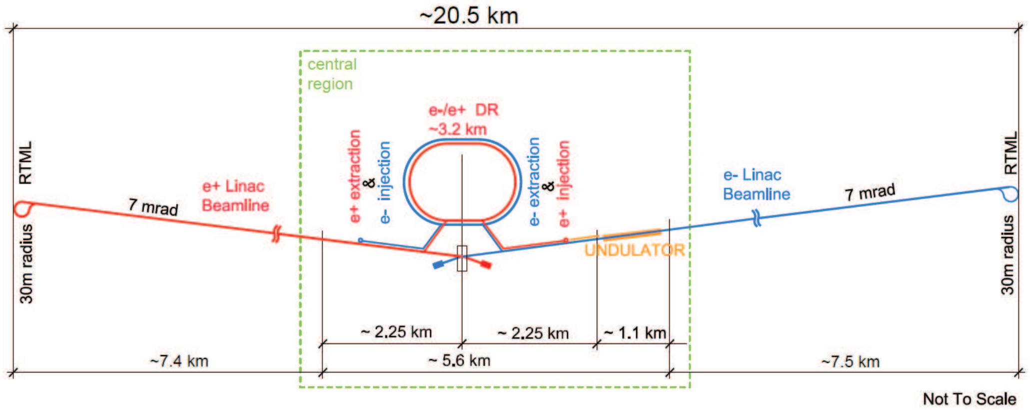
Contents

SOURCES : Talks at VERTEX-2019 & FCCee workshops

The International Linear Collider

- **ILC $\equiv$ Linear e^+e^- collider anticipated to be hosted in Japan (Kitakami mountains)**
  - TDR (2012), industrialisation assessed (XFEL, LCLS-II, SHINE, ...) $\Rrightarrow$ ready for preparing construction
  - 1st stage ("Higgs factory") in preparation by Japanese Gov. Discussions on-going with governments in US & Europe ICFA $\Rrightarrow$ International Devt Team preparing Pre-Lab (202
  - E_{cm} = **250 GeV**, 350/380 GeV, $\gtrsim$ 500 GeV Extensions: $\nearrow \gtrsim$ 1 TeV, $\searrow$ 90 GeV, 160 GeV
  - Polarised beam(s): typically P_- = 80 %, P_+ = 30 %
  - Timeline (prepa. + construct.) $\Rrightarrow$ data taking $\sim$ 2035

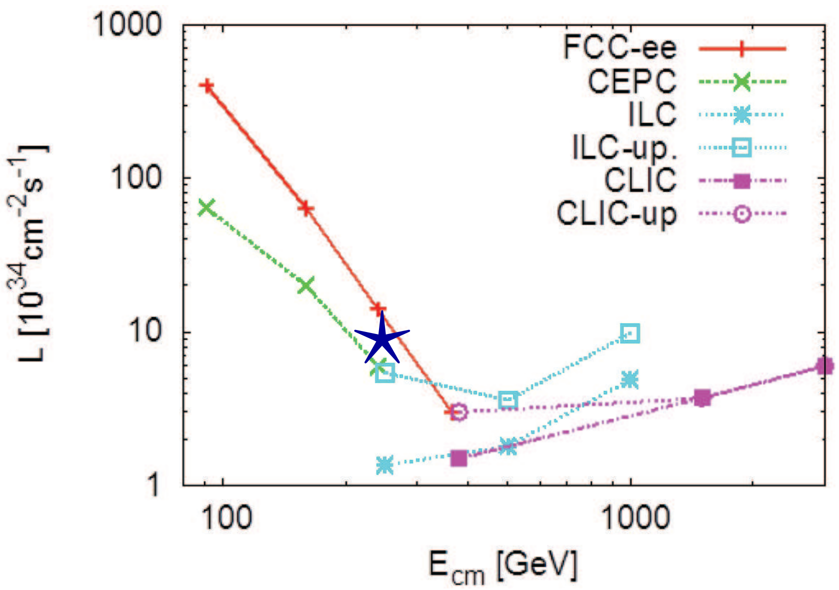
  $\Rrightarrow$ **O(10) yrs available for R&D on vertex detector**



- **Updated characteristics of Higgs factory:**

  (EPPSU input documents Nr.77 & 66)
  - design resumed for 250 GeV (TDR: optimised at 500 GeV)
  - $\mathcal{L}_0$ = 1.35·10^{34} $cm^{-2}s^{-1}$
  - Upgrades considered: $\mathcal{L}_0$ x 4 (ILC-up)

  $\hookrightarrow$ recently $\mathcal{L}_0$ x 6 (prelim. estimate: $<$ 300 MW, + 1 BUSD)



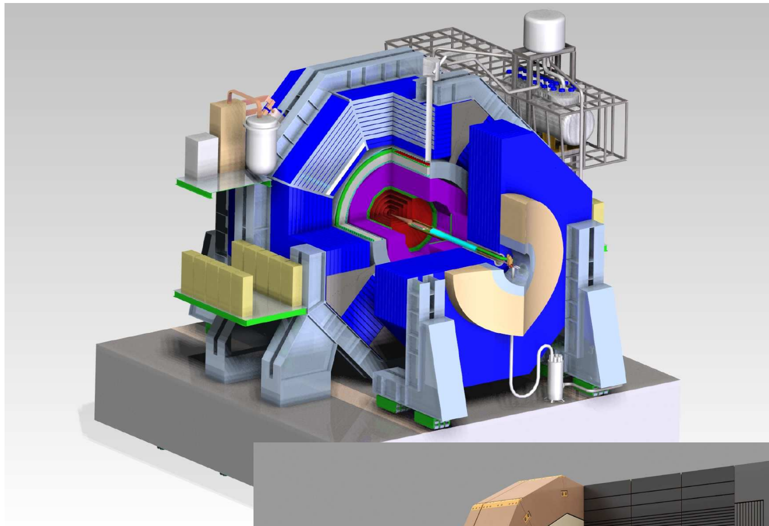
Major Aspects of the Detector Concepts

- 2 DETECTOR CONCEPTS :
  - SiD: full silicon tracker (most compact)
  - ILD: gaseous main tracker (TPC)
- PRIORITY: GRANULARITY & SENSITIVITY
- EXPLOIT COLLIDER SPECIFICITIES:
  - **e^+e^- collisions:**
    - precisely known collision conditions (E_{cm}, Pol., Lumi.)
    - suppressed QCD background $\Rrightarrow$ moderate radiation level

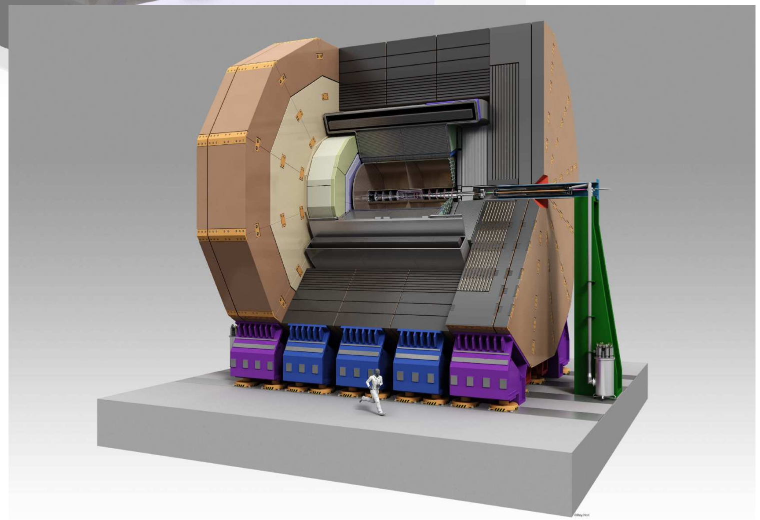
      H occur in 1% of coll. (LHC: 1 H for 10^{10} collisions)

      $\Rrightarrow$ triggerless data taking adapted to faint & rare phenomena
  - **beam time structure:**
    - $\lesssim$ 1% duty cycle $\Rrightarrow$ power cycling $\equiv$ saving $\Rrightarrow$ allows high granularity
    - $\gtrsim$ 300 ns bunch separation $\Rrightarrow$ moderate Δt required

SiD

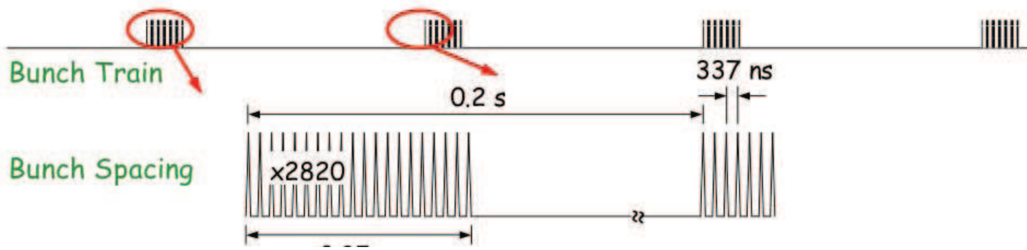


ILD



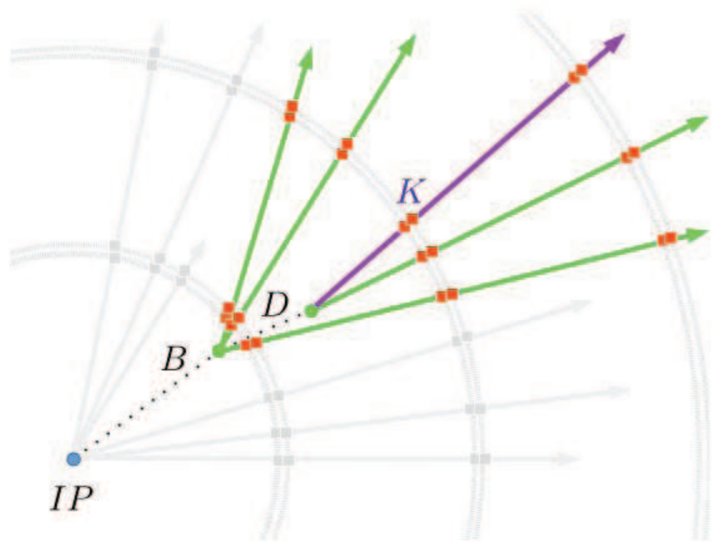
- AMBITIONNED PERFORMANCE HIGHLIGHTS:
  - $\Delta_{2ryVx} < 10\ \mu m$
  - charged track rec.: $\Delta(1/p)$ = $2{\cdot}10^{-5}$ GeV^{-1}

    Q_{2ryVx} $\Rrightarrow$ rec. $P_t \lesssim$ 100 MeV tracks
  - mat. budget: $\lesssim$ 10% X_0 in front of calorimetres
  - $\sigma_E^{jet}/E^{jet} \simeq 30\%/\sqrt{E^{jet}}$ (neutral had. !) $\Rrightarrow$ PFA



Vertex Detector Performance Goals

- **Vertex detector requirements governed by physics oriented parametres rather than running conditions**
  - ⋇ emphasis on granularity & material budget (very low power)
  - ⋇ much less demanding running conditions than at LHC
    - $\Rrightarrow$ alleviated read-out speed & radiation tolerance requests
  - ⋇ ILC duty cycle $\gtrsim$ 1/200 $\Rrightarrow$ power saving by power pulsing

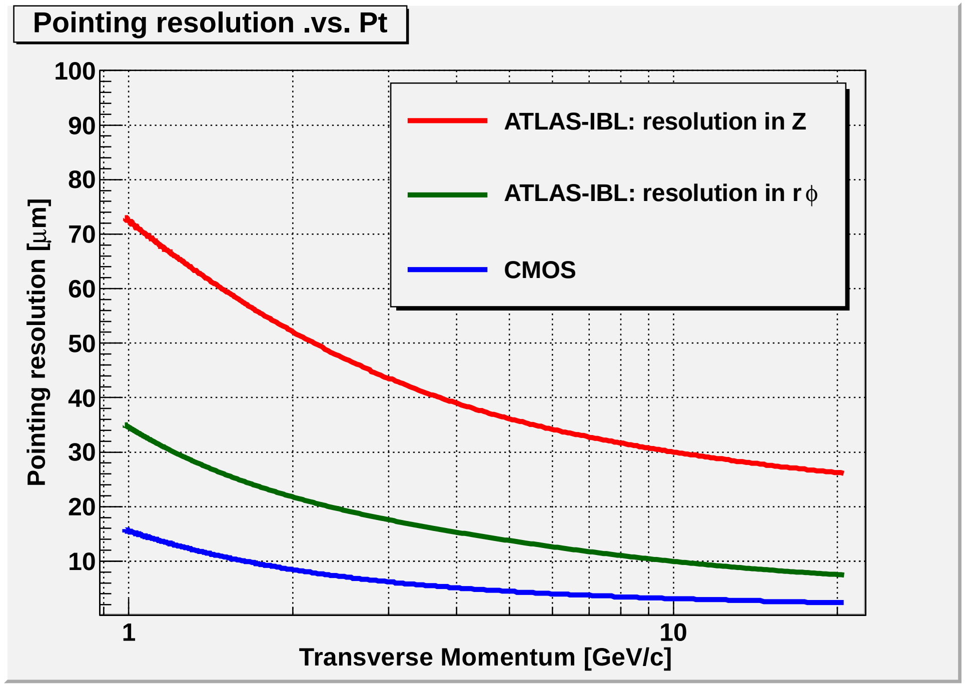


- **Vertexing goal:**
  - ⋇ achieve high efficiency & purity flavour tagging
    - $\rightarrowtail$ charm & tau, jet-flavour !!!
  - ⋇ reconstruct momentum of soft tracks ($P_t <$ 100 MeV)
  - ⋇ reconstruct displaced vertex charge

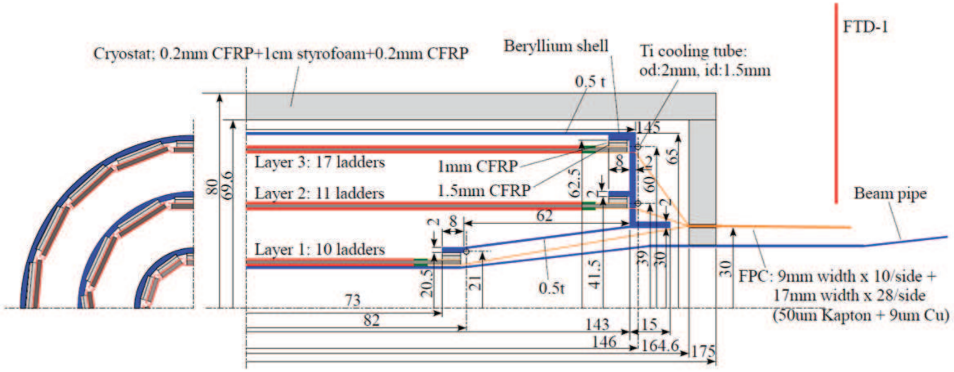
$\hookrightarrow$ $\sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta \;\; \mu m$

- $\triangleright$ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$

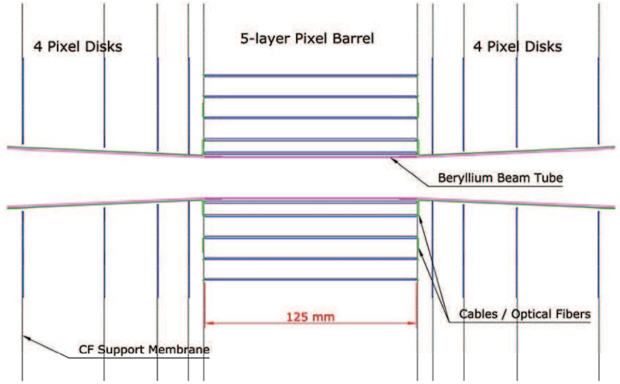
$\triangleright$ Comparison: $\sigma_{R\phi,Z}$(ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels $\rightarrowtail$



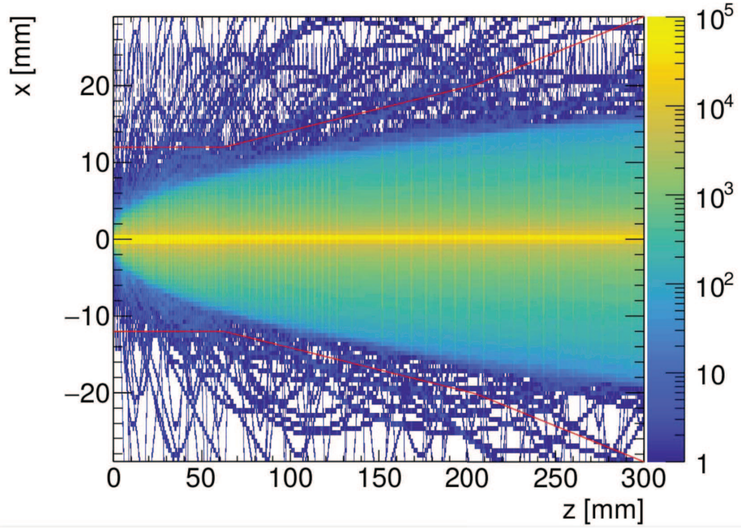
Vertexing Concepts & Challenges



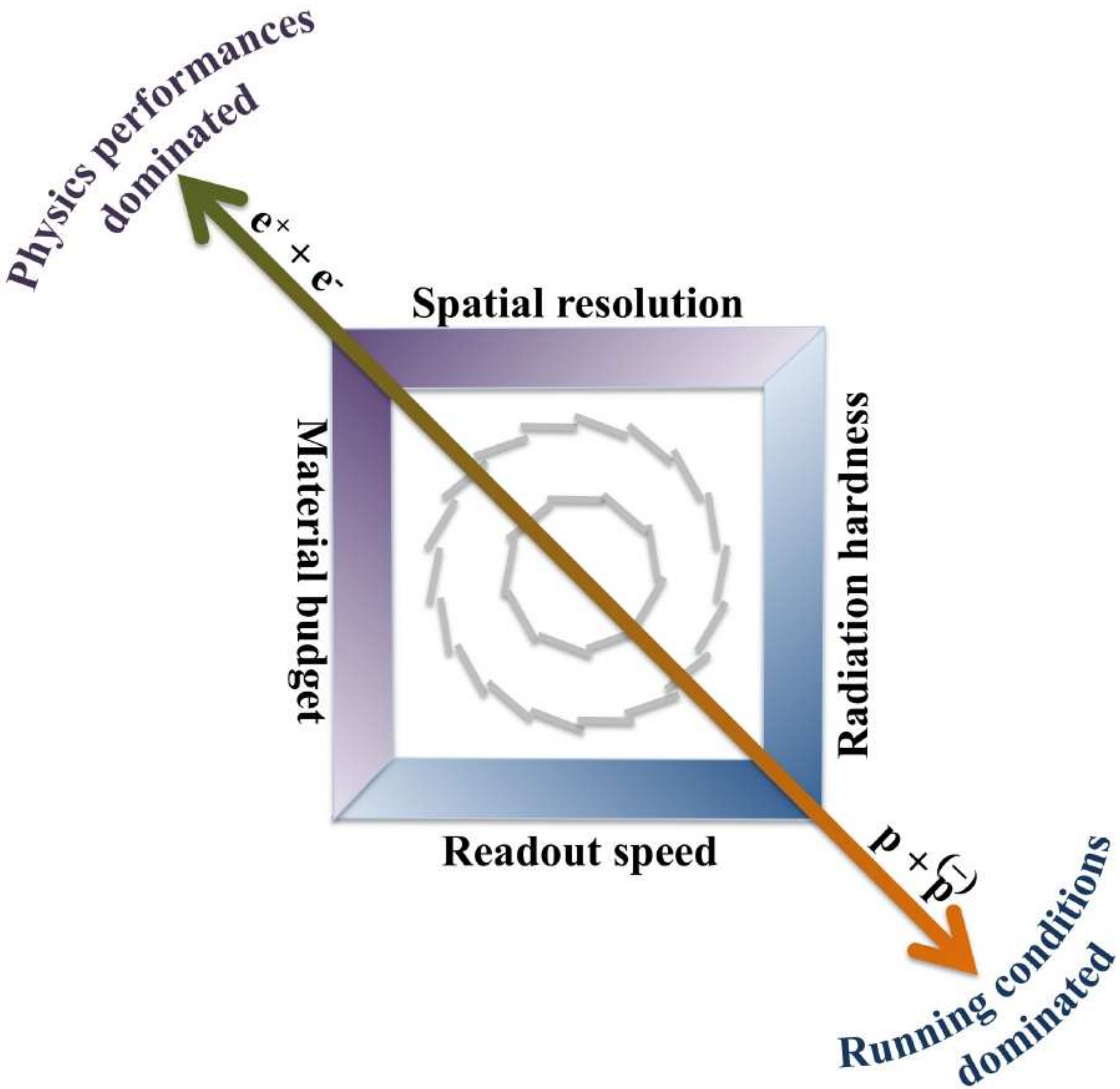
- TWO ALTERNATIVE PIXELATED DESIGNS :
  - **ILD:** long barrel of 3 dble layers (R: 16 - 60 mm)
    0.3% X_0 / layer, $\sigma_{sp} \lesssim 3\ \mu m$
  - **SiD:** short barrel of 5 single layers (R: 14 - 60 mm)
    0.15% X_0 / layer, $\sigma_{sp} \lesssim$ 3-5 μm
  - several (small & thin) pixel technology options under development
  - other devts: mat. budget suppression, cooling, 2-sided ladders, ...



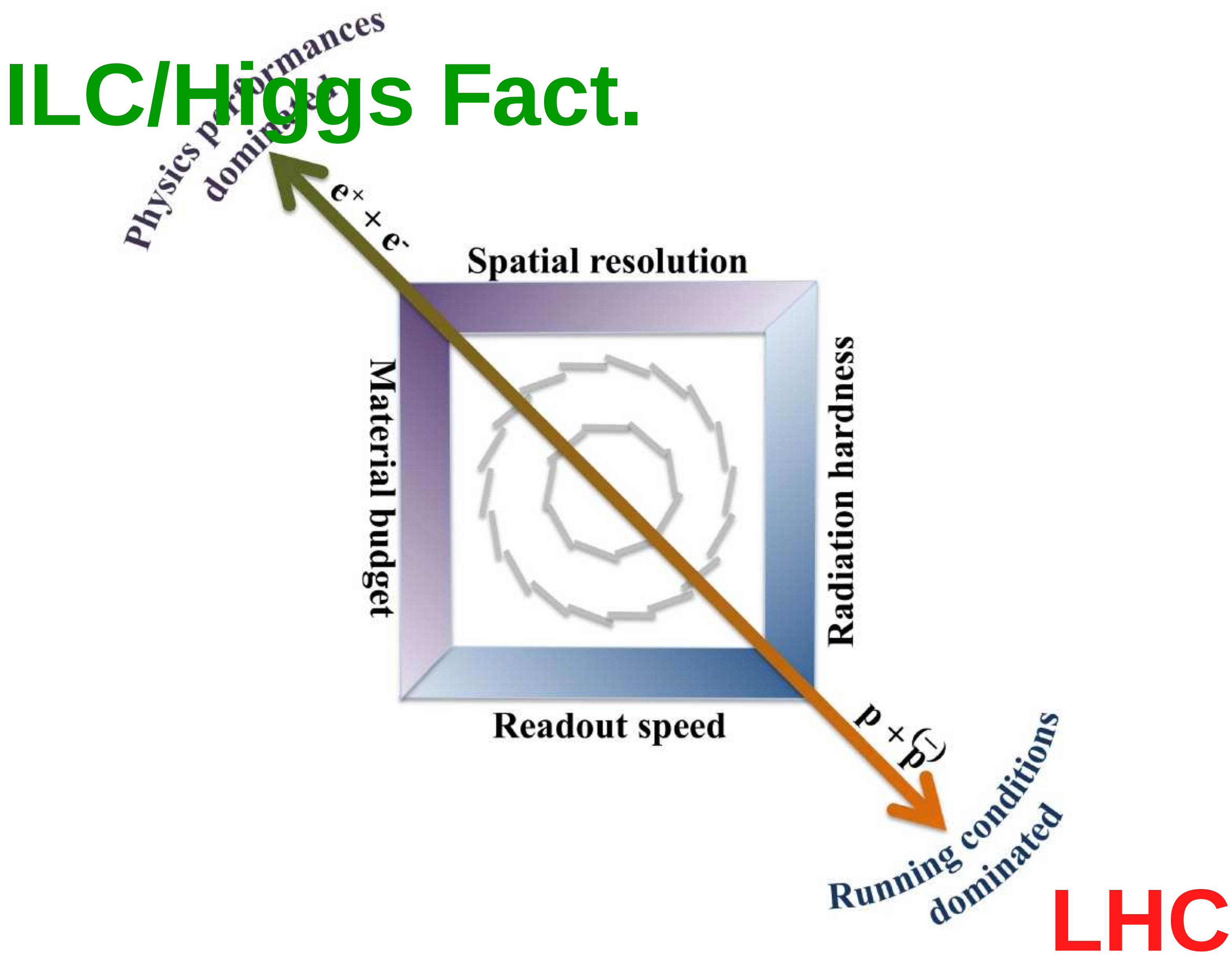
- RUNNING CONDITIONS DOMINATED BY BEAMSTRAHLUNG $e^{\pm}$:
  - Radiation doses: O(100) kRad, $< 10^{12}$ n_{eq}/cm^2/yr
  - Rate of $e^{\pm}_{BS}$ impacts: several tens/cm^2/BX
    - $\Rrightarrow$ governs time resolution requirements
  - sizeable uncertainties: σ_{BS}, luminosity
    - $\Rrightarrow$ substantial safety factors mandatory !



Motivation for High Precision Sensors

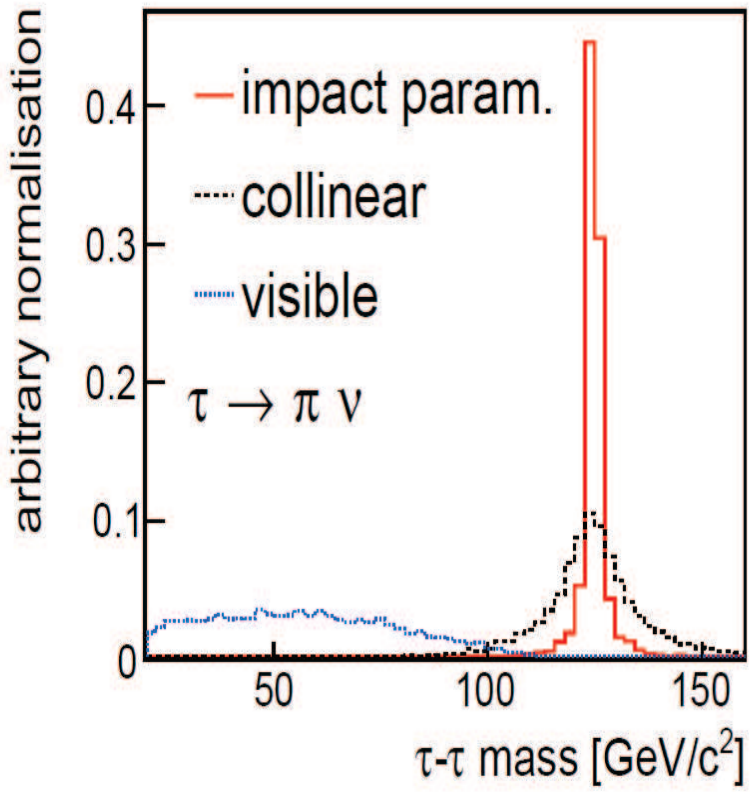


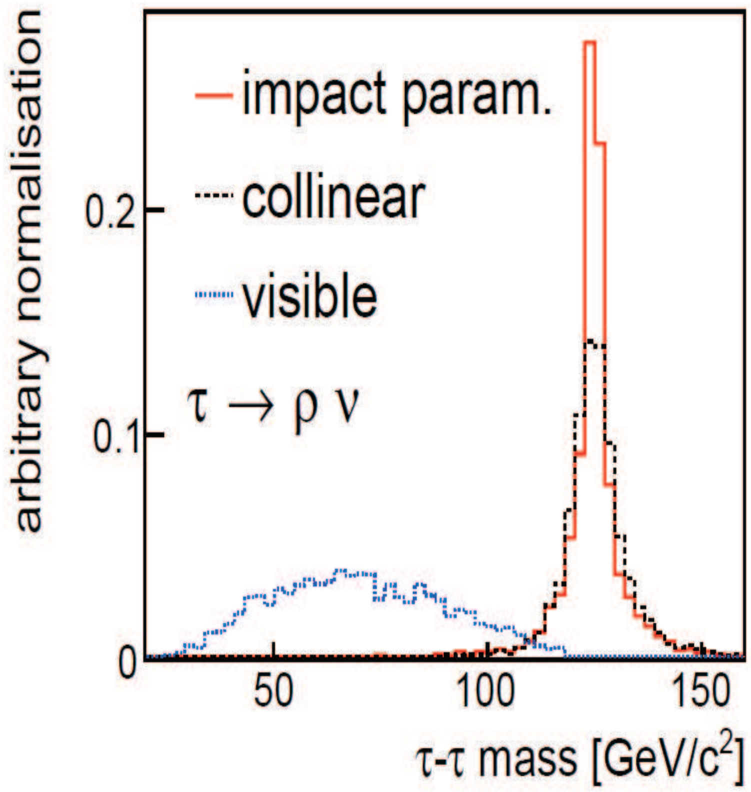
Motivation for High Precision Sensors



Role of Vertex Detector: Reconstruction of τ lepton

- IMPACT OF VERTEX DETECTOR ON τ RECONSTRUCTION: EXAMPLE OF ILD
  - ⋇ use measurements of τ spin state in $e^+e^- \rightarrowtail ZH \rightarrowtail \mu^+\mu^-\tau^+\tau^-$ to probe the CP nature of the Higgs boson and search for BSM manifestation by investigating CP conservation in Higgsstrahlung process and Higgs decay
  - ⋇ concentrate on hadronic decays of τs (one ν only) using displaced vertex reconstruction

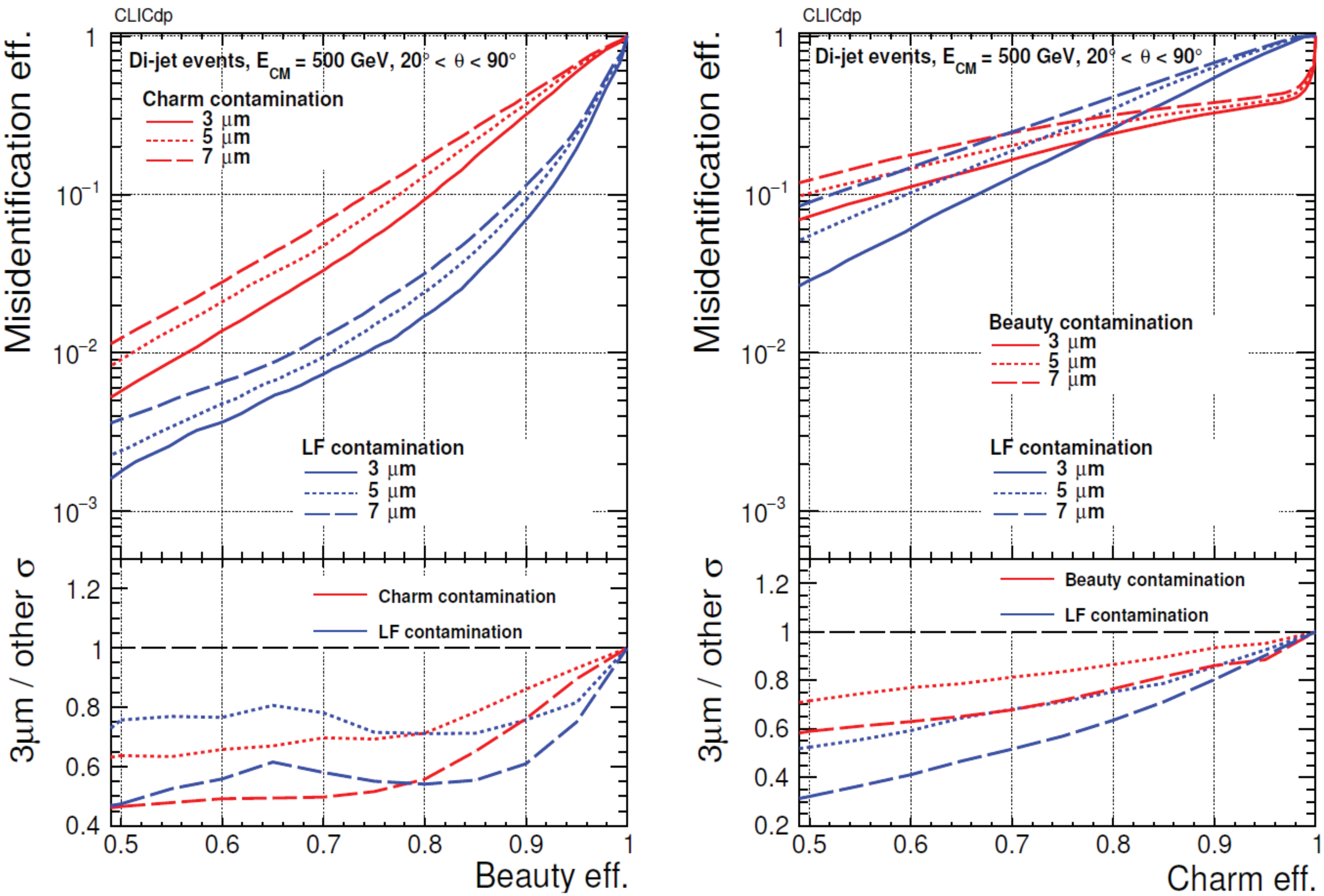




⋇ D. Jeans, Nucl. Instrum. Meth. A810, 51 (2016), arXiv:1507.01700 [hep-ex]

⋇ D. Jeans and G. Wilson, Phys. Rev. D 98, 013007 (2018), arXiv:1804.01241 [hep-ex]

Role of Vertex Detector: Impact of Spatial Resolution on b, c Tagging



- fermion-pair production at E_{CM} = 500 GeV (CLICdet vertex detector : R_{in} = 31 mm)

  D. Arominski et al., CLICdp-Note-2018-005, arXiv:1812.07337 [physics.ins-det] (2018)

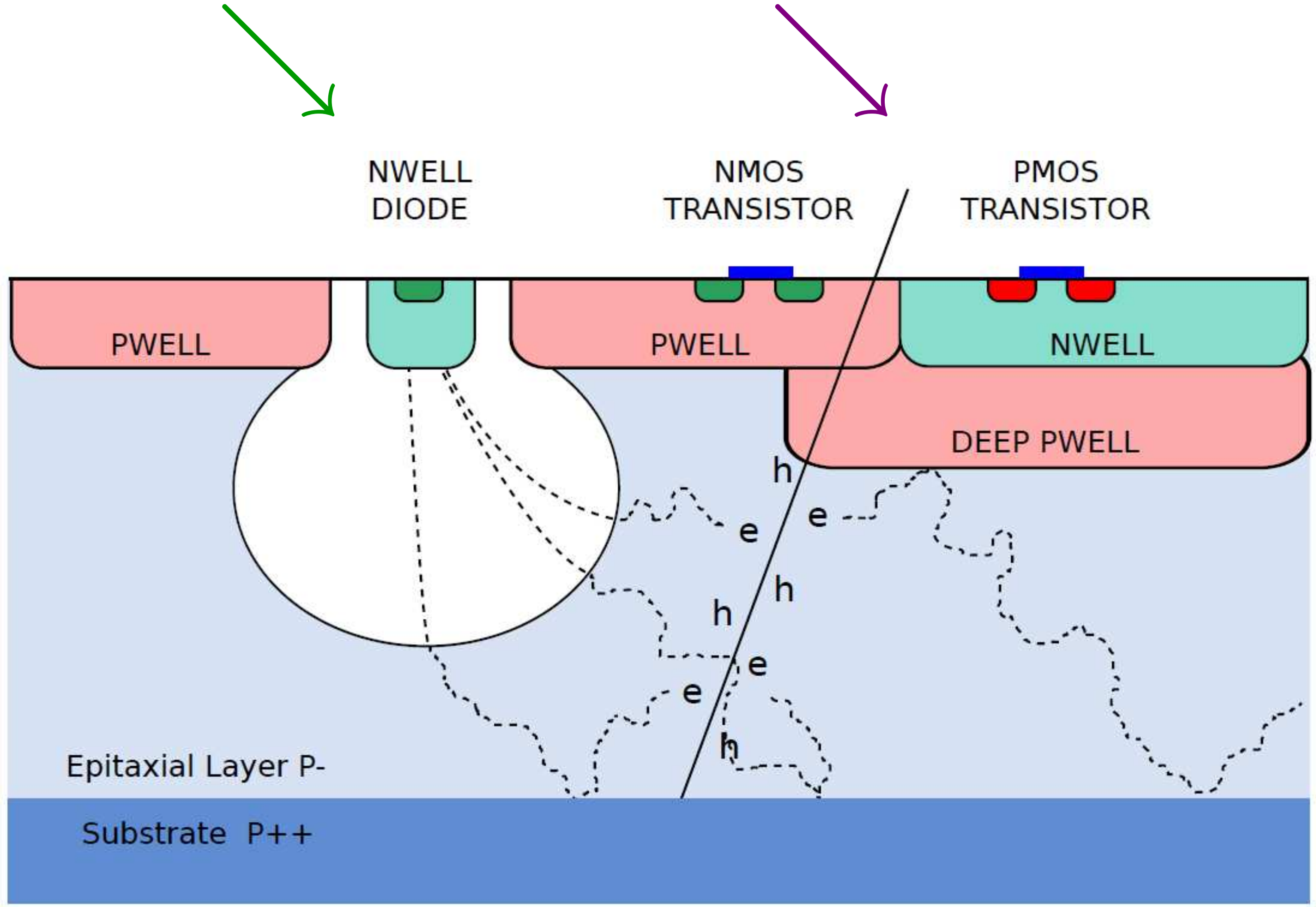
- σ_{sp} = 7 $\mu m \rightarrowtail$ 3 $\mu m \Rrightarrow$ contaminations suppressed by $\sim$ 20% to 40% for 90% tagging efficiency

Pixel Technologies under Development

- TWO ALTERNATIVE READ-OUT APPROACHES:
  - continuous during train, possibly alternated with power cycling inbetween trains
  - delayed after end of train
- FINE PIXEL CCDs (FPCCD): delayed read-out
  - \+ **very granular (5 μm pitch)**
- DEPFET: continuous read-out (used in BELLE-II PXD)
  - \+ **very low material budget (e.g. 0.19 % X_0 in BELLE-II PXD)**
- SILICON ON INSULATOR (SOI): delayed or continuous read-out
  - \+ **2-tier process expected to allow very high density integrated μcircuits $\Rrightarrow$ pixel dim.**
- CMOS PIXEL SENSORS (CPS): delayed (Chronopix) or continuous (PSIRA) read-out
  - \+ **exploits CMOS industry evolution (e.g. feature size $\Rrightarrow$ speed, pixel dim., stitching)**
- INVERSE LGAD:
  - \+ **made for high resolution time stamping $\Rrightarrow$ PID**
- SYSTEM INTEGRATION DEVELOPMENTS BESIDES PIXEL TECHNOLOGIES:
  - ultra-light 2-sided ladders
  - cooling free of extra material in fiducail volume

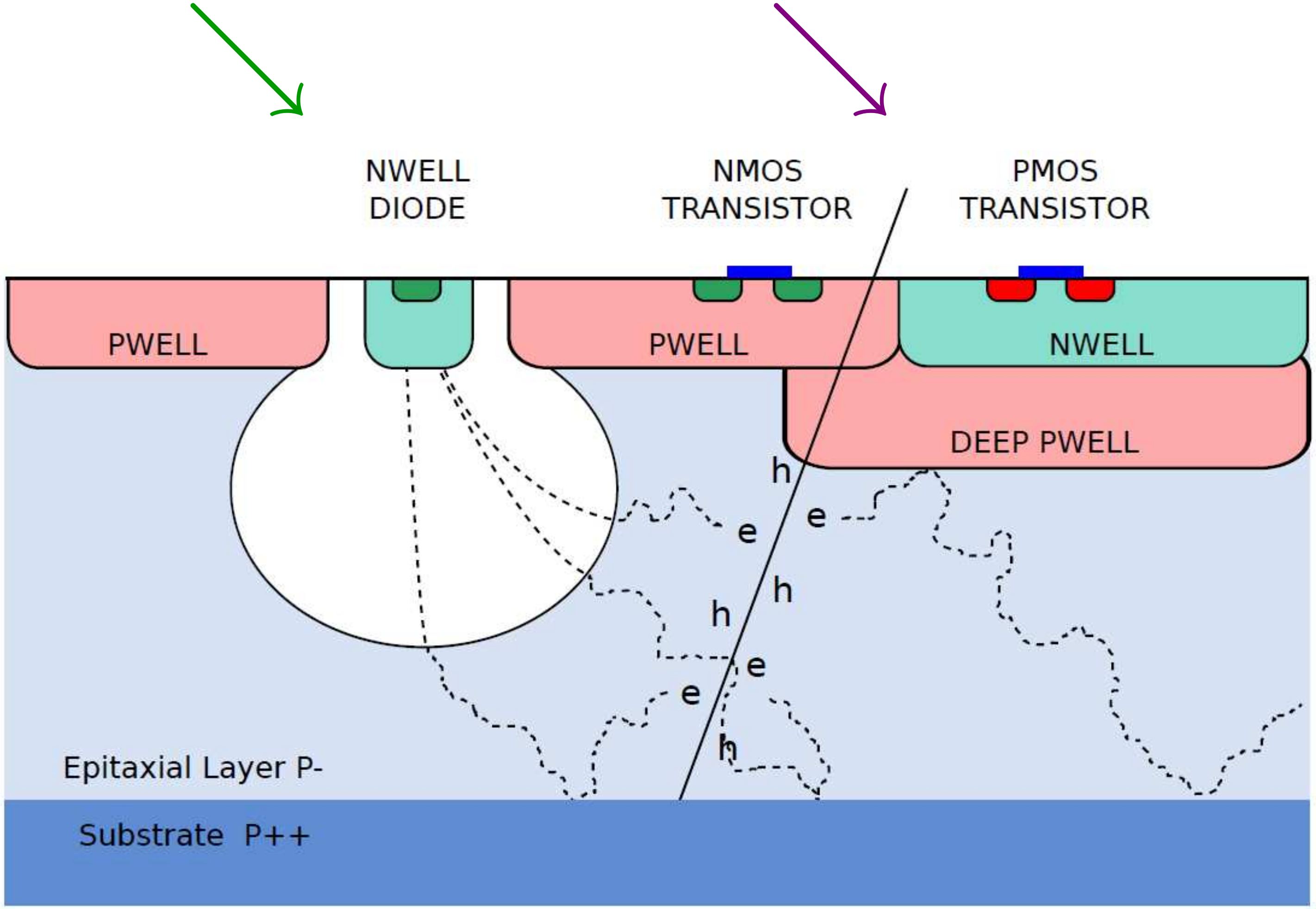
CMOS Pixel Sensors (CPS): Main Features

- **CMOS Pixel Sensors ≡ Detector ⊕ Front-End Electronics in same die**



CMOS Pixel Sensors: Main Features

- R&D addresses **Sensing Element** ⊕ **Read-Out μcircuitry**



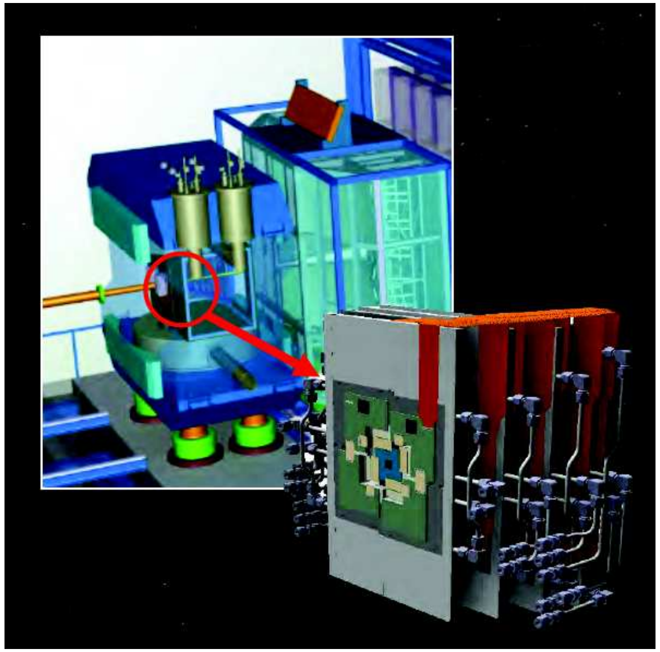
Location of Devices based on CPS (developed at IPHC)

Present R&D of Monolithic CMOS Pixel Sensors (CPS)

- **ILC requirements similar to those of Heavy Ion expts**

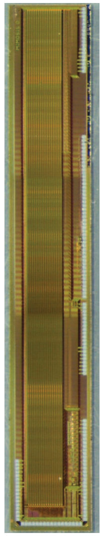
  ⇛ CPS developed for CBM expt (FAIR/GSI)

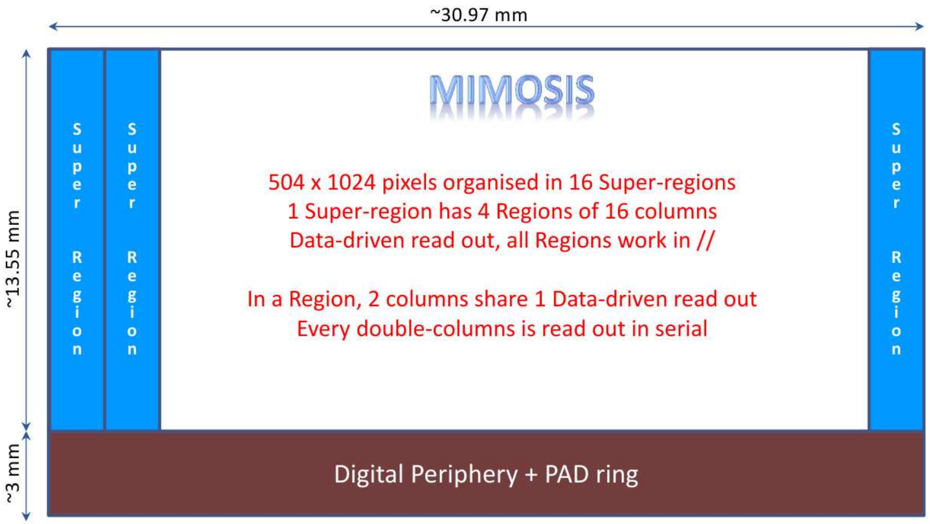
  ≡ acts as a forerunner for ILC vertex detectors



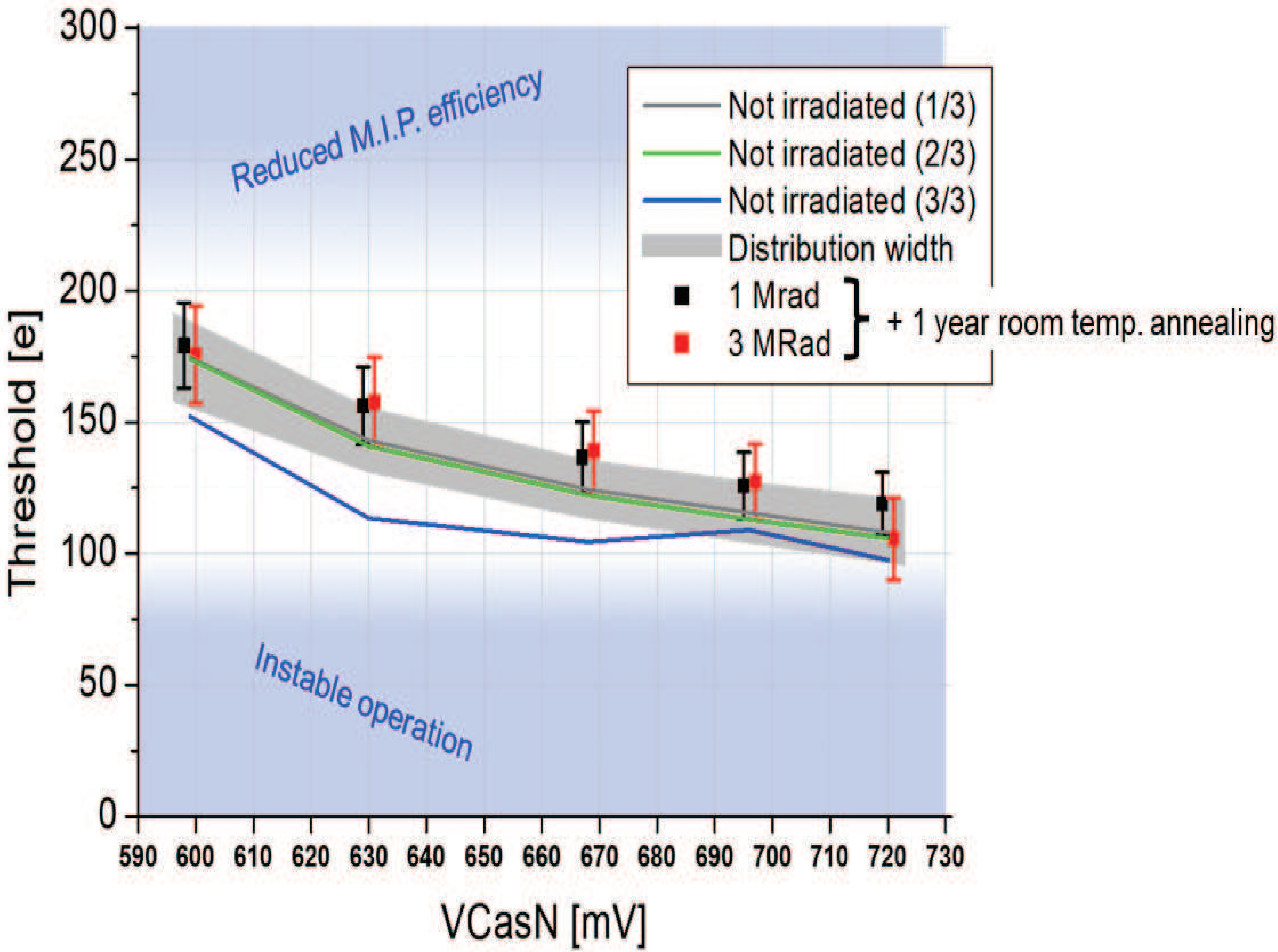
- **Main characteristics of MIMOSIS**
  - ⋇ TJsc 180 nm imager process with high-res (25 μm thick) epitaxy
  - ⋇ modified high-res (25 μm thin) epitaxy ⇛ full depletion
    ⇛ sub-ns charge collection time (+ enhanced rad. tol.)
  - ⋇ 1024 col. of 504 pixels with asynchronous r.o. (ALPIDE)
    in-pixel discri. with binary charge encoding
  - ⋇ pixel: 27x30 μm^2 ⇛ $\sigma_{sp} \gtrsim$ 5 μm (vs depletion depth)
  - ⋇ affordable hit density $\simeq 10^8$ hits/cm^2/s
  - ⋇ $\Delta t \sim$ 5 μs
  - ⋇ Power density $\sim$ 40–50 mW/cm^2 (vs hit density)
- Step-1: MIMOSIS-0 proto. ≡ 1/32 slice of final sensor
  - ⋇ pixel array μcircuitry validated at 5 μs
  - ⋇ validated rad.tol.$>$ 3 MRad, 3·10^{13} n$_{eq}$/cm^2
- Step-2: MIMOSIS-1 full size proto.

  ⇛ back from foundry, under test





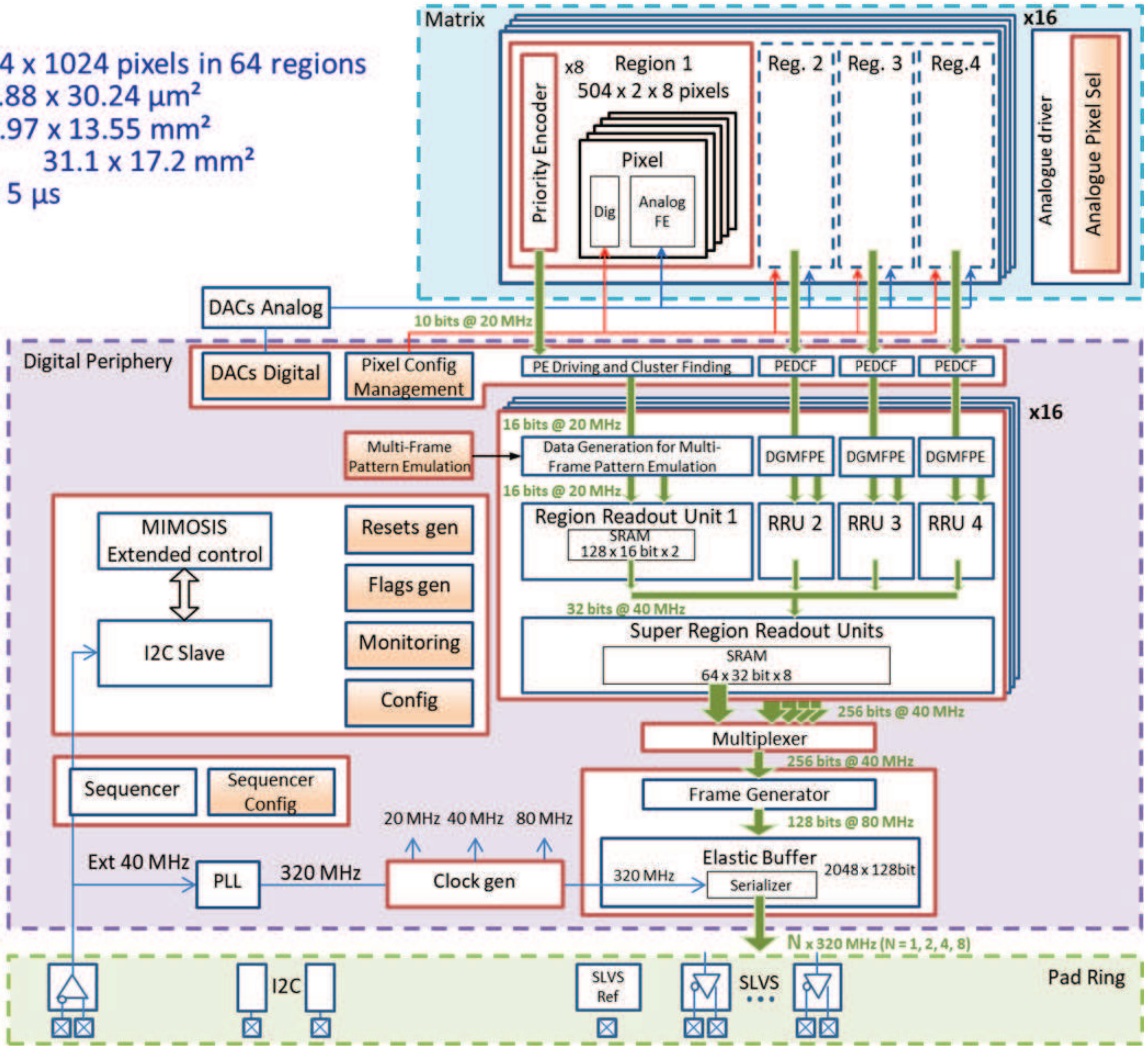
MIMOSIS-0 Test Results



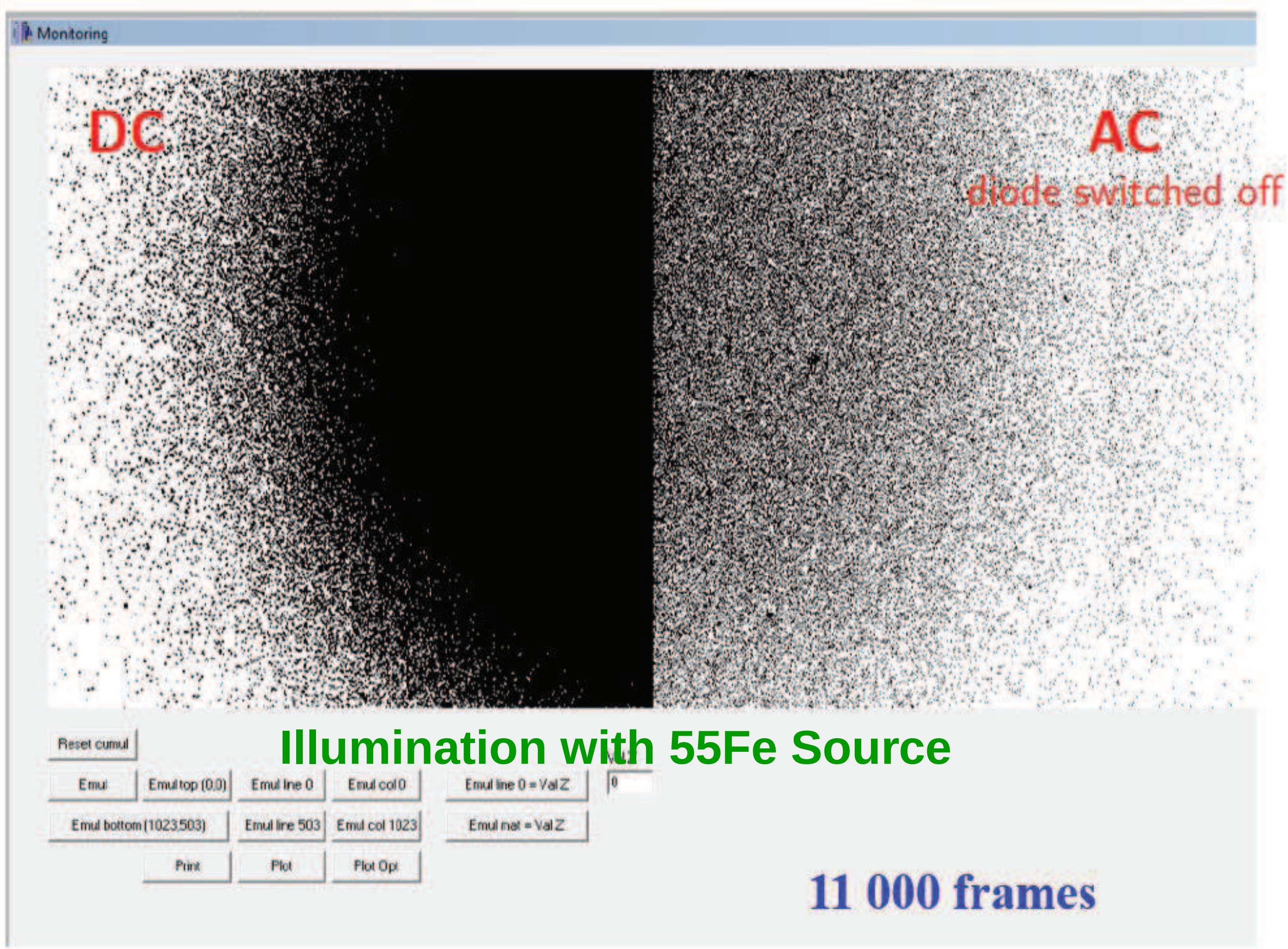
MIMOSIS-1 Block-Diagramme

- Pixel array: 504 x 1024 pixels in 64 regions
- Pixel pitch: 26.88 x 30.24 µm²
- Active area: 30.97 x 13.55 mm²
- Chip dimension: 31.1 x 17.2 mm²
- Integration time: 5 µs

- Pixel array:
  - Analog part of pixel similar to ALPIDE, but 2 versions
  - Digital part of pixel redesigned
  - Priority encoder: same
- Fully reworked digital part

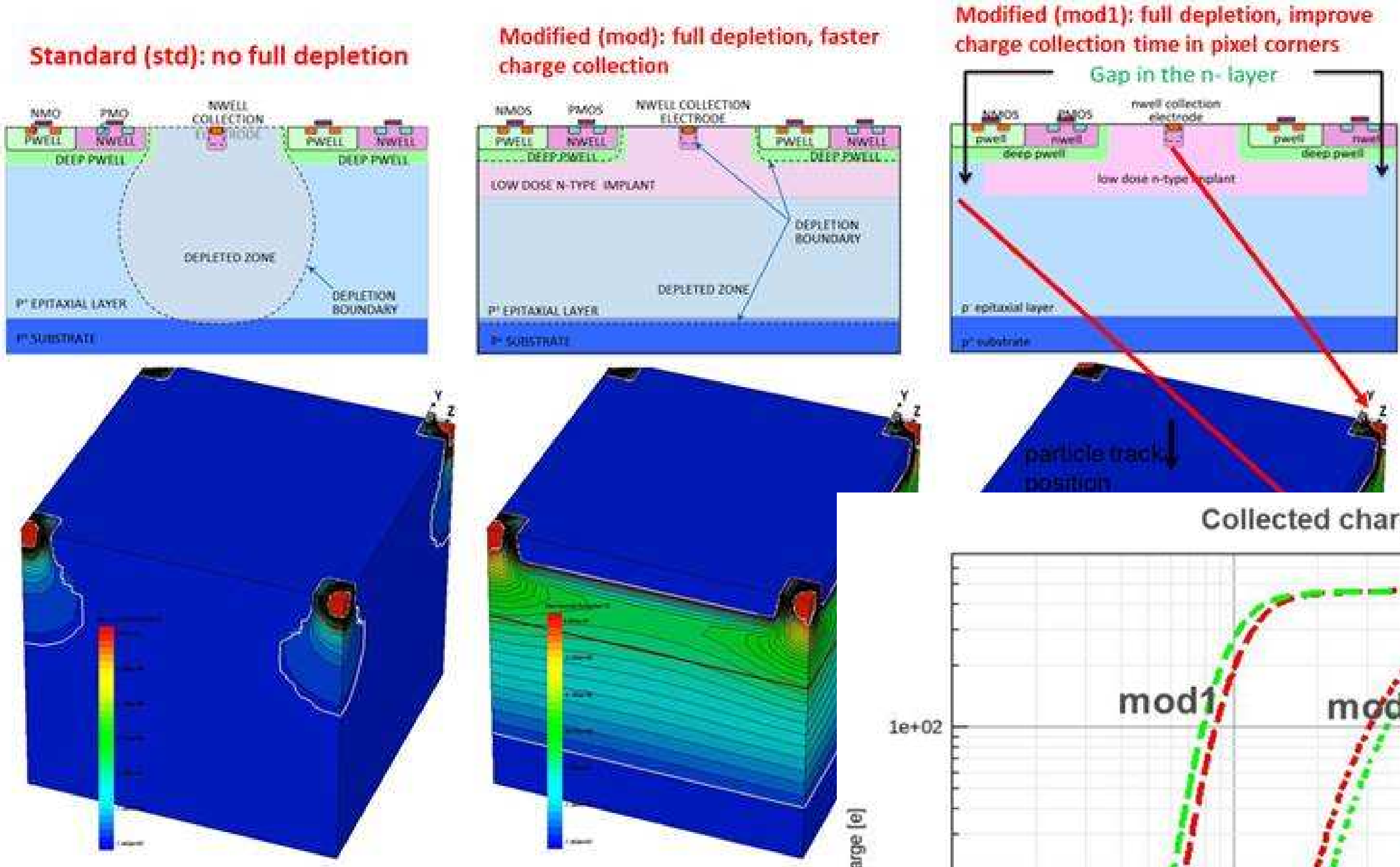


MIMOSIS-1 (very) Preliminary Test Results



- 1st electronic noise performance evaluated at T_{room} on 128 DC pixels (1/8 row):
  - Pixel (thermal) Noise $\simeq 4.6 \pm 0.4$ e^- ENC
  - Fixed Patter Noise $\simeq 9.4 \pm 0.6$ e^- ENC (in-pixel discri. threshold ~ 130 e^- ENC)

MIMOSIS Spin-Off: Starting Material Options

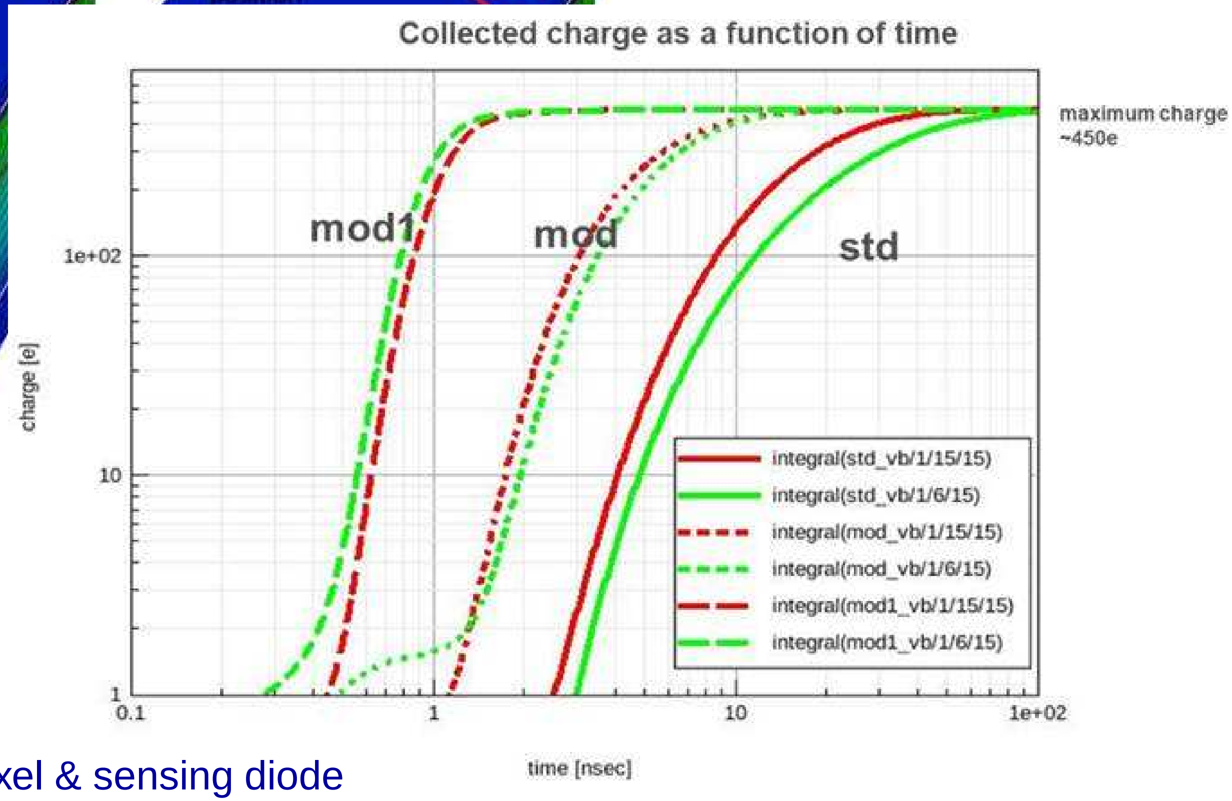


TCAD simulation:

Tower-Jazz 180 nm CIS

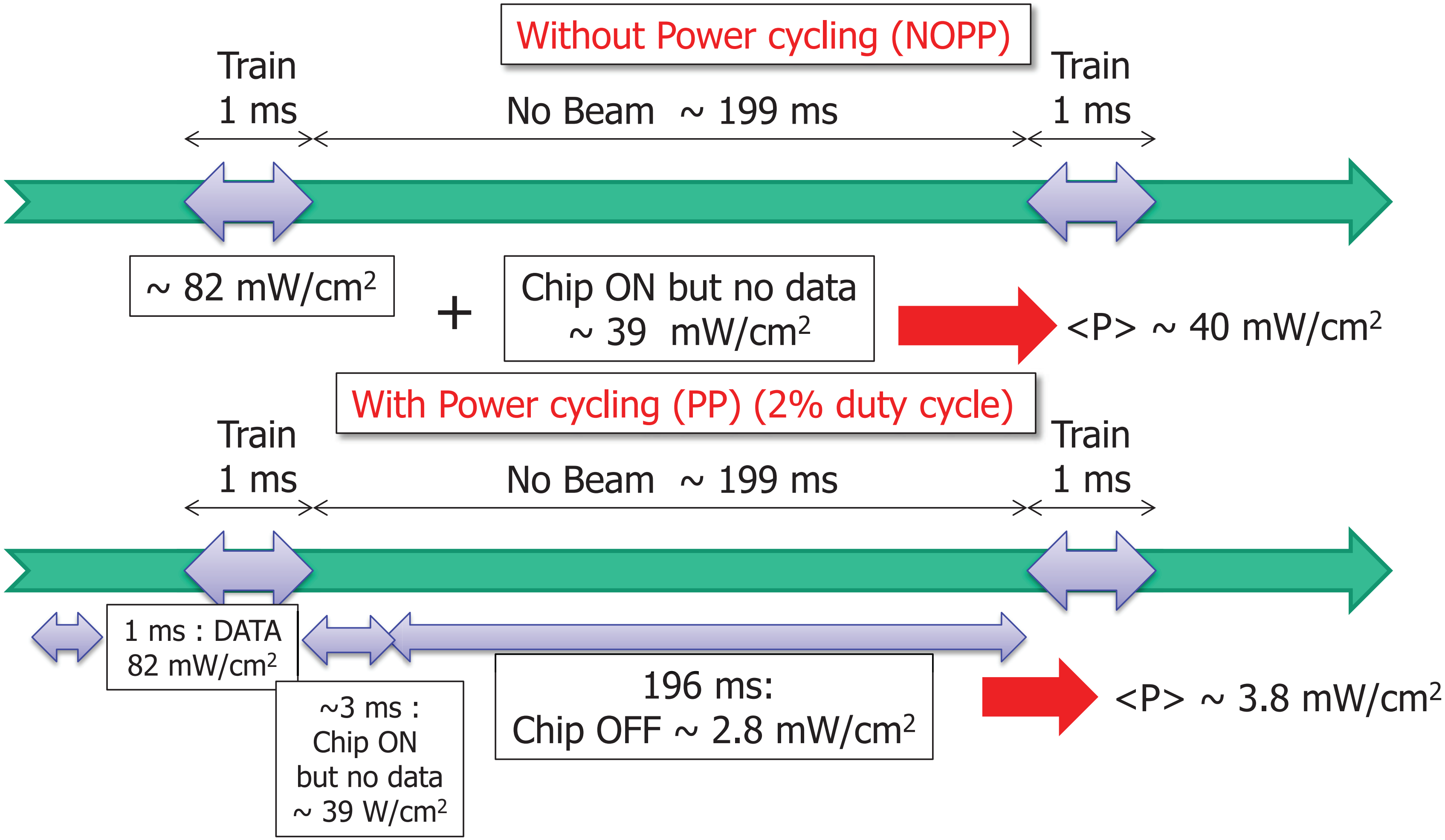
27x30 μm^2 pixels

3x3 μm^2 sensing diode



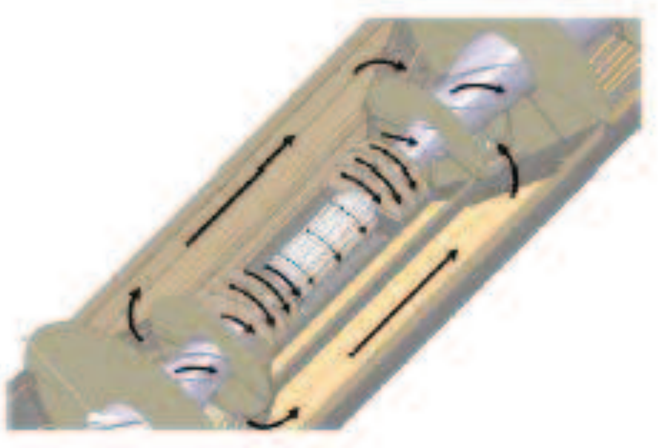
- Q coll. time improved by factor $\sim$ 10
- radiation tolerance improvement being assessed
- 1st HEP application: CBM-MVD HI expt / FAIR
- still O(10) improvement expected from smaller pixel & sensing diode

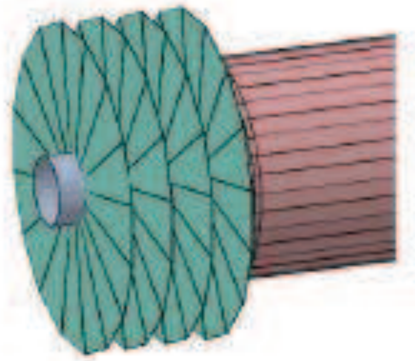
Power scheme for VTX-ILD (inner layer)

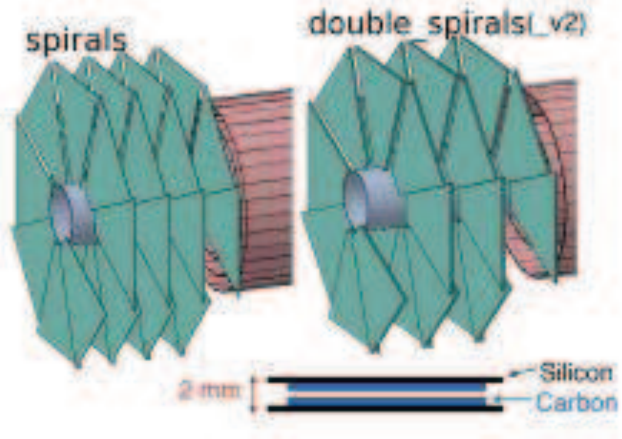


Hypothesis: 3 double sided layers (3483 cm^2), PSIRA architecture (4 μs / 4 μm), TDR background @ √s = 500 GeV, no safety factor

Issue: Link to Forward Tracking System







- Cooling pipes introduce dead material near the IP

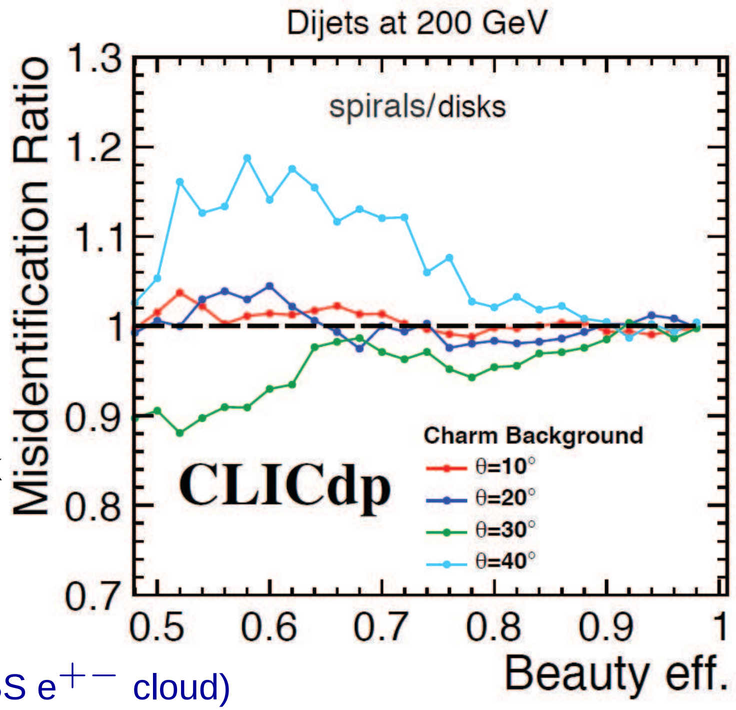
  ⇛ alternative (CLICdp approach) : cooled air flowing from outside through end-cap tracking sub-system & traversing vertex detector volume

  (see N. Alipour Tehrani & P. Roloff, "Optimisation studies for the CLIC vertex-detector geometry", CLICdp-Note-2014-002).

- "40° corner":

  b-tagging impacted by increased <distance> from barrel edge to 1st disk

  c-tagging suspected to be significantly more impacted: how much ?



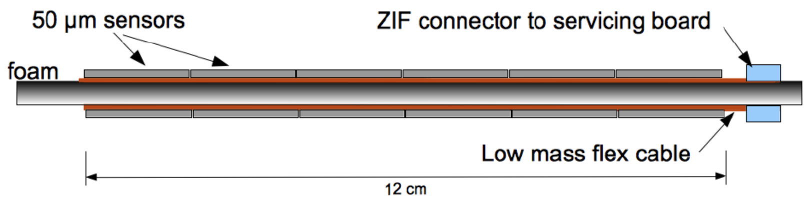
- Other delicate areas:

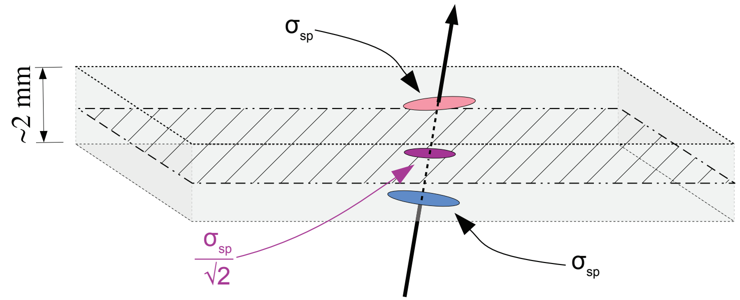
  ⋇ near the beam pipe (cone ?) ⇛ minimal polar angle intercepted (fct of outgoing BS e^{+-} cloud)

  ⋇ distance between barrel end and first foward disk ⇛ impact on small polar angle tagging

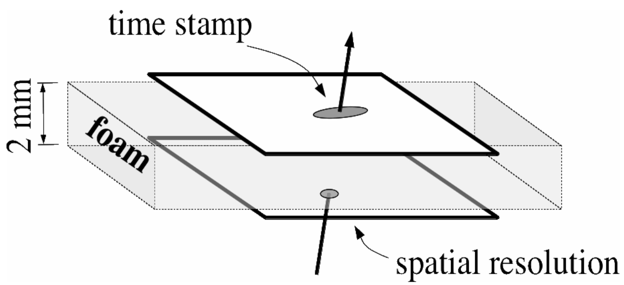
Ultra-Light Double-Sided Pixelated Tracker Modules

- **General remarks:**
  - Double-sided ladders for
    - excellent spatial resolution (granularity, face-to-face correlation)
    - coping with very high hit densities (speed, face-to-face correlation
  - Caveate: material budget oughts to be suppressed enough
  - PLUME $\equiv$ Existing prototype, based on MIMOSIS:
    8 million pixels, $\gtrsim 3\ \mu m$, 115 μs, 0.4 % X_0
  - 1st goal: improve r.o. speed to O(1) μs & squeeze mat. budget
    to $\lesssim 0.3$ % X_0, validate face-to-face sensor correlation
  - 2ry goal: investigate wireless face-to-face signal transmission
  - Possibly: investigate power pulsing in mag. field ? (tbc)





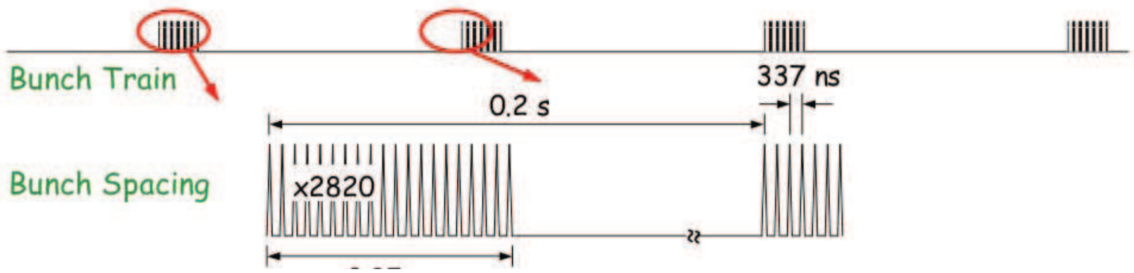
- **Sensor related objectives:**
  - Baseline MIMOSIS proto.: $\gtrsim 4\ \mu m$ (tbc), $\lesssim 5\ \mu s$, $\lesssim 50$ mW/cm^2, $\gtrsim 50$ MHz/cm^2
  - Assess spatial resolution of ladder based on face-to-face correlations
  - Ideally: develop mixed MALTA-MIMOSIS ladders (complicated !)



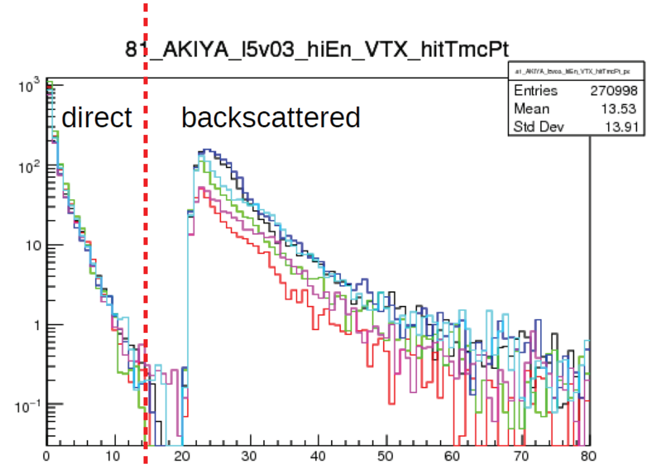
- **System related objectives:**
  - revisit structure of PLUME to compress its material budget
  - investigate new materials & micro-channel cooling

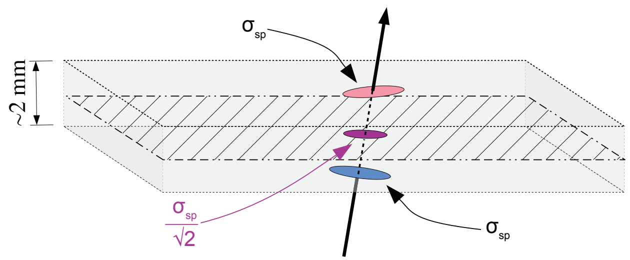
Objectives of R&D in upcoming Years: Time Stamping

- Motivations for time resolution improvements:
  - ⋇ minimise perturbations due to beamstrahlung $e^{\pm}$
  - ⋇ 1st step: single bunch tagging
    - ↪ bunch spacing: 554 or 337 ns (fct of lumi.)
  - ⋇ 2nd step: reject backscattered $e_{BS} \rightarrowtail \Delta t <$ 20 ns
  - ⋇ ultimately: allow for particle ID $\Rrightarrow$ O(10) ps
    - ↪ extension to fully pixellated tracking



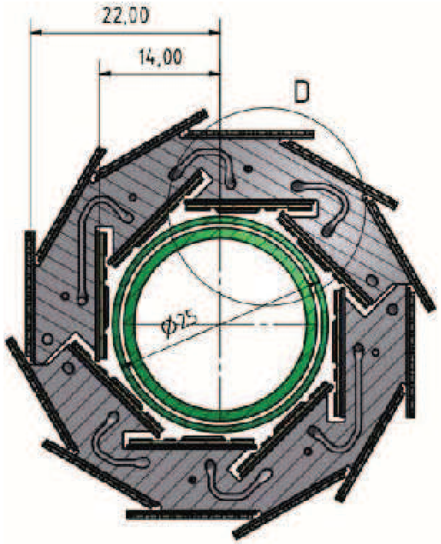
- R&D activities and difficulties
  - ⋇ main difficulty: improve time resolution while keeping high spatial resolution (& affordable power consumption)
  - $\Rrightarrow$ 2 main options addressing single bunch tagging:
    - ∘ $<$ 0.1 μm CMOS process (e.g. TJsc 65 nm)
    - ∘ 2-tier SoI process
  - ⋇ e.g.: MIMOSIS may be adapted to 300 ns but granularity will be degraded in absence of smaller feature size
  - ⋇ oversized pixel dimensions (due to in-pixel circuitry) may be compensated by 2-sided impact correlations

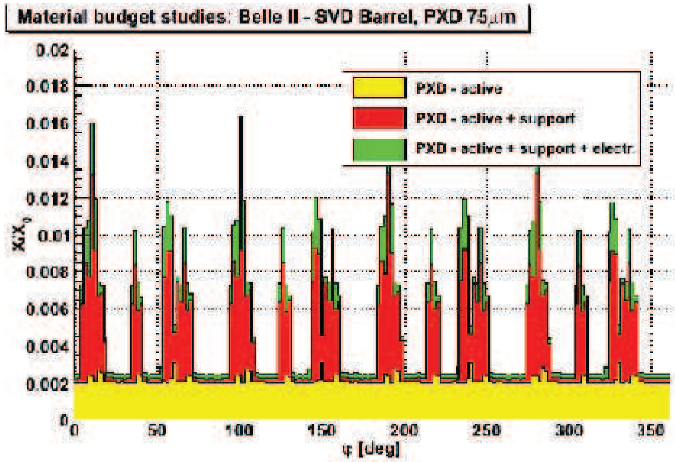




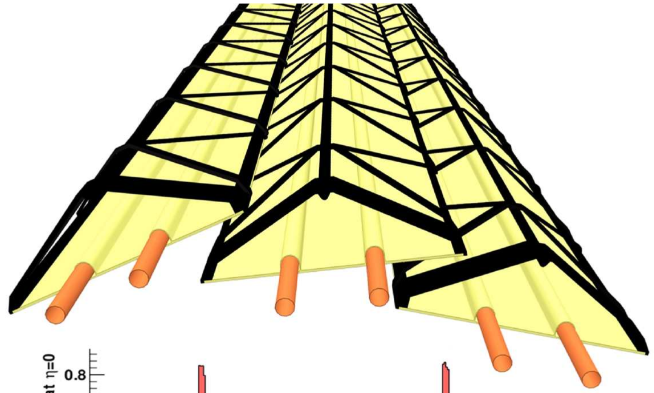
Objectives of R&D in coming Years: Material budget reduction

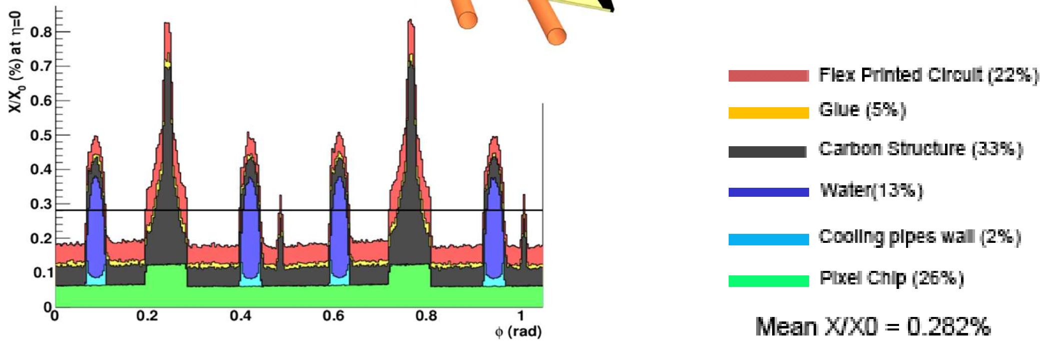
- Physics perfo. limited by material budget of services & overlaps of neighbouring modules/ladders





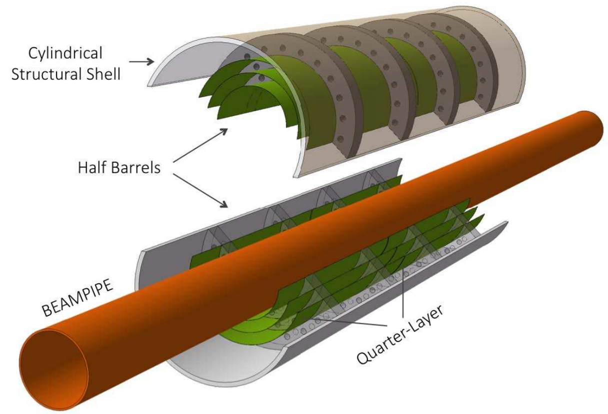
BELLE-II PXD





ALICE-ITS

- Contribution of sensors to total material budget of vertex detector layer is modest: 15 - 30%
- **R&D objective beyond TDR/DBD concepts:**
  - Innermost layer: try stitched & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process
  - Concept with minimised mechanical support (e.g. using beam pipe) See Talk of M. Mager at Vertex-19, Lopud Island, Oct.'19



SUMMARY

- The requirements for an ILC vertex detector are particularly demanding in terms of spatial resolution & material budget. They are addressed with various pixel technologies by compromising the time resolution to a tolerable level (w.r.t. beamstrahlung) and exploiting the modest radiation load

- The performances achieved up to now are quite satisfactory w.r.t. DBD/TDR specs, but:
  - ⋇ tension between granularity & r.o. speed ($\Rrightarrow$ occupancy) $\rightarrowtail$ little safety margin
  - ⋇ material budget issues (power cycling, cooling) not fully addressed $\Rrightarrow$ room for improvement

- Main present concerns, addressed by emerging R&D steps:
  - ⋇ beam related (beamstrahlung) background: rate subject to sizeable uncertainties

    $\Rrightarrow$ trend of R&D: evolve time stamping toward a few 100 ns (bunch-tagging)

    $\hookrightarrow$ performance perspectives depend on pixel technology: CPS, SoI ?, others ?

    N.B.: pixel dimensions will depend on process feature size
  - ⋇ material budget: reduce impact of mechanical supports and services

    $\Rrightarrow$ industrial stitching seems promising but there are issues to be addressed soon ...

  N.B. **ILC objectives overlap with those of heavy ion (collider) expts** $\Rrightarrow$ shared effort possibilities ?

- Timeline:
  - ⋇ techno. choices of pixel sensors & system integration for an ILC vertex detector may still wait 5 - 10 years
  - ⋇ physics performances described in TDR/DBD (2012) anticipated to improve significantly meanwhile

Issue: σ_{sp} & Δ_t in same sensor

- SPATIAL RESOLUTION :
  - Target value: $\lesssim$ 5 to 3 μm
  - Function of pixel pitch

    $\times$ signal charge sharing

    $\times$ charge amplitude

    $\times$ charge encoding (nb of bits, SNR)

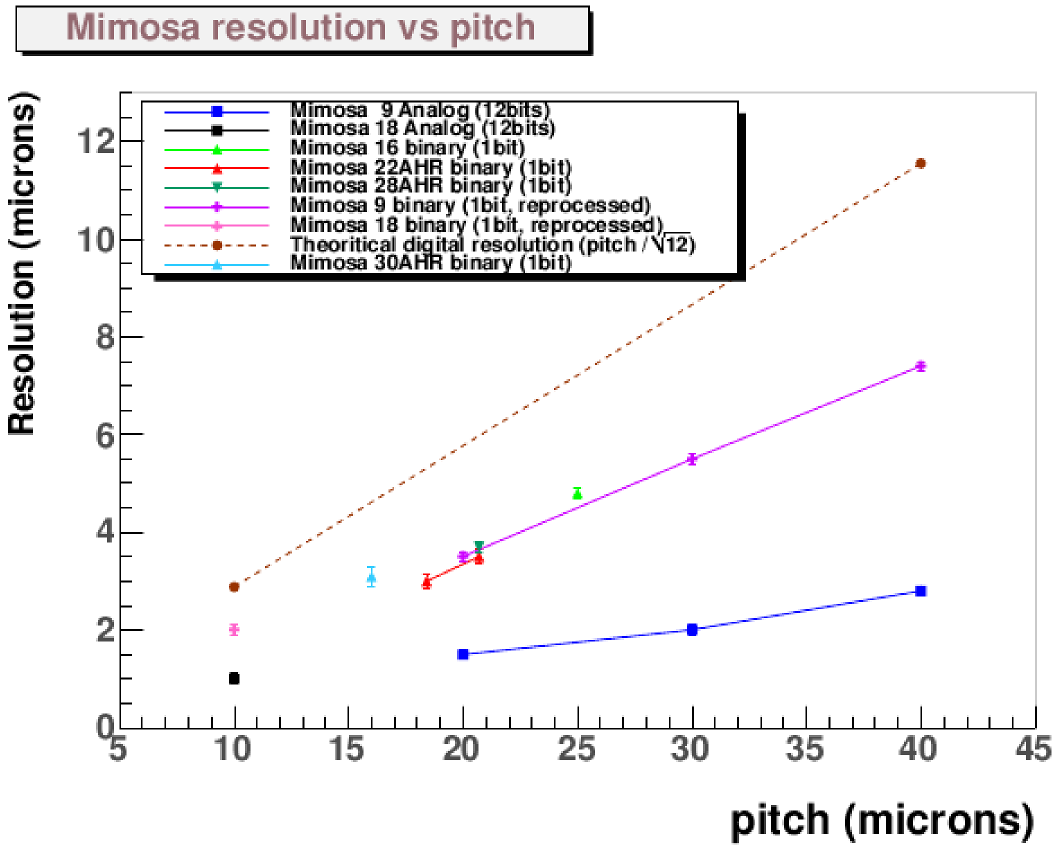
    Ex: 25 μm pitch $\times$ M$_{clus}$ = 1 (full depletion, $\theta \sim 90^\circ$)

    $\Rrightarrow \sigma_{sp} \simeq 7\ \mu m$!
  - Correlation with read-out speed:

    $\Delta_t \simeq$ few ns imposes fast charge collection

    (full depletion, large collection diode, ...)

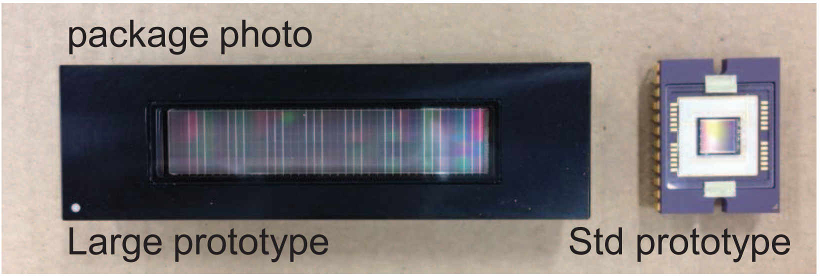
    $\Rrightarrow$ charge sharing suppressed
  - Tension mitigated IF $\Delta_t \gtrsim$ 100 ns



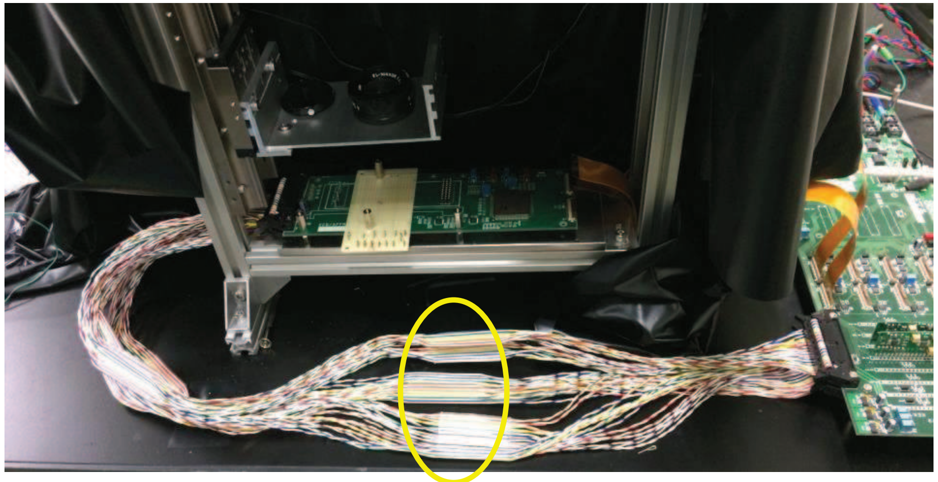
- TIME STAMPING :
  - mainly dictated by beam related background rate (similar at ILC & FCCee)
  - $\sigma_t \lesssim 1\ \mu s \Rrightarrow$ hit rate $\sim$ few 10^{-4}/cm^2/s $\times$ safety factor (e.g. 3-5)

    $\Rrightarrow$ pixel array occupancy $\sim$ O(10^{-3}) at ILC250 & FCCee $\Rrightarrow$ Affordable !

Large Prototype FPCCD test status



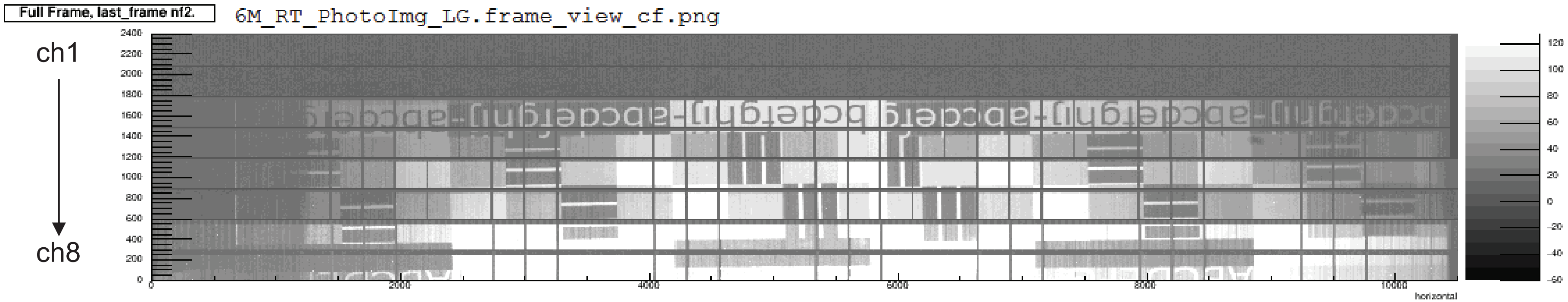
Large prototype die size is 62.4 X 12.3, that is similar size of FPCCD VTX detector 1st layer sensor.



CCD clock : P1H/P2H/P1V/P2V
Input capacitances are large, 10nF~100nF.
It's important to manage clock cabling. In our test bench, 9 twisted-pare are paralleled for each clocks. Z_0 = 11~12 [ohm]

LargeCCD	DUT:CPK1-14-CP01-08				ASIC ch.
	V. pix. size	H. pix. Size	Horizontal num. pixel	Vertical num. pixel	
OS8	6 x 6	6 x 6	10400	255	ch1
OS7					ch2
OS6	6 x 6	6 x 12	10400	254	ch3
OS5					ch4
OS4	8 x 8	8 x 8	7800	191	ch5
OS3					ch6
OS2	12 x 12	12 x 12	5200	127	ch7
OS1					ch8

Photo Image test, read out 0.625Mpix/sec



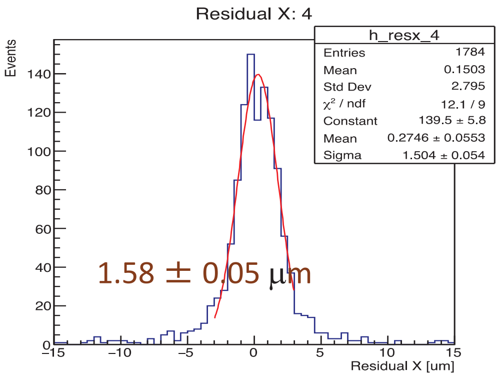
Large prototype CCD is working except ch7 and ch8, of which H. pix size 6 x 6 um^2.
We are working on Fe55 radiation test, and to raise the readout speed up to 10Mpix/sec.

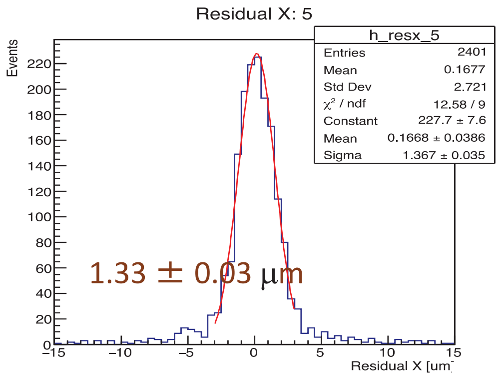
SoI Development (1/2)

SOFIST: SOI Fine measurement of Space and Time

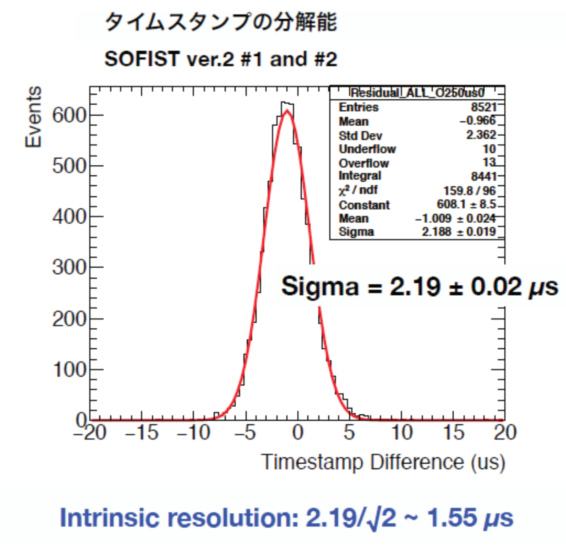
KEK, U Tsukuba, Tohoku U.

Each pixel records multiple hit data (charge and time) to read between beam train



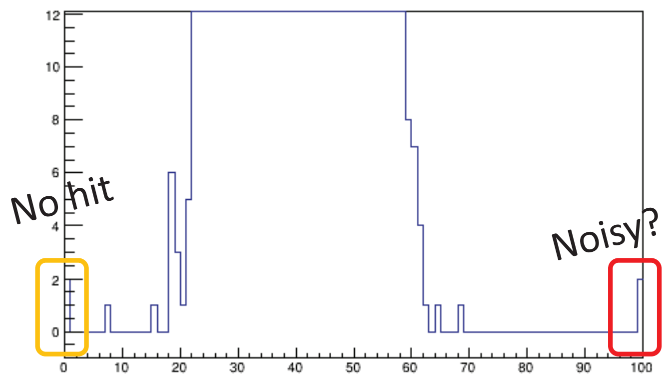


Spatial resolution of 20µm pixel V1 sensors measured in a beam. (X and Y directions)
Values for 100 µm depletion depths are shown



Timestamp difference of two V2 chips measured in a beam.
Precession of 1.55µs is obtained for 500µs gate width

V4: first SOI 3D stack (see next page and Tsuboyama presentation)

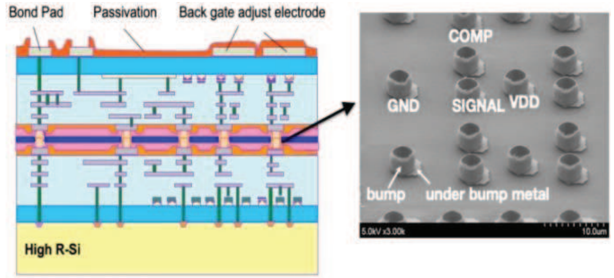


Hit distribution to β source (top truncated)
0-hit corresponds to 0.04% of failed contact

SOI development at IPHC

New features available in the SOI technology

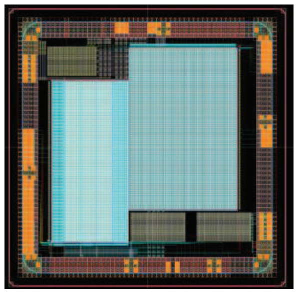
- Double tier “3D” – 5 µm pitch bonding *NIMA A 924 (2019) 422–425*
- Pinned photo-diode – *doi : 10.3390/s18010027*



Prototyping at IPHC

- Developed a Digital Library in cooperation with KEK
- Submitted two sensors in the last MPW run
  - Digital – for the Digital Library characterization
  - Analog

300µm thick - 6x6 mm^2



Analog Sensor features:

- Pixels in 18 µm pitch
- Matrix of Mimosis pixels
- New amplifier architecture
- Pixels with different collecting diodes

Study:

- Charge collection & Timing
- Radiation damage influence

Perspectives

- 20 x 20 µm^2 Mimosis pixel with a digital tier on top
- Assembled structure thinned down to ˜ 50 – 75 µm

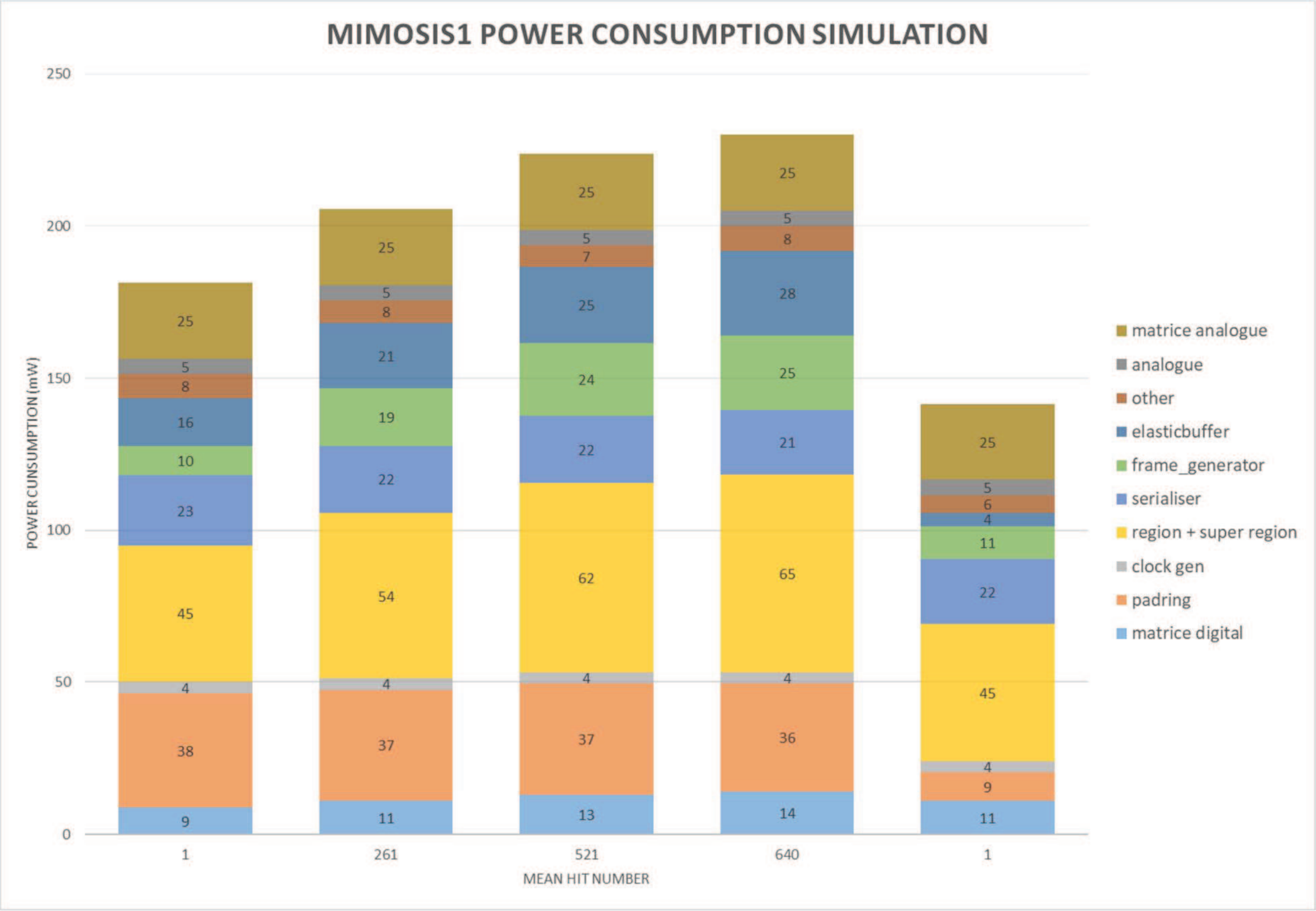
Next MPW submission in May 2020

Power Consumption of MIMOSIS-1 (1/2)

- Analogue Power: 30 mW (analogue pixel+PLL+DAC+ analogue buffers)
- Total Power = Analogue Power + Digital Power
- Total Power Density 1= Total Power/5.33 cm^2 (total surface)
- Total Power Density 2= Total Power/4.20 cm^2 (active surface)
- Power consumption with 8 outputs

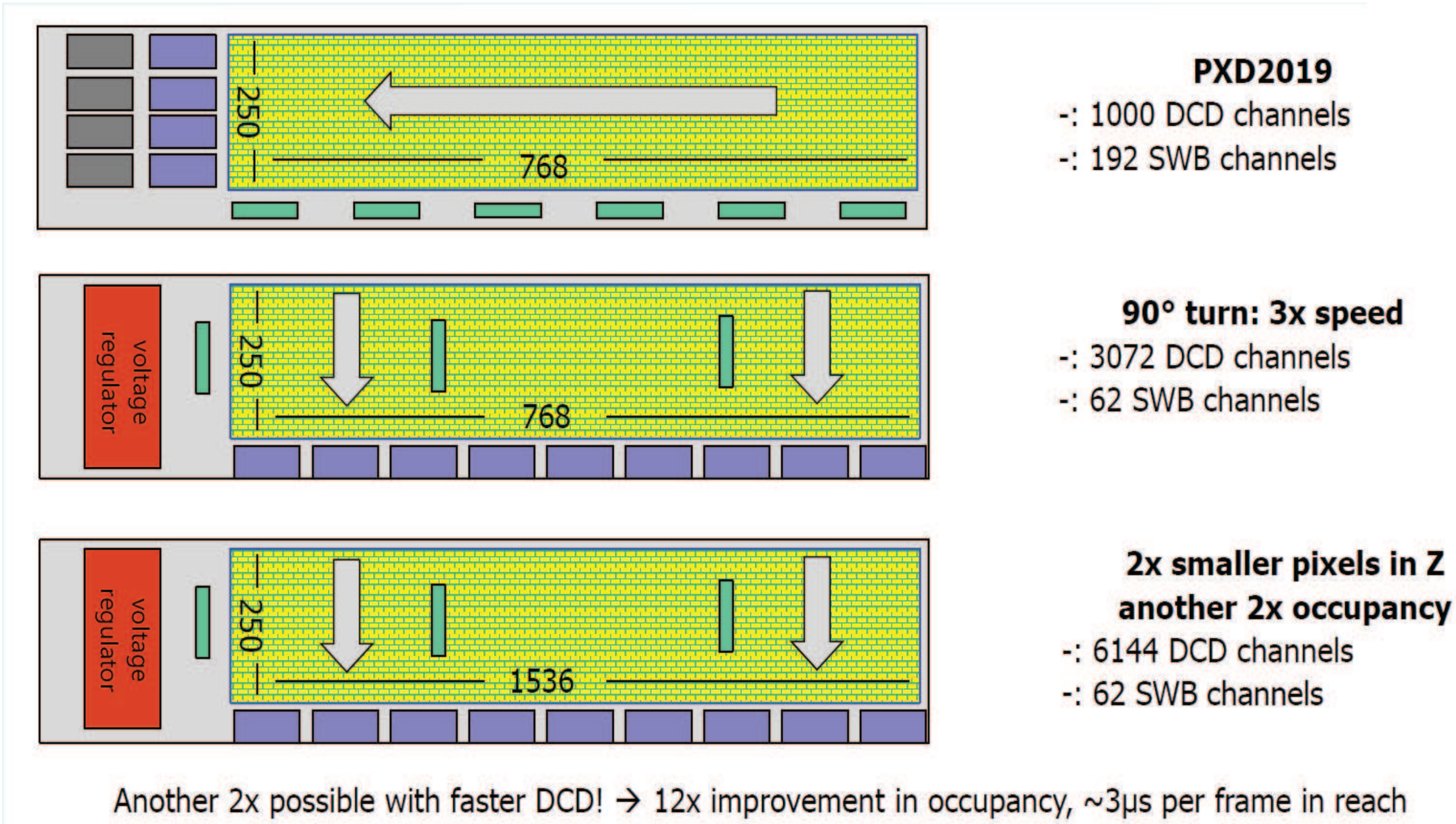
	1 pixel/frame	~260 pixels/frame	~520 pixels/frame	~640 pixels/frame	1 pixel/frame 2 outputs
Digital Power mW	150	175	195	200	110
Total Power mW	180	205	225	230	140
Total Power Density 1 mW/cm^2	34	39	42	43	27
Total Power Density 2 mW/cm^2	43	49	53	55	34

Power Consumption of MIMOSIS-1 (2/2)



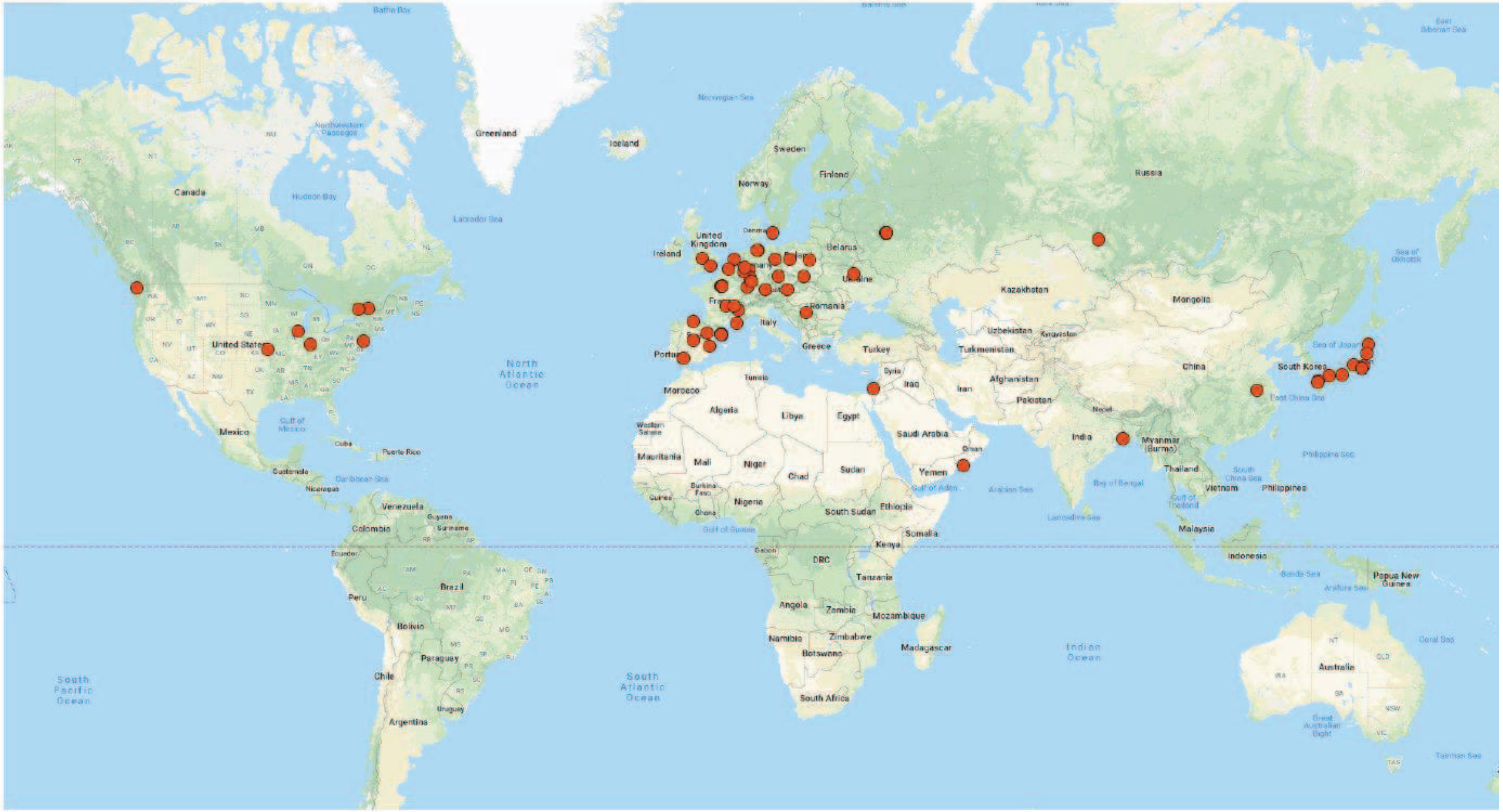
Ex: DEPFET Potential Approach for Shorter Integration Time

- DEPFET pixels (50 μm pitch, 20 μs r.o.) equip the PXD detector of BELLE-II



courtesy of Laci Andricek

The ILD Collaboration (70 Institutes)


Greenland
Iceland
Canada
Hudson Bay
Labrador Sea
Baffin Bay
Norwegian Sea
Sweden
Norway
Finland
Russia
Ireland
United Kingdom
Belarus
Ukraine
Romania
Italy
Greece
Turkey
Portugal
Kazakhstan
Mongolia
Uzbekistan
Turkmenistan
Afghanistan
Pakistan
China
South Korea
Sea of Japan
East China Sea
United States
Mexico
Gulf of Mexico
Cuba
Puerto Rico
Guatemala
Nicaragua
Caribbean Sea
Venezuela
Colombia
Guyana
Suriname
Ecuador
Peru
Brazil
Bolivia
Paraguay
Chile
Uruguay
Argentina
North Atlantic Ocean
South Atlantic Ocean
South Pacific Ocean
Morocco
Tunisia
Algeria
Libya
Egypt
Western Sahara
Mauritania
Mali
Niger
Chad
Sudan
Burkina Faso
Guinea
Ghana
Nigeria
Gulf of Guinea
Gabon
South Sudan
Ethiopia
Somalia
Kenya
DRC
Tanzania
Angola
Zambia
Mozambique
Namibia
Zimbabwe
Botswana
Madagascar
South Africa
Syria
Iraq
Iran
Saudi Arabia
Oman
Yemen
Gulf of Aden
Arabian Sea
India
Nepal
Bay of Bengal
Myanmar (Burma)
Thailand
Vietnam
Philippines
Philippine Sea
South China Sea
Malaysia
Indonesia
Papua New Guinea
Indian Ocean
Australia
Coral Sea
Tasman Sea
Great Australian Bight