

# On-Going Evolution of CMOS Pixel Sensors

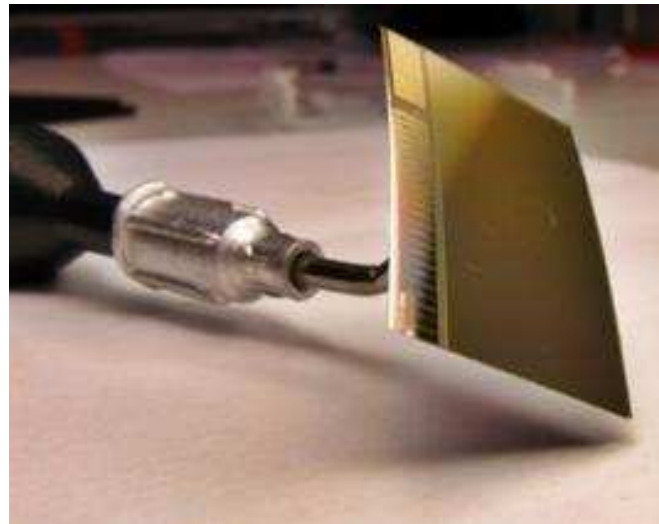
## Joint French-Ukrainian Workshop 2021

M.Winter / IJCLab, 28 Octobre 2021

- **CONTENTS:**

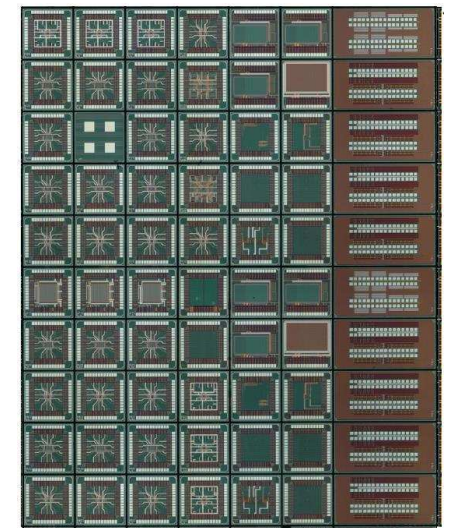
- Reminder:
  - Specificities of CMOS Pixel Sensors
  - Driving goals of their development
- Recent steps in 180 nm technology
- First results in 65 nm technology
- First results on bent sensors
- Summary & Outlook

TJsc: 180 nm



MIMOSIS-1 thinned to 60  $\mu m$

65 nm



MLR-1 Reticule

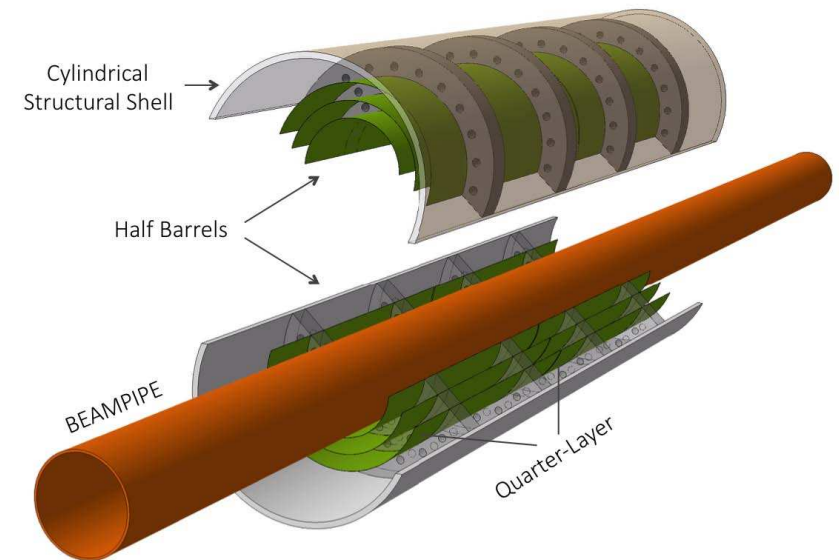
- **French involvement:** 3 laboratories,  $\lesssim 10$  physicists,  $\gtrsim 20$  engineers

# Questions Addressed with Monolithic CMOS Pixel Sensors

## w.r.t. Future $e^+e^-$ Colliders (and Heavy Ion Experiments)

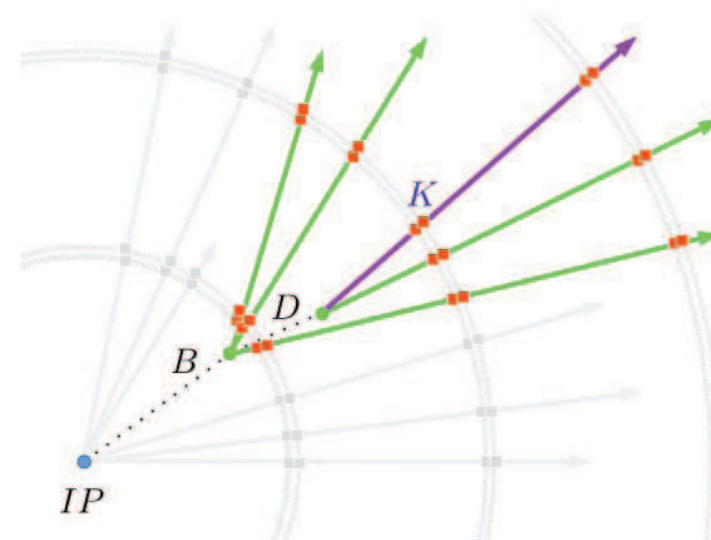
- How well can present sensor read-out architectures be extended to future lepton collider requirements ?
- In how far are known CMOS processes optimisable for future lepton collider vertexing and tracking devices ?
- In how far can the traditionnal detector concept material budget be suppressed with more advanced concepts exploiting contemporary industrial technology ?
- In how far is the recently available 65 nm imaging process of TJsc suited to charge particle detection and to the ambitionned detection performance improvements w.r.t. the limits of the known 180 nm process (granularity, power, etc.) ?

### Emblematic future vertex detector

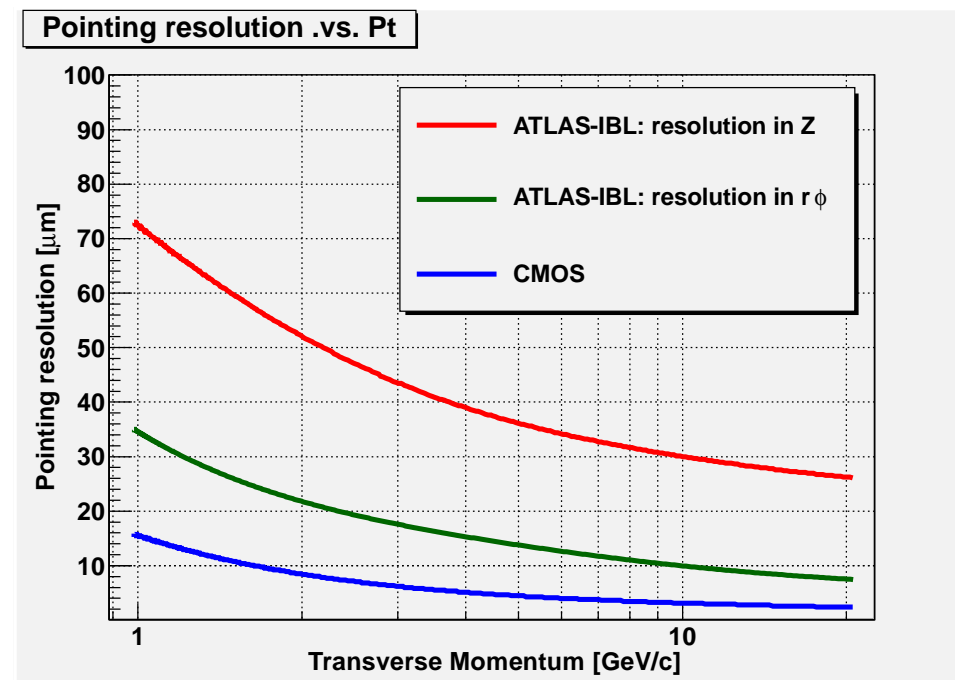


# Motivation for Very Granular & Thin Sensors

- Vertex detectors suited to future lepton colliders (e.g. Higgs-factory) & Heavy-ion experiments
  - \* pixels mandatory for targetted high precision vertexing & tracking
  - \* much less demanding running conditions than at LHC-pp
    - alleviated read-out speed & radiation tolerance requests
- ⇒ **privilege granularity & material budget concerns (power !)**



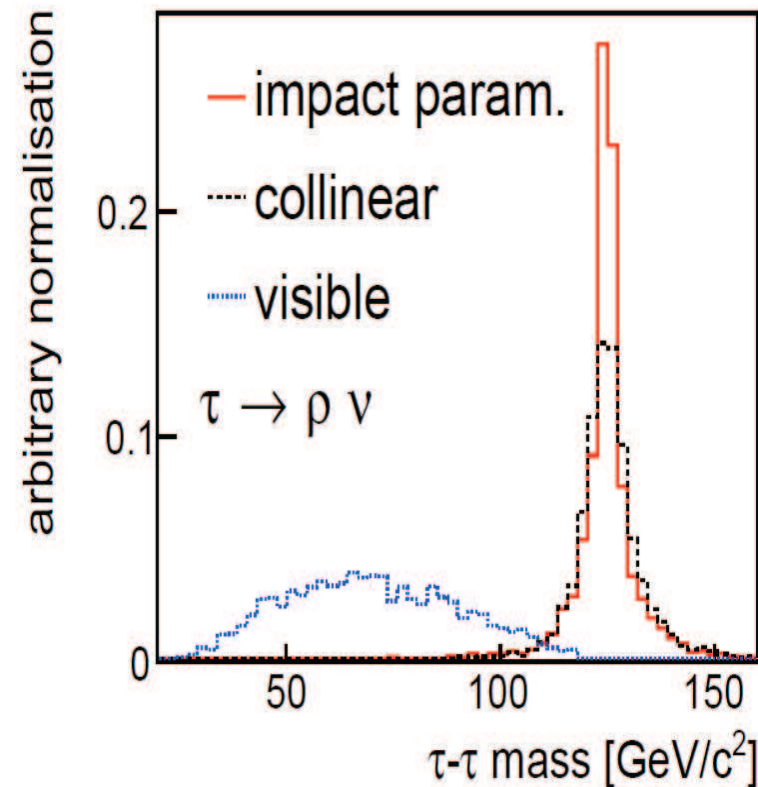
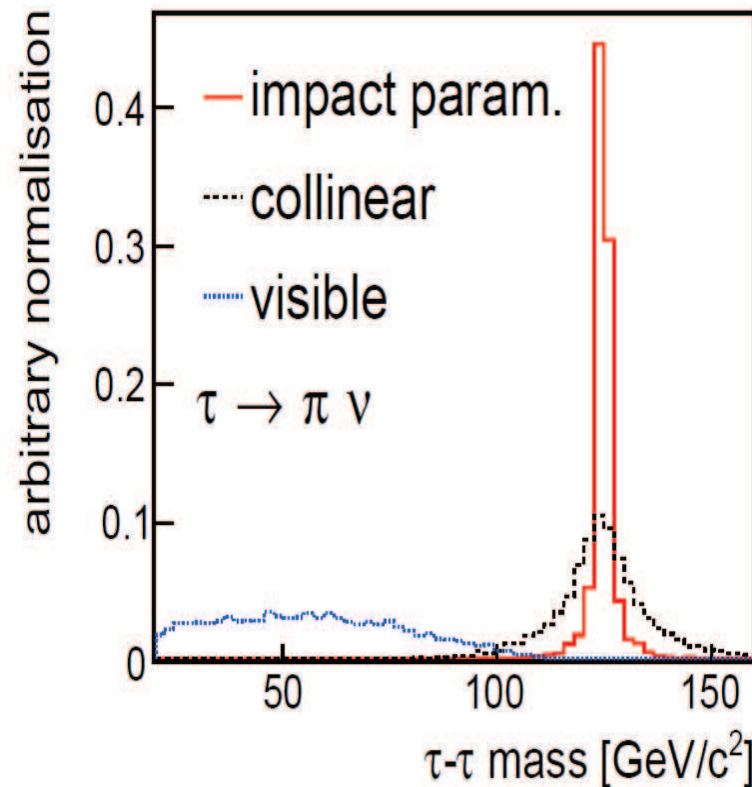
- Generic vertexing goal:
  - \* achieve high efficiency & purity flavour tagging
    - charm & tau, jet-flavour !!!
  - \* reconstruct momentum of soft tracks ( $P_t < 100$  MeV)
  - \* reconstruct displaced vertex charge
- $\sigma_{R\phi, Z} \leq 5 \oplus 10/p \cdot \sin^{3/2}\theta \text{ } \mu m$ 
  - ▷ LHC:  $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot \sin^{3/2}\theta$
- ▷ Comparison:  $\sigma_{R\phi, Z}$  (ILD) with VXD
  - made of **ATLAS-IBL** or ILD-VXD pixels



# Impact of Vertex Detector on $\tau$ lepton reconstruction

## IMPACT OF VERTEX DETECTOR ON $\tau$ RECONSTRUCTION: EXAMPLE OF ILD

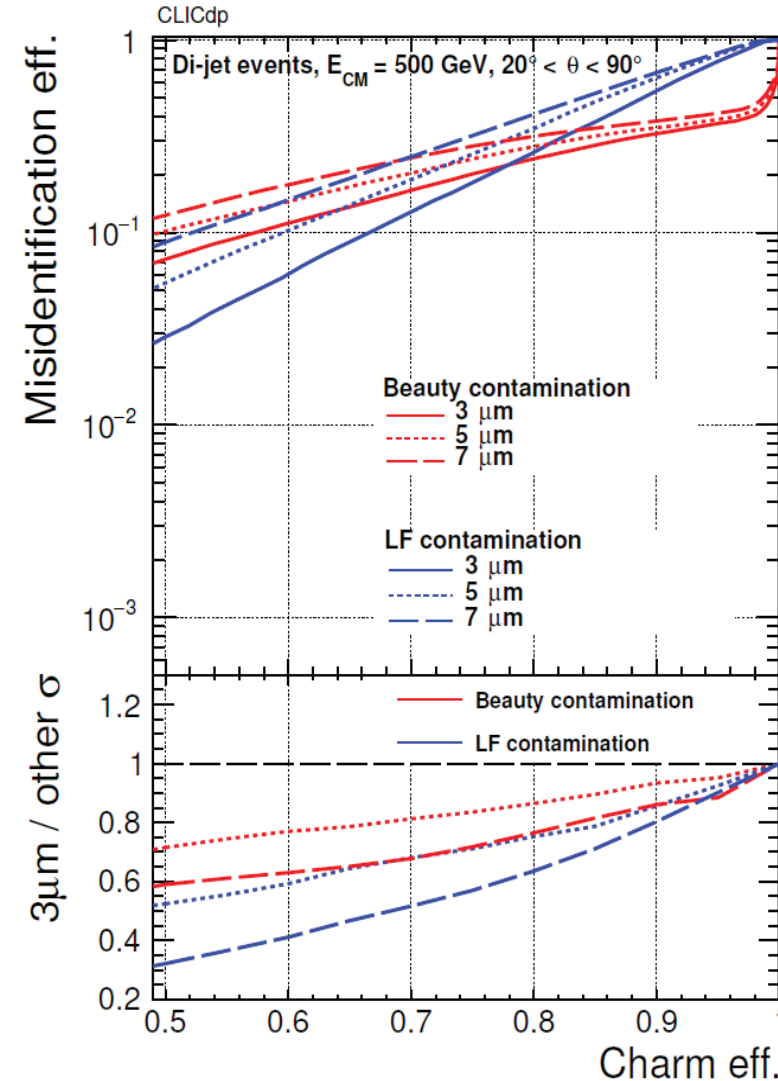
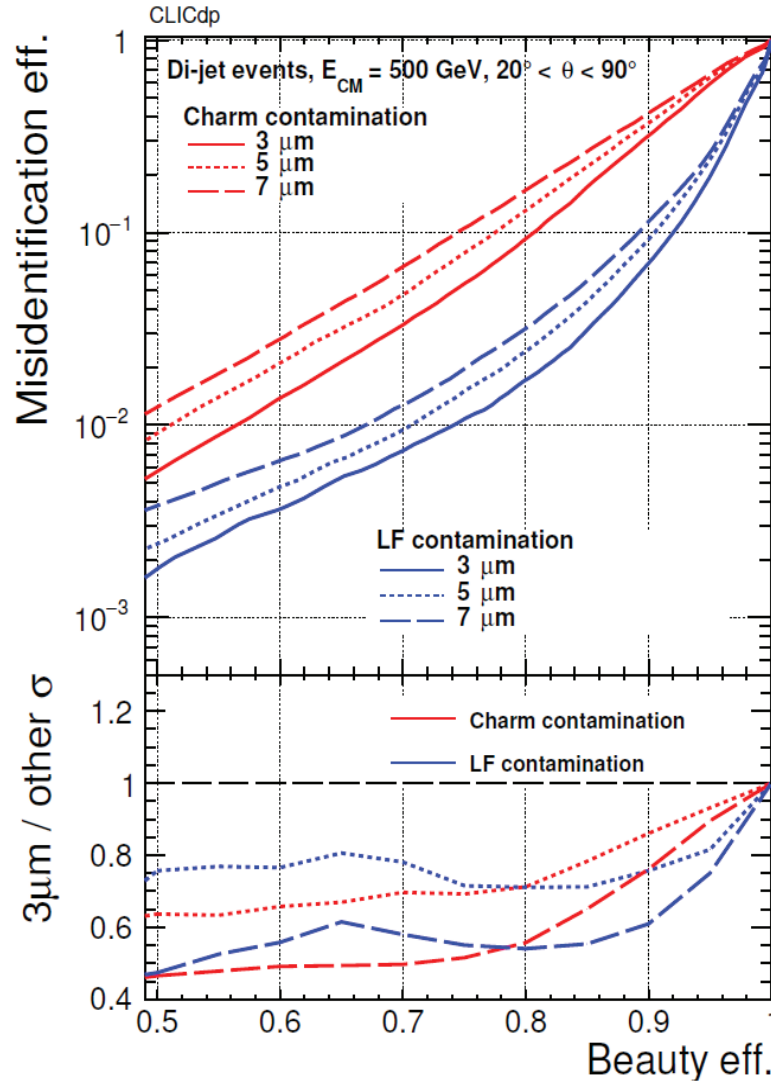
- ✧ use measurements of  $\tau$  spin state in  $e^+e^- \rightarrow ZH \rightarrow \mu^+\mu^-\tau^+\tau^-$  to probe the CP nature of the Higgs boson and search for BSM manifestation by investigating CP conservation in Higgsstrahlung process and Higgs decay
- ✧ concentrate on hadronic decays of  $\tau$ s (one  $\nu$  only) using displaced vertex reconstruction



- ✧ D. Jeans, Nucl. Instrum. Meth. A810, 51 (2016), arXiv:1507.01700 [hep-ex]
- ✧ D. Jeans and G. Wilson, Phys. Rev. D 98, 013007 (2018), arXiv:1804.01241 [hep-ex]



# Impact of the Vertex Detector Spatial Resolution on b, c Tagging

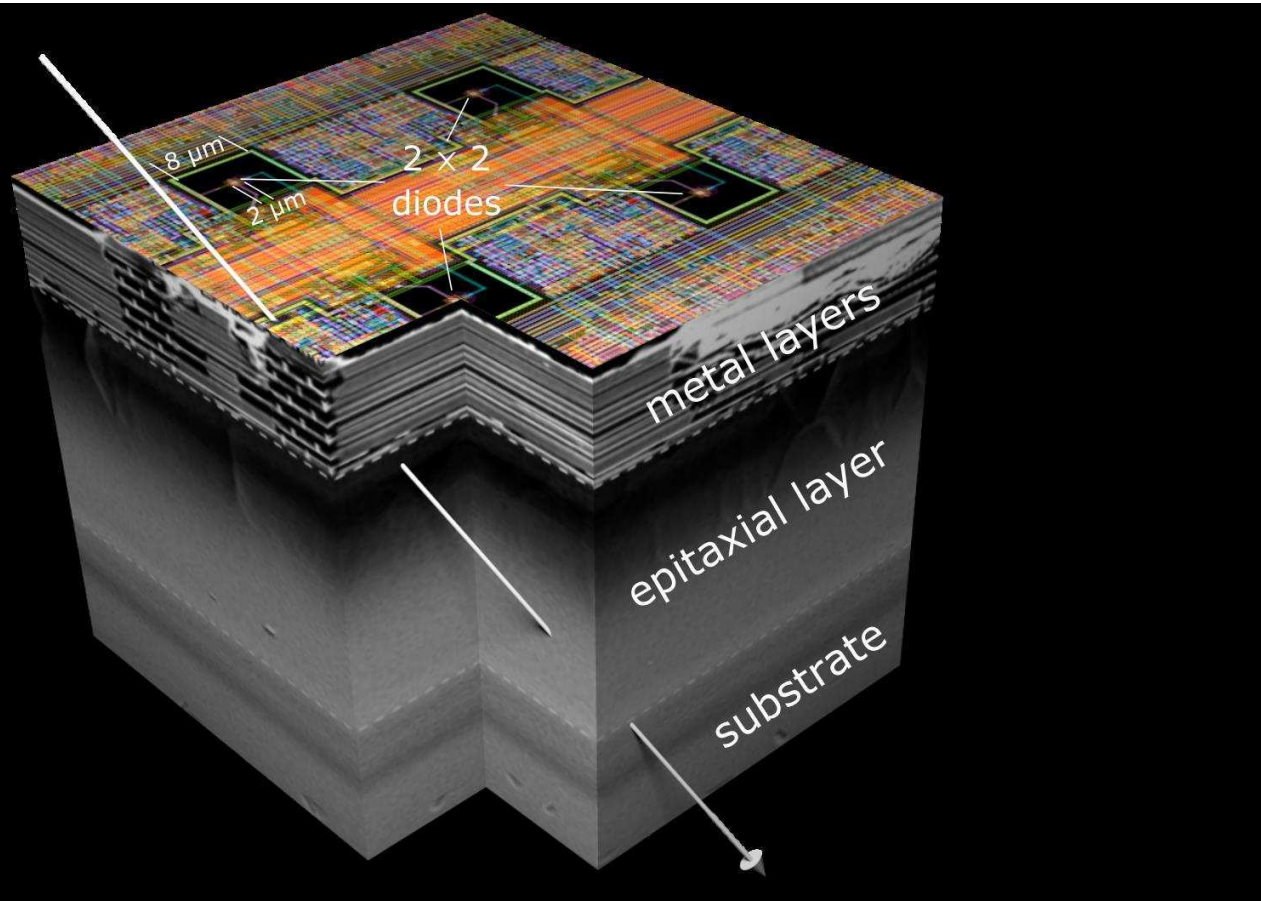


- fermion-pair production at  $E_{CM} = 500$  GeV (CLICdet vertex detector :  $R_{in} = 31$  mm)

D. Arominski et al., CLICdp-Note-2018-005, arXiv:1812.07337 [physics.ins-det] (2018)

- $\sigma_{sp} = 7 \mu\text{m} \rightarrow 3 \mu\text{m} \Rightarrow$  contaminations suppressed by  $\sim 20\%$  to  $40\%$  for 90% tagging efficiency

# CMOS Pixel Sensor $\equiv$ DETECTOR with INTEGRATED FRONT-END CIRCUITRY



Cross-section of ALPIDE sensor (Courtesy of M. Mager et al.)

- \* **Detector  $\oplus$  Readout**  
 **$\oplus$  Steering  $\oplus$  Slow control**  
 **$\mu$ circuits in same die**
- \* **R&D addresses**  
**SIMULTANEOUSLY**  
**Sensing Element**  
 **$\oplus$  Read-Out  $\mu$ circuitry**

- **Thin sensitive volume ( $\pm 30 \mu m$ )**  $\Rightarrow$  small signal charge/pixel ( $\sim 10^{2-3} e^-$ )  
 $\Rightarrow$  very low noise  $\mu$ circuits ( $< 30 e^-$  ENC)

# Emerging Sensor in 180 nm: MIMOSIS

- **MIMOSIS development driven by the MVD of CBM/FAIR (final sensor expected in 2023)**  
ALSO: deliverable of CREMLIN+ & forerunner for vertexing & tracking devices at future  $e^+e^-$  machines

- **MIMOSIS pixel array derived from ALPIDE:**

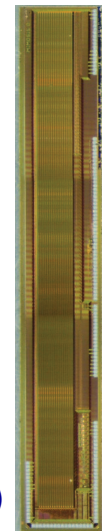
- ✳ TJsc 180 nm imager process with high-res ( $\geq 25 \mu m$  thick) epitaxy
- ✳ modified high-res epitaxy to enhance depletion against NI radiation ( $\sim 10$  times higher than ALPIDE)
- ✳ 1024 col. of 504 pixels with asynchronous r.o. (ALPIDE)  
in-pixel discri. with binary charge encoding  
with DC-coupling (a la ALPIDE) & AC-coupling (new)
- ✳ affordable hit density  $\simeq 50 \times$  ALPIDE (new digital circuitry)
- ✳  $\Delta t \sim 5 \mu s$  = twice faster than ALPIDE
- ✳ power density  $\gtrsim 50 \text{ mW/cm}^2$  (vs hit density)

- **Step-1 (2018): MIMOSIS-0 proto. (32 col. of 504 pixels)**

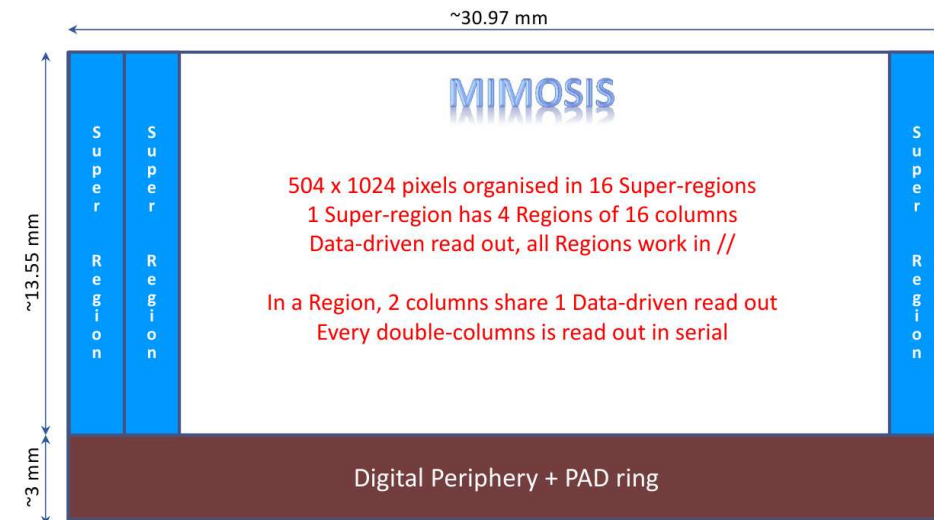
- ✳ validated in-pixel circuitry variants ( $\sim 200 \text{ T/pixel}$ )
- ✳ allowed exploring the limit of time resolution

- **Step-2 (2020): MIMOSIS-1 full size proto.**

- ✳ fabricated in 2020  $\Rightarrow$  fonctionnality tests
- ✳ 2021: noise & detection performance evaluation (3 beam tests)



Physics parameter	Requirements
Spatial resolution	$\sim 5 \mu m$
Time resolution	$\sim 5 \mu s$
Material budget	$0.05\% X_0$
Power consumption	$< 100 - 200 \text{ mW/cm}^2$
Operation temperature	$-40^\circ \text{C}$ to $30^\circ \text{C}$
Temp gradient on sensor	$< 5 \text{ K}$
Radiation tol* (non-ion)	$\sim 7 \times 10^{13} n_{eq}/\text{cm}^2$
Radiation tol* (ionizing)	$\sim 5 \text{ MRad}$
Data flow (peak hit rate)	@ $7 \times 10^5 / (\text{mm}^2 \text{s})$ $> 2 \text{ Gbit/s}$

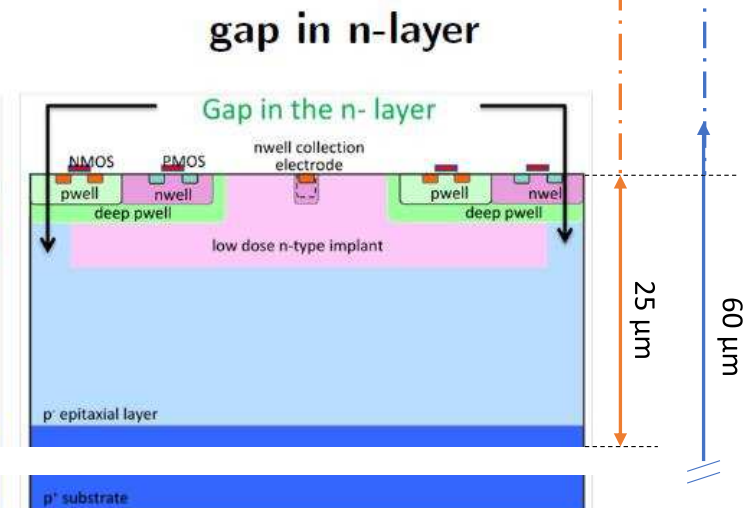
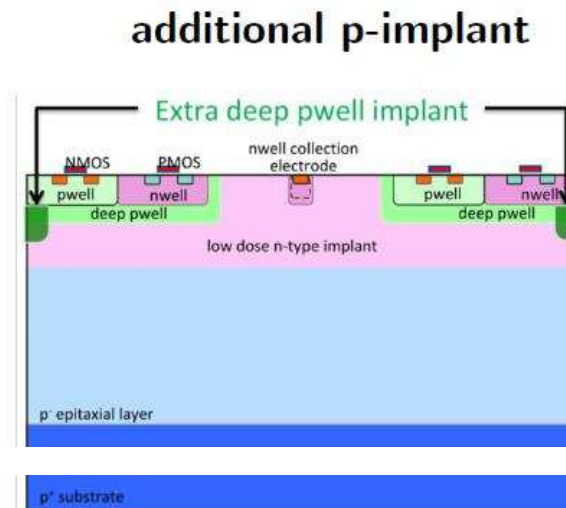
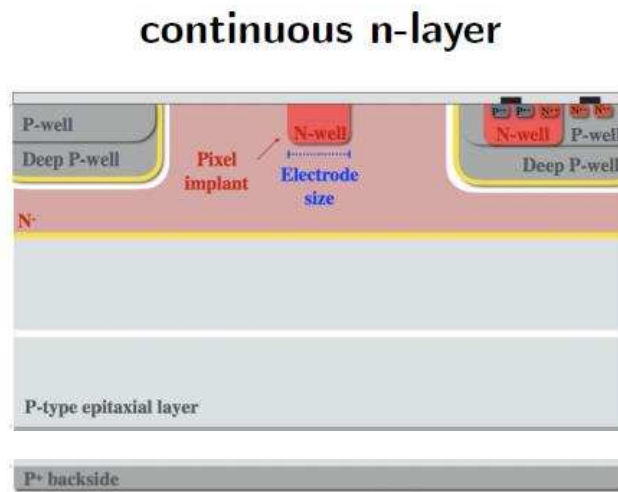


# MIMOSIS-1: EXPLORATION OF EPITAXY VARIANTS

## MIMOSIS-1 – TECHNOLOGY

- Tower/Jazz 180 nm CIS technology
- Various epi:
  - standard process
  - modified (continuous n-layer, additional p-implant, gap in n-layer)
    - to increase lateral depletion field
    - anticipated radiation tolerance improvement

Parameter	Value
Sensor thickness	60 $\mu\text{m}$
Epi layer thickness	$\sim 25 \mu\text{m}$
Epi layer resistivity	$> 1 \text{ k}\Omega\text{cm}$



W. Snoeys, "FASTPIX: sub-nanosecond radiation tolerant CMOS pixel sensors", ATTRACT

from R. Bugiel - TWEPP-21

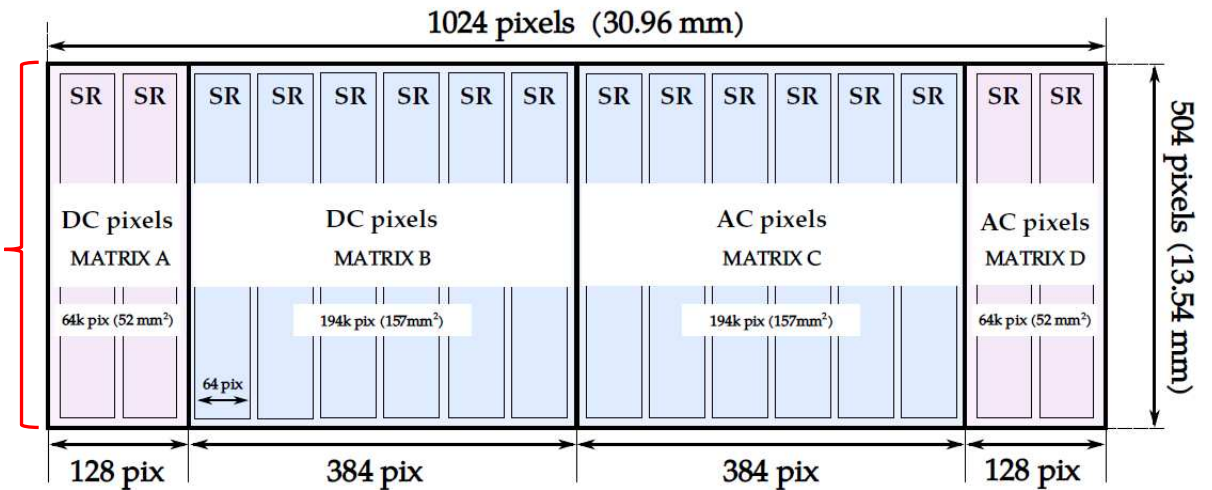


# MIMOSIS-1: EXPLORATION OF IN-PIXEL CIRCUITRY VARIANTS

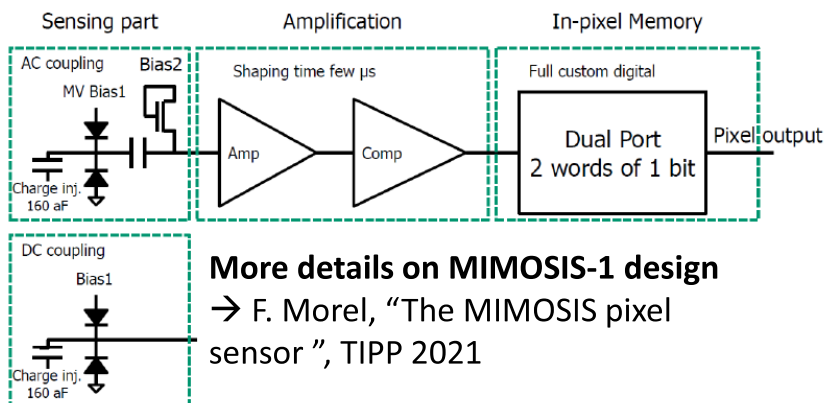
## MIMOSIS-1 – SENSOR OVERVIEW



MIMOSIS-1 fabrication reticules



- 4 submatrices
  - A, D → optimization of CE18 for radiation hardness
  - B, C → similar to MIMOSIS-0
- Pixel size:  $26.88 \mu\text{m} \times 30.25 \mu\text{m}$
- Pixel types:
  - DC pixels: ALPIDE-derived
  - AC pixels: top bias up to  $> 20\text{V}$
- Possibility of pulse injection and pixel masking
- Matrix active area:  $\approx 4.2 \text{ cm}^2$
- Power consumption:  $40 - 70 \text{ mW/cm}^2$  → depending on hit rate



**More details on MIMOSIS-1 design**  
→ F. Morel, "The MIMOSIS pixel sensor", TIPP 2021

from R. Bugiel - TWEPP-21



# MIMOSIS-1: NOISE PERFORMANCE

## GENERAL PERFORMANCE – LABORATORY CHARACTERIZATION

### Laboratory characterization

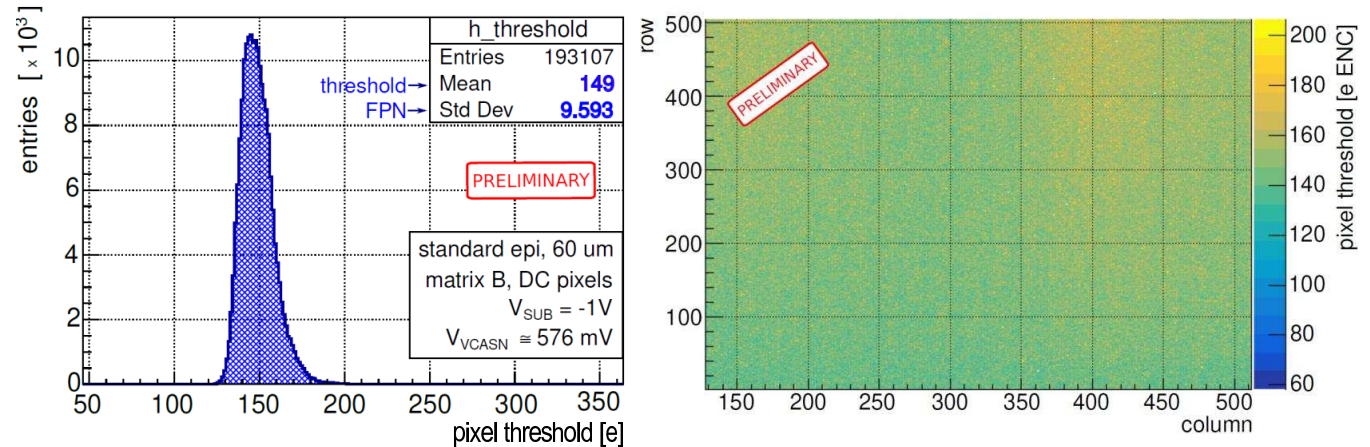
- characterization by pulse injection
- complex phase space of MIMOSIS1 (tuning parameters needed)
  - estimation of thresholds, Fixed Pattern Noise (FPN) and Thermal Noise (TN)
  - all measurements at 15°C
- Ex: performance of matrix B @ 150e threshold (before irradiation):
  - TN: ~3.5 e ENC
  - FPN: ~10 e ENC

Preliminary conversion factor from 1 mV  $\rightarrow$  1 e- (within +/- 25%)

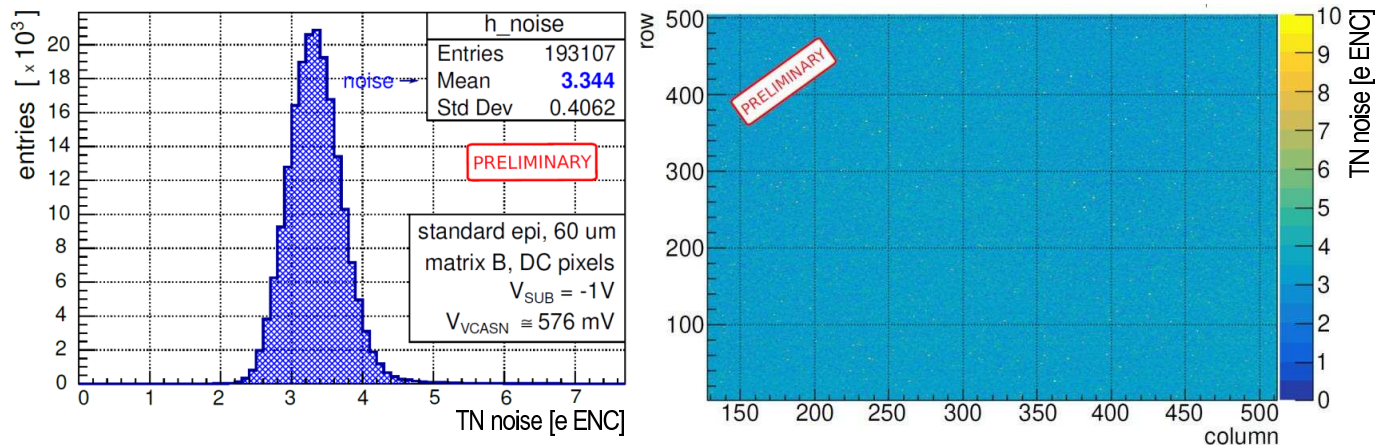
### Summary performance before irradiation:

- Similar, satisfactory performance of all matrices
- **TN: 3-5 e ENC**
- **FPN: 7-10 e ENC** in the operation range
- **AC pixels slightly lower FPN than DC**

### DC PIXELS (mat B) – PIXEL THRESHOLD



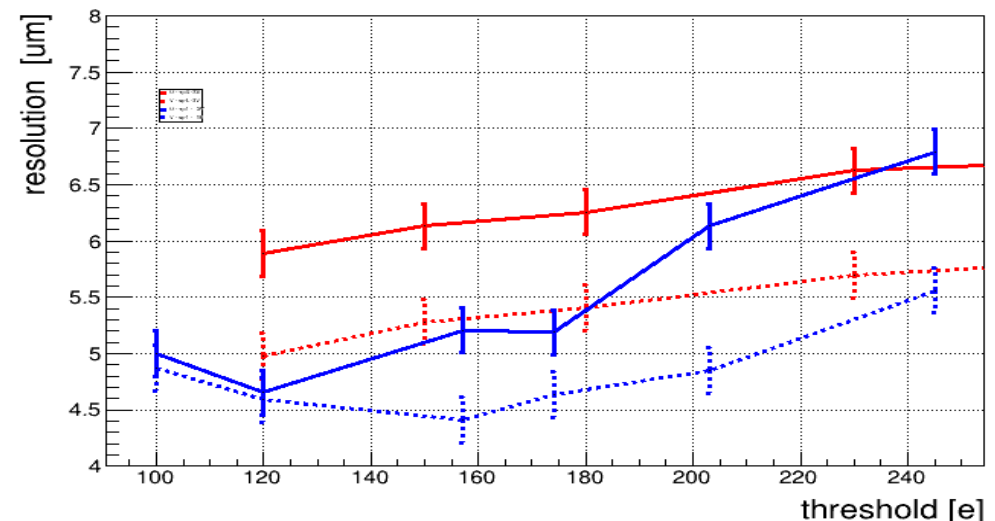
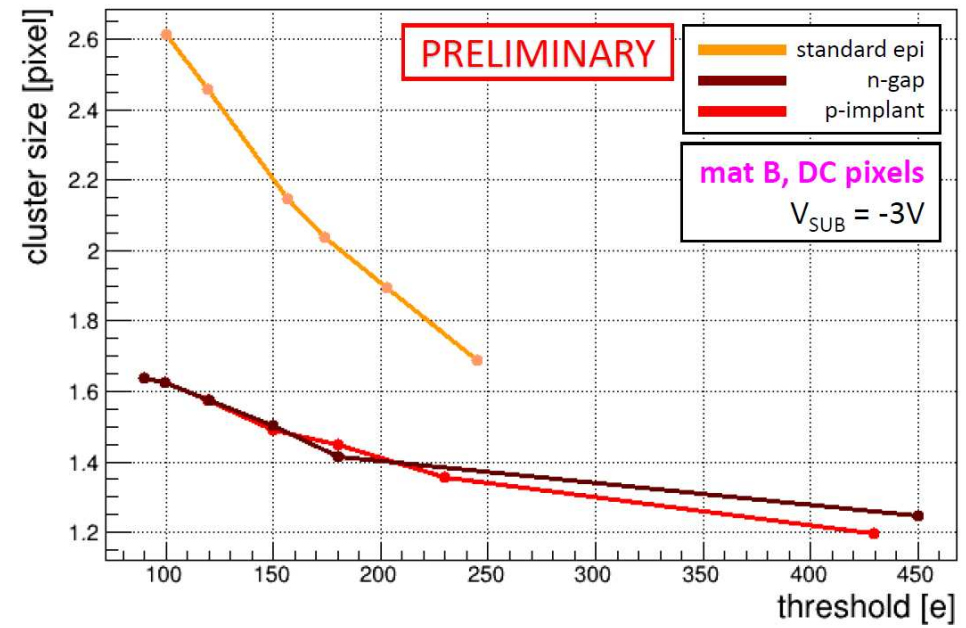
### DC PIXELS (mat B) – THERMAL NOISE



from R. Bugiel - TWEPP-21

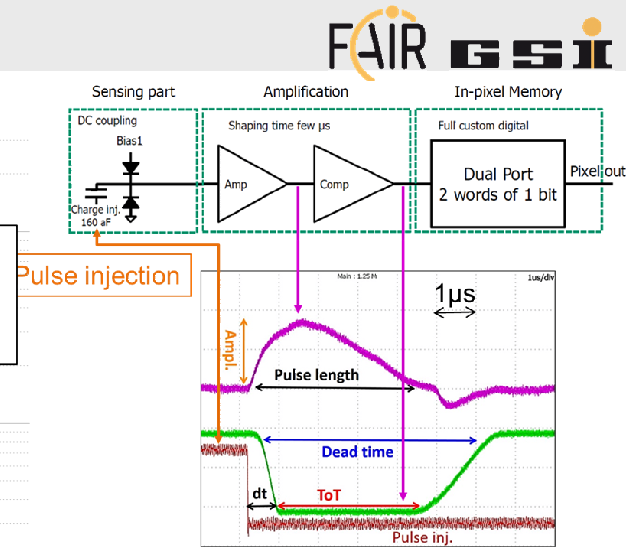
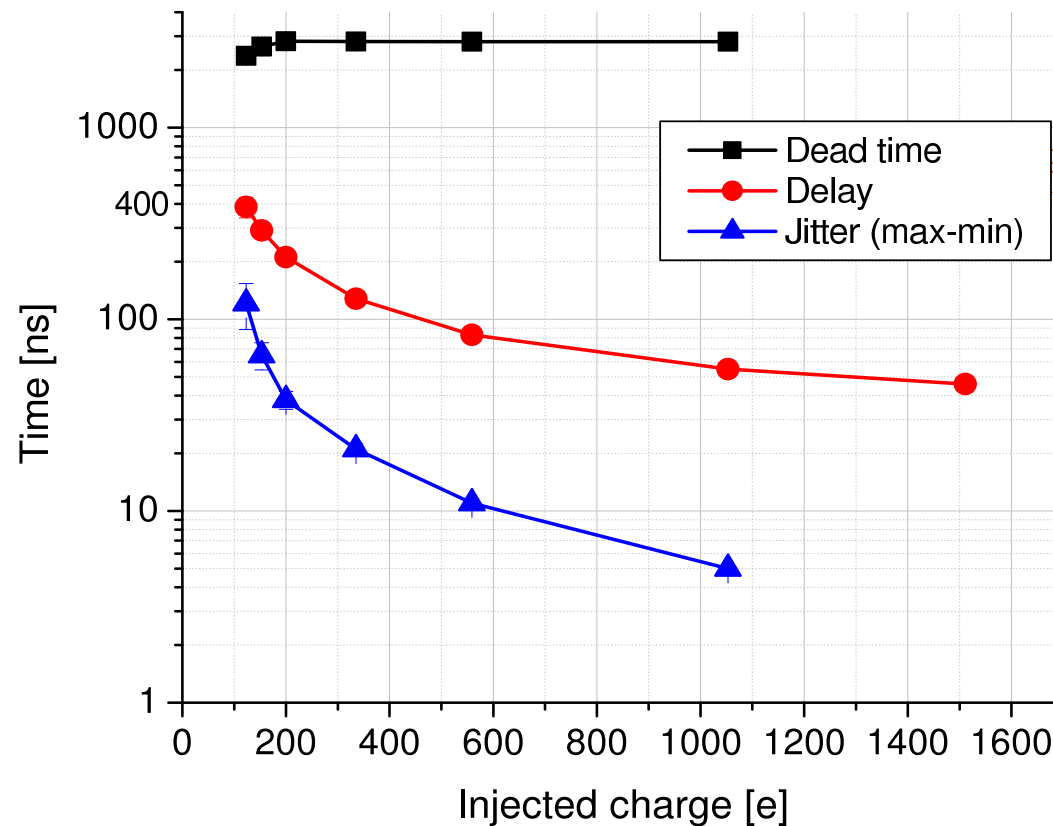
# MIMOSIS-1: M.I.P. PREMINARY DETECTION PERFORMANCE ESTIMATES

- DESY & CERN-SPS (June, Sept., Oct.):
  - \* tests of 3 epitaxy variants: standard, n-gap, p-implants
  - \* results still preliminary
- Cluster Size & Spatial Resolution:
  - \* cluster multiplicity has direct impact on  $\sigma_{R\phi z}$
  - \* significantly smaller for modified epitaxy
    - ↪  $\sigma_{st} \simeq 5 \mu m \rightarrow \sigma_{mod} \gtrsim 6 \mu m$
  - \* cluster multiplicity still smaller with AC-coupling pixels
    - ⇒ try thicker epitaxy
- Detection Efficiency (analysis on-going)
  - \* close to 100 % for all epitaxy and pixel variants over a wide range of threshold values  $\gtrsim 100 e^-$
  - \* Noisy pixel rate seems  $\lesssim 10^{-6}$
- Radiation Tolerance at  $T_{room}$  (very preliminary):
  - \* Impact of NIEL studied up to  $3 \cdot 10^{14} n_{eq}/cm^2$  ✓
  - \* Impact TID studied up to 5 MRad ✓



# MIMOSIS READ-OUT SPEED POTENTIAL FOR FUTURE ELECTRON MACHINES

## MIMOSIS-0: Pulse tests

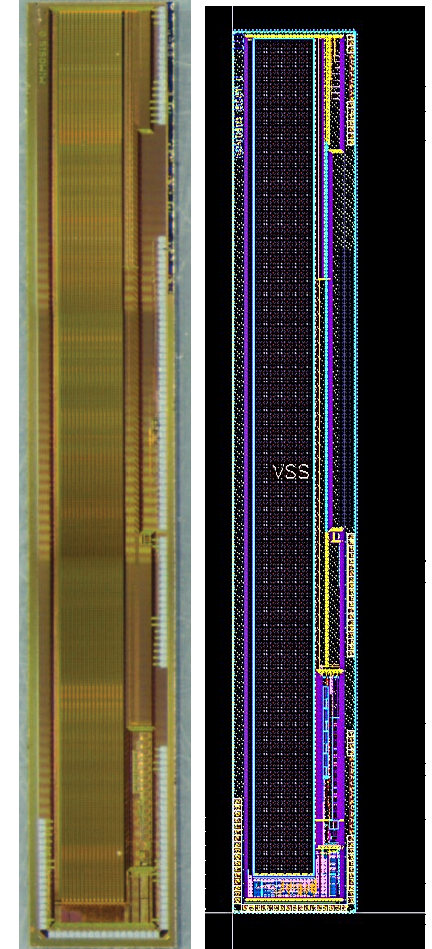


After optimizing trim voltages:

- Time walk + jitter < 1  $\mu$ s, dead time  $\sim$  3  $\mu$ s
- AC pixel (not shown) 30% slower than DC pixel
- Might reach time accuracy < 1  $\mu$ s (target frame readout time 5  $\mu$ s)

# MIMOSIS READ-OUT SPEED POTENTIAL: NEXT STEP

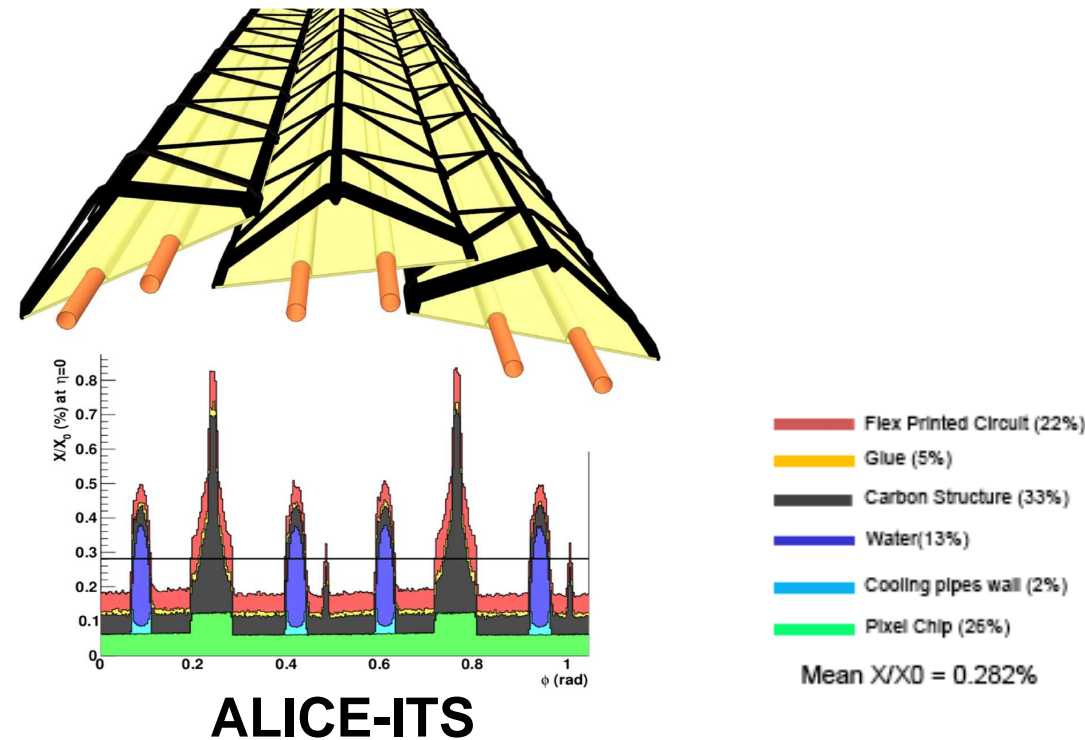
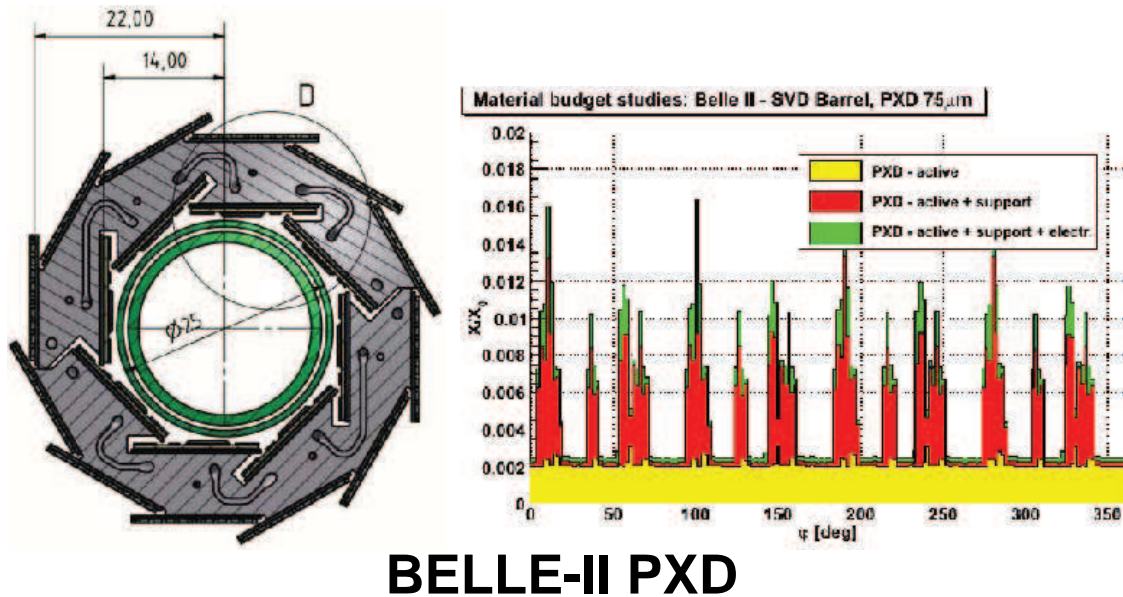
- New foundry submission in Octobre: MIMOSIS-0<sub>Fast</sub>
  - objective: about 10-20 times faster read-out than MIMOSIS ( $5\ \mu s$ )
  - ✱ 2 flavours of in-pixel Pre-AMP: MALTA-like & IPHC
    - ↪ operating in the 200 ns–500 ns range
  - ✱ minor modifications of the digital circuitry
  - adaptation of DAC polarisations to the new in-pixel Pre-AMPs
  - avoid MIM capacitors in DACs
  - **increase in-pixel current typically by factor O(10)**
  - ✱ New EPI variants investigated (incl.  $50\ \mu m$  thick)
- Status: submitted, expected back from foundry in Q1/'22





# Major R&D Goal in Coming Years: Material Budget Reduction

- Physics perfo. limited by material budget of services & overlaps of neighbouring modules/ladders

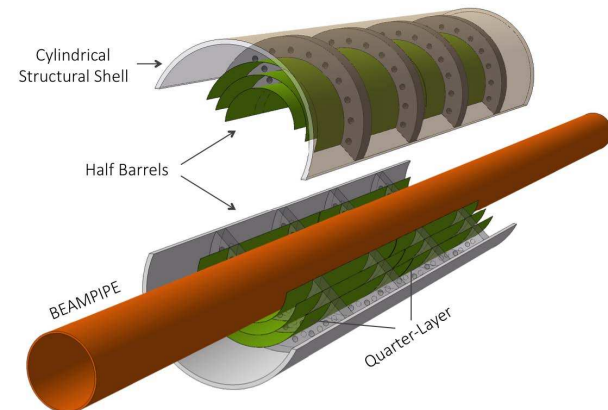


- Contribution of sensors to total material budget of vertex detector layer is modest: 15 - 30%

- R&D objective beyond "classical" concepts:**

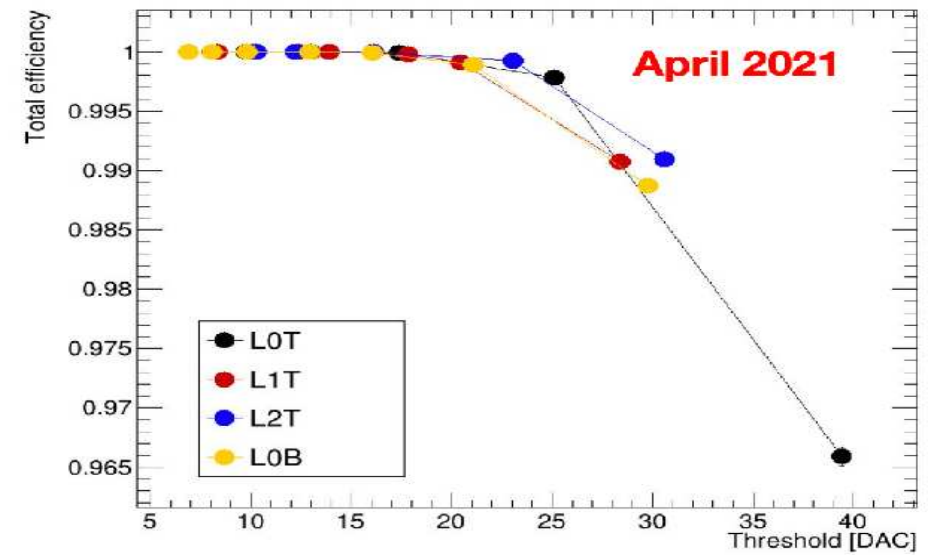
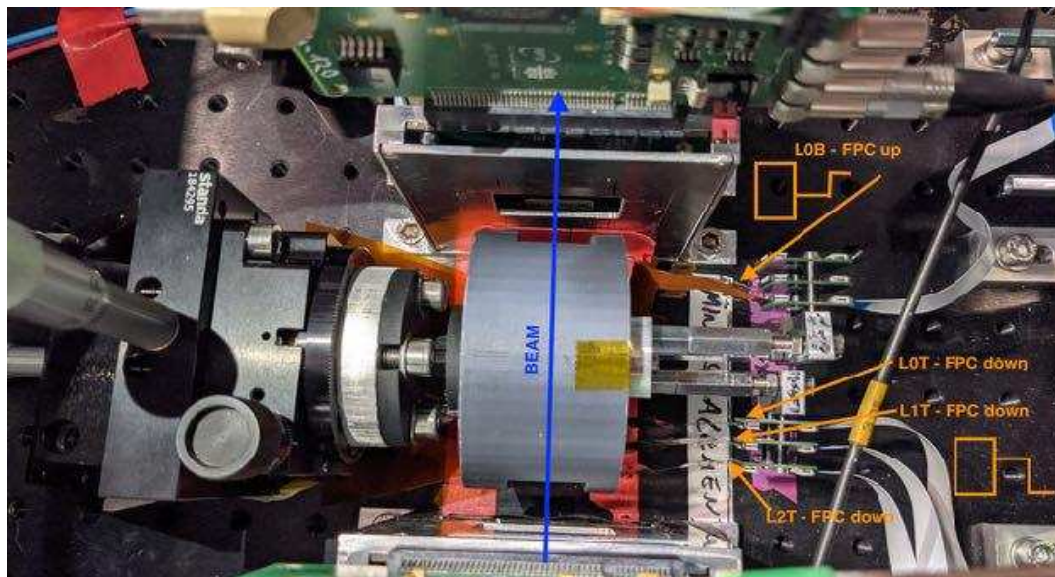
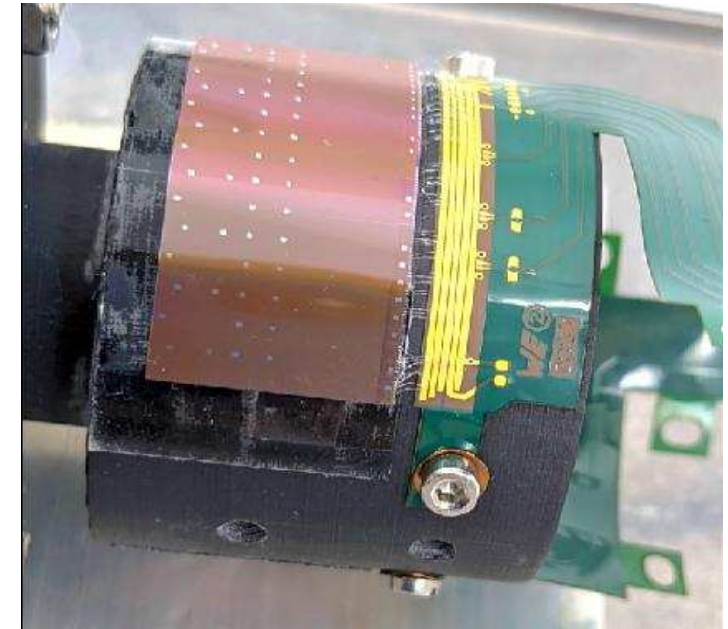
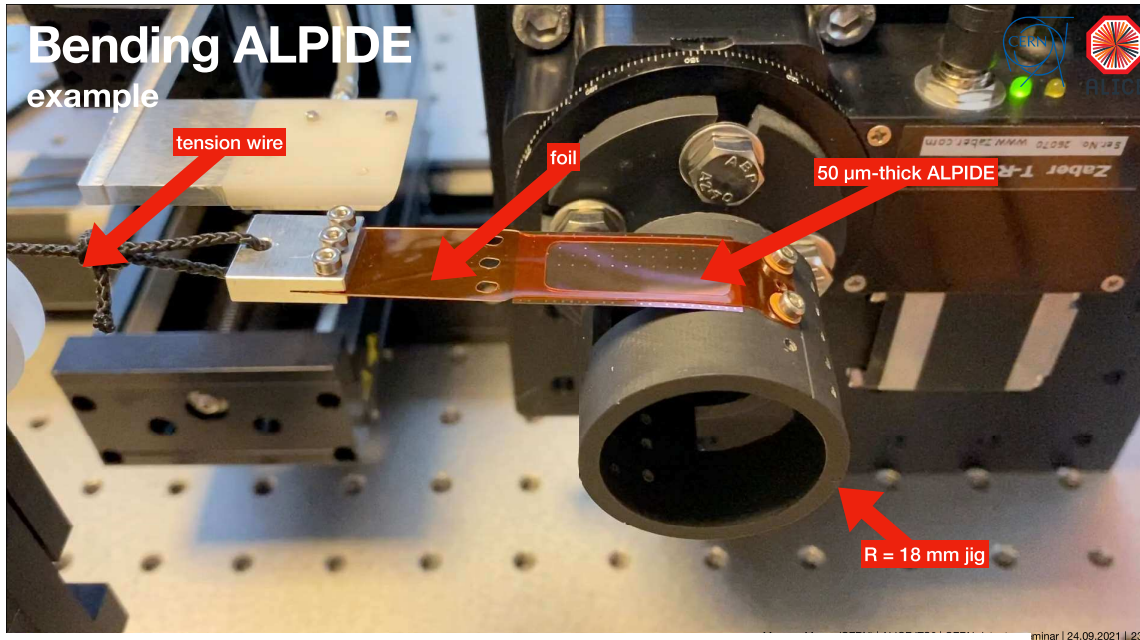
- Innermost layer: try stitched & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process
- Concept with minimised mechanical support

(e.g. using beam pipe) See Talk of M. Mager at Vertex-19, Lopud Island, Oct.'19





# BENDING ACHIEVEMENTS WITH ALPIDE SENSORS



from M. Mager - CERN

# DEVELOPING A NEW VERTEX DETECTOR CONCEPT VIA ITS-3

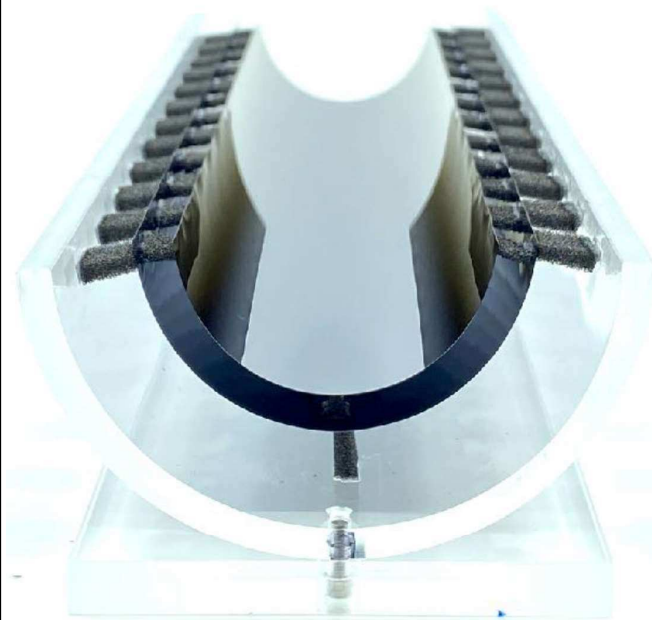
## Layer assembly



Layer 2



Layers 2+1



Layers 2+1+0



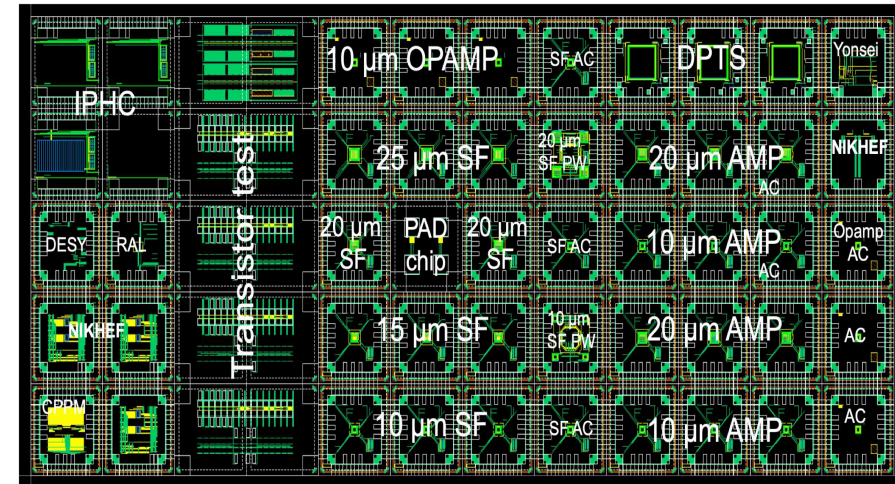
3-layer integration successful!



## Exploration of a 65 nm Imaging Technology

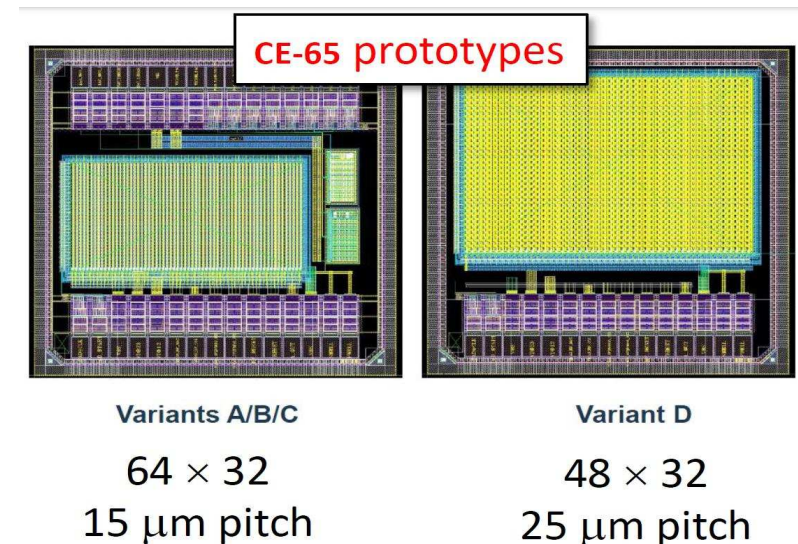
- **Motivations of the R&D:**

- ✱ Smaller feature size than 180 nm technology used for MIMOSIS  
⇒ smaller pixels, more in-pixel functionalities,  
less power consumption, faster readout, ...
- ✱ Imaging technology available since ~ Spring 2020:  
includes stitching ⇒ multireticle sensors
- ✱ R&D coordinated at CERN (ALICE-ITS3 & EP-div)
- ✱ ITS3 goals: small pixels and very low material budget  
exploiting stitching for "supportless" detector layer



- **Prototyping at IPHC for MLR1 (2020):**

- Design of "elementary" test structures with CERN
- Design of 2 chips featuring arrays of  $15 \times 15$  &  $25 \times 25 \mu m^2$  pixels with rolling shutter readout & analog output
- Grouped submission (MLR1) submitted to TowerJazz for fabrication during Winter-Spring 2020-21
- Tests just starting



# CONCLUSIONS

- MIMOSIS IN 180 NM IMAGING PROCESS:
  - ✧  $5\ \mu\text{m} / 5\ \mu\text{s} / < 100\ \text{mW}/\text{cm}^2 / > 10^{14}\ \text{n}_{eq}/\text{cm}^2$ , etc. ✓
  - ✧ Added value of AC-coupling & EPI variants  $\pm$  evaluated
  - ✧ Next steps:
    - CBM-MVD: MIMOSIS-2 (Nov.'21)  $\rightarrow$  MIMOSIS-3 (2023)
    - 200 - 500 ns variant: medium prototype submitted for fabricationPromising design for trackers adapted to future  $e^+e^-$  colliders
- 65 NM EXPLORATION:
  - ✧ MLR1 chips tests starting: prelim. beam test results indicate that the process is adapted to tracking (not trivial)
  - ✧ Next step: ER1 with stitched reticles to be fabricated in Spring '22
  - ✧ First multi-reticle proto. foreseen in 2023 for ALICE-ITS3
- LARGE CURVED CHIPS:
  - ✧ Bending trials with ALPIDE ( $R \simeq 2\ \text{cm}$ ) successful (tested on beam)
  - ✧ Next steps: tests with combined sets of ALPIDE forming a plane, & with sectors of MLR1 wafers
  - ✧ Trials with 65 nm multireticle chips being prepared for ER1

