Future LAr calorimeter

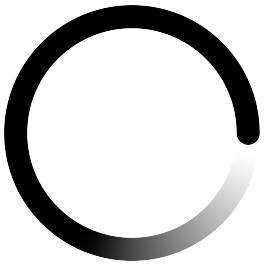
PCB simulations

(from a non expert in electronics...)

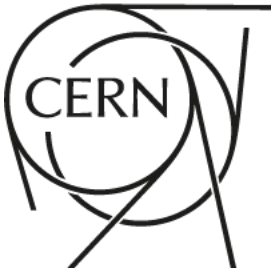
Brieuc François (CERN)

GranuLAr workshop

April 7th, 2022



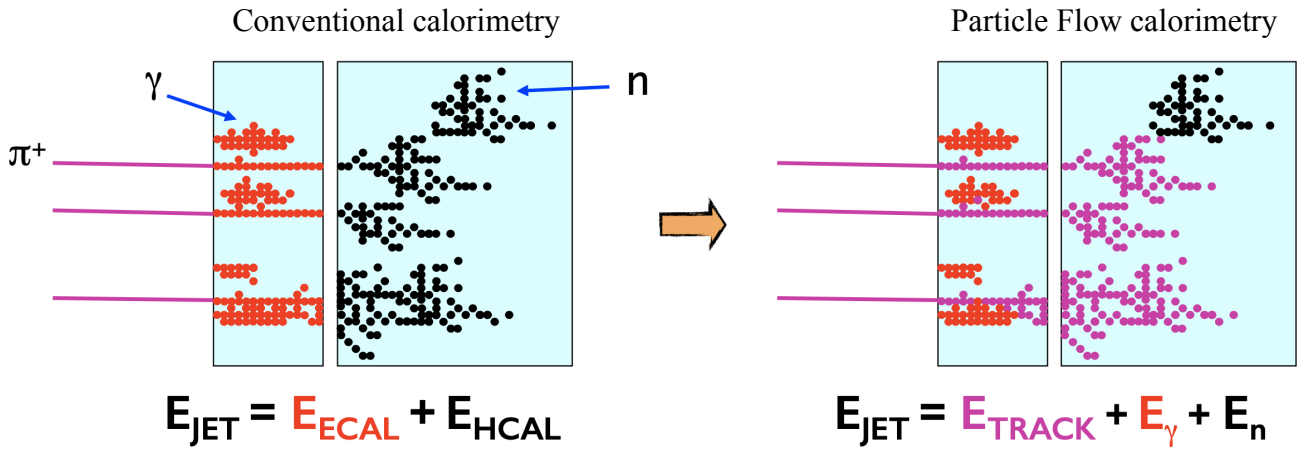
FUTURE CIRCULAR COLLIDER



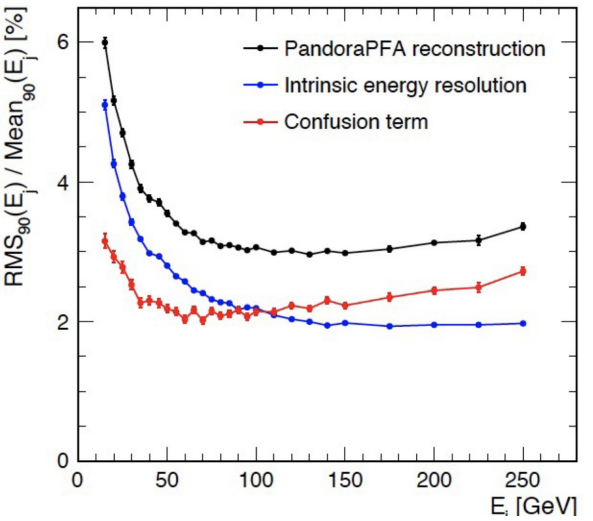
Outline

- Detector Readout Electrodes
- PCB Computer Aided Design (CAD)
- Capacitance Matrix and Detector Noise
- X-talk
- Prototyping
- Discussion

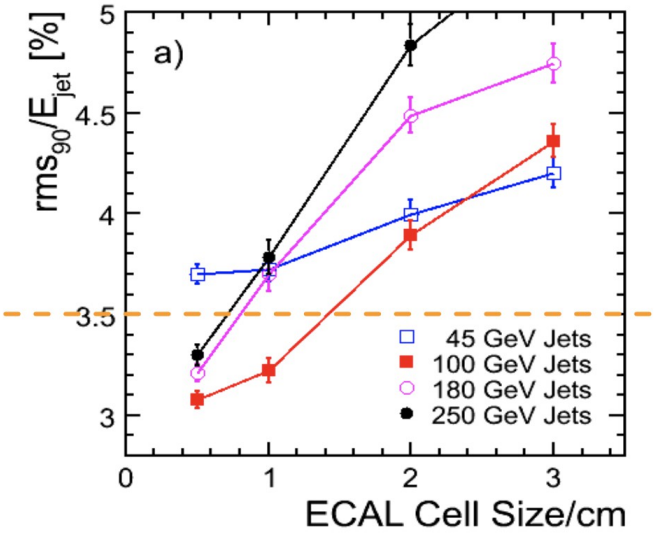
Introduction



ILD studies

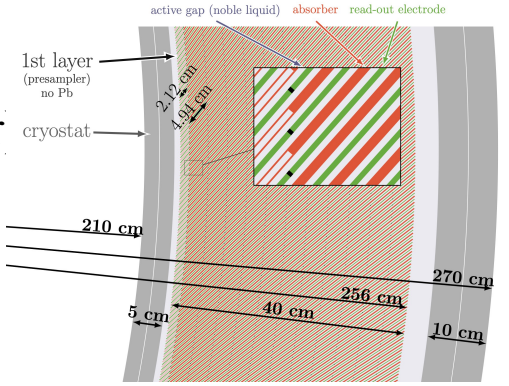


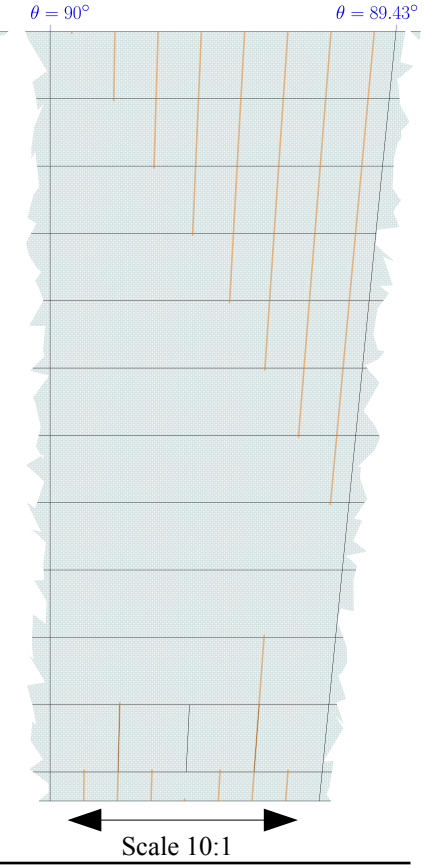
- Excellent relative jet energy resolution can be achieved with Particle Flow → build future detectors with this in mind
  - Need to avoid double counting and wrong merging
  - Calls for an imaging calorimeter
- High granularity! (and small Moliere radius)
  - Both transverse and longitudinal
  - Challenge for Noble Liquid calorimeters: signal extraction
    - High density feedthroughs (Maria's talk yesterday)
    - **Finely segmented readout electrodes (this talk)**

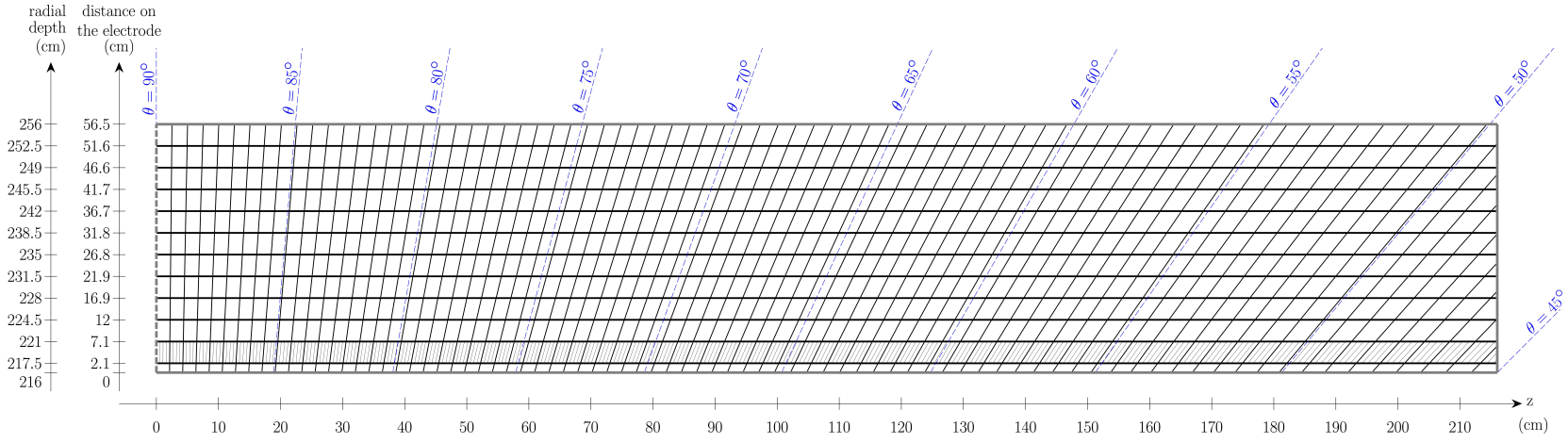


Finely Segmented Electrodes

- Targeted granularity
  - $\Delta\eta = 0.01$ (0.0025 strip layer), ATLAS: $\Delta\eta = 0.025$ (0.0031 strip layer
  - ~12 longitudinal layers, ATLAS: 3 (ignoring pre-sampler)
  - Phi granularity
    - Not directly linked to the readout electrode design (except maybe to its thickness)
    - Will depend on the cell merging scheme (to be optimized)
    - With "2 electrodes = 1 readout cell" → $\Delta\Phi = 8$ mrad
      - ATLAS $\Delta\Phi = 24$ mrad

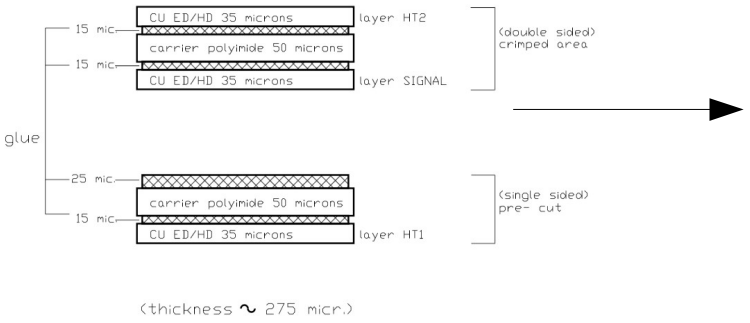


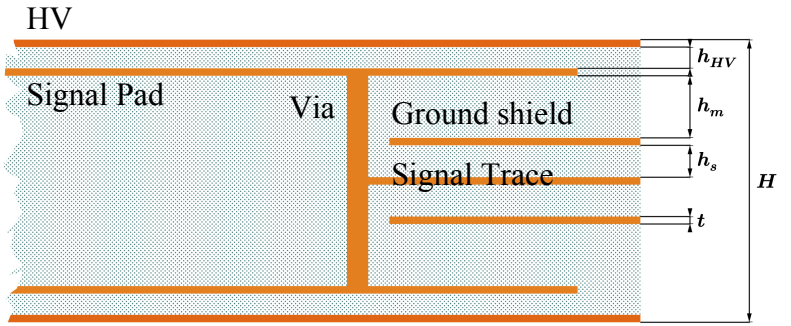


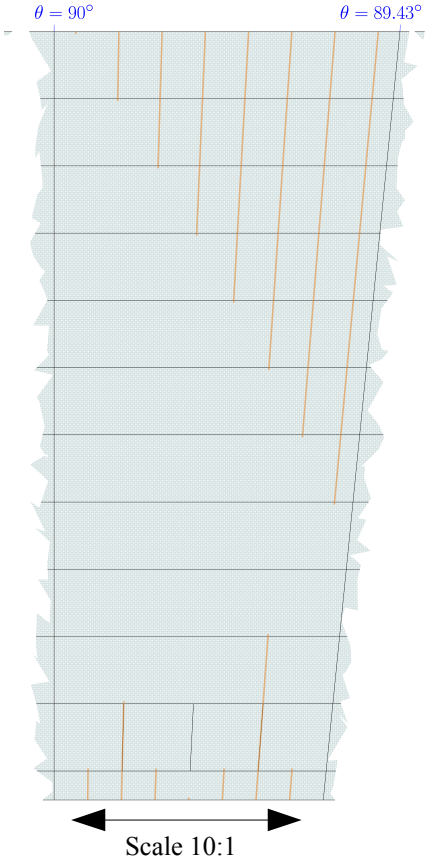


Finely Segmented Electrodes

- Most challenging point w.r.t. electrodes: **longitudinal segmentation**
  - Too many traces to route them in the anti-etch between towers
    - Solution: multi-layer PCB with signal traces running inside
  - Capacitive coupling between trace and other cells signal pad → X-talk
    - Solution: sandwich traces with ground shields → increase cell capacitance to ground → noise?
    - Need to **simulate and optimize the readout electrode PCB**!

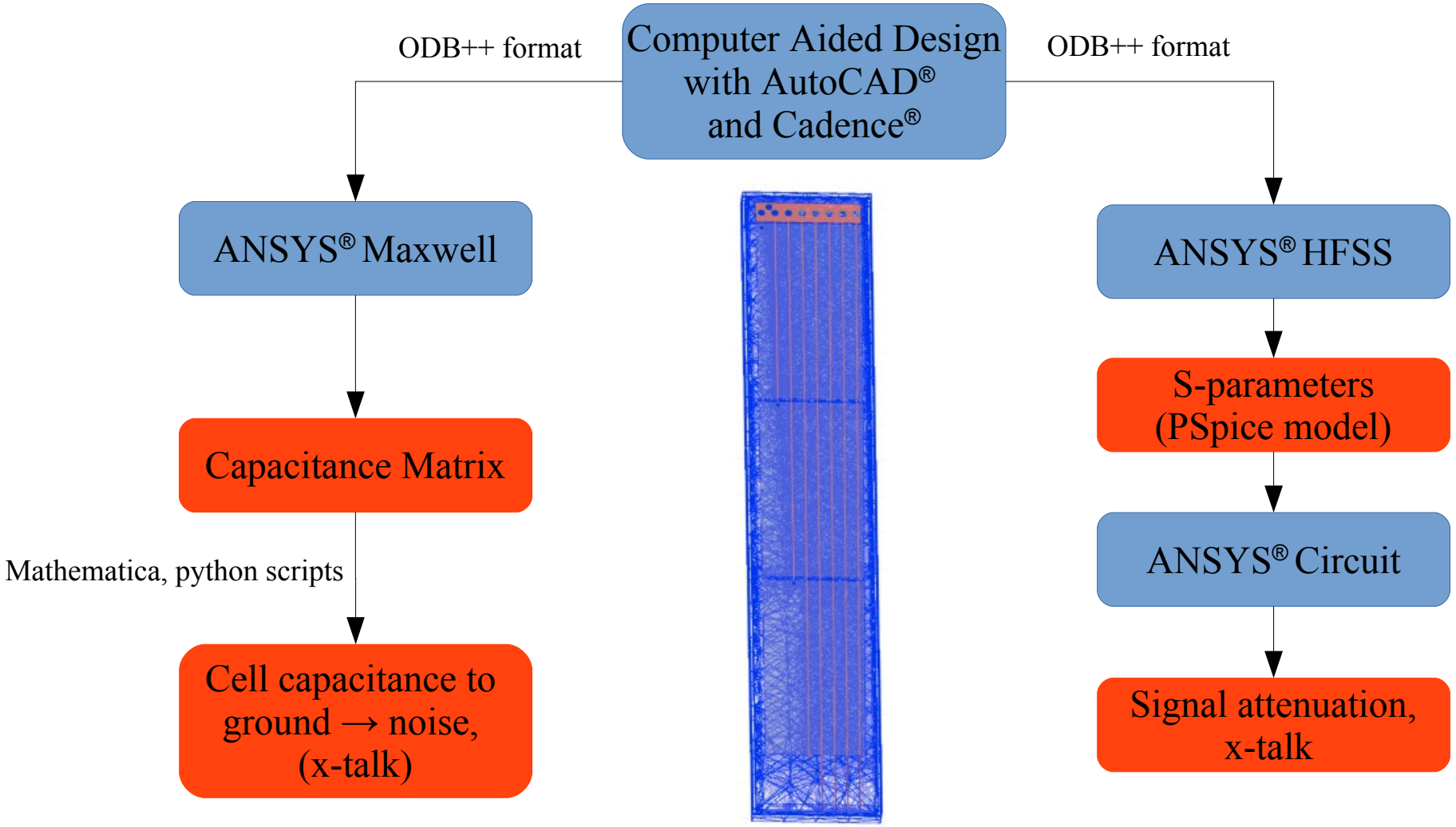






PCB simulation: how to?

- PCB simulation in a nutshell (workflow found by trial and errors, there is probably more straightforward ways)

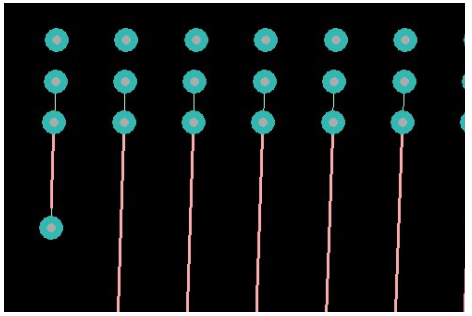


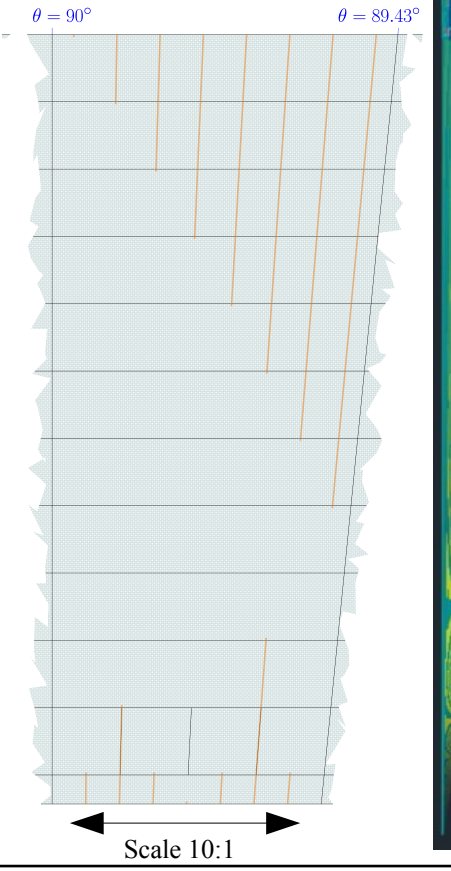
PCB CAD

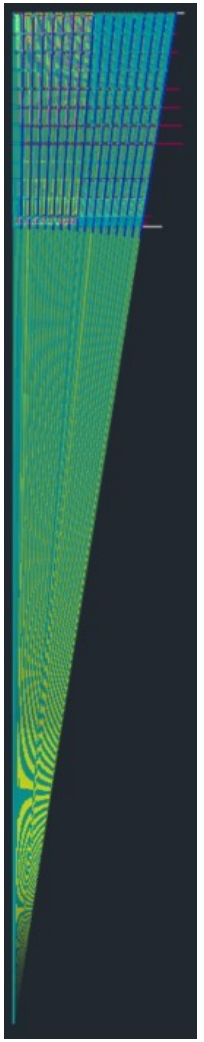
Computer Aided Design with AutoCAD® and Cadence®

- Implementation done with the CERN PCB Design office
  - The edges of the tower and the transmission lines point to the interaction point
  - Each tower can be obtained by **rotational symmetries** of the first one + application of a **cutting mask**
    - Structural layout done in AutoCAD, imported in Cadence to place the various components
  - One via per copper trace to distribute the GND and read the signal (will be replaced by connectors for the final design)
  - Signal extracted from front until layer 4, then from the back
    - Constant spacing between traces
    - To be optimized

Top edge of the PCB



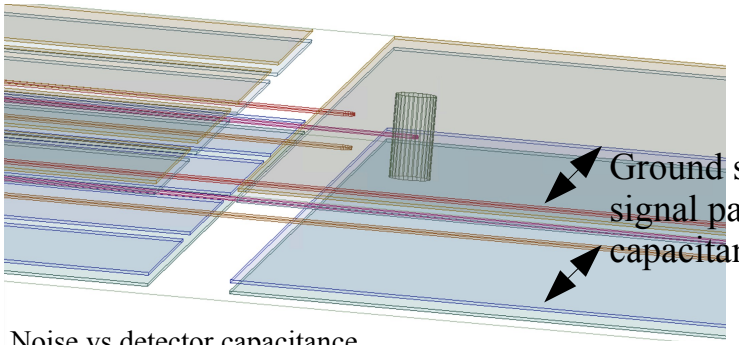


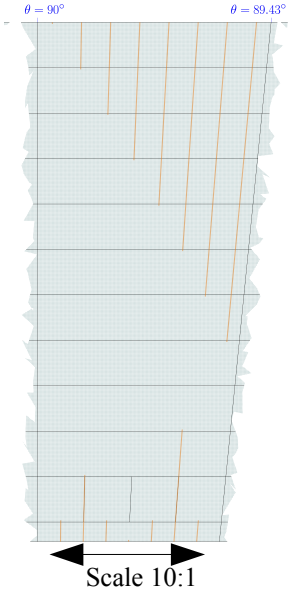


Capacitance Matrix: noise

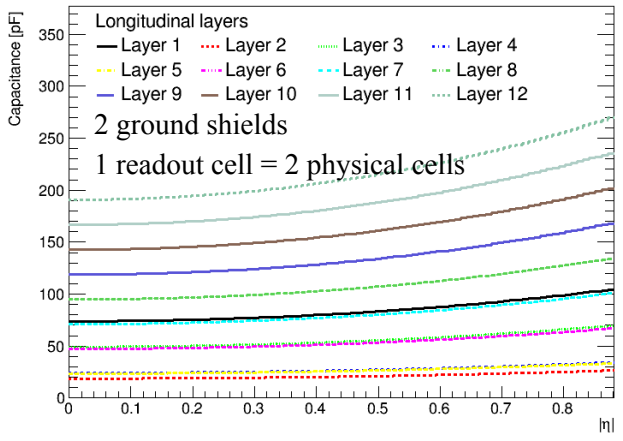
ANSYS® Maxwell

- CAD imported in ANSYS Maxwell to derive the capacitance matrix
- Total cell capacitance to ground (sources in parallel)
  - Ground shield to signal pad: derive capacitance per unit length in Maxwell, then scale with the cell length and number of shield
  - Signal pad to absorber capacitance from simple analytical formula
- Combine Martin's noise derivation and cell capacitance from Maxwell to get the noise per cell
  - Derive MIP S/N from full simulation

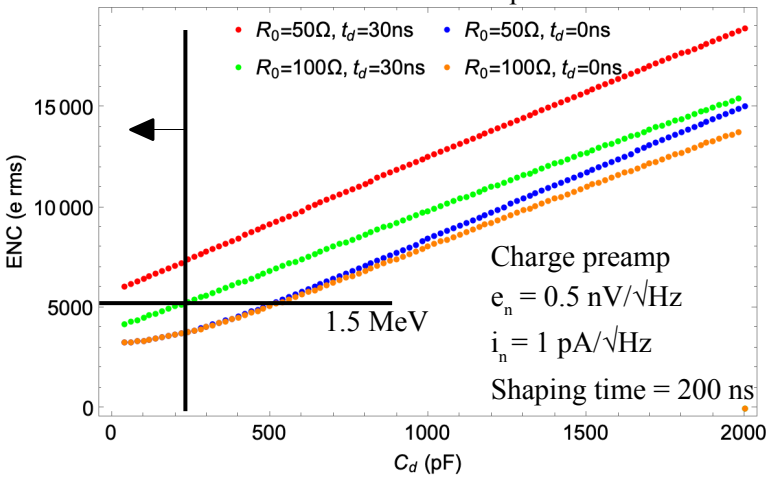




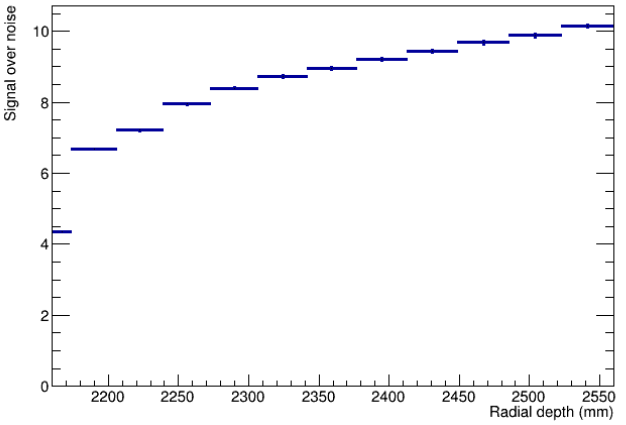
Total capacitance



Noise vs detector capacitance



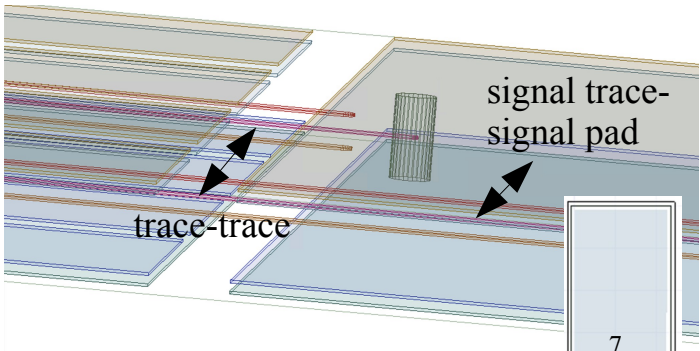
MIP <S/N> per layer

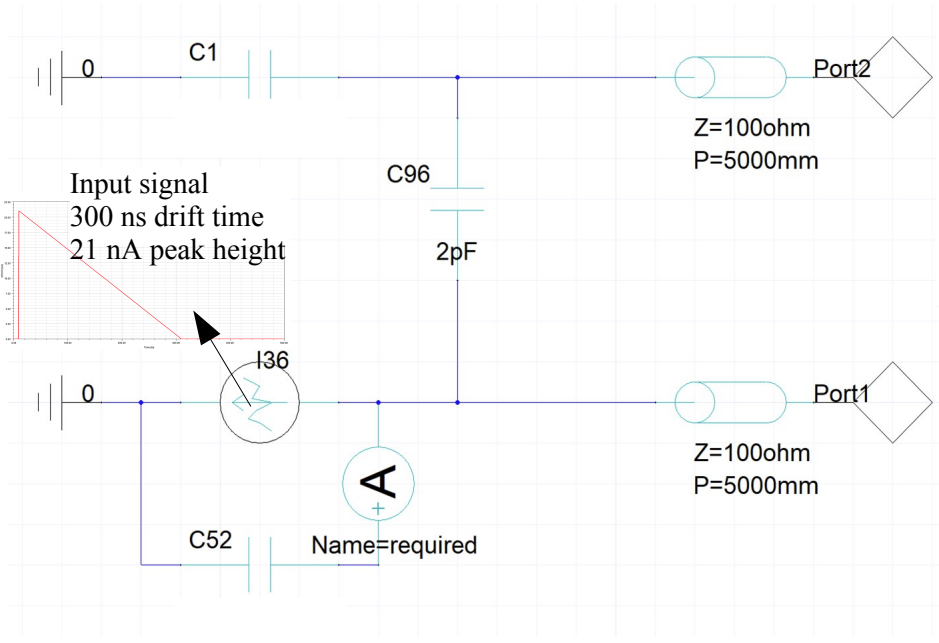


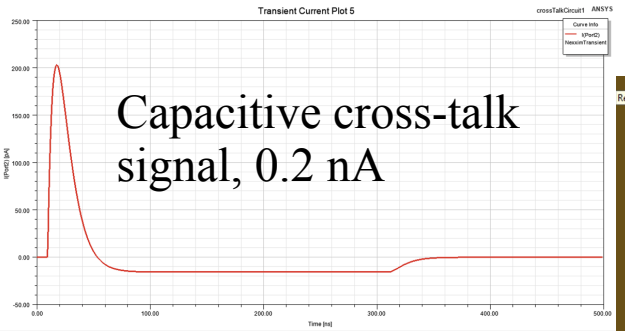
Capacitance Matrix: x-talk

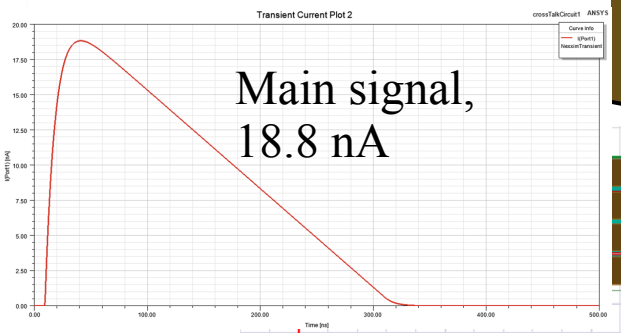
- X-talk capacitance
  - Signal trace to other cells signal pad: **0.6 pF** for cell 7 to 6 (x2)
  - Signal pad to other signal pads: **0.28 pF** for cell 6-7 top-top, **0.18** top-bot
  - Signal trace to adjacent signal trace: from 0.03 pF (cell 7 to 4/5) to **0.4 pF** (cell 9 to 10)
  - Other contributions neglected (via, …)
- Implement a simplified circuit description of the x-talk
  - Typical peak-to-peak x-talk of ~1% for neighboring cells
  - Similar results from analytical circuit

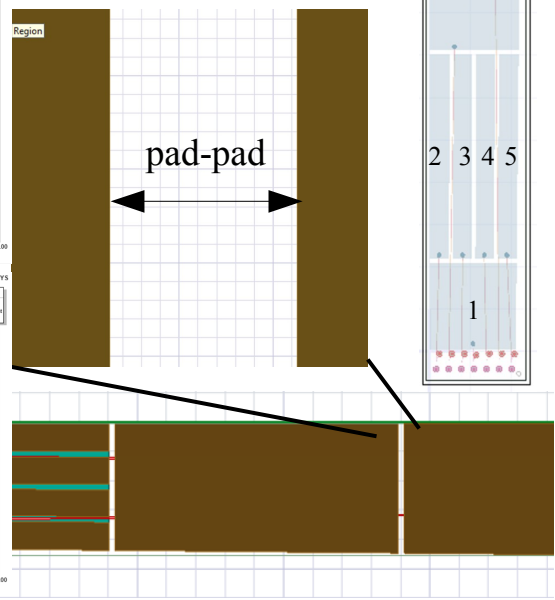
ANSYS® Maxwell





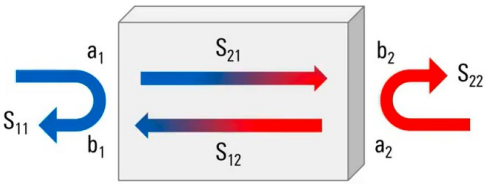




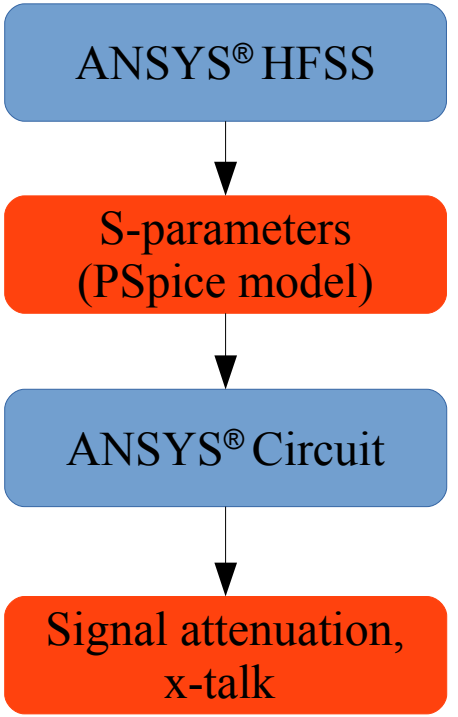


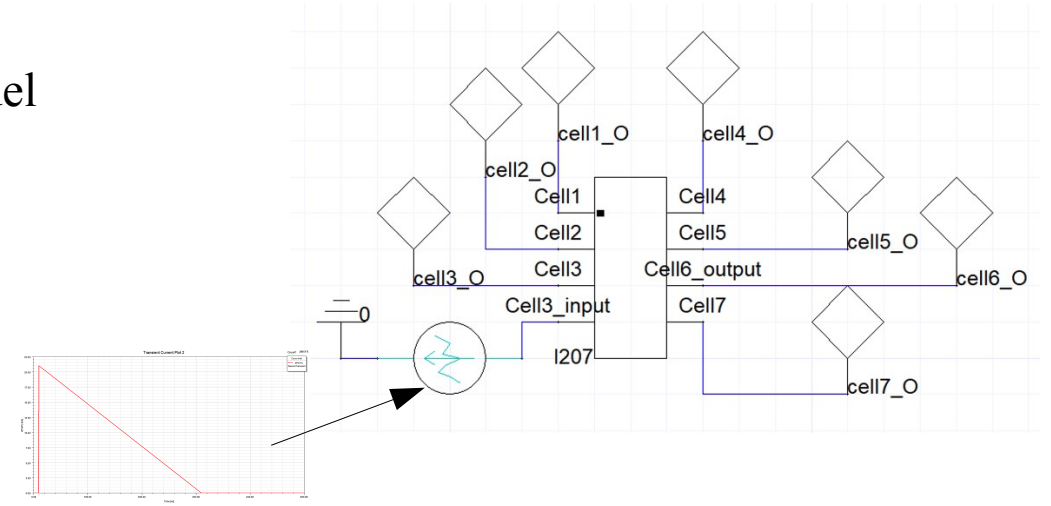
X-talk from full FEM

- X-talk from simplified circuit
  - Considers only capacitive x-talk
  - Lumps all sources into one single capacitance
  - Is cumbersome (need to get relative capacitance for each cell combination)
- Preferred to move to a **full FEM x-talk derivation**
  - Import the CAD into ANSYS HFSS 3D layout
    - Tried ANSYS SIWave → not general enough (only 'co-planar' x-talk)
  - Define ports and solve the S-parameters
  - Export the equivalent circuit as a PSpice model
  - Import in Ansys Circuit for the signal studies



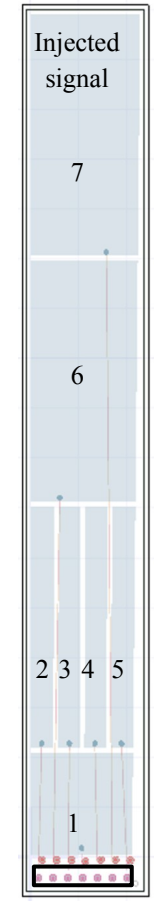
$S_{11} = b_1/a_1$
$S_{21} = b_2/a_1$
$S_{12} = b_1/a_2$
$S_{22} = b_2/a_2$

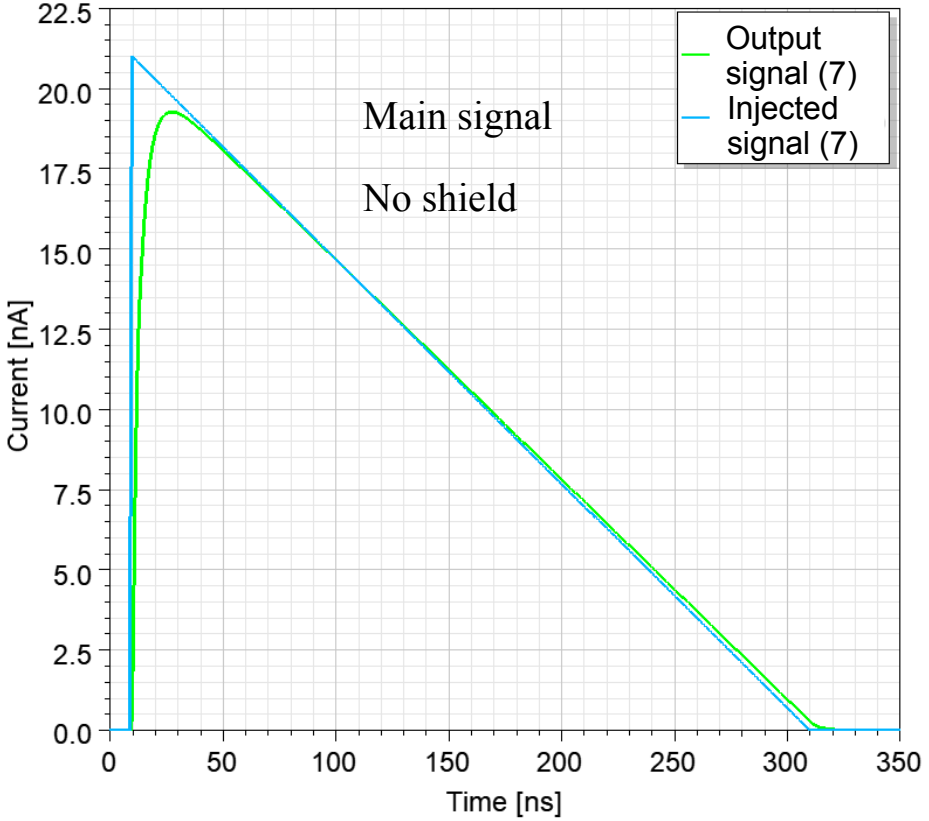


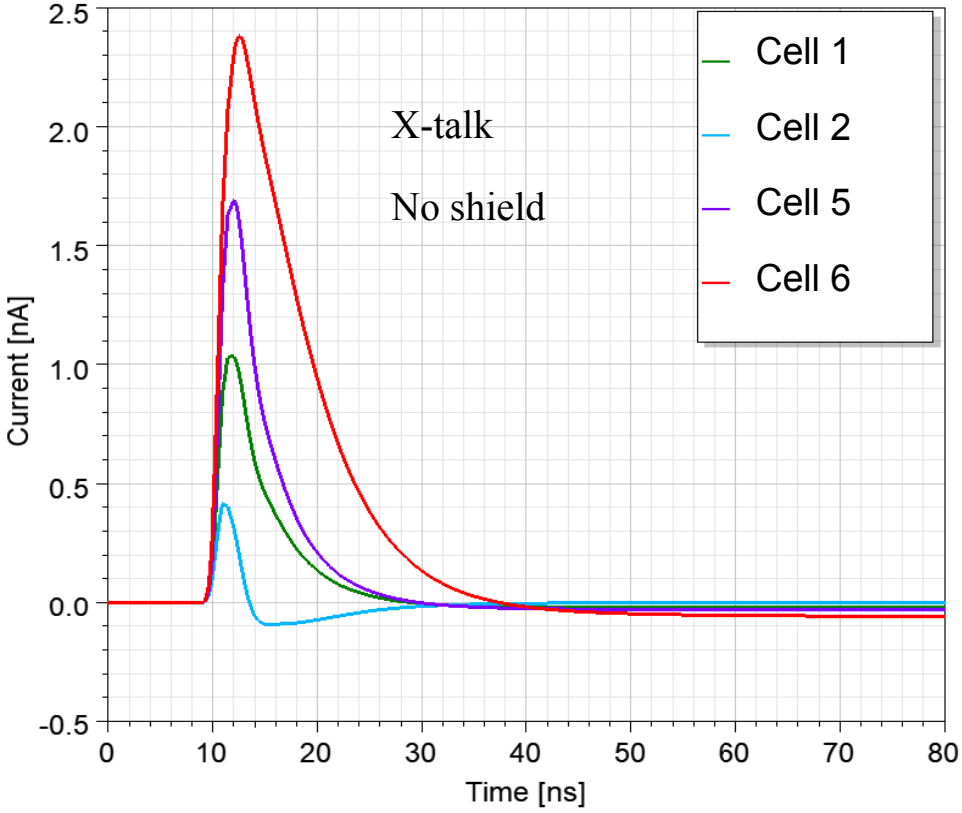


X-talk from full FEM

- Can unfortunately not solve the whole tower at once due to computing resources
  - Implement only chunks of the PCB (inner radius side of the detector shown here, **no GND shield**)
  - Transmitted current has a peak value of ~93% of the injected one
  - Cell 7 to Cell 6 (direct neighbor) peak-to-peak x-talk: 12% without shield
    - Other cells also show x-talk: Cell 5, 4 and 1 due to TL/pad coupling, cell 2 and 3 probably from indirect coupling

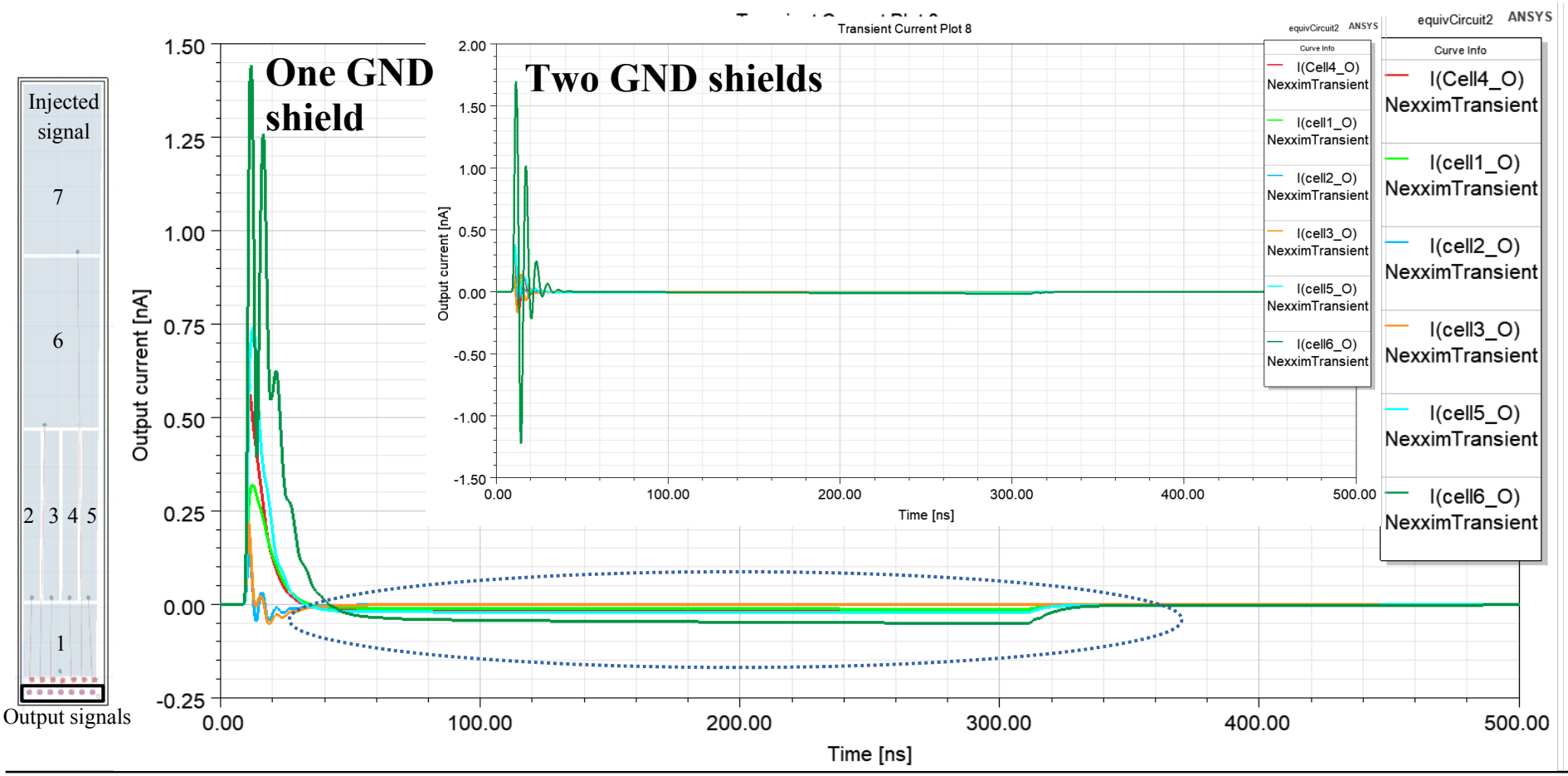






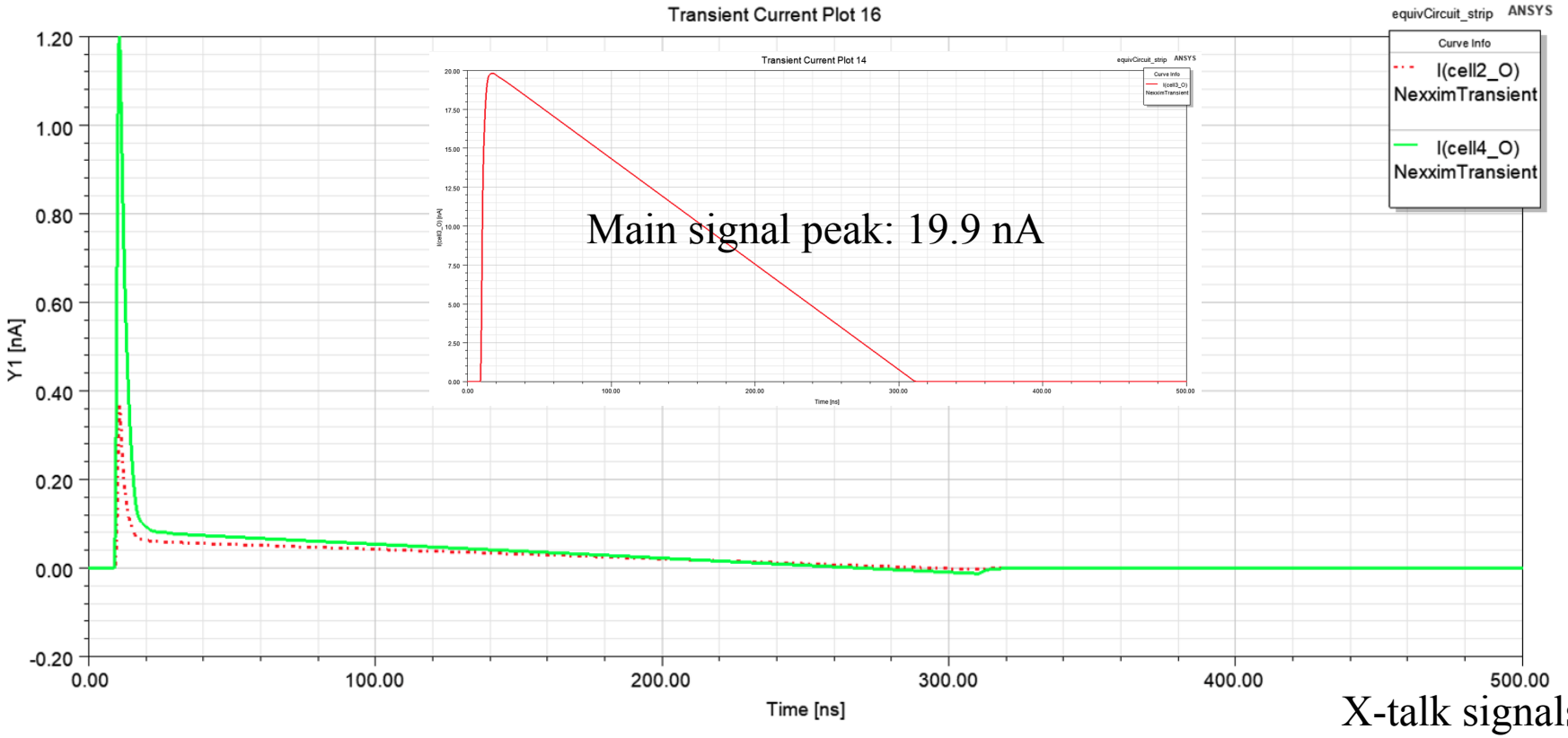
X-talk from full FEM

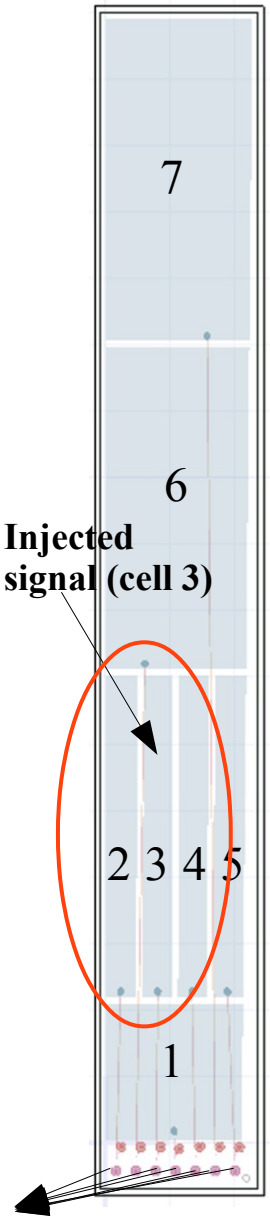
- When adding ground shields, x-talk signals lower but show reflection patterns
  - Difficult to define peak-to-peak ratios → use the value of the undershoot and compare with the case without shield
  - X-talk peak-to-peak values cell 7 to 6 (direct neighbor): 12% for 0 shields, 6% for 1 shield, **2% for 2 shields (chosen baseline)**
    - Next step is to include the front-end in the simulated chain to see integrated x-talk current values (lower)



X-talk in strip layer

- Studying now the X-talk from the strip layer (injecting on cell 3, 2 shields)
  - Different x-talk current shape, use the peak-to-peak values
  - **Cell 3 → Cell 4: 6 % x-talk, Cell 3 → Cell 2: 1.8 % x-talk**
    - Cell 2 is partially protected by the shields from cell 6 TL unlike cell 4
    - Having GND shields, even on a different layer, mitigates the pad-pad x-talk!

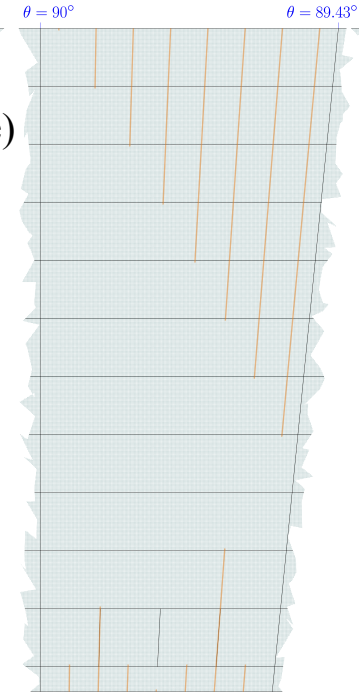


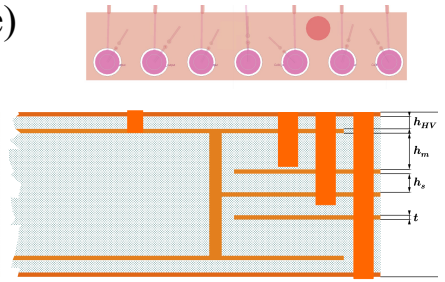


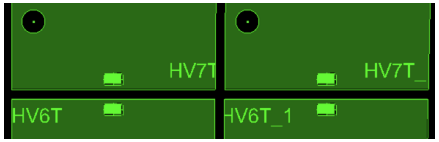
PCB prototype

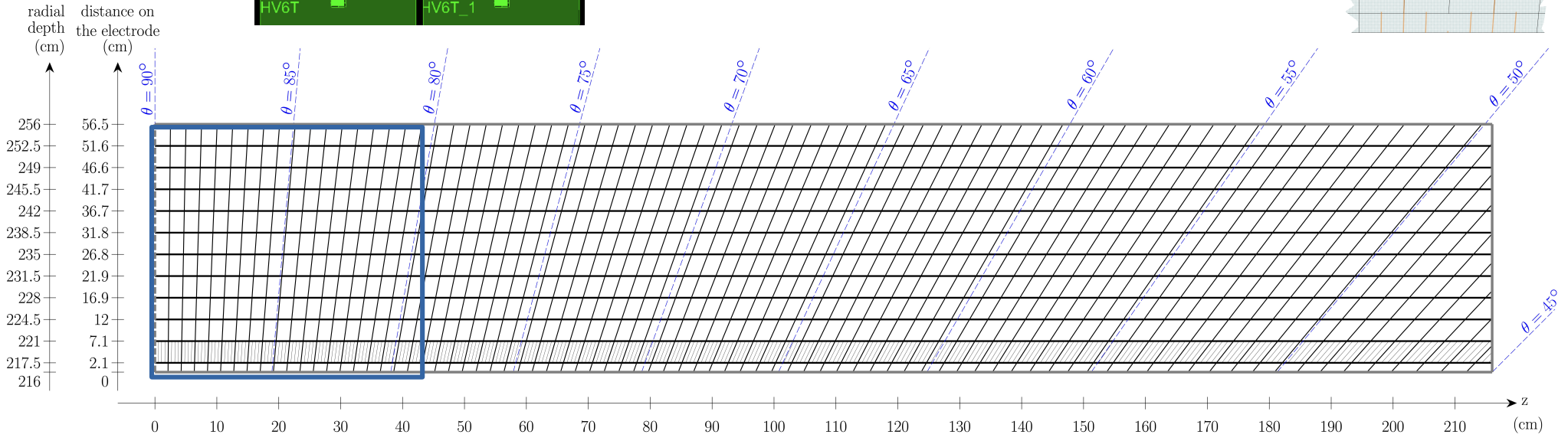
First PCB prototype

- Drawing of the prototype finalized with the CERN PCB Design Office
  - Will be 1:1 scale in the radial direction and feature 16 'theta towers' with different layouts
    - Small production → cost driven by labour hours (not the material/components nor PCB size)
    - Remains within standards (limiting factor = validation equipment)
  - Definition of the baseline 'theta tower'
    - Each shield has one via to distribute the GND (no plate anymore)
    - Via allowing to inject signal directly on the signal pad
    - Trace surrounded by two shields (twice wider as the trace)
      - Also for he first and last cells
    - Soldering pads added to the HV cells → study resistive x-talk



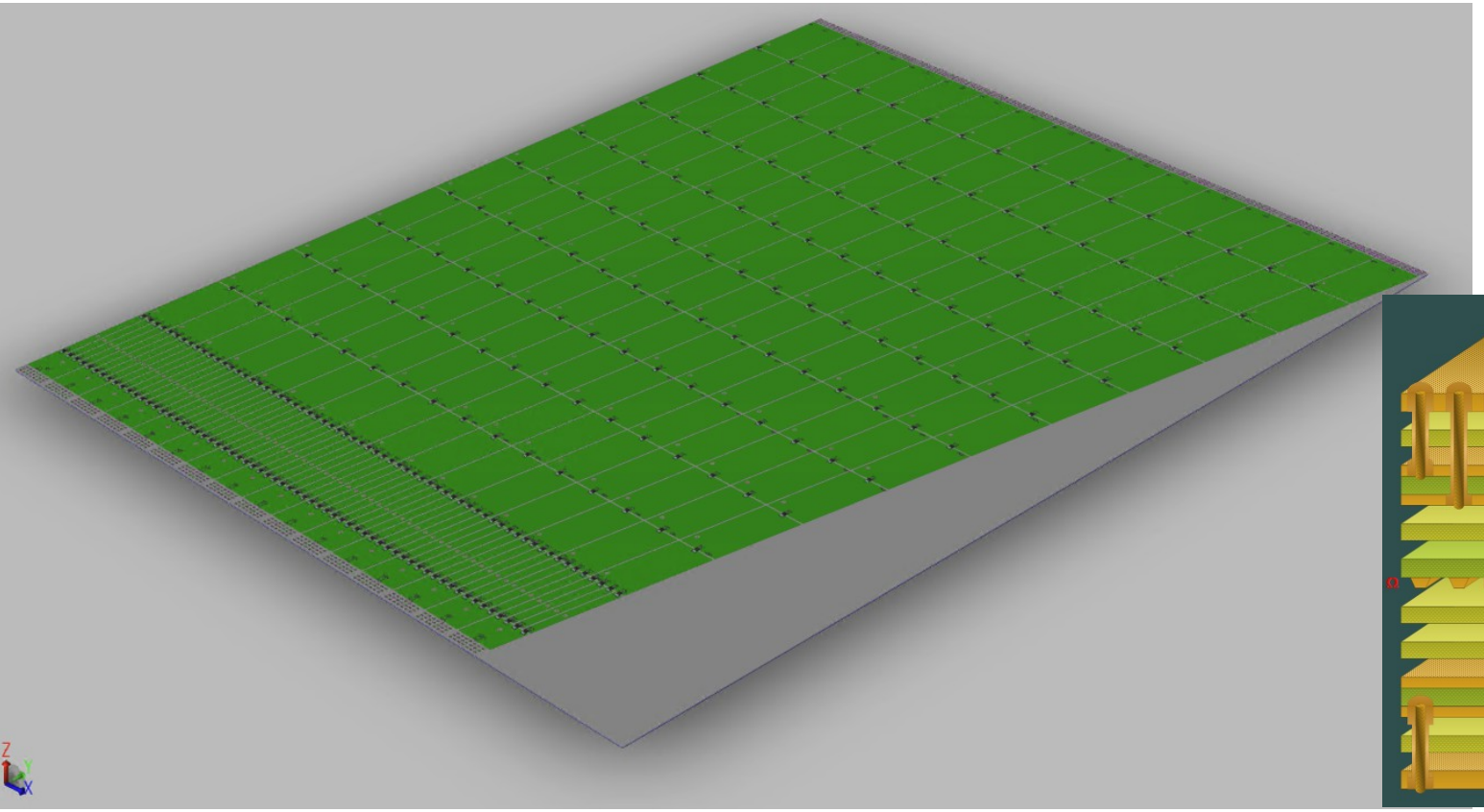


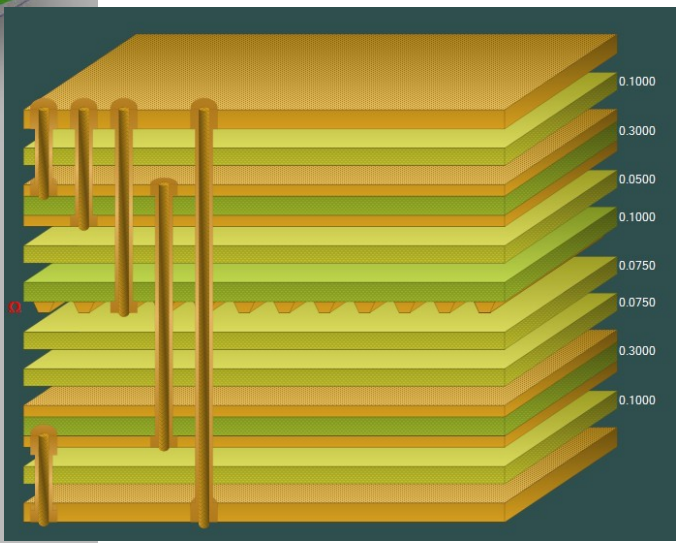




PCB Drawing status

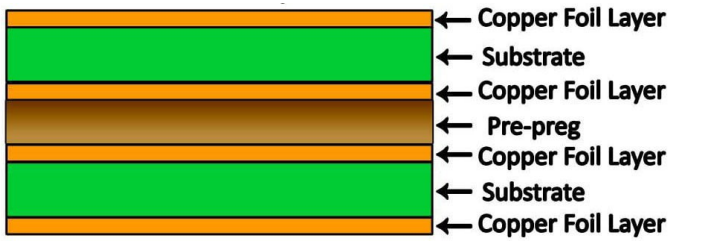
- Various tower layouts (full list in back-up), keeping the same copper layer position
  - Number and width of the shields, signal extraction schemes, GND distribution
  - Validate simulation with several benchmarks

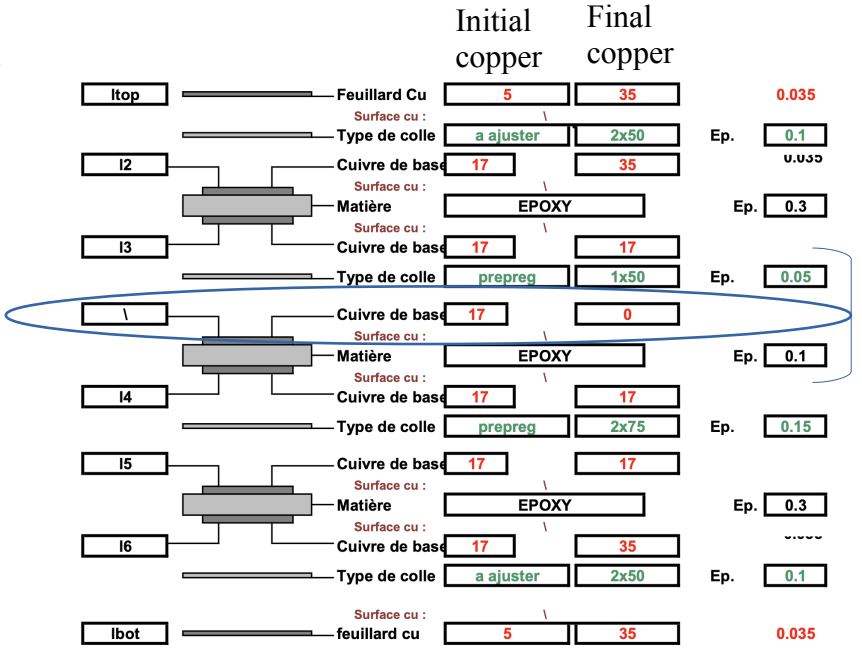


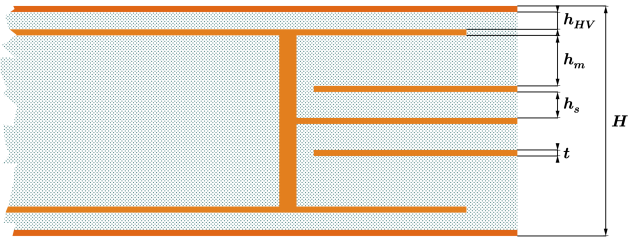


7-layer PCB

- Multi-layer PCB's are produced using double-sided copper pre-preg core, finished with copper foils
- **Odd number of layer** PCB's
  - Can be achieved by chemically removing one of the copper plane from the pre-preg core
  - Symmetrical PCB can be produced by playing with the gluing thickness between two pre-preg cores
  - Adds more manufacturing step
    - Need to understand if it is ok for mass production
- Shortage in 35 µm copper pre-preg cores (the standard)
  - Weeks delay for delivery
  - Produce 35 µm thick planes from 17 µm by metalization (except for the shield planes)
- Most dimensions slightly modified to have standard components (e.g. h_m 285 µm → 300 µm, h_s 170 µm → 150 µm + adapt trace width to keep 50 Ohms)
- Total PCB thickness **around** 1.2 mm
  - Copper from layer with trace penetrates more or less in the FR4 at the pressing step
- ETA by the end of April





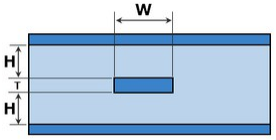


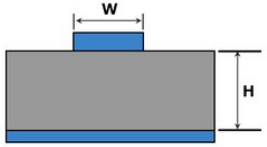
Summary

- A design of the readout electrode for a straight inclined plate has been proposed
- Detector cell capacitance to ground derived from a FEM approach
  - Noise estimated from analytical readout chain implementation
  - MIP S/N > 5 seems achievable per cell (charge pre-amp, long shaping time) even in the warm electronics scenario
- X-talk derived from a FEM approach
  - Below 2(6) % for regular(strip) cells with two ground shields
- Moving to a first prototype to confront simulation with real measurements!

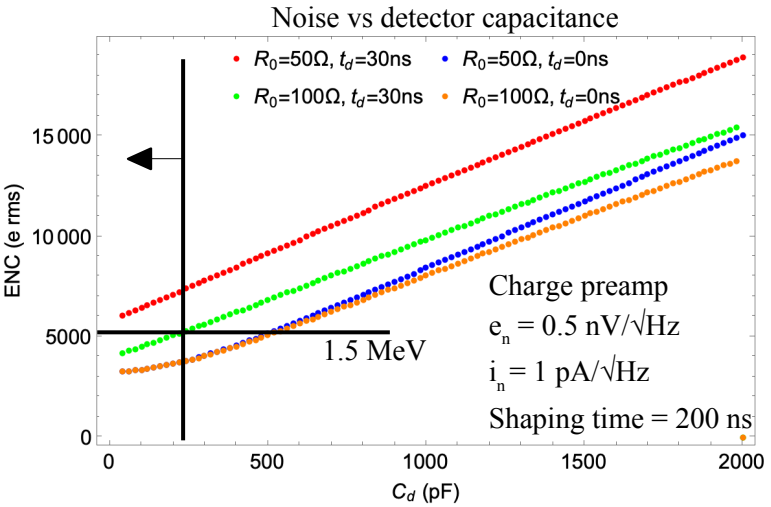
Discussion: Impedance mismatch

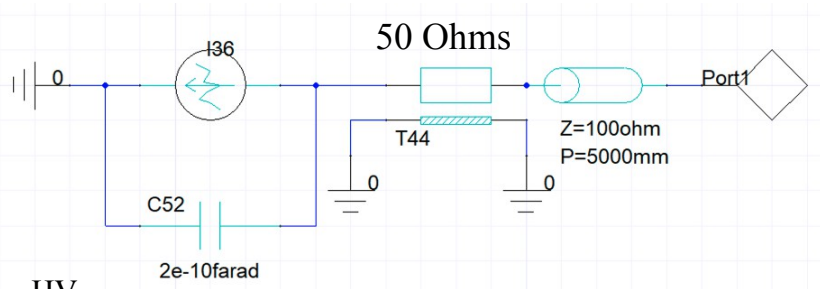
- 50 or 100 Ohms PCB TL? (warm electronics)
  - In the warn electronics scenario, having the (long) coax cables at 100 Ohms seems to mitigate their impact on the noise
  - 100 Ohms TL inside the PCB

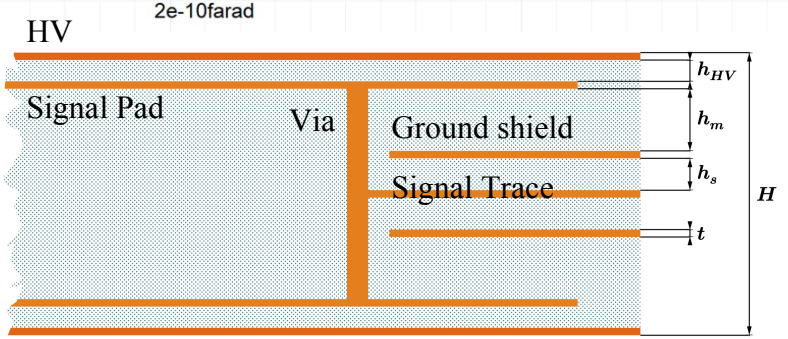




  - Can hardly be reached in the stripline scenario without enlarging its thickness (sampling fraction loss)
  - Possible to get to 100 Ohms in the microstrip scenario to the price of a higher x-talk and higher cell capacitance to ground
  - On the other hand, having a short 50 Ohms TL followed by long 100 Ohms coaxial cable leads only to a ~4% signal peak loss
  - Decided to keep 50 Ohms TL for now

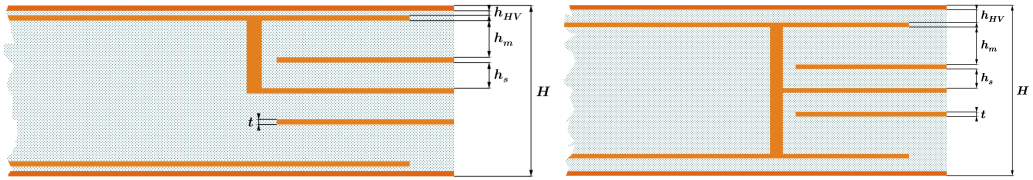


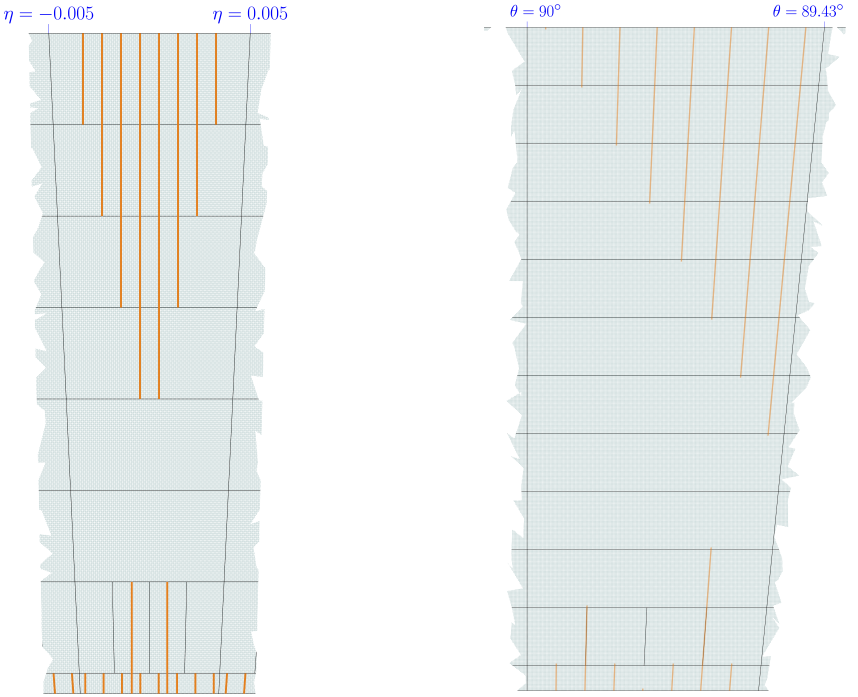




Discussion: TL

- **One TL per pad** instead one TL for two pads (as proposed for FCC-hh)?
  - Number of ground shield?
    - Capacitance to ground does not have such a big impact on noise
  - Trace density
    - Space for connectors
    - Strip-strip x-talk
  - Signal over noise?
  - Provided that we have the two signal traces on different planes we could have an even number of layer in the PCB
    - Easier and cheaper to manufacture

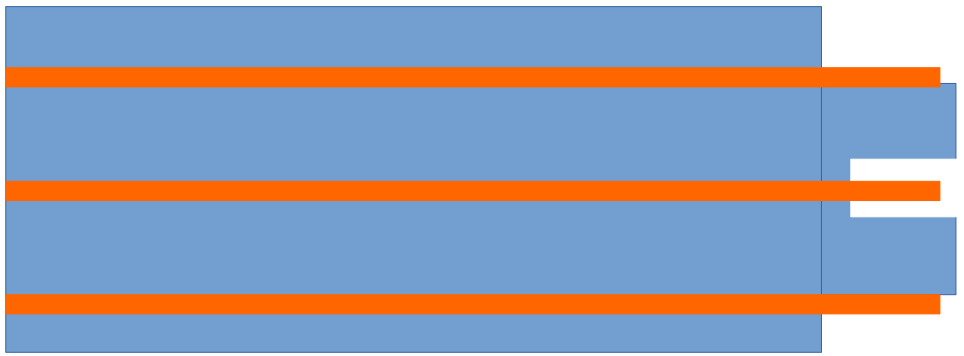


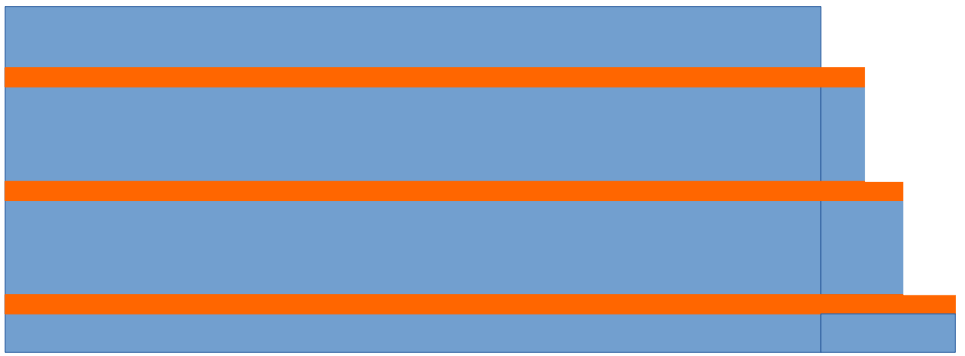


Discussion: Connectors

- Pitch
  - Inner radius cell width ~2 cm, 7 traces → pitch of 2.85 mm maximum
  - Outer radius cell width: 2.65 cm, 8 traces → pitch of 3.3 mm maximum
- Shell thickness at inner radius (inner LAr gap x 2 + 1 absorber + 1 PCB = 5.68 mm)
  - Horizontal mating seems preferable, even probably 'enclosing' the board
- Bring signal (35 μm) and two GND (35 μm) with 150 μm distance between them
  - Did not find any standard conductor so far...
- How to bring the high voltage?

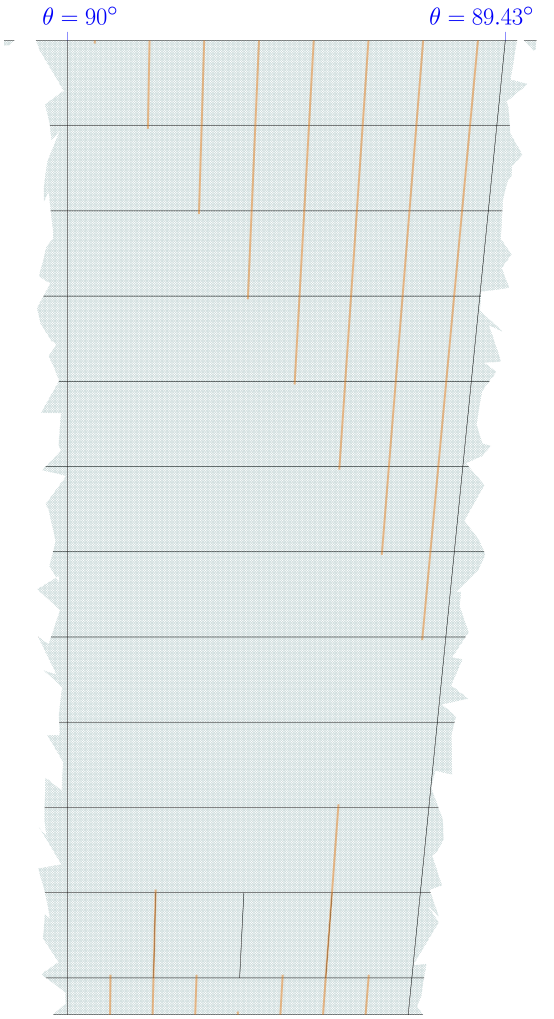
Fig. 1 Vertical mating connector (left) and horizontal mating connector (right)





Discussion: miscellaneous

- Cell size evolving with radius?
  - Small differences needed to have cells aligned in phi
  - Larger cells towards high radius? (need PFlow to optimize)
- Signal extraction scheme: which cell from front/back?
- Good figures of merit for the optimization of the ECAL longitudinal segmentation?
  - Evolving sampling fraction
  - Cell phi 'imprint'
  - What else?
- High voltage layer segmentation/resistive link
  - Two high voltage supply?
  - Resistive layer → thicker PCB → sampling fraction loss?
- …

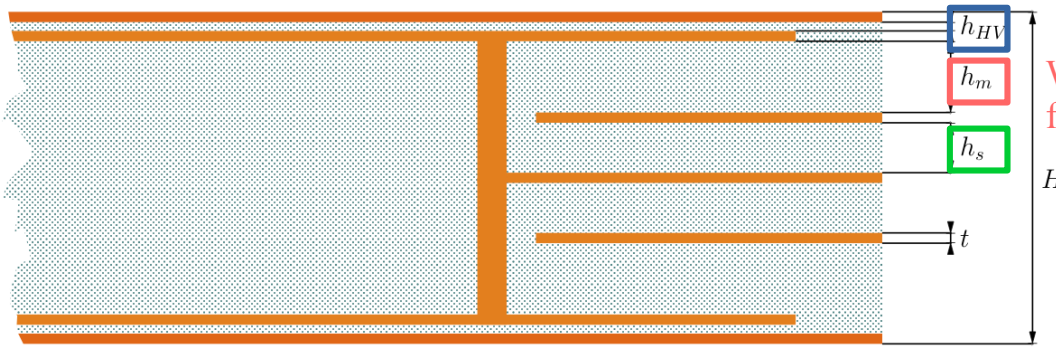


Additional material

PCB Dimensions

- Simulations
  - Trace width: 127 µm
  - Trace thickness: 35 µm
  - Shield width: 250 µm
- Prototype (standards)
  - h_{HV} = 100 µm
  - h_m = 300 µm
  - h_s = 150 µm
  - Adapt trace width to keep 50 Ohms
    - 90 µm

	Name	Type	Negative	Material	Dielectric Fill	Thickness	Etch	Rough	Solver	Lower	Upper	Transparency
	smt	dielectric		FR4_epoxy		0um				1.285mm	1.285mm	60
	top	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.25mm	1.285mm	60
	dielectric_0	dielectric		FR4_epoxy		100um				1.15mm	1.25mm	60
	l2	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.115mm	1.15mm	60
	dielectric_1	dielectric		FR4_epoxy		250um				0.865mm	1.115mm	60
	l3	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.83mm	0.865mm	60
	dielectric_2	dielectric		FR4_epoxy		170um				0.66mm	0.83mm	60
	l4	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.625mm	0.66mm	60
	dielectric_3	dielectric		FR4_epoxy		170um				0.455mm	0.625mm	60
	l5	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.42mm	0.455mm	60
	dielectric_4	dielectric		FR4_epoxy		250um → 207.5 um				0.17mm	0.42mm	60
	l6	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.135mm	0.17mm	60
	dielectric_5	dielectric		FR4_epoxy		100um				0.035mm	0.135mm	60
	bottom	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0mm	0.035mm	60
	smb	dielectric		FR4_epoxy		0um				0mm	0mm	60



Was 285 in the Calo for FCC-hh paper

Noise for Charge Preamp & CR²-RC²

- **Series noise:** Case of charge preamp and CR²-RC² shaper
  - ideal transmission line of length *L* with $t_d = L/v$ the line delay
    - no attenuation, no skin effect, but these effects are small (negligible) at cryogenic temperatures
  - charge preamplifier, CR²-RC² shaper (different to ATLAS LAr!),
  - see NIM A330 (1993) 228-242

$$V_n^2 = \int_0^\infty \frac{e_n^2}{|R_0 + Z|^2} \frac{1}{\omega^2 C_f^2} |H(i\omega)|^2 \frac{\mathrm{d}\omega}{2\pi}$$

- **Similar procedure for parallel noise** (not shown here)

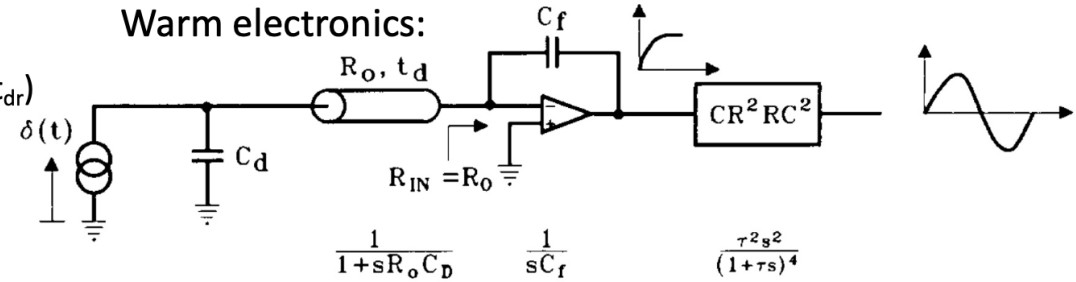
$$V_n^2 = \int_0^\infty \frac{e_n^2}{|R_0 + Z|^2} \frac{1}{\omega^2 C_f^2} |H(i\omega)|^2 \frac{\mathrm{d}\omega}{2\pi} \quad \text{with} \quad Z = \frac{iR_0 \tan(\omega t_d) - \frac{i}{\omega C_d}}{\frac{\tan(\omega t_d)}{R_0 \omega C_d} + 1}$$

$$V_n^2 = \frac{\tau^4 C_d^2 e_n^2}{2\pi \tau_p^2 C_F^2} \int_0^\infty \frac{\omega^2 \left(\tau_p \omega \cos(\omega t_d) + \sin(\omega t_d)\right)^2}{\left(\tau^2 \omega^2 + 1\right)^4 \left(\tau_p^2 \omega^2 + 1\right)} \mathrm{d}\omega \qquad \tau_p = R_0 C_d$$

- This series noise needs to be normalised to signal response V(x) of unit charge Q_0:
  - either Dirac delta-function $Q_0\delta(t)$,
  - or triangular signal (t_{dr} is the e⁻-drift time): $2Q_0/t_{dr}(1 - t/t_{dr})$

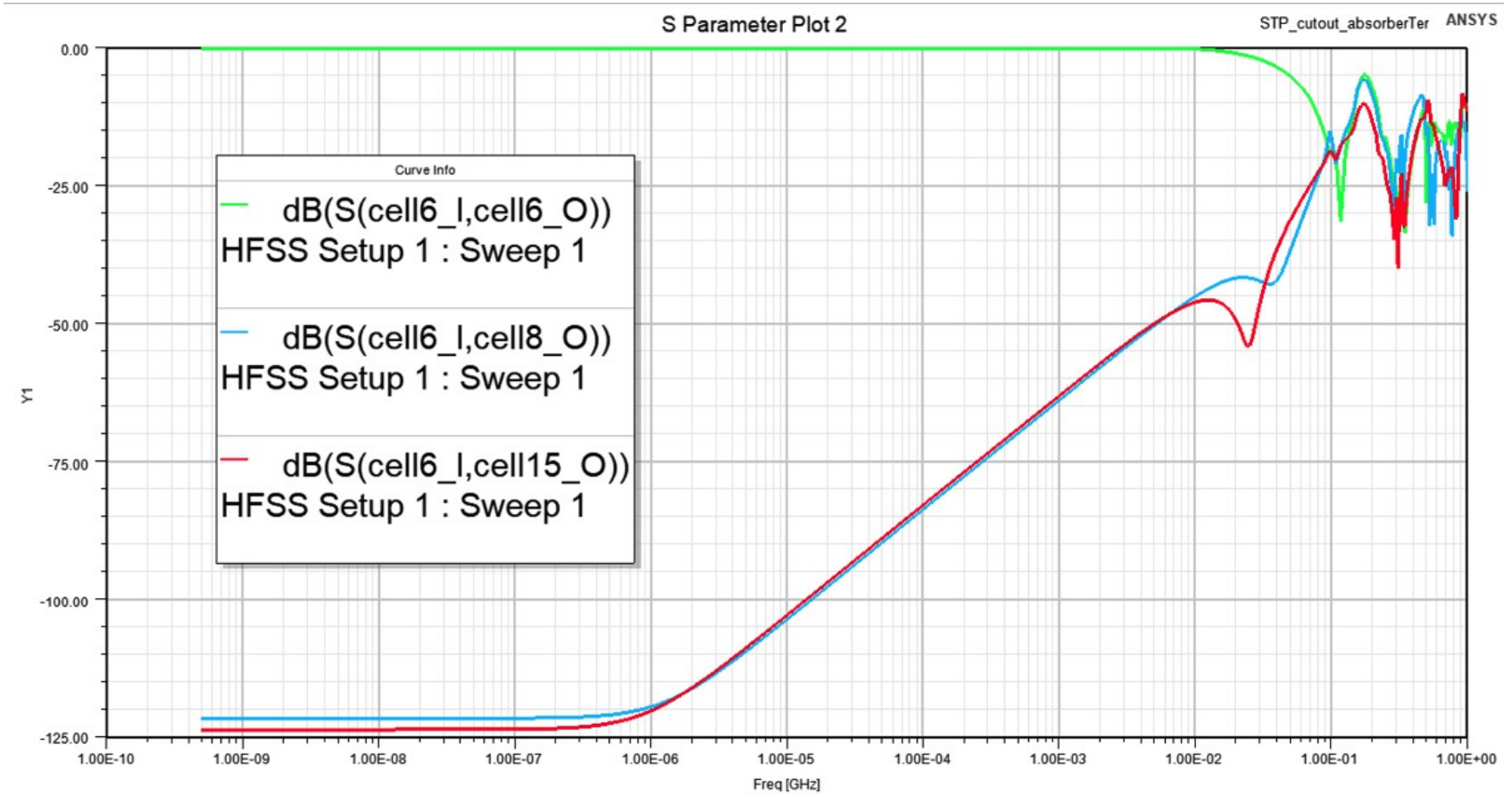
$$\mathrm{ENC} = Q_0 \frac{V_n}{\max|_x(V(x))}$$

Warm electronics:

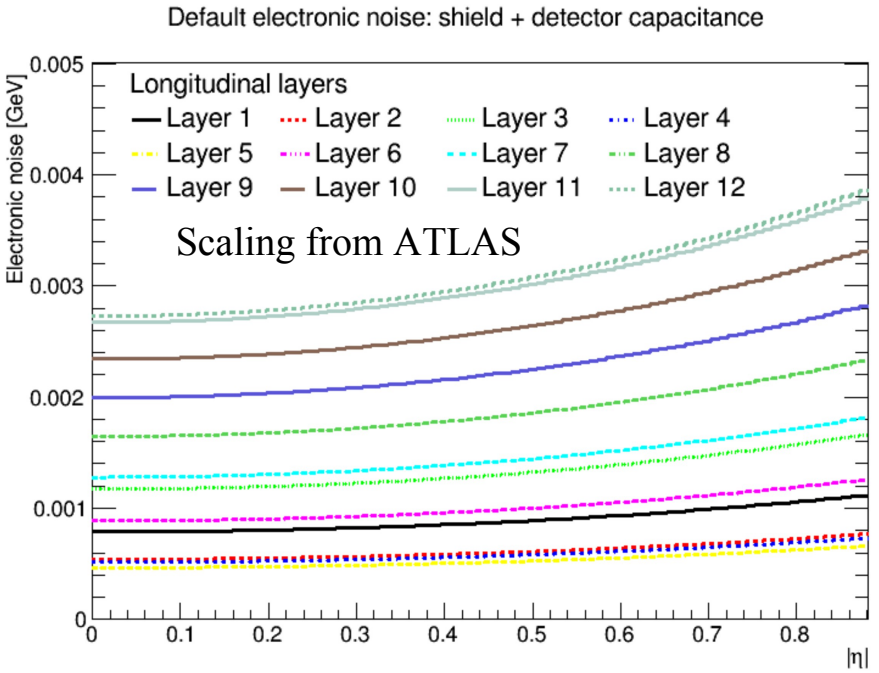


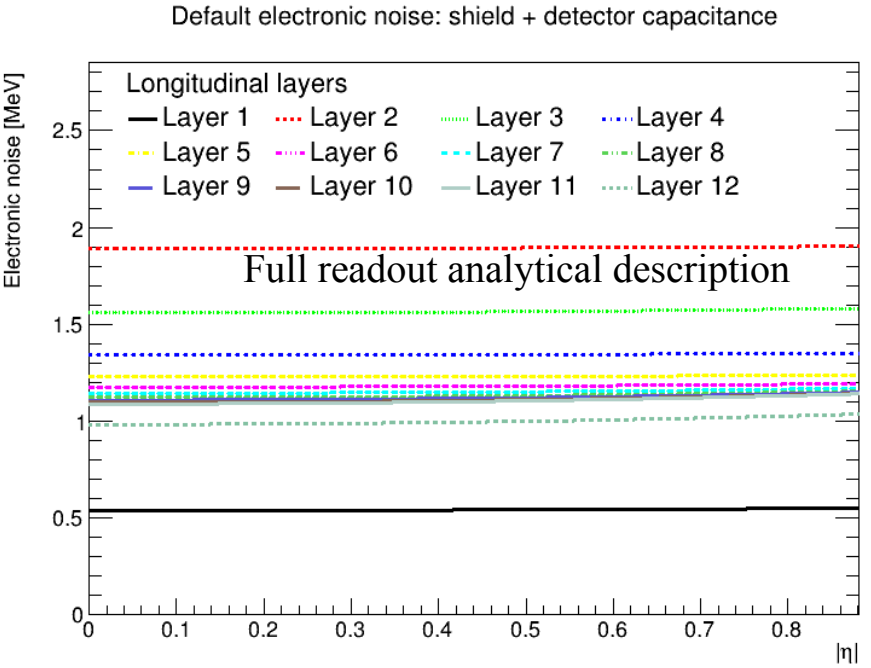
S-parameters

- S-parameters from Ansys HFSS



Noise values in MeV

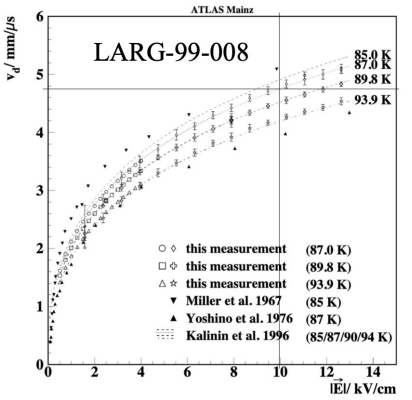




Noise normalization

- Noise current normalization: induced **peak current for 1 MeV** energy deposit in a cell (cell = active + passive material)
  - $W_{LAr} = 23.6$ eV, $r_{recomb} = 4\%$, $q_e = 1.602 \times 10^{-19}$ C, $v_{LAr} = 4.75$ mm/μs

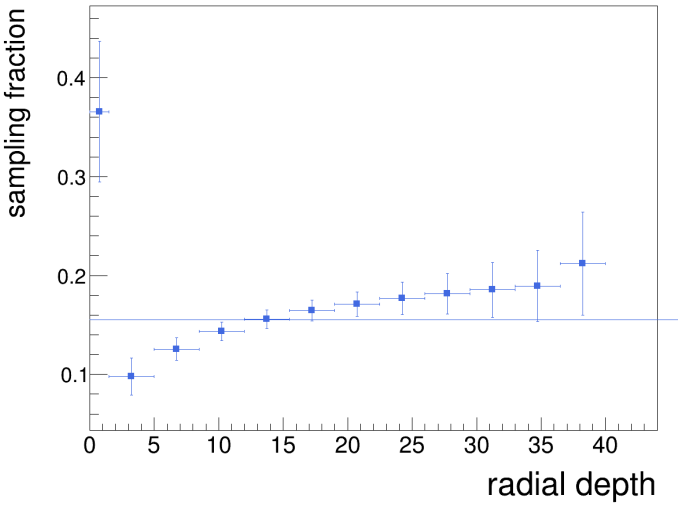
Neglect variation due to the LAr gap widening impacting the electric field: with two HV supply (outer and inner radius) the electric field will vary by up to 40%, leading to a v_{LAr} variation of up to 20%

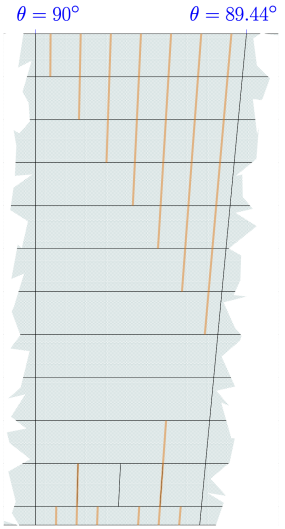


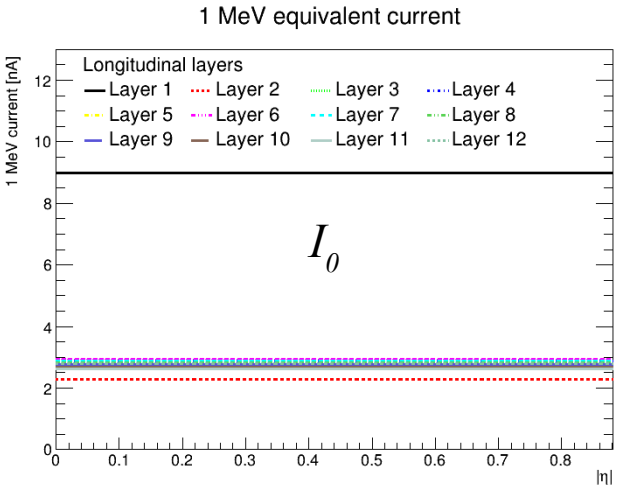
$$I_0 = \frac{E_{dep} f_{sampl}(1 - r_{recomb})}{W_{LAr}} \cdot \frac{q_e v_{LAr}}{d_{LAr}}$$

Shokley-Ramo theorem

Taken at the middle of the layer. Properly take into account the variation of the LAr gap size for each longitudinal layer: 1.26 – 2.34 mm





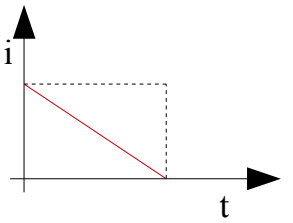


Noise implementation

- Noise charge normalization
  - First normalize the noise voltage rms to the shaper peak voltage when injecting a unit charge
    - Shaper response to current 2 * Q/t_{drift} * (1 - t/t_{drift})
  - Transposed then to an energy deposit
    - Integral of 1 MeV induced current over shaping time → 1 MeV equivalent charge
    - Assuming $t_{shaping} \sim t_{drift} \rightarrow$ $I_0 = \frac{E_{dep} f_{sampl}(1 - r_{recomb})}{W_{LAr}} \cdot \frac{q_e v_{LAr}}{d_{LAr}}$
    - Noise [MeV] = ENC / Q(1 MeV)
  - Neglecting: t_{drift} is different per cell and enters the ENC computation

Noise value from analytical derivation

$$\mathrm{ENC} = Q_0 \frac{V_n}{\max|_x(V(x))}$$



$Q = ½ * i * t_{drift}$

$v_{LAr}/d_{LAr} = 1/t_{drift}$

Shokley-Ramo theorem

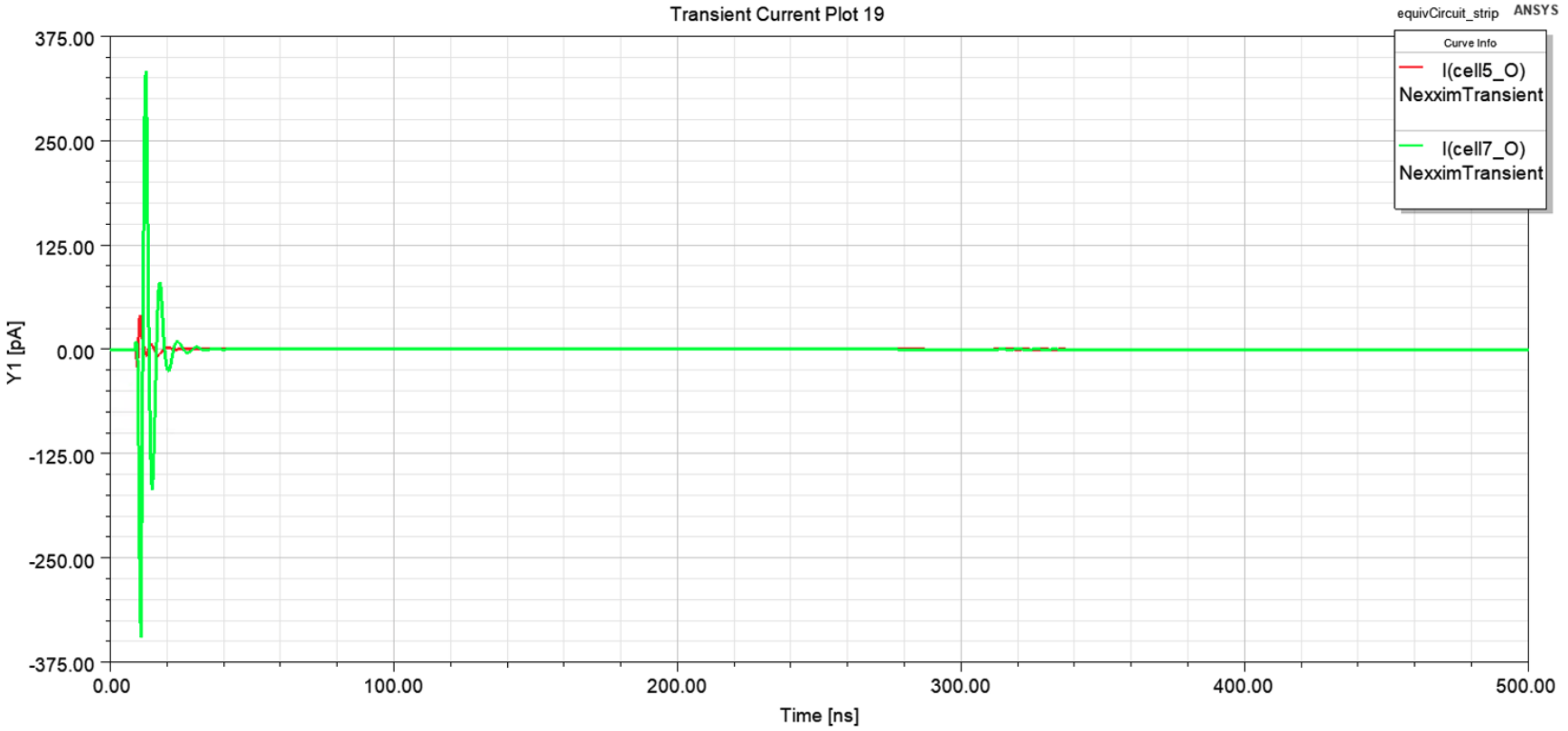
W_{LAr} = 23.6 eV, r_{recomb} = 4%,
q_e = 1.602x10^{-19} C

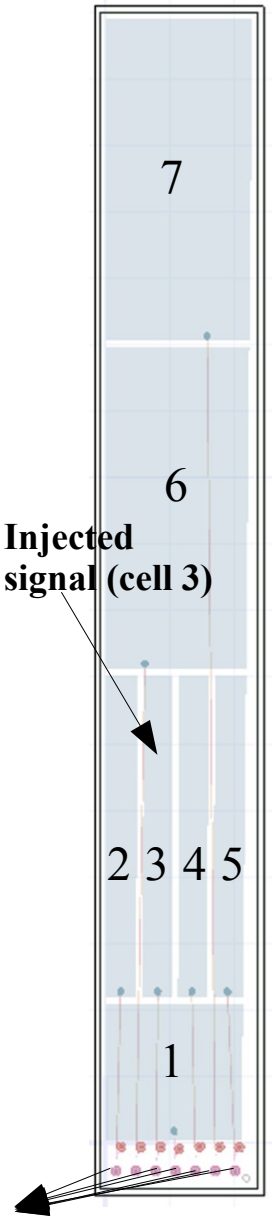
Strip layer noise

- Why is the strip layer noise higher (while it has low capacitance)?
  - Constant term dominates w.r.t. the slope in the noise to capa plot (mild effect)
  - Sampling fraction enters the noise in MeV – after cell calibration
    - SF: [0.365, **0.099**, 0.124, 0.14, 0.154, 0.163, 0.172, 0.178, 0.183, 0.189, 0.193, 0.217]

X-talk in strip layer

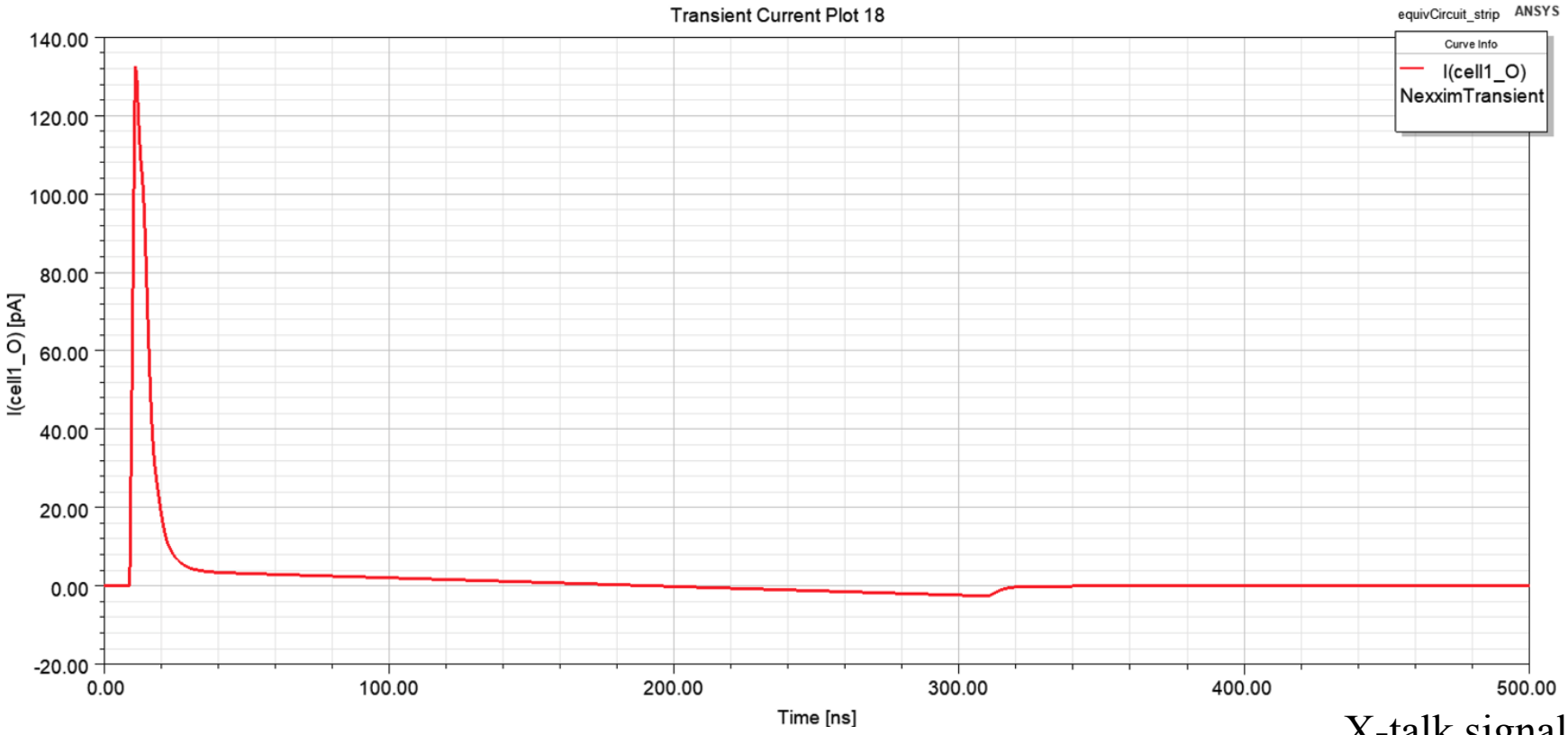
- Studying now the X-talk from the strip layer (injecting on cell 3, 2 shields)
  - Cell 5 and 7
    - Signal could be induced through the cell 4 victim current
      - Cell 5 is 'shielded' by the cell 7 TL

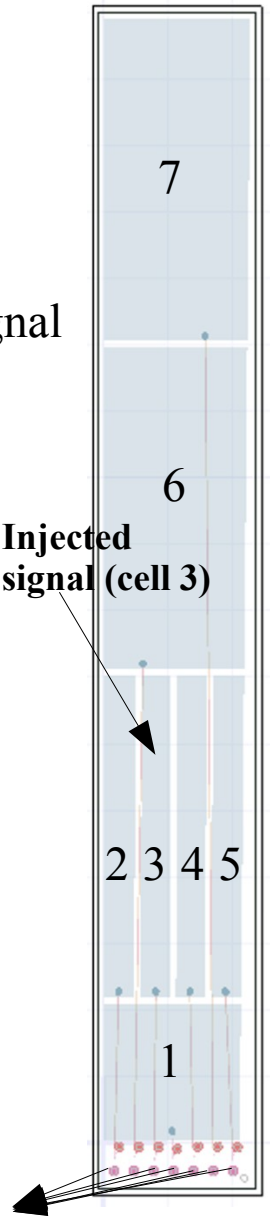




X-talk in strip layer

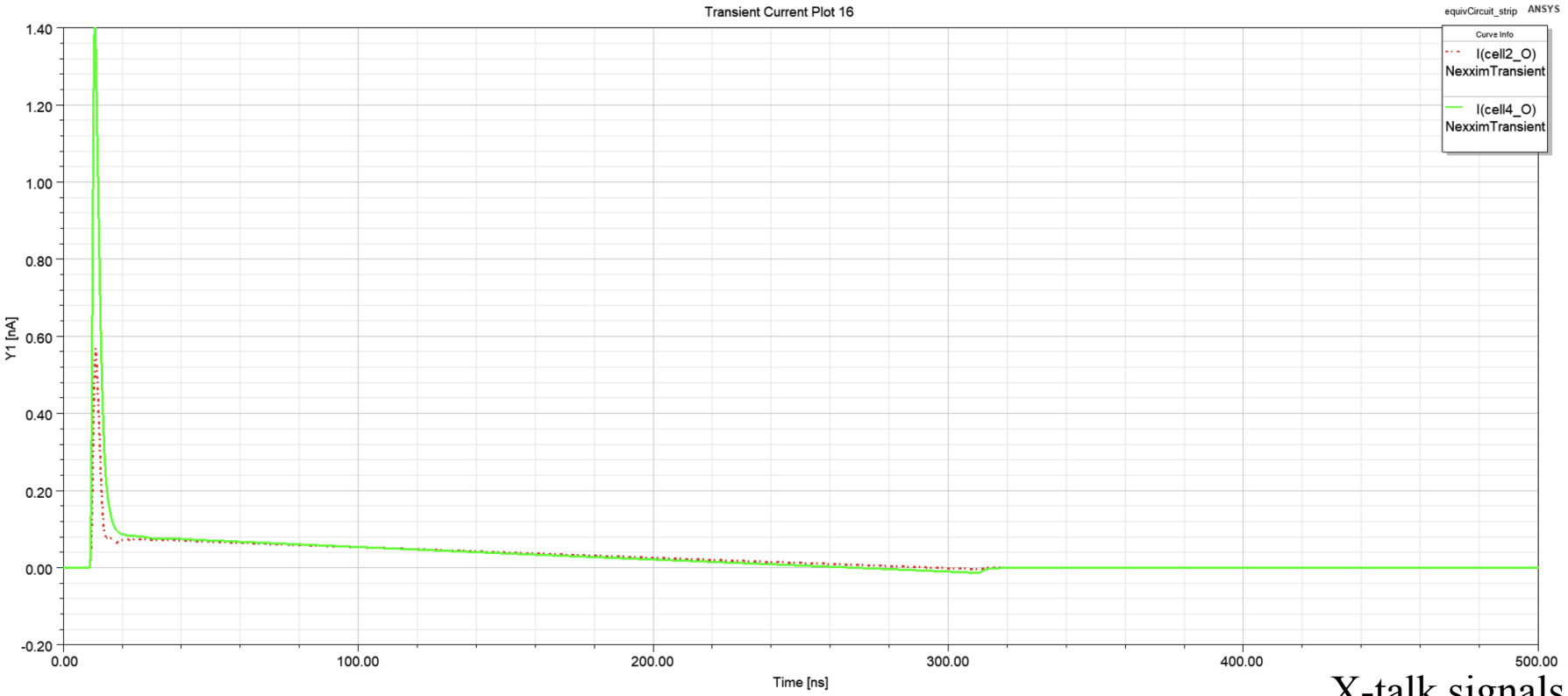
- Studying now the X-talk from the strip layer (injecting on cell 3, 2 shields)
  - Cell 1 x-talk: 0.7 %
    - Small pad-pad coupling
    - TL from Cell 3 runs for a short distance under the Cell 1 pad (pre-sampler)
  - Other cells show mostly reflections that will probably be filtered when integrating signal over time

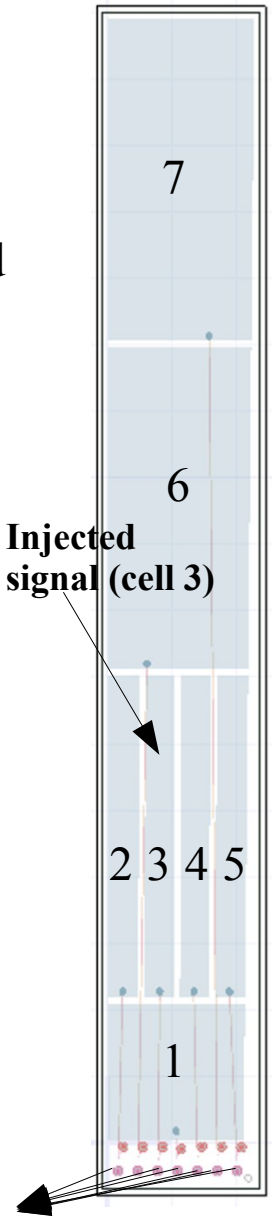




X-talk in strip layer

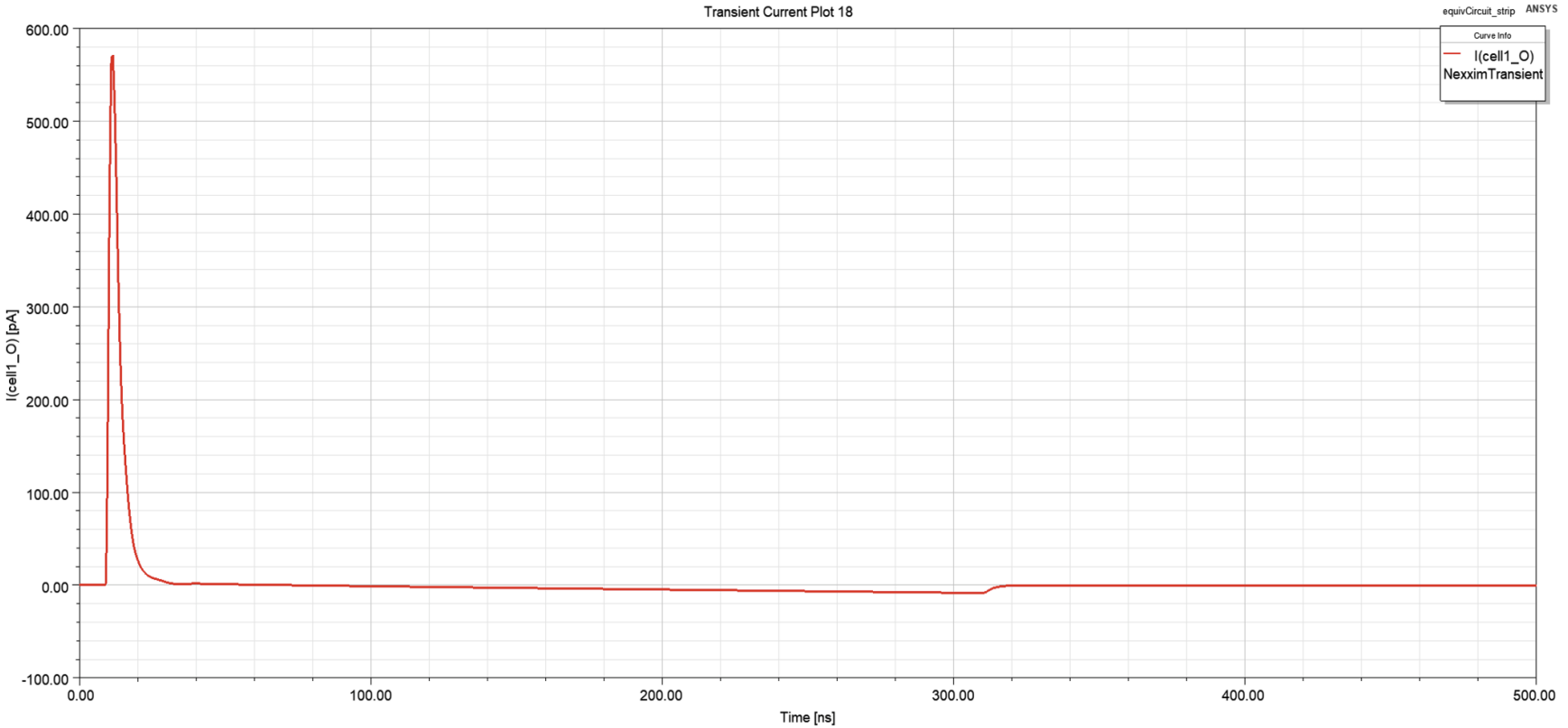
- Studying now the x-talk from the strip layer (injecting on cell 3, **1 shield**)
  - Cell 3 → Cell 4: 7 % x-talk (instead of 6%)
  - Cell 3 → Cell 2: 2.8 % x-talk (instead of 1.8%)
  - **Small difference for Cell 4,** expected since this x-talk comes mainly from signal pad coupling
  - More **sizable difference for Cell 2** which was protected by the shield

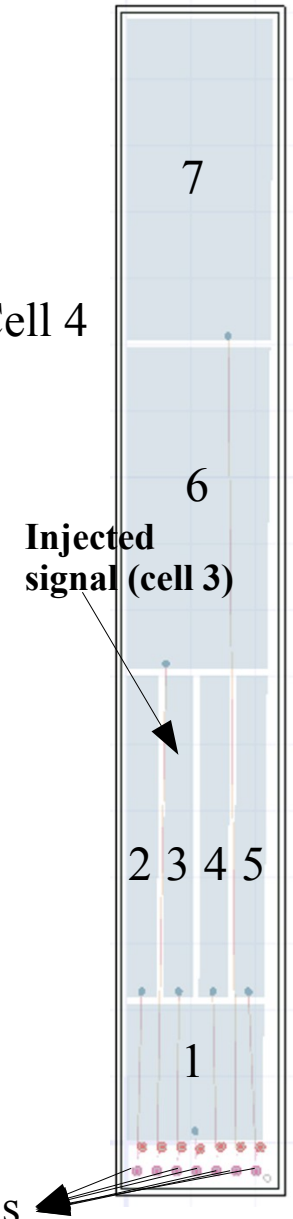




X-talk in strip layer

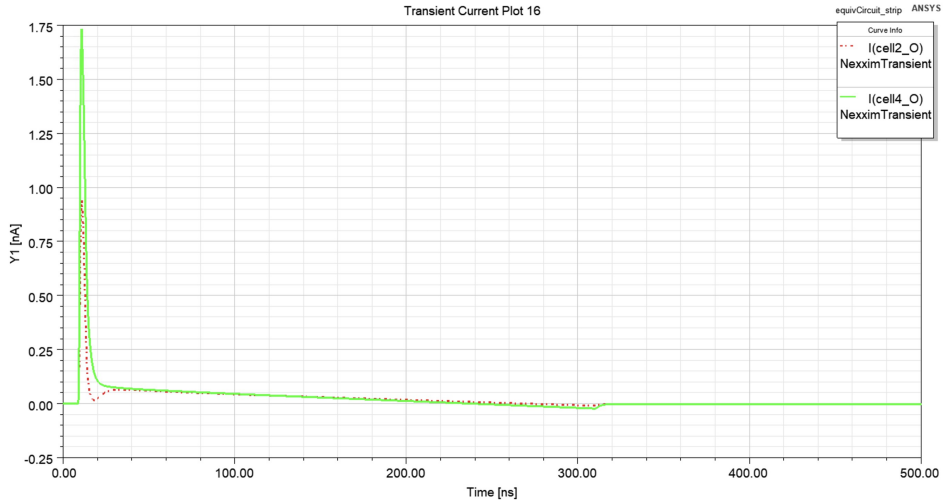
- Studying now the X-talk from the strip layer (injecting on cell 3, **1 shield**)
  - Cell 1 x-talk: 2.8 % (instead of 0.65%)
  - Factor 4 bigger than in the 2 shields scenario
    - Dominant source comes from the signal trace to pad capacitive coupling
  - 0 shield results in back-up (page 30): x-talk current on Cell 6 similar to the one on Cell 4

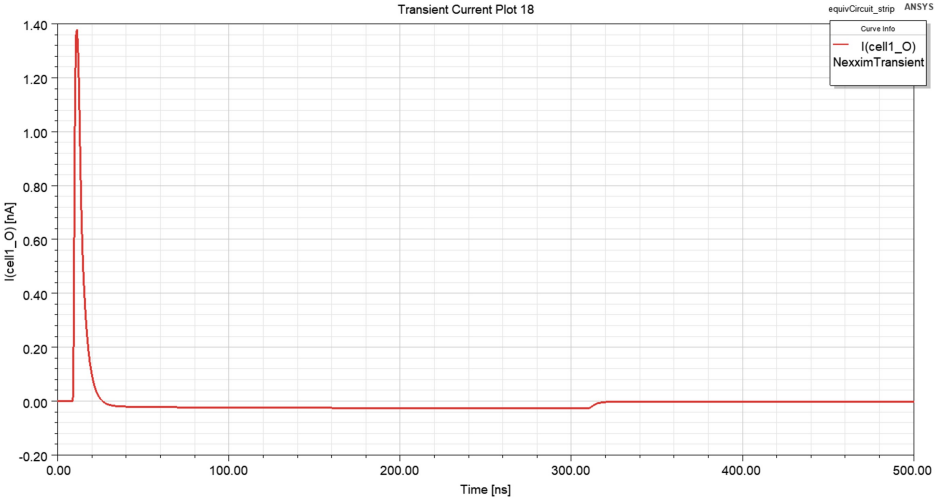


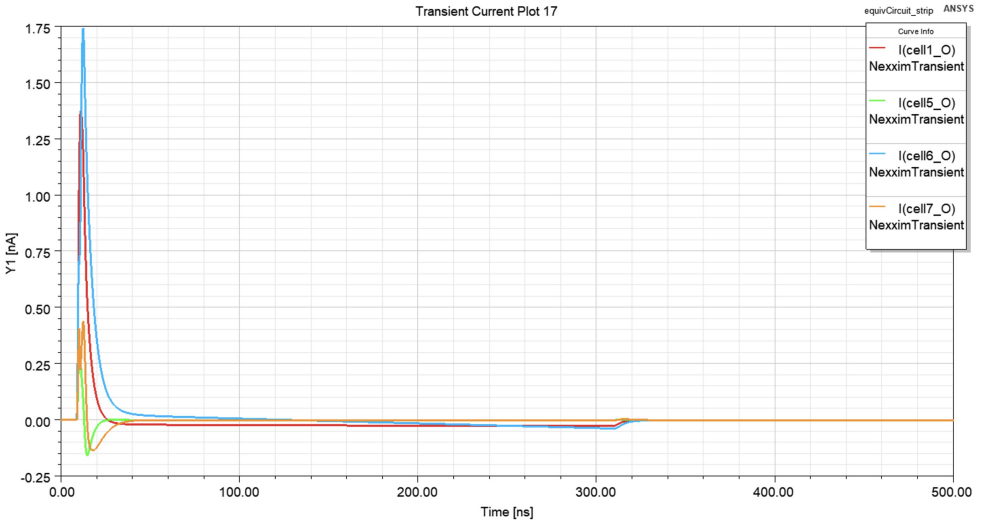


Strip x-talk 0 shield

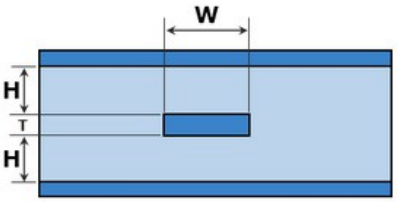
- Studying now the X-talk from the strip layer (injecting on cell 3, 0 shield)





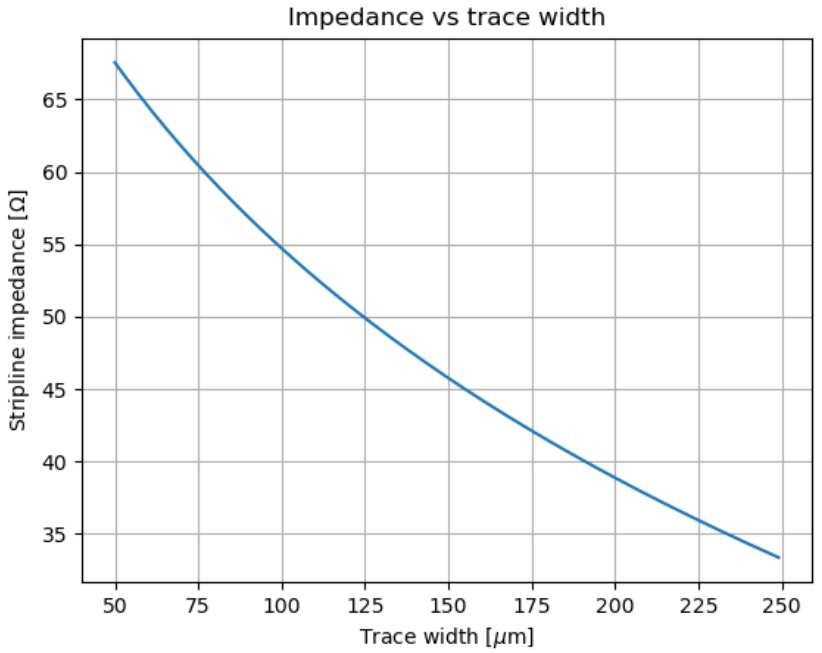


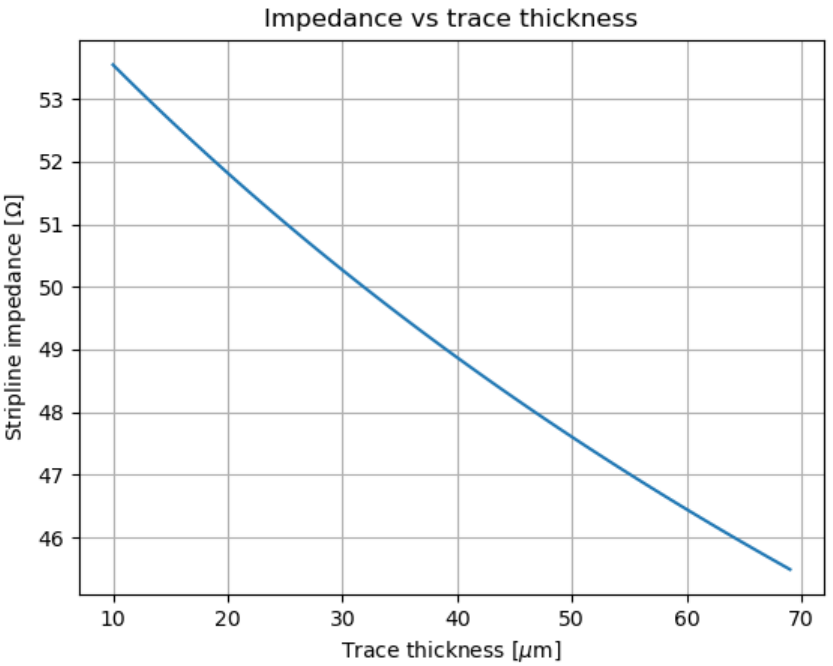
PCB TL impedance



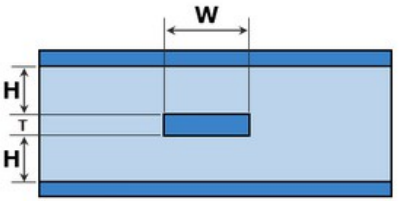
- Results shown today are obtained with a PCB TL of 100 Ohms
- Previous results were shown for TL of 50 Ohms ('baseline')
  - H = 170 µm, W = 127 µm, T = 35 µm, $\varepsilon_R = 4$
- Can we tune the stripline impedance to have 100 Ohms?

$$Z_o = \frac{60}{\sqrt{\varepsilon_R}} \ln\left(\frac{1.9(2h+t)}{0.8w+t}\right)$$



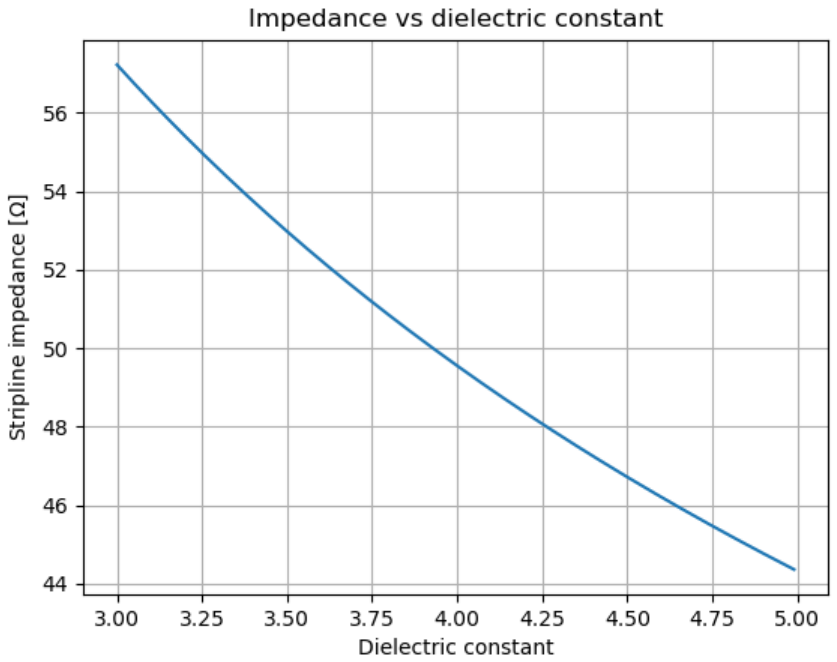


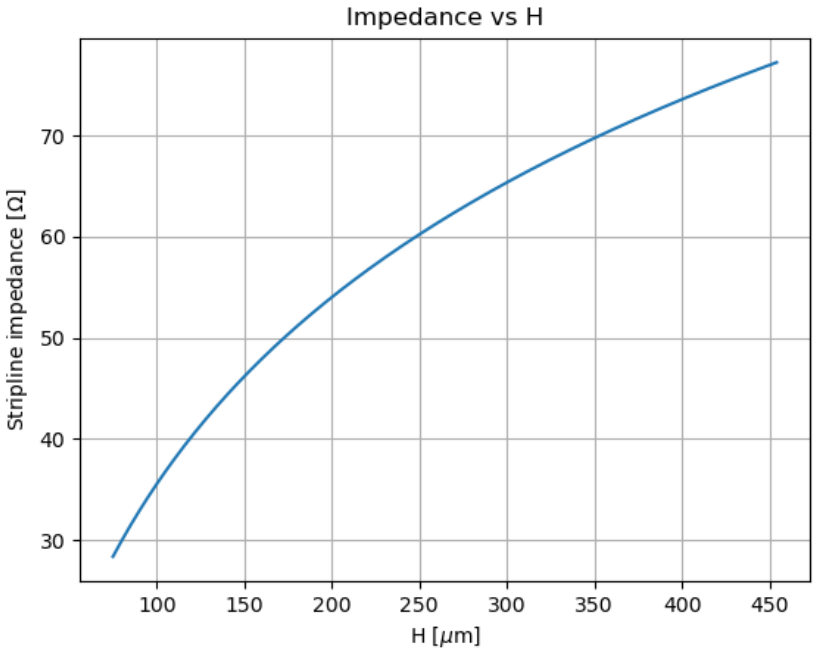
PCB TL impedance



- Results shown today are obtained with a PCB TL of 100 Ohms
- Previous results were shown for TL of 50 Ohms ('baseline')
  - H = 170 µm, W = 127 µm, T = 35 µm, $\varepsilon_R = 4$
- Can we tune the stripline impedance to have 100 Ohms?
  - Seems not so easy (+ if H increases, the detector capacitance to ground will increase)

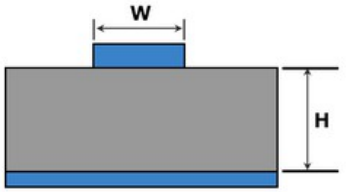
$$Z_o = \frac{60}{\sqrt{\varepsilon_R}} \ln\left(\frac{1.9(2h+t)}{0.8w+t}\right)$$

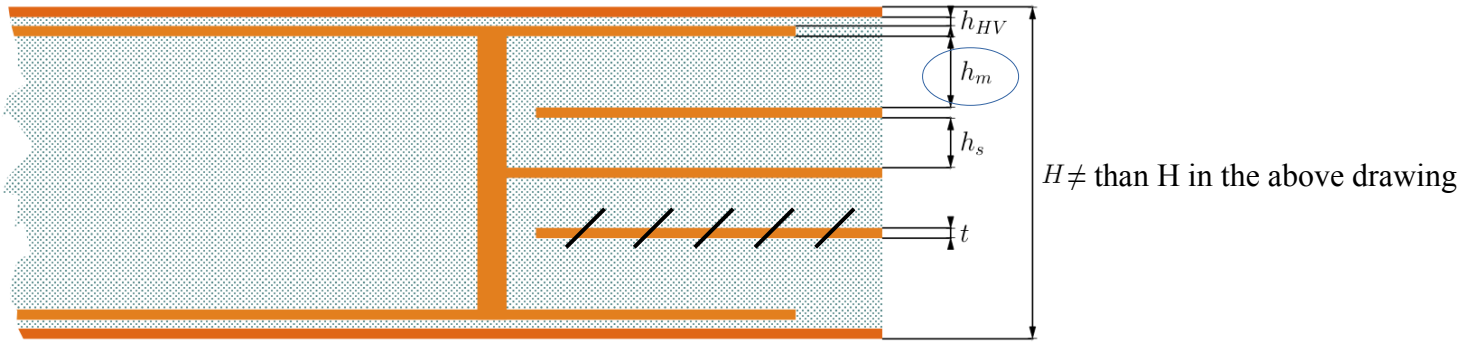




PCB TL impedance

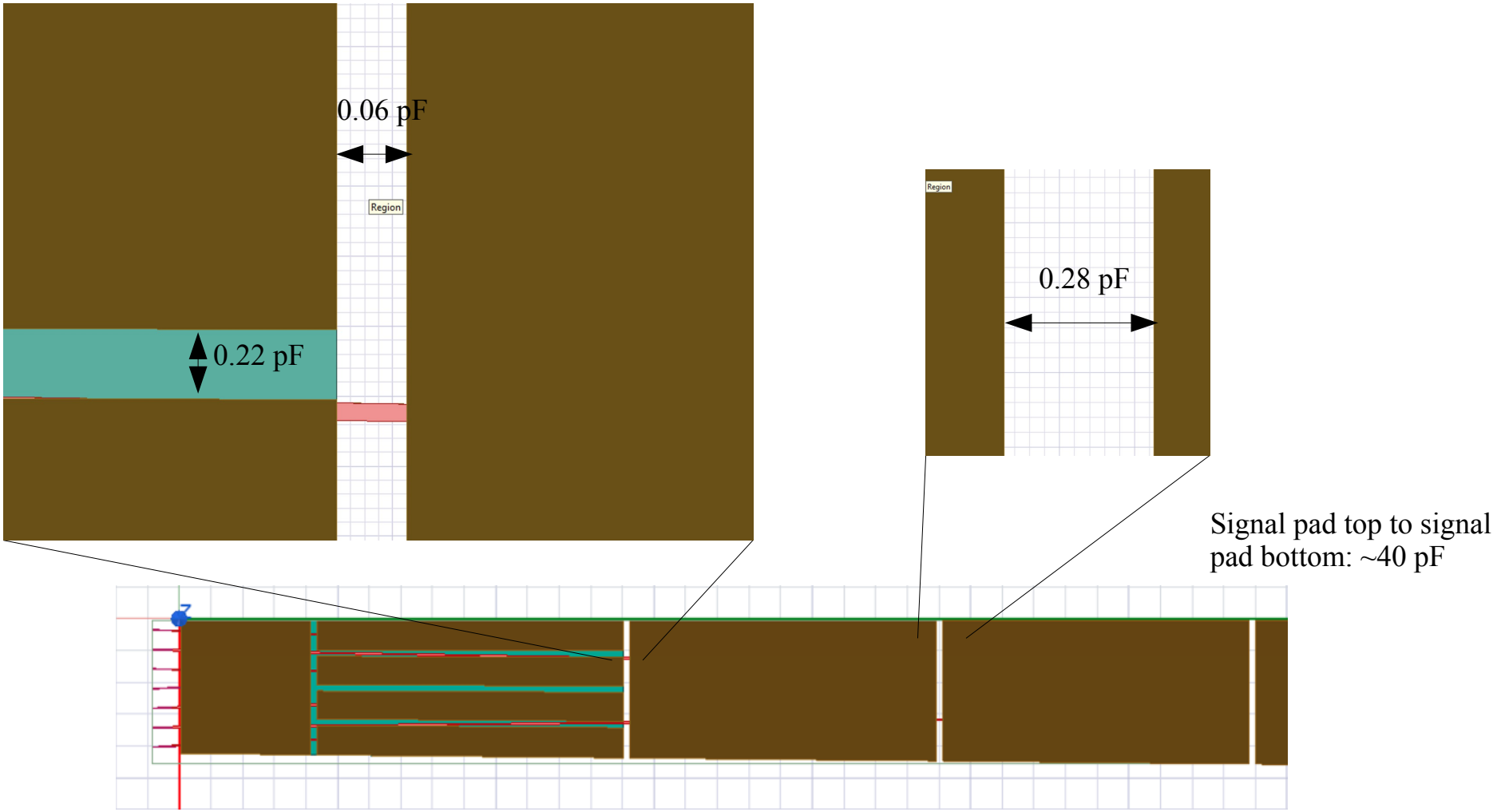
- Another solution could be to remove one shield (stripline → microstrip)
  - Keeping the default values H = 170 µm, W = 127 µm, ε_R = 4 leads to ~85 Ohms
  - With H = 270 µm we have ~100 Ω
    - Would imply h_m ~ 142 µm (baseline is 207.5 µm)
  - Will impact the cross talk and the detector capacitance to ground
    - To be evaluated





Capacitances between signal pads

- 1 mm 'horizontal' spacing between signal pads



Prototype tower layout

Tower 0: baseline
Tower 1: baseline
Tower 2: baseline
Tower 3: Additional ground shield between the signal trace from cells 8 and 9
Tower 4: GND plate instead of one via per shield
Tower 5: No via to inject signal directly on the pad
Tower 6: One shield (on l5)
Tower 7: No shield
Tower 8: Doubled width shields
Tower 9: Halved width shields
Tower 10: One shield with doubled width (on l5)
Tower 11: 70 Ohms (signal trace on the shield layer l3, one shield doubled width on l5, nothing l4)
Tower 12: Outer radius extraction for cells 6 and 7
Tower 13: GND traces between strips (under the anti-etch of Cell 3 to Cell 4)
Tower 14: baseline
Tower 15: baseline

Readout electrodes