IN2P3 CSNSM LAL LPN IPN rsay

Omega

PArISROC

Photomultiplier Array Integrated in Sige Read Out Chip

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PMm²

Orsay MicroElectronic Group Associated

Microelectronics at in2p3

- Large force of microelectronics experienced engineers (~50)
- Expertise in detectors, chip design and test
- Experience in designing and building large particle physics detectors (trackers, calorimeters…)
- Common Cadence tools

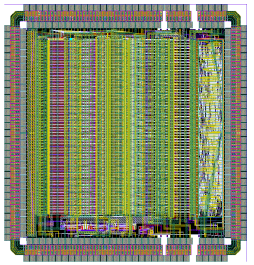
- Actions :
  - Building blocks (SiGE, 130nm)
  - Networking
  - poles

Motivation for poles

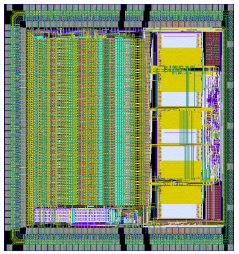
- Continuous increase of chip complexity (SoC, 3D…)
- Importance of critical mass
  - Daily contacts and discussions between designers
  - Sharing of well proven blocks
  - Cross fertilization of different projects
- Creation of poles at in2p3
  - OMEGA at Orsay
  - Strasbourg
  - Dipole Lyon-Clermont

Orsay Micro-Electronics Groups Associated

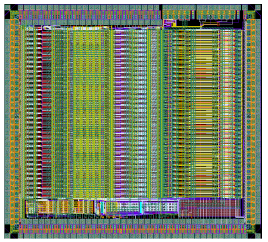
- A strong team of 10 ASIC designers…
  - = 20% of in2p3 designers
  - = 60% of department research engineers
  - A team with critical mass : pole created in 2007 = OMEGA
  - Expertise in low noise, low power high level of integration ASICs
  - 2 designers/ project
  - 2 projects/designer
  - Regular design meetings
- …Within an electronics departmt of 50
  - Support for tests, mesaurements, PCBs…
- A steady production
  - A strong on-going R&D
  - Building blocks SiGe 0.35µm



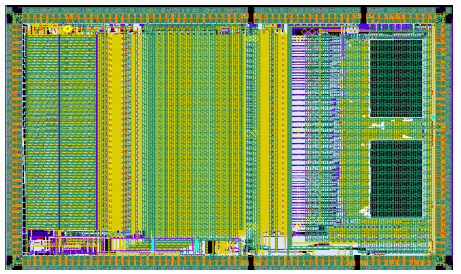
MAROC 2



HARDROC



SKIROC



SPIROC

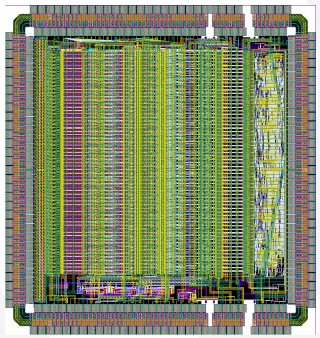
Orsay micro-electronics team

- 8 research engineers (1 IR0, 2 IR1, 5 IR2)
- 1 phD student
- 1 visitor from China IHEP Beijing

Recent chips

- Several chips developped for ATLAS LAr, OPERA, LHCb, CALICE in BiCMOS 0.8µm and installed on experiments
- Turn to Silicon Germanium 0.35 µm SiGe BiCMOS technology in 2005
- Readout for MaPMT and ILC calorimeters
- Very high level of integration : System on Chip (SoC)
- Parallel activity of building blocks

MAROC 2



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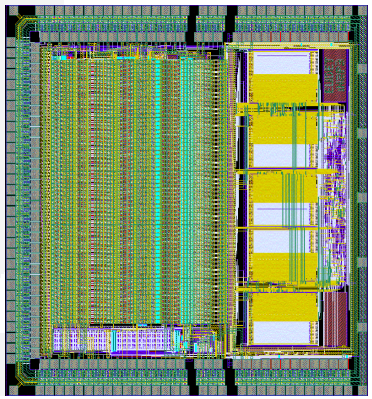

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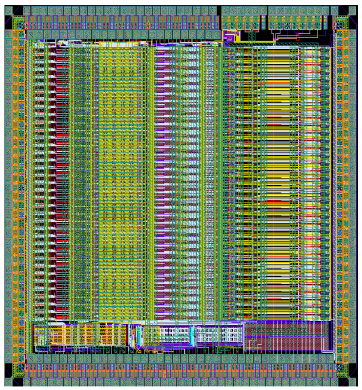
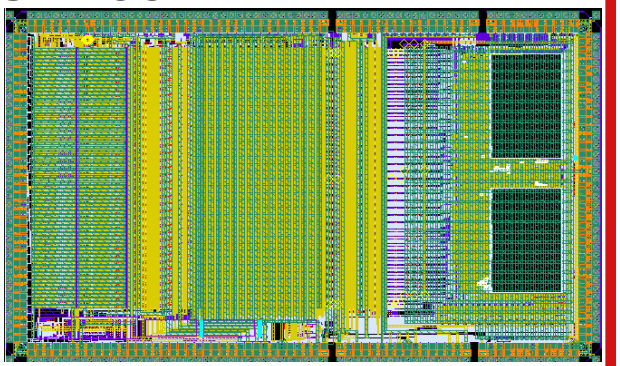
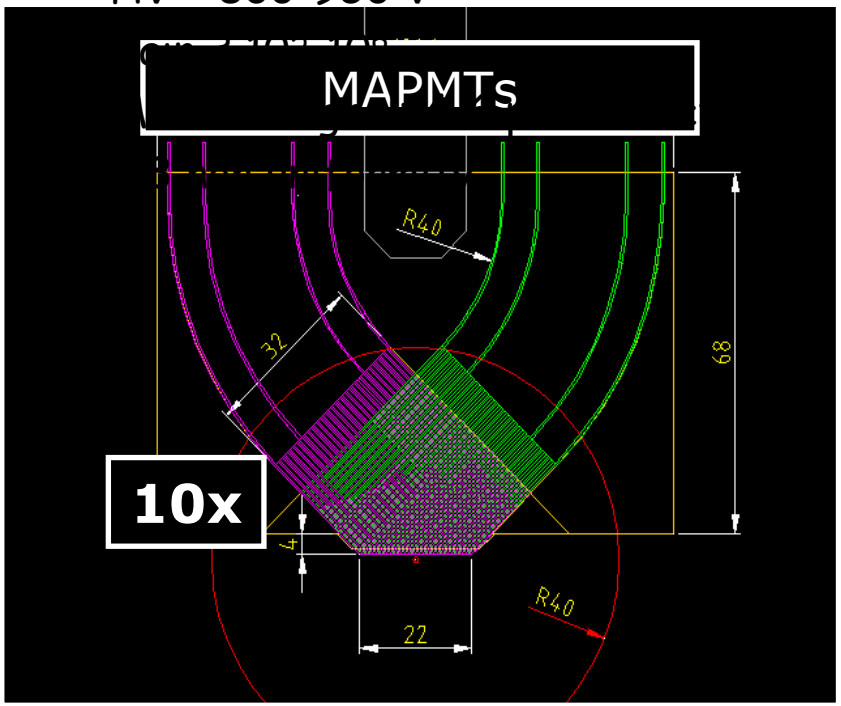


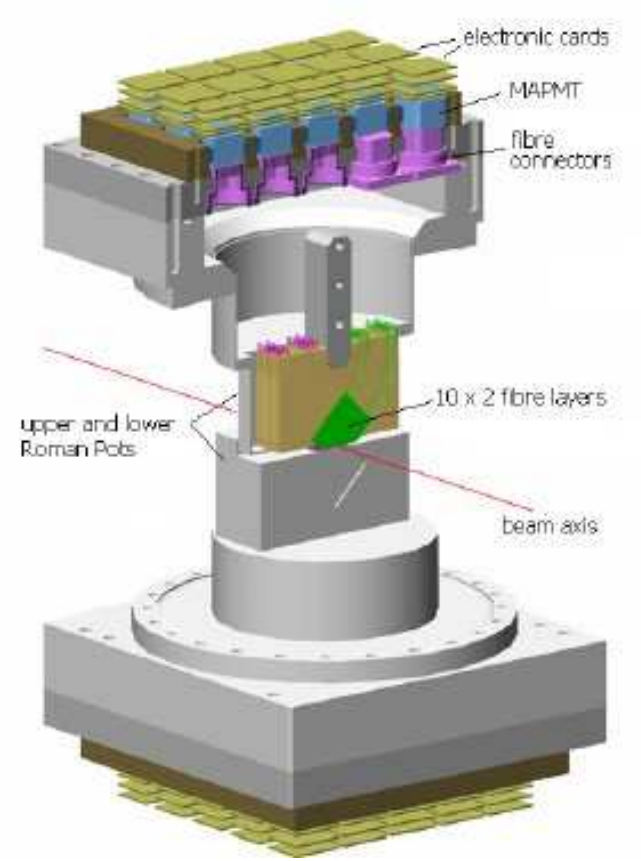
SPIROC



MAROC for ATLAS luminometer

- Absolute measurement of the luminosity
- Roman Pots:
  - 0.5mm^2 scintillating fibers
  - 1 RP = 10*64 fibers in U + 10*64 fibers in V
  - 240m from the Interaction Point
- Multi Anode PM Tubes
  - 64ch Hamamatsu H7546
  - HV = 800-950 V

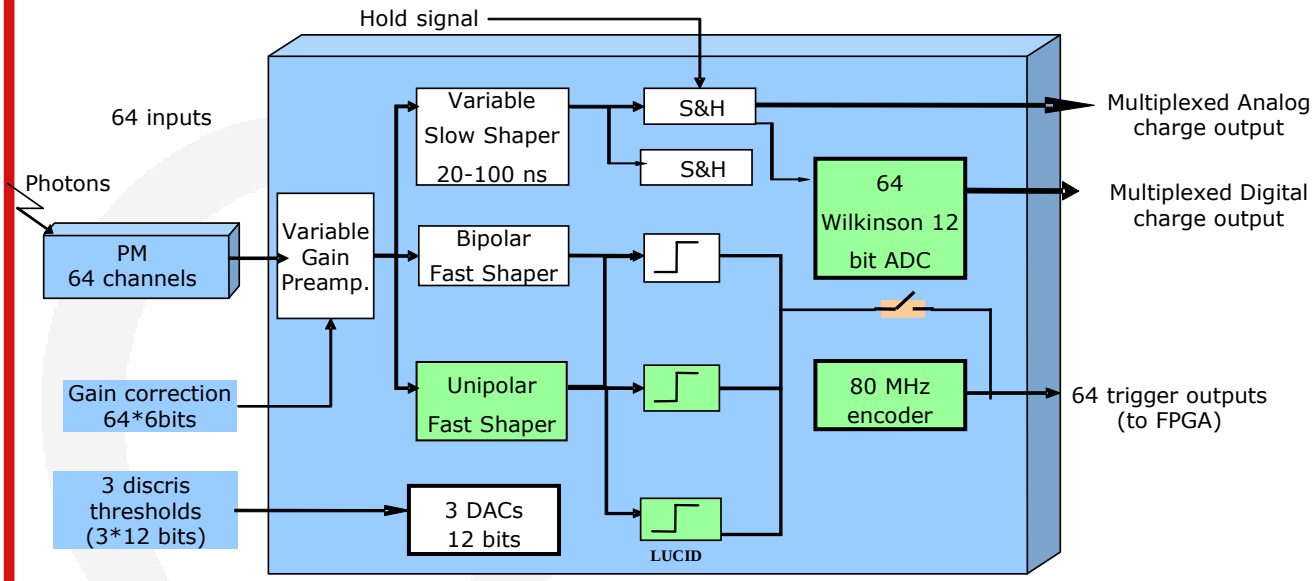


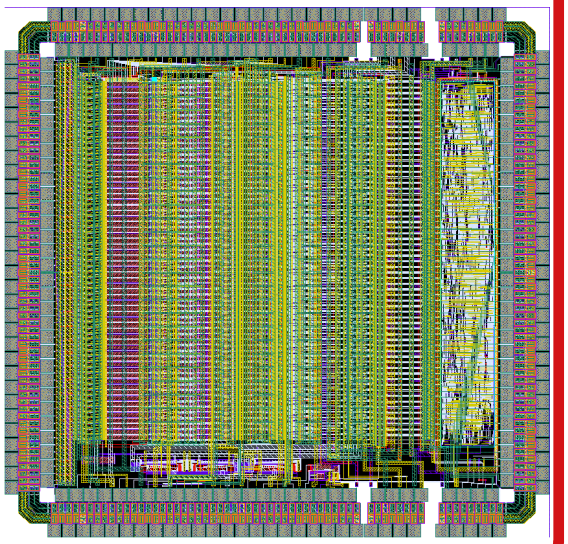


MAROC : 64 ch MAPMT chip for ATLAS lumi

Complete front-end chip for 64 channels multi-anode photomultipliers

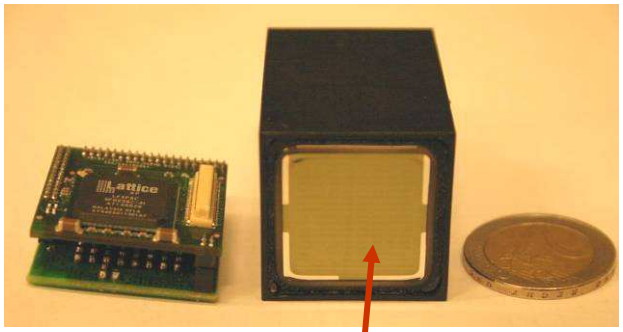
- Auto-trigger on 1/3 p.e. at 10 MHz, 12 bit charge output
- SiGe 0.35 µm, 12 mm2, Pd = 350mW



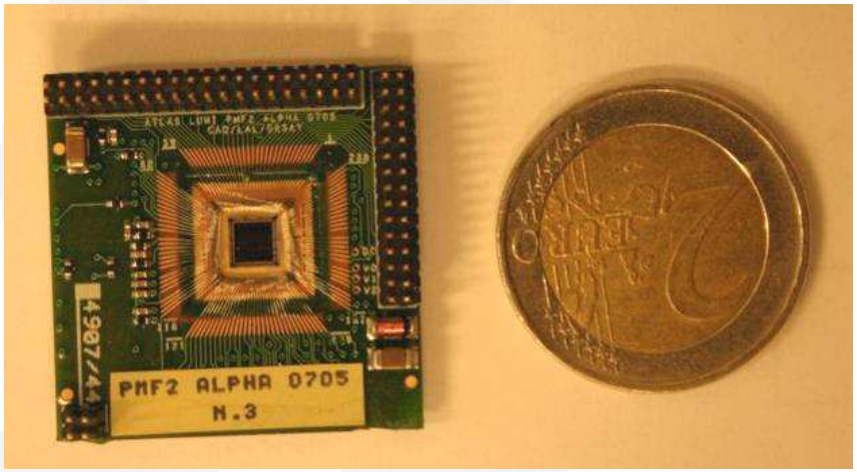


Active board pictures

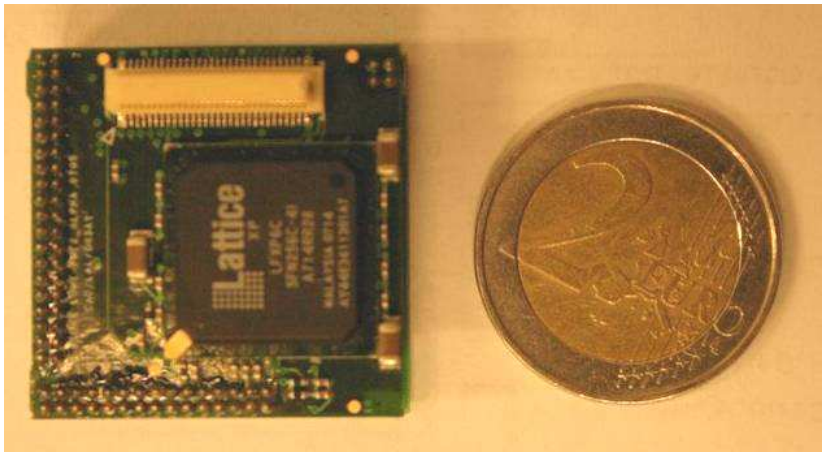
MAROC2 chip bounded at CERN



64 ch PMT

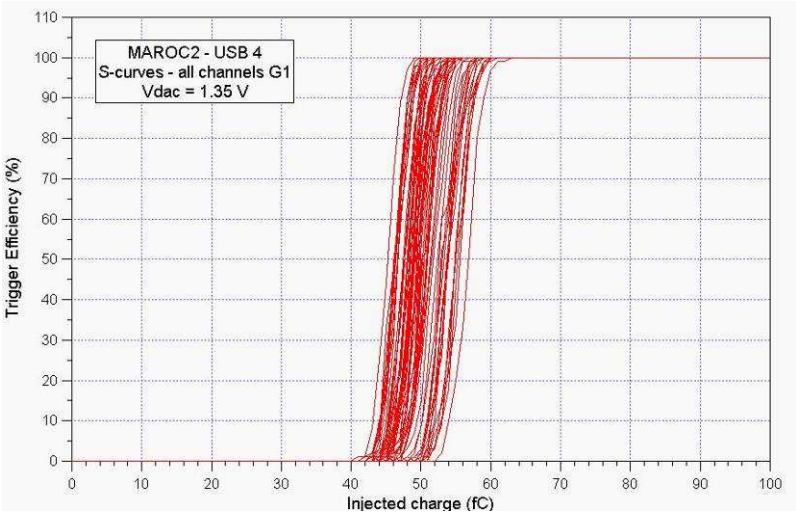


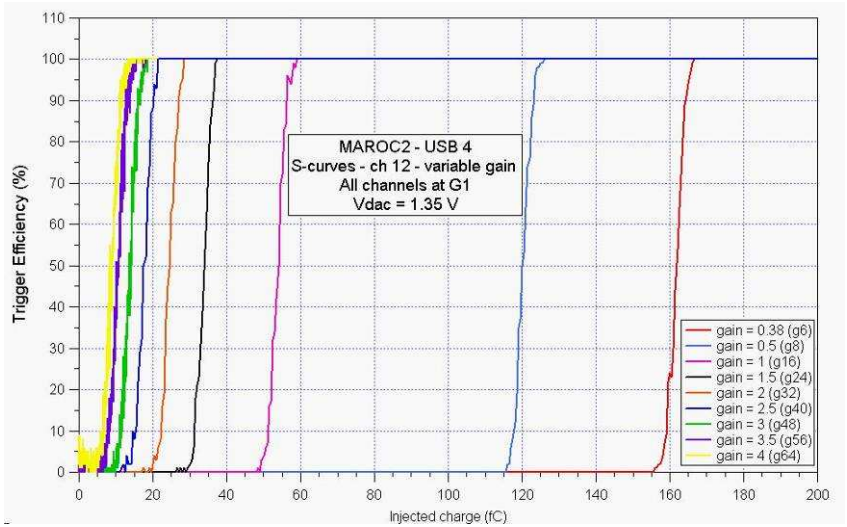
MAROC side

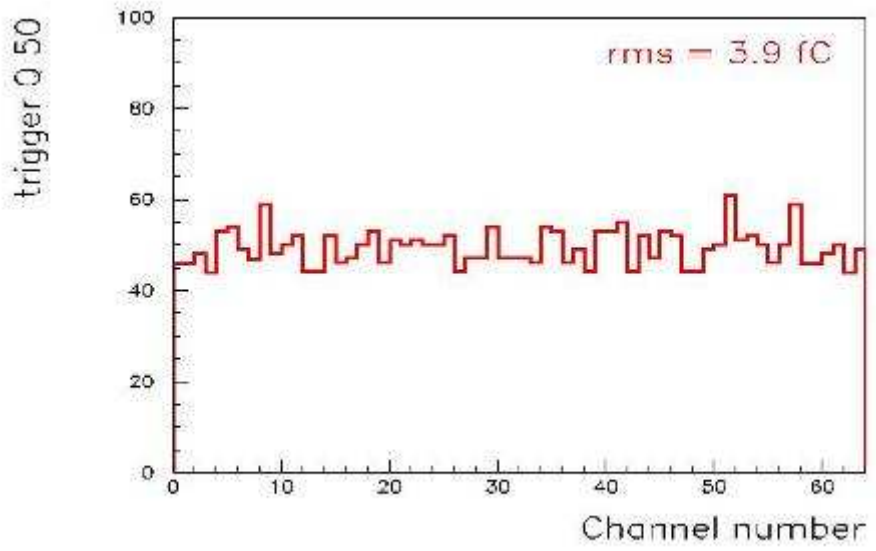


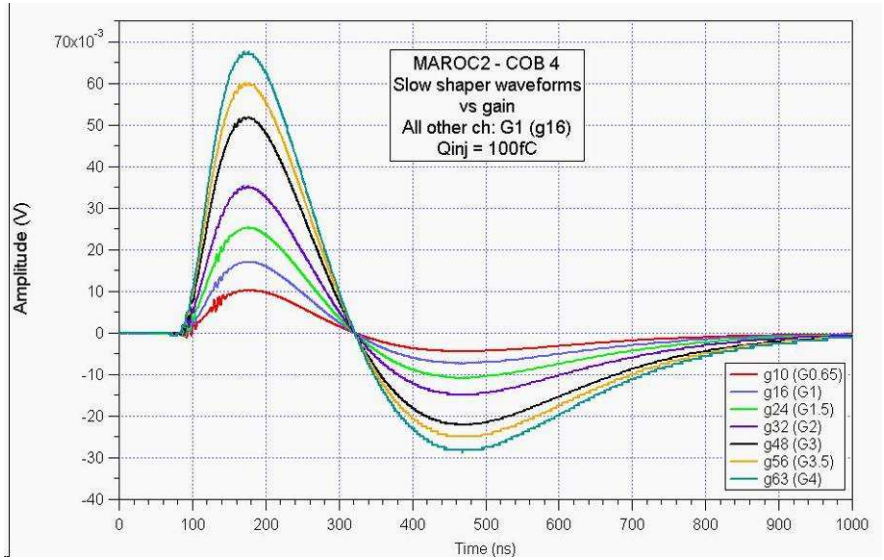
Lattice side

MAROC Efficiency curves

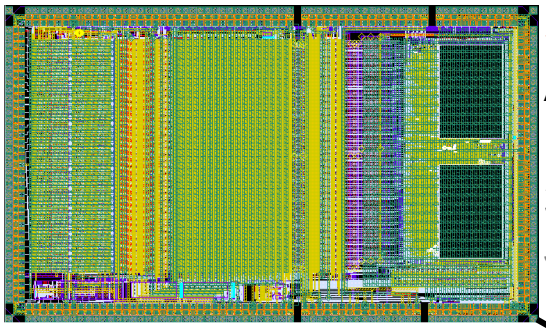




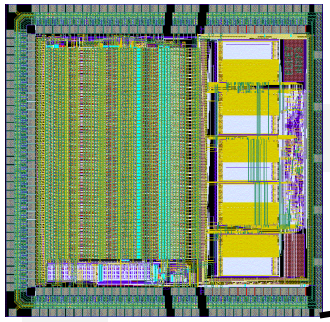




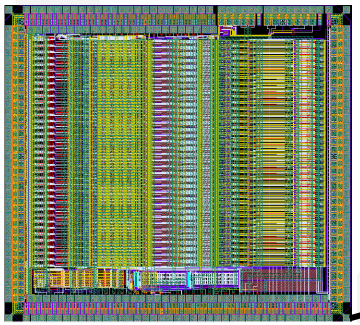
The front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

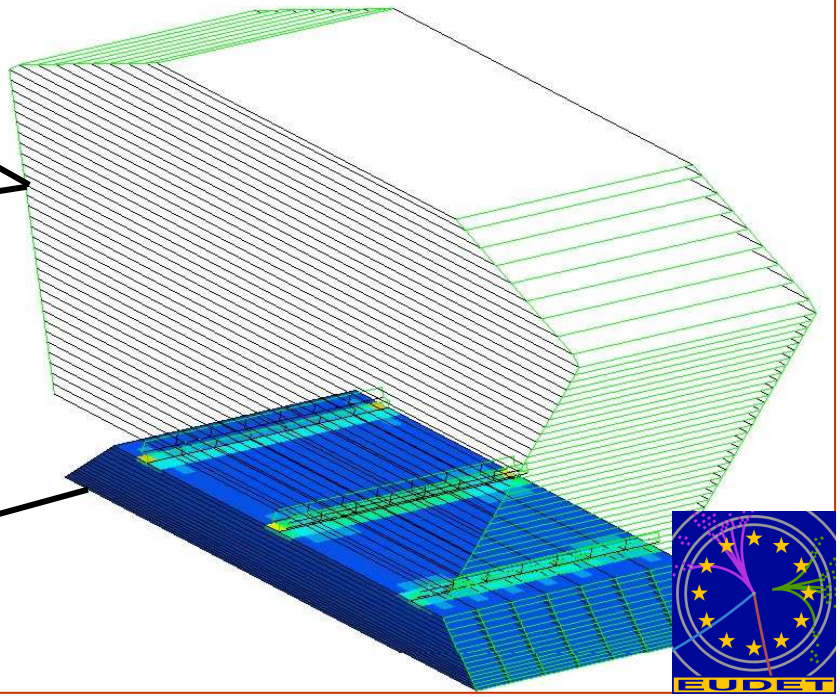


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T



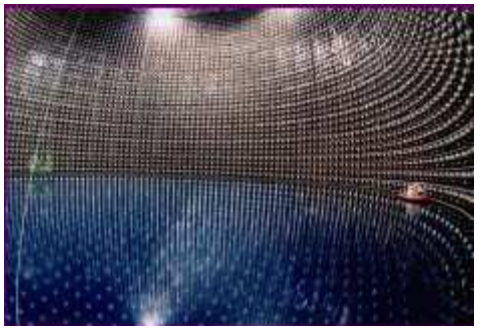
PMm² project (1)

- ***PMm² :*** *"Innovative electronics for array of photodetectors used in High Energy Physics and Astroparticles".*

- R&D program funded by French national agency for research (ref. ANR-06-BLAN-0186) (LAL, IPNO, LAPP and Photonis) (2007-2010)

- Application : large water Cerenkov neutrino

  (more generally: exp. with large number of PMs)



Cost approach [Photonis NNN05]

C. Marmonier, NNN05, France, April 2005
LIGHT06, Israel, January 2006

Size (Diameter)	20	20(17)	12	Inch
Photocathode area	1660	1450	615	cm^2
Quantum efficiency	20	20	24	%
Collection efficiency	60	60	70	%
Cost	2500	2500	800	€
	12.6	14.4	7.7	€ /PE_U/cm^2

Cost/cm^2 per useful photoelectron

Cost / (cm^2 x QE x CE)

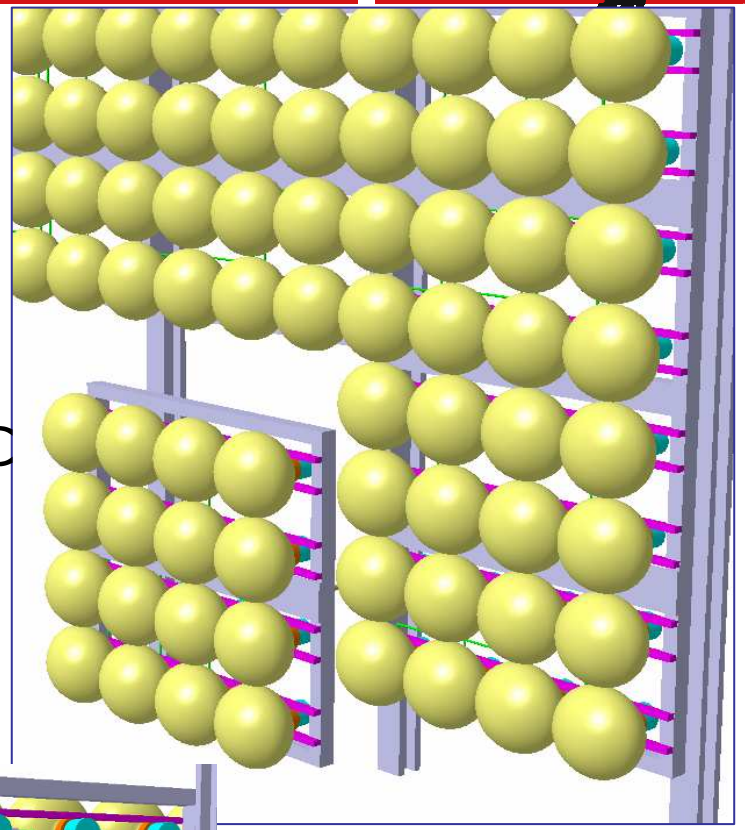
12" is better in SER and timing

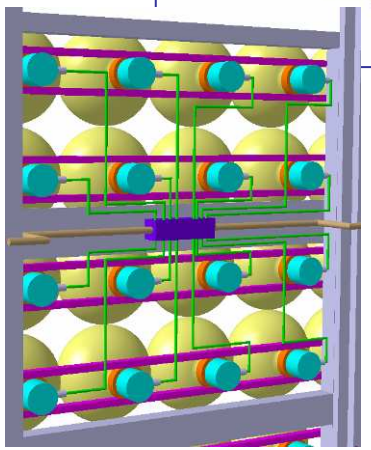
12" provides a higher granularity

But, the number of channels is increased

PMm² project (2)

- The project proposes to segment the very large surface of photodetection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics.
- Replace large PMTs (20") by groups of 16 smaller ones (12") with central ASIC
  - **Independent channels**
  - **charge and time measurement**
  - **water-tight, common High Voltage**
  - **Only one wire out (DATA + VCC)**
- **Target :**
  - **1pe efficiency**
  - **Triggerless**
  - **1ns time resolution**
  - **High granularity**
  - **scalability**
  - **Low cost**



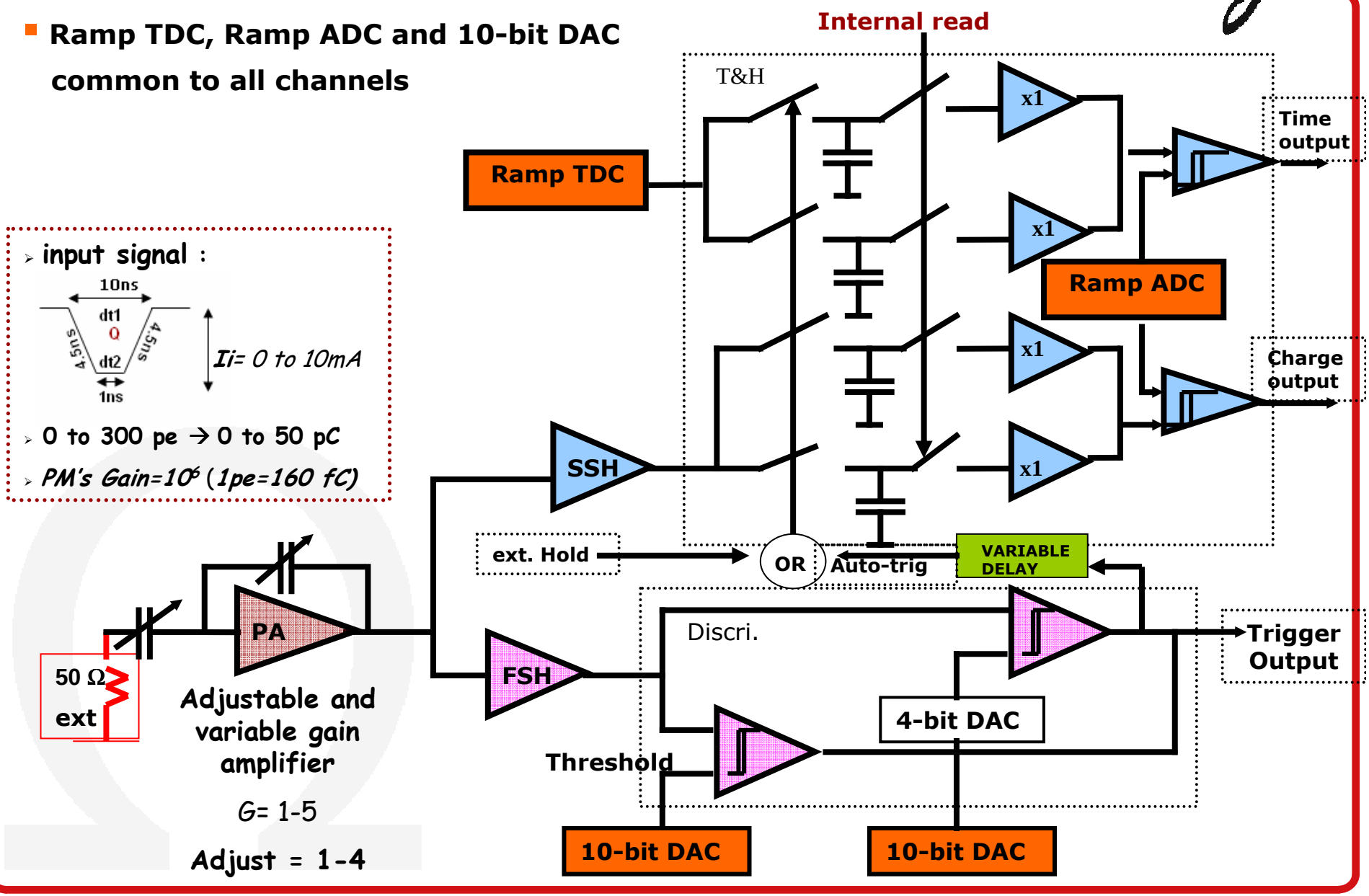


PARiSROC description (1)

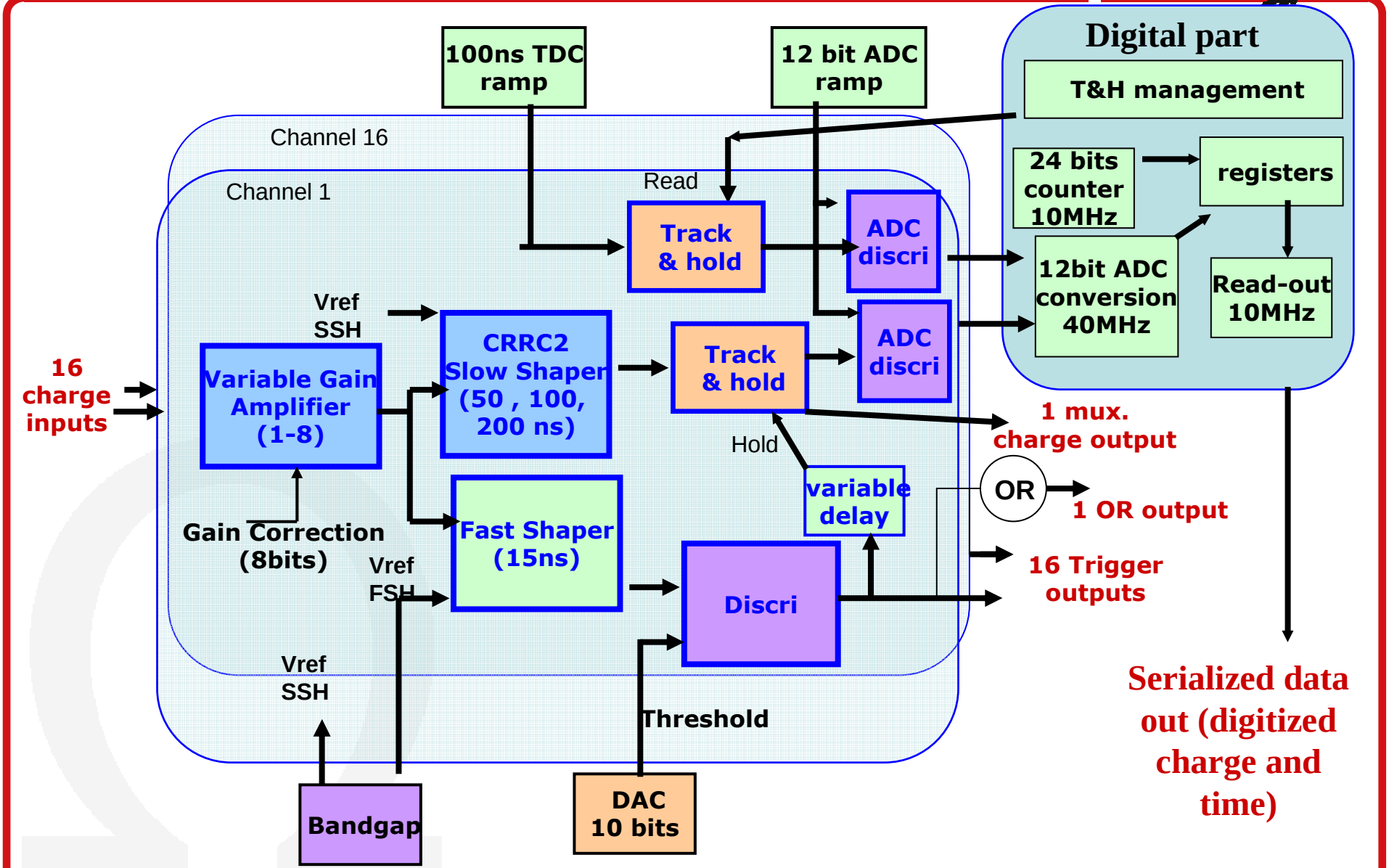
- Characteristics :
  - 16 preamplifier inputs
    - Variable gain :1 → 8 (3bits) (common on 16 channels)
    - PMTs gain adjustment by a factor 4 (8 bits) (channel by channel)
    - Input dynamic range : 0 → 300 pe (0 → 50pC) with 1% linearity
  - 16 trigger outputs:
    - Fast shaper (τ=15ns) + low offset discriminator
    - Threshold provided by common internal 10bit DAC (1/3 pe)
    - "OR" of 16 triggers output
  - 1 digitized and multiplexed charge output :
    - Slow shaper with variable shaping time (τ=50ns,100ns,200ns)
    - Dual Track & Hold + multiplexed analog output or internal ADC
  - 8 to 12-bit internal ADC (Wilkinson) for charge and fine time measurement
  - Internal TDC : 24 bits counter (coarse) + fine 1 ns
  - One serial output : 2channel number + BCID + Charge + time
  - Dissipation : 5mW/ch

One channel synoptic

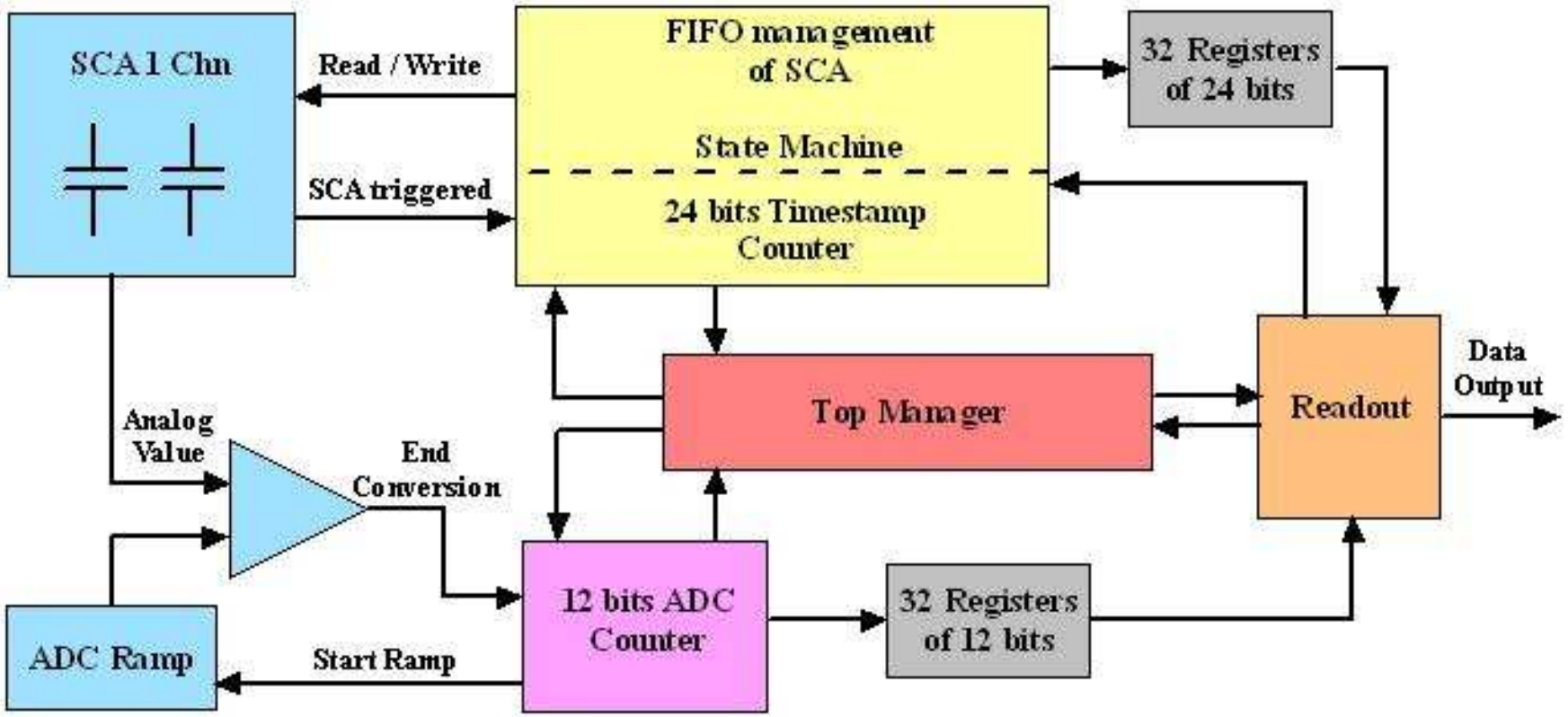
- **Ramp TDC, Ramp ADC and 10-bit DAC common to all channels**



PARiSROC architecture



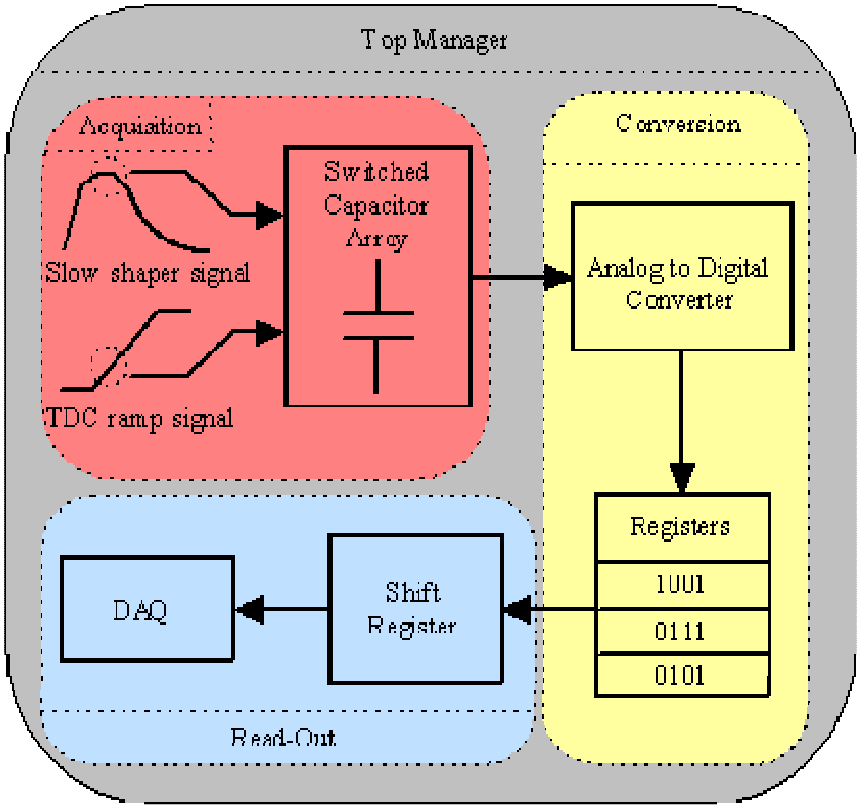
Digital part architecture



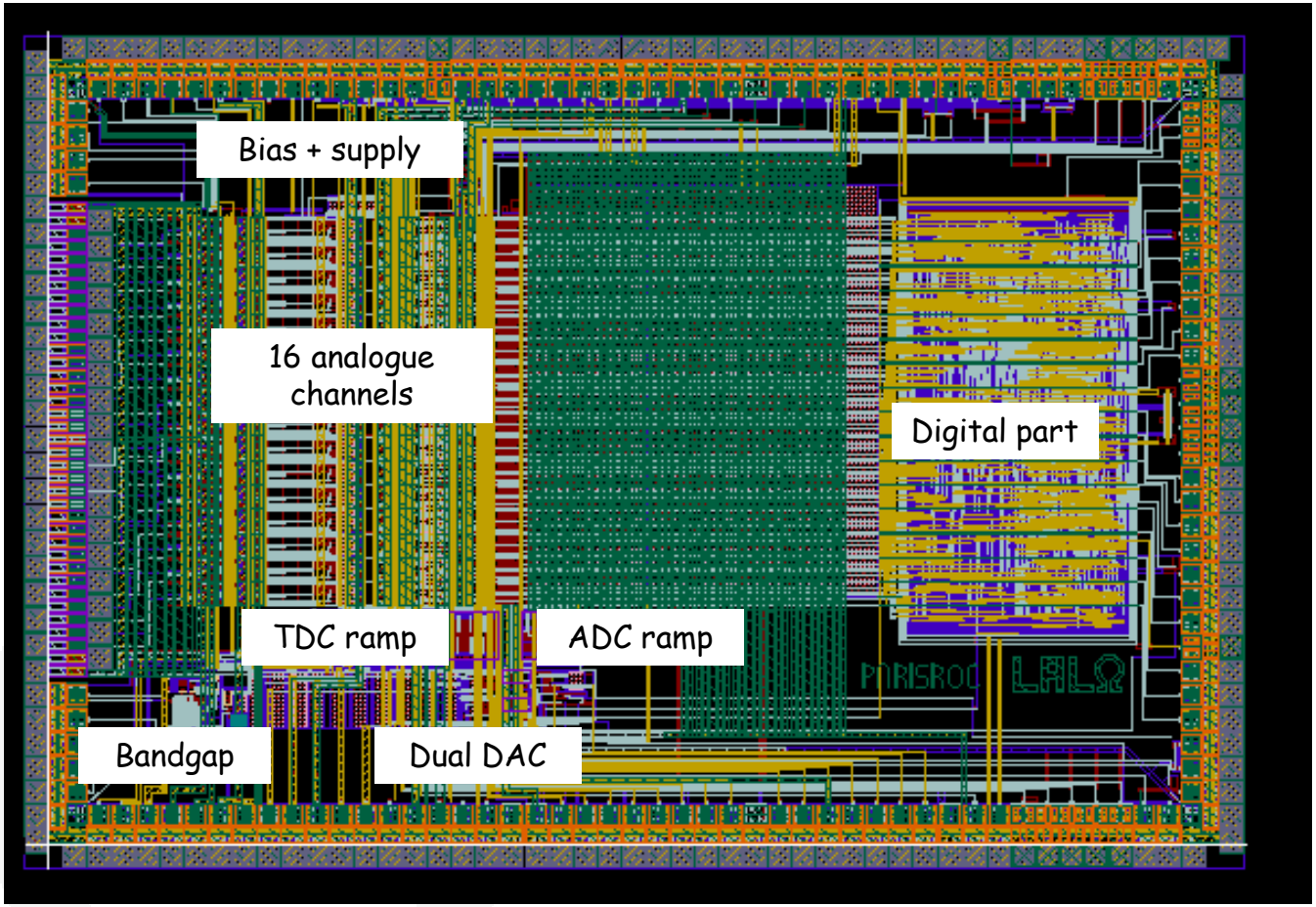
- SCA depth of 2 for time and charge measurement
- SCA management like FIFO
- Timestamp 24b counter @ 10 MHz (1.67s)
- 40 MHz clock for ADC + SCA management
- 10 MHz clock for Timestamp + Readout

Selective Read Out

- Only hit channels are readout
- Readout clock : 10 MHz
- Max Readout time (16 ch hit) : 100 us
- 52 bits of data / hit channel (all gray)
- Readout format (MSB first) :
  - (MSB) 4 bits channel # + 24 bits timestamp
  - 12 bits charge + 12 bits time (LSB)



PARiSROC layout



Technology :

AMS SiGe 0.35µm

Size **:**

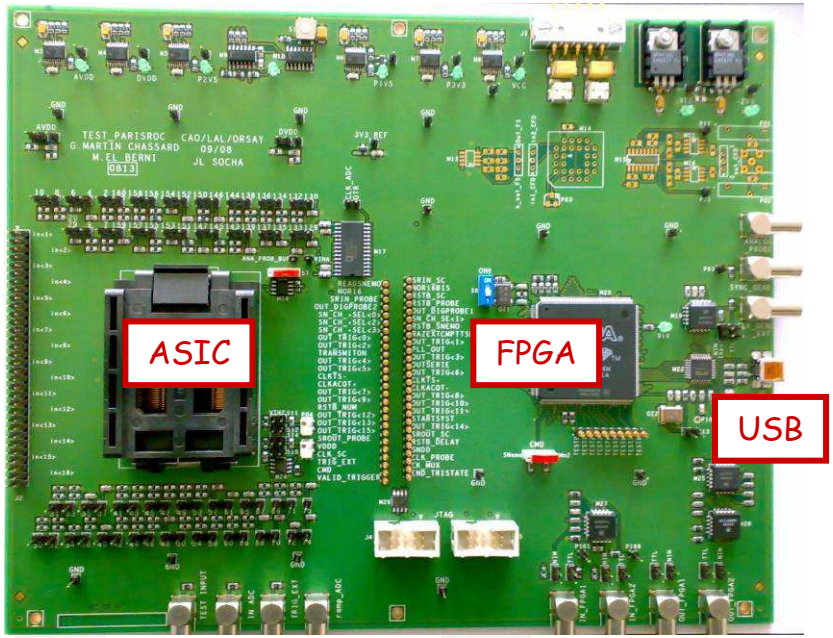
5mmX3.4mm

Package **:**

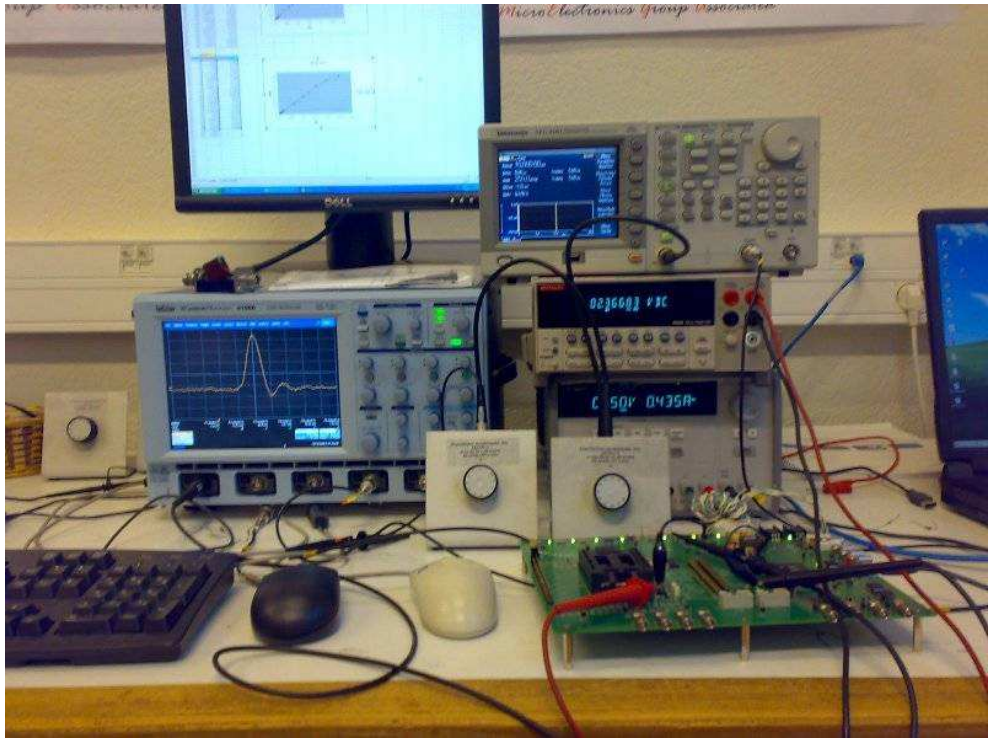
CQFP160

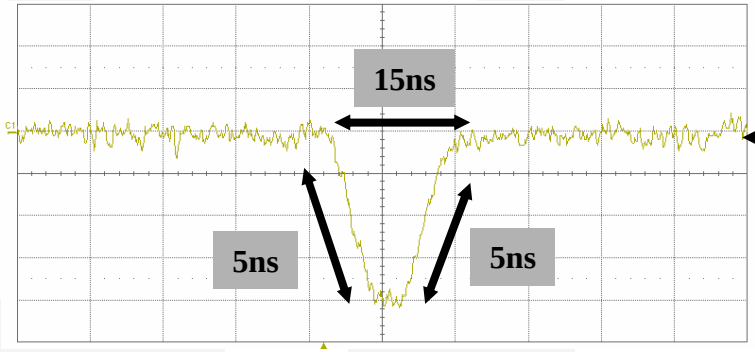
Measurements

TEST BOARD



TEST BENCH



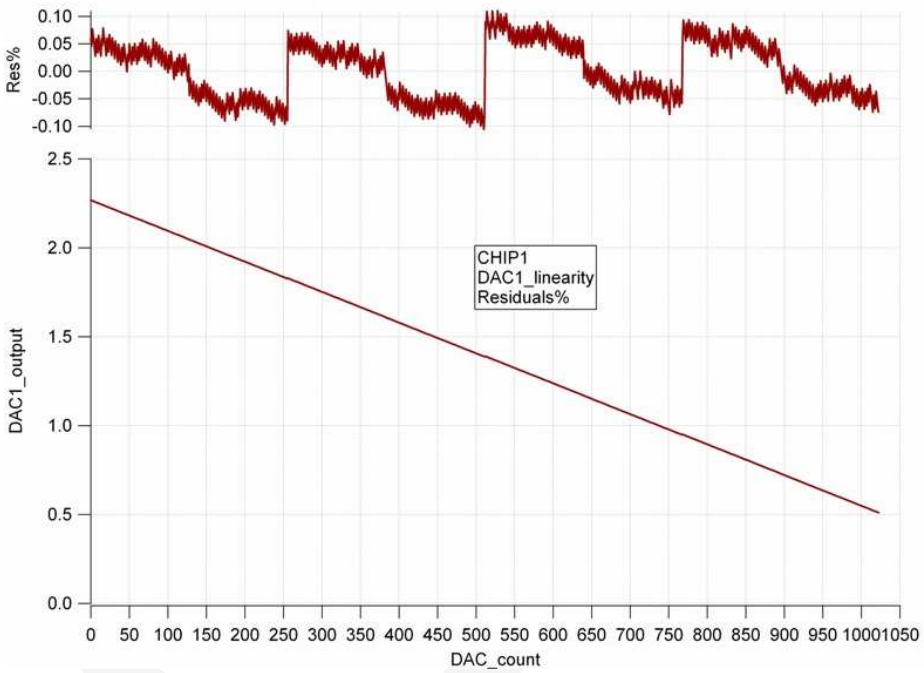


input signal : ***Ii= 0 to 5mA***
0 to 300 pe → 0 to 50 pC
PM's Gain=10⁶ (1pe=160 fC)

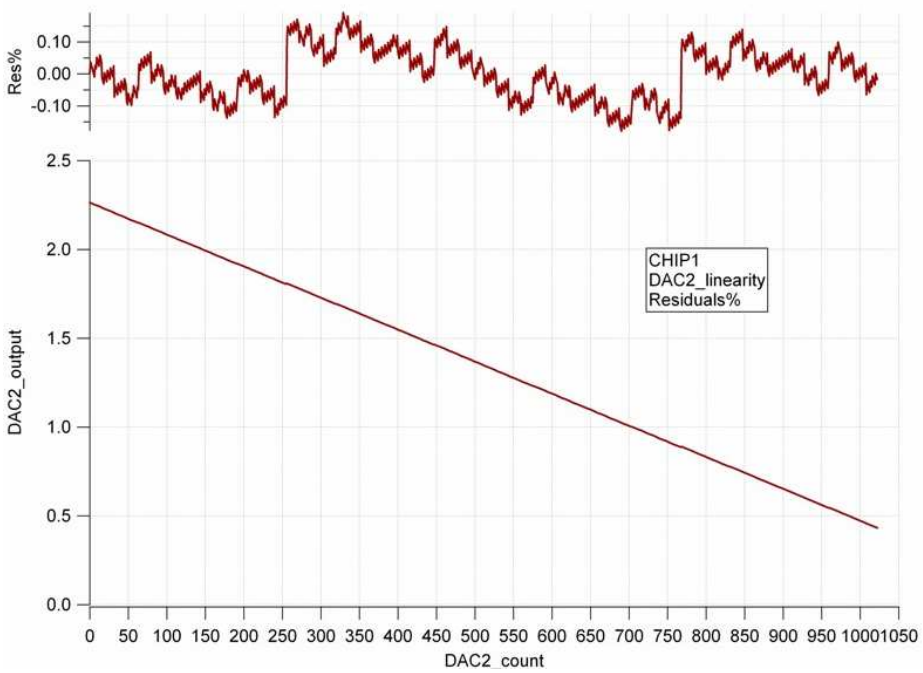
Internal 10bit DAC linearity

	Residuals(%)
DAC1_Chip 1	-0.1 to 0.1
DAC2_Chip 1	-0.1 to 0.1

DAC1_LINEARITY_CHIP1



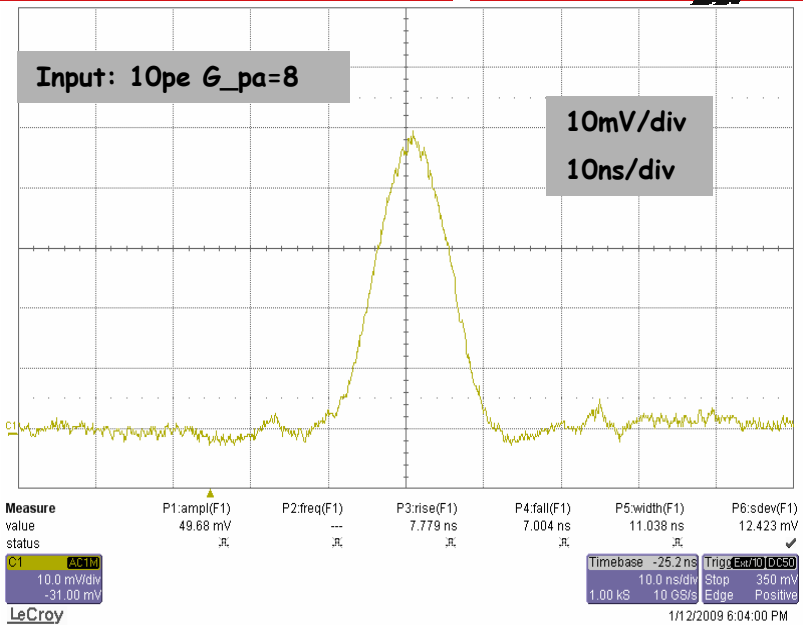
DAC2_LINEARITY_CHIP1



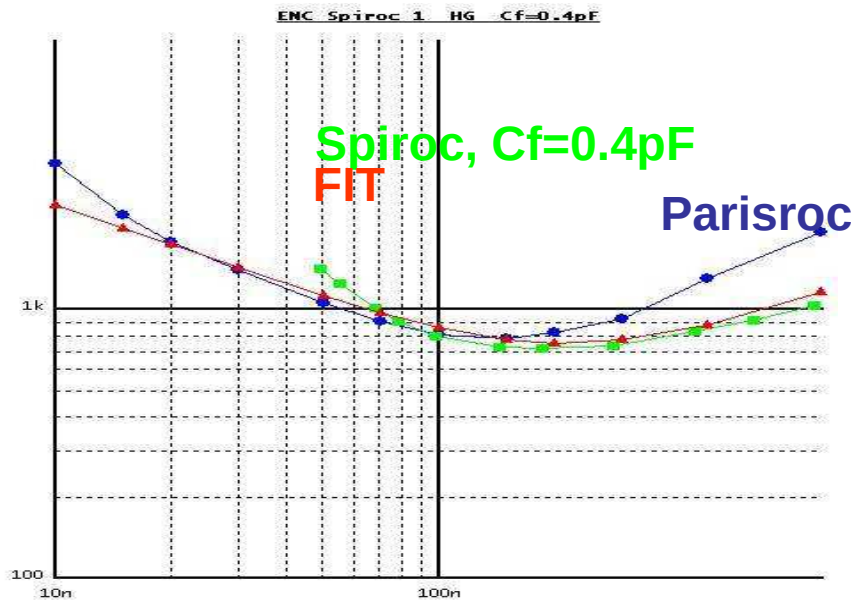
Preamplifier measurements

- High speed : tr~5ns

Preamp	G=8	G=14
Vout(1pe)	5 mV	7.3 mV
Rms noise	1 mV	1.2 mV
Noise in pe	0.2	0.16
SNR	5	6.2

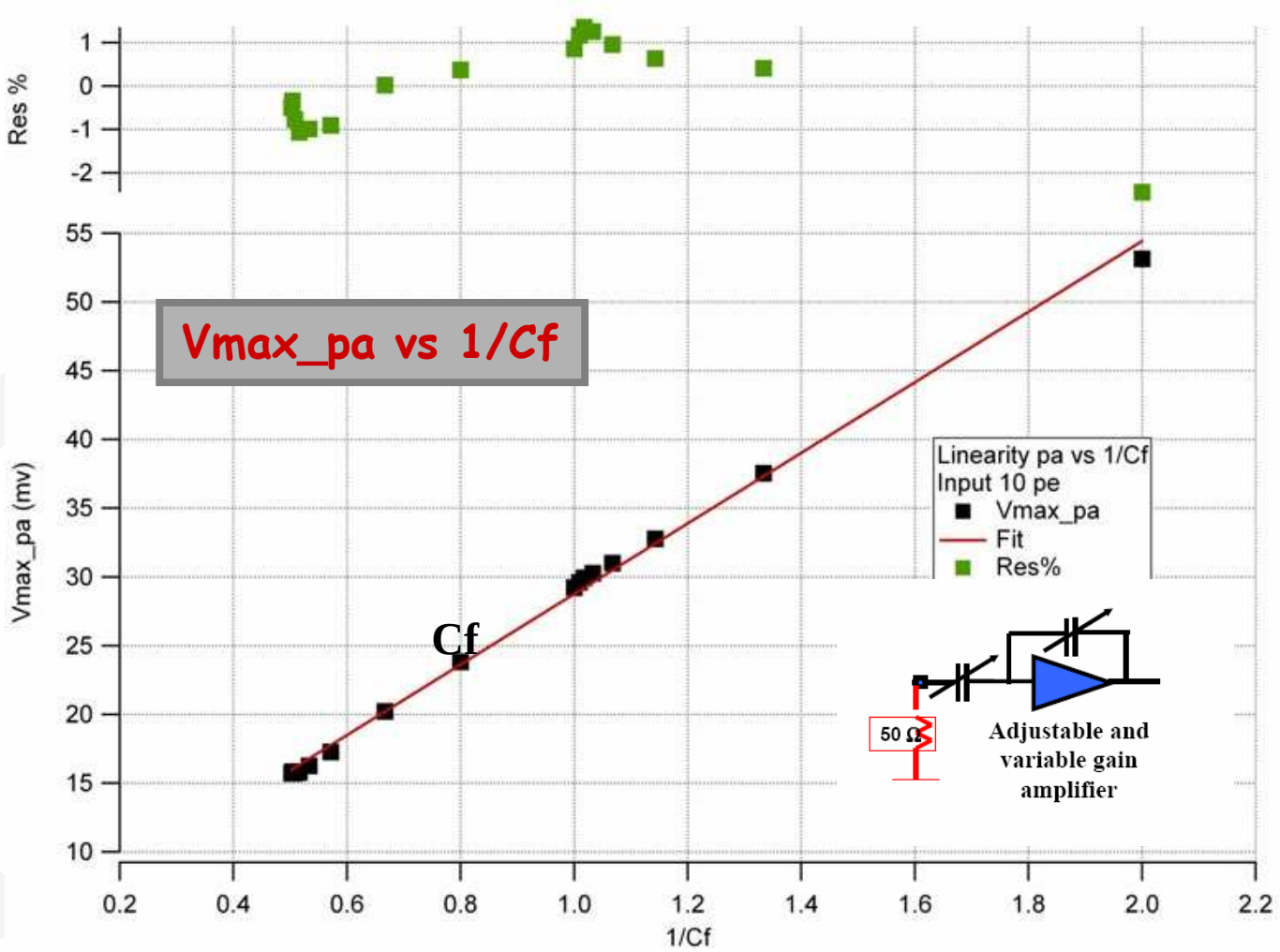


- Extra noise sources
  - 10 MHz clock : doubles the noise
  - Low frequency noise



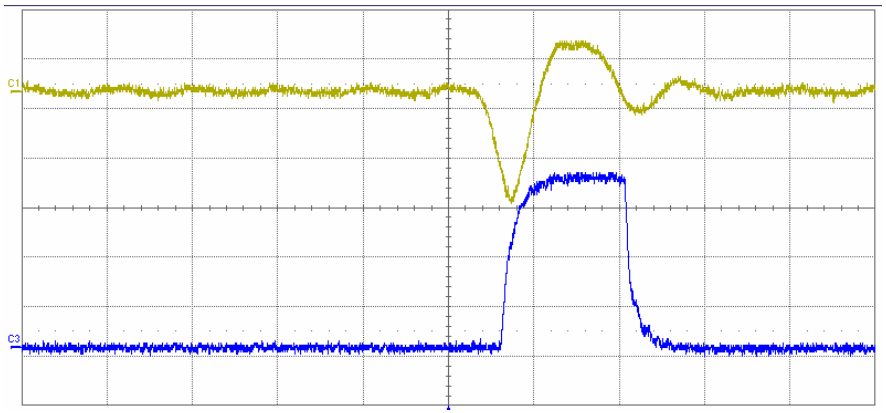
Preamplifier measurements

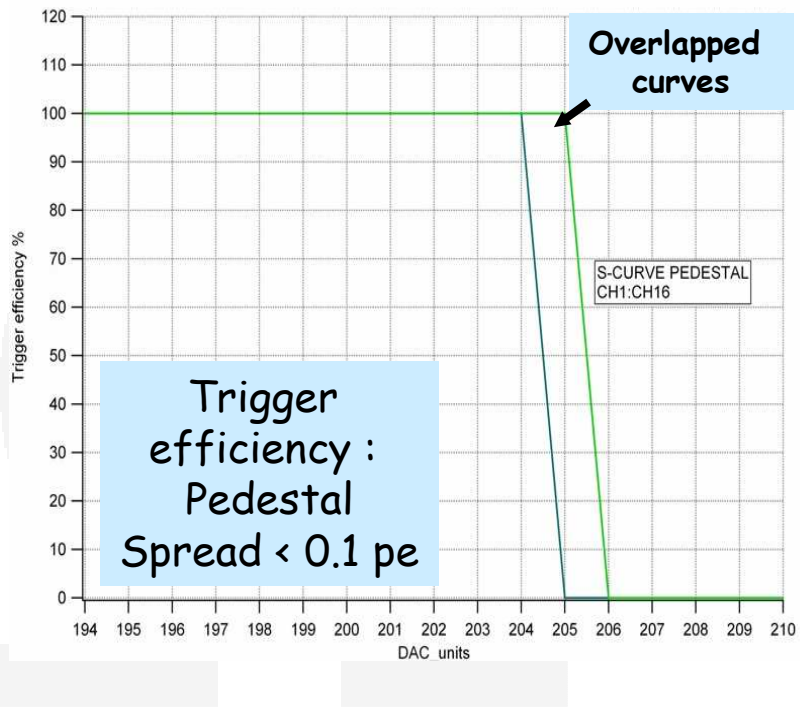
- Gain adjustment linearity : 2% on 8 bits

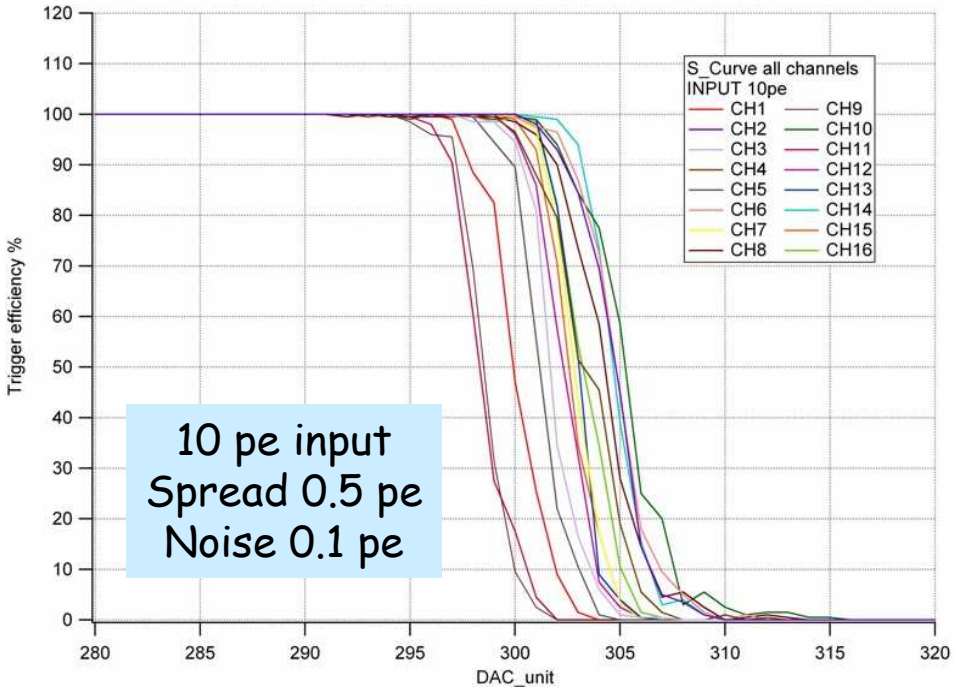


Fast shaper and discriminator

Fast shaper	G=8	G=14
Vout (1pe)	25 mV	35 mV
Rms noise	2.5 mV	2.5 mV
SNR	10	14
Rise time	7 ns	7 ns

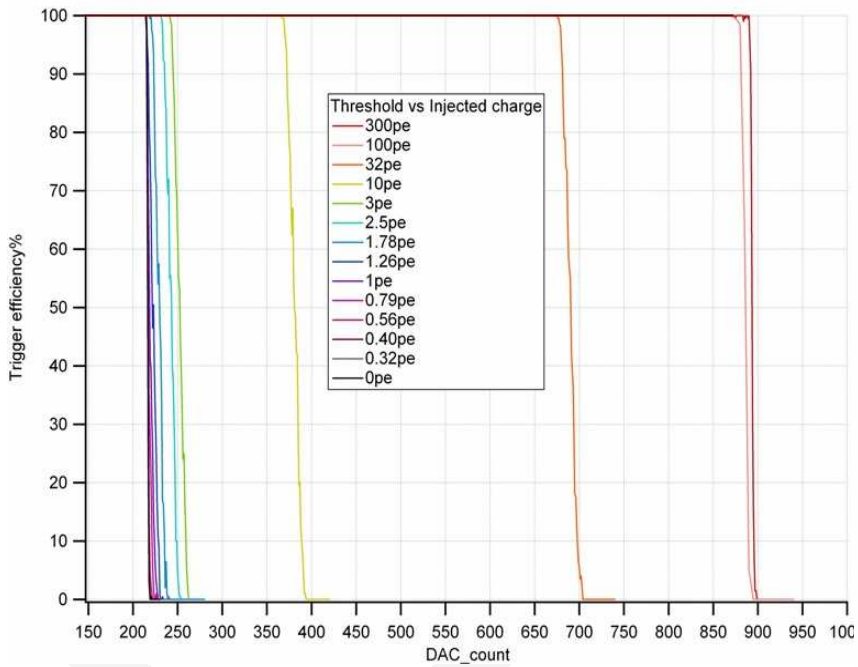


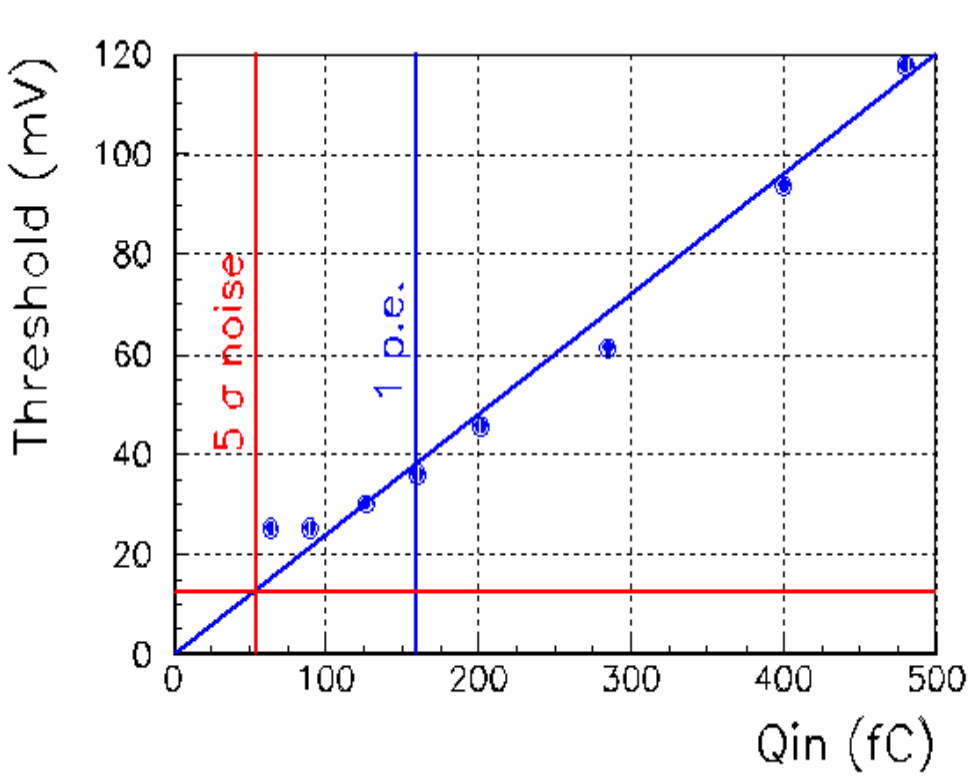




Trigger efficiency

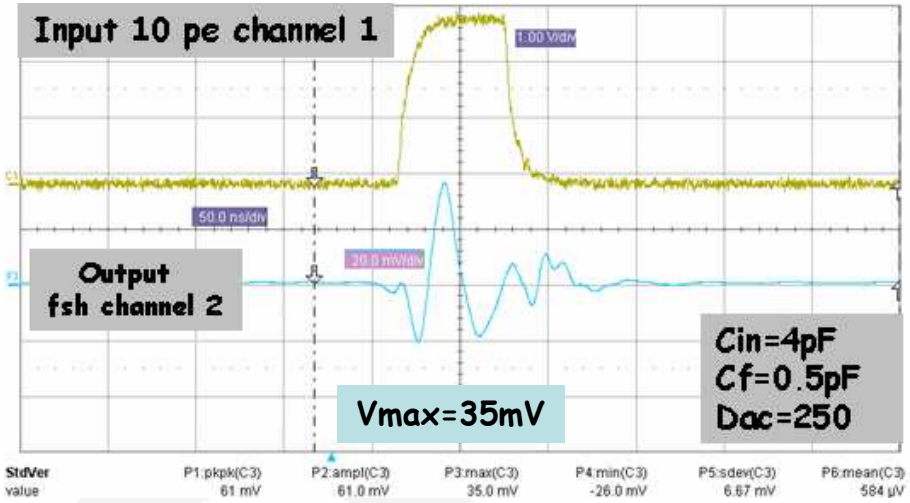
- Trigger down to 100 fC and up to 5 pC
- Noise ~10 fC
- Limited to ~10 σ noise due to discriminator coupling

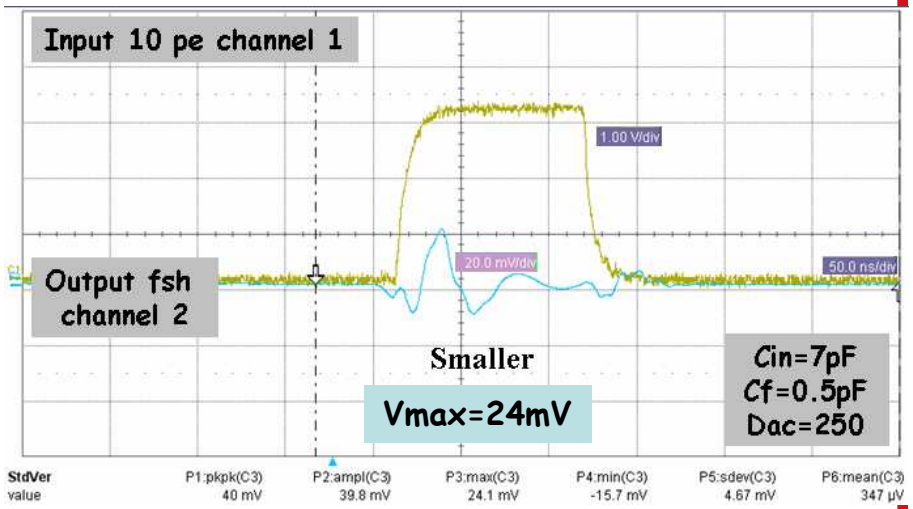


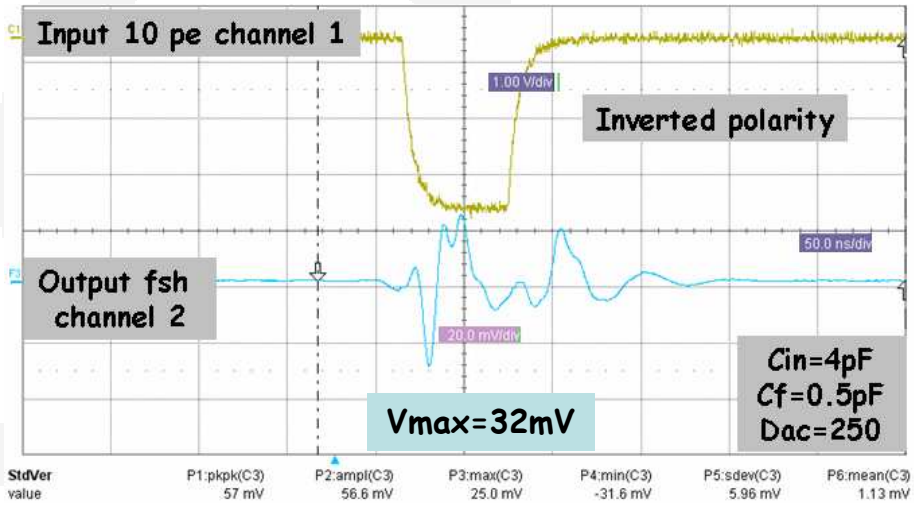


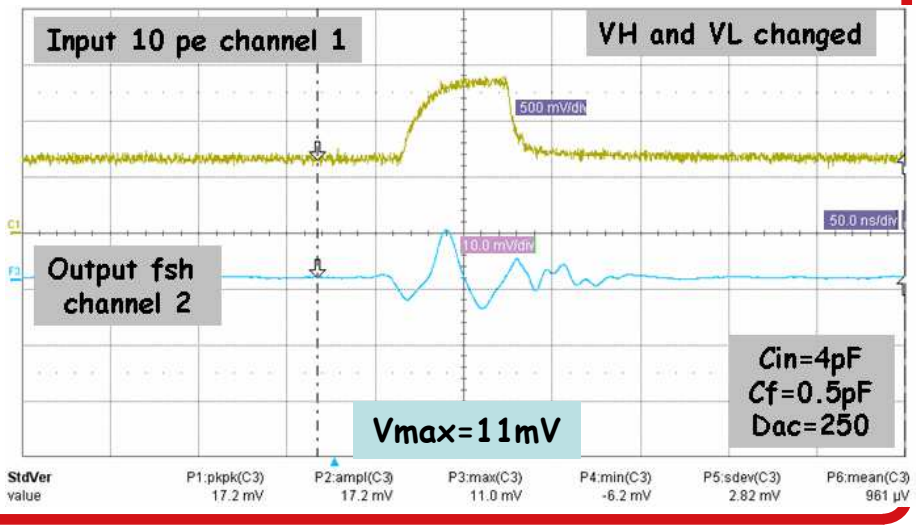
Discriminator coupling

- Coupling around 25 mV ⇔ 100 fC
  - Couples to the input through Vss or Vdd_pa





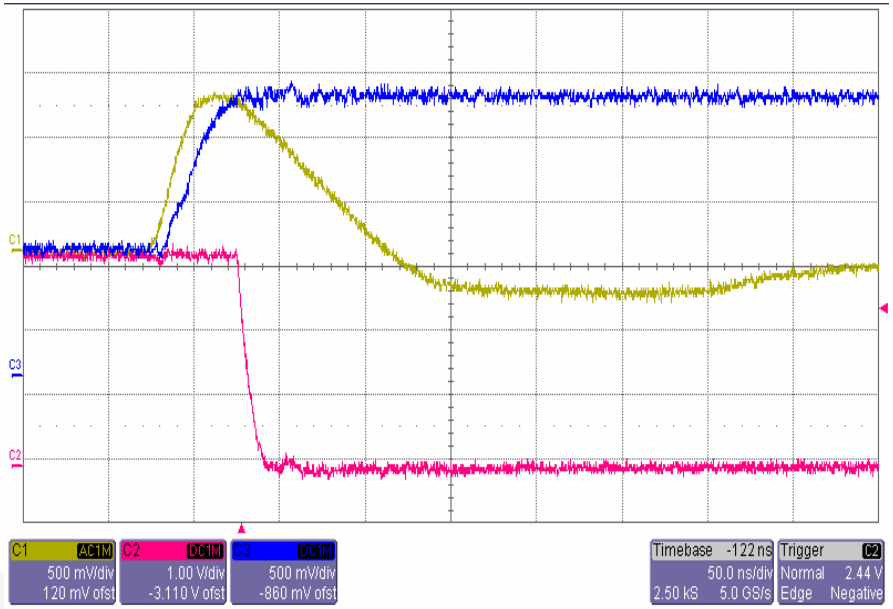


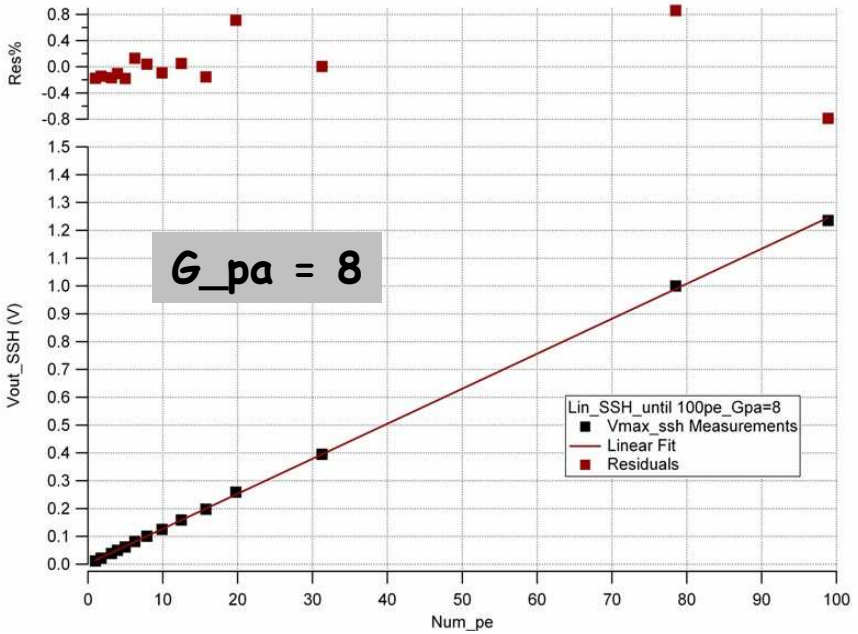


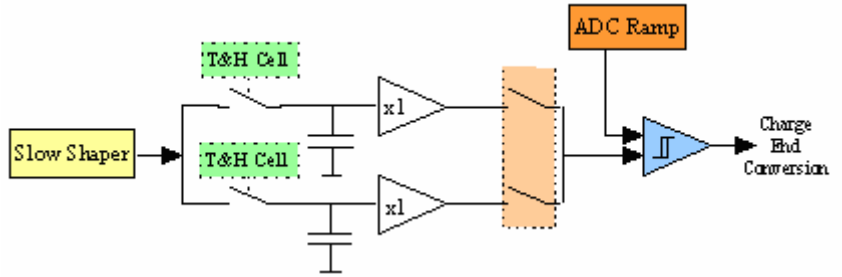
Slow shaper

Slow shaper	50ns	100ns
Vout (1pe)	21 mV	13 mV
Rms noise	3.3 mV	2.6 mV
SNR	6.4	5
Rise time	28 ns	50 ns

Low frequency to be understood and removed (power supply noise ?)



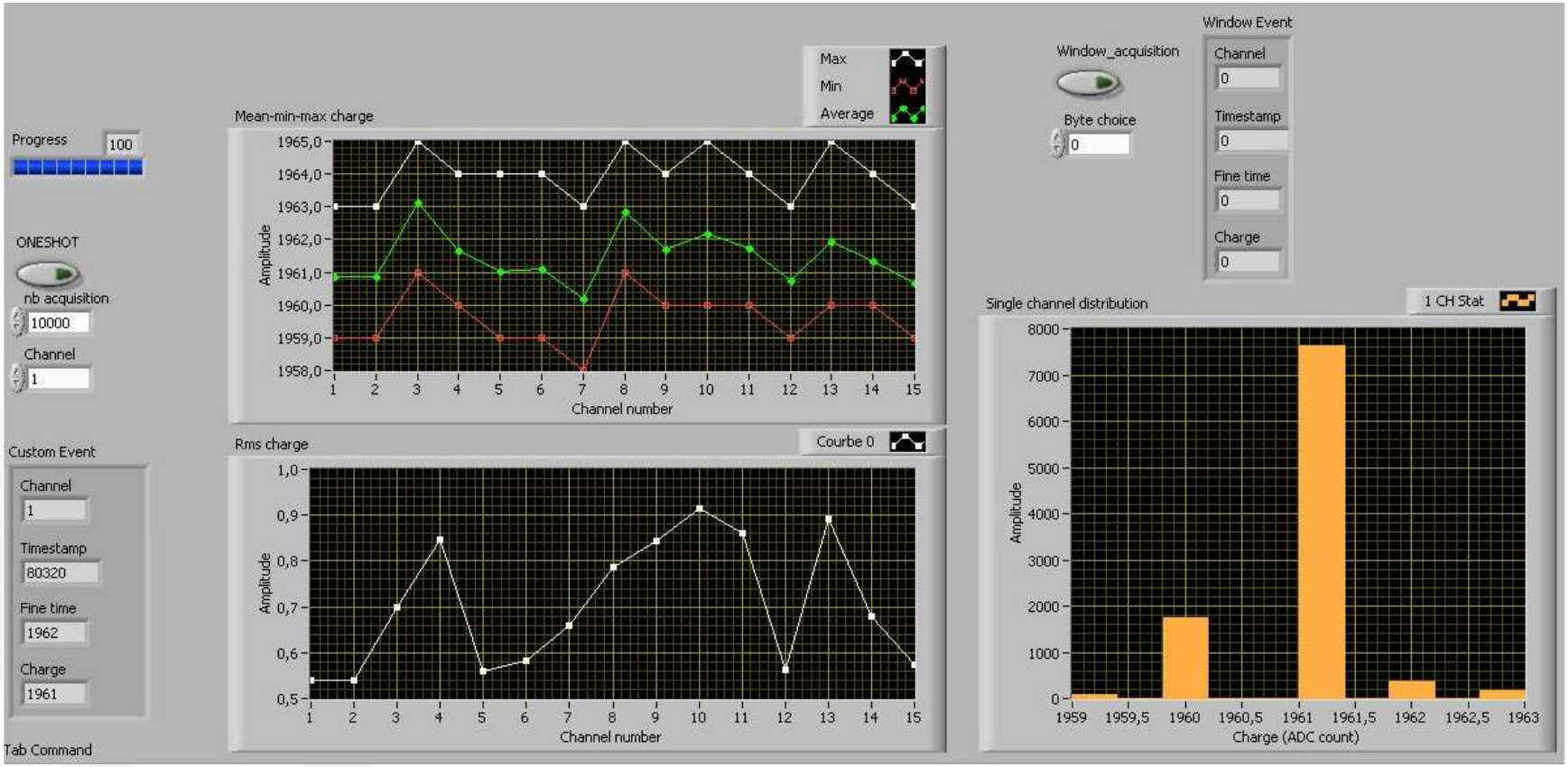




Internal 12bit Wilkinson ADC

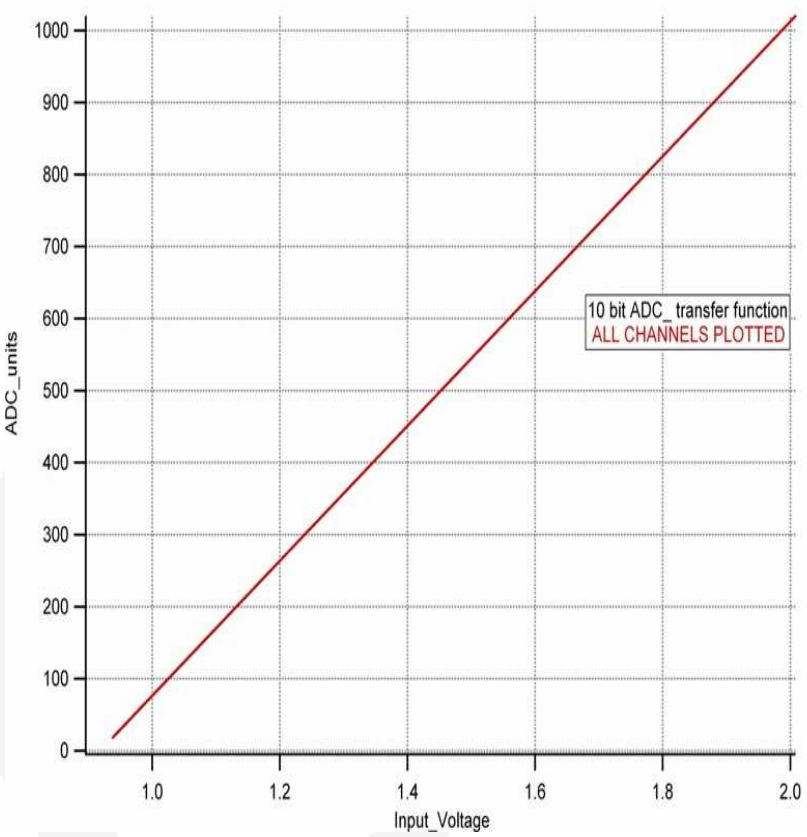
Input signal : DC = 1.4523V (middle scale)
Number of acquisitions: 10000 per channel

Mean : 1961
ADC_UNITS
with spread of 5 LSB

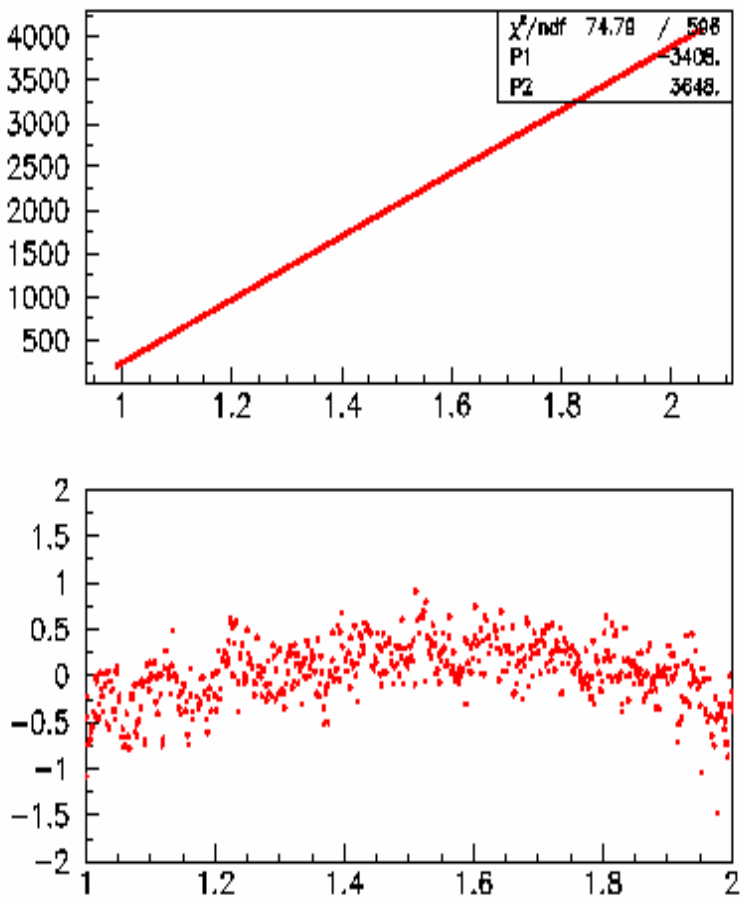


Internal Wilkinson ADC

- Wilkinson ADC well suited to multichannel conversion
- Very good uniformity and linearity



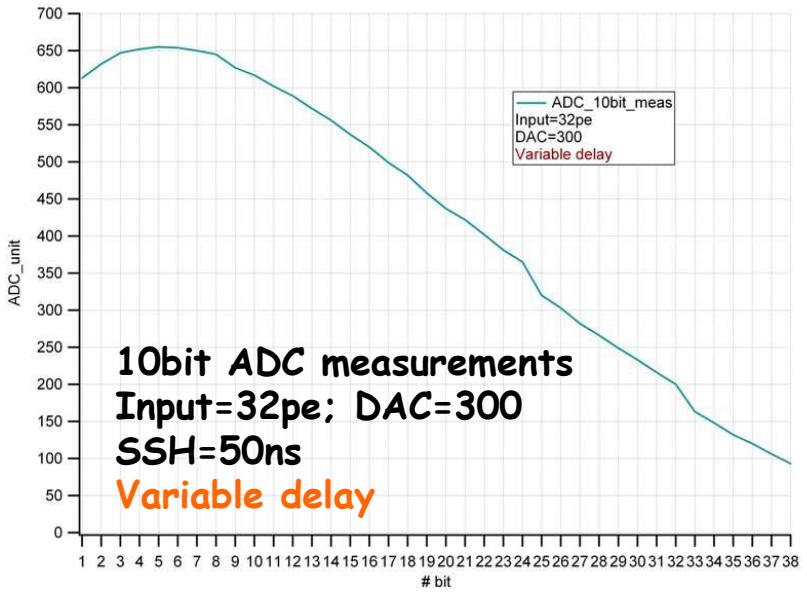
Uniformity of 10bit Wilkinson ADC
16 channels superimposed !

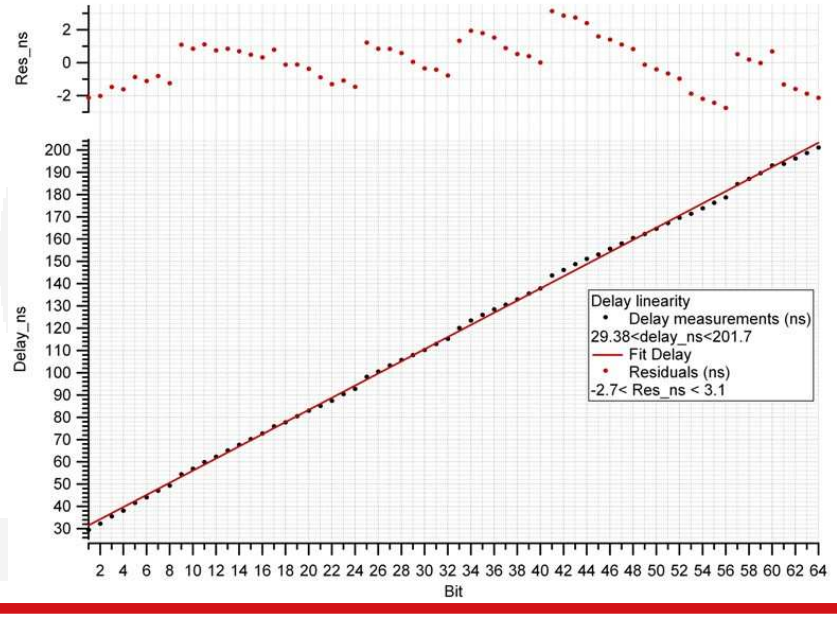


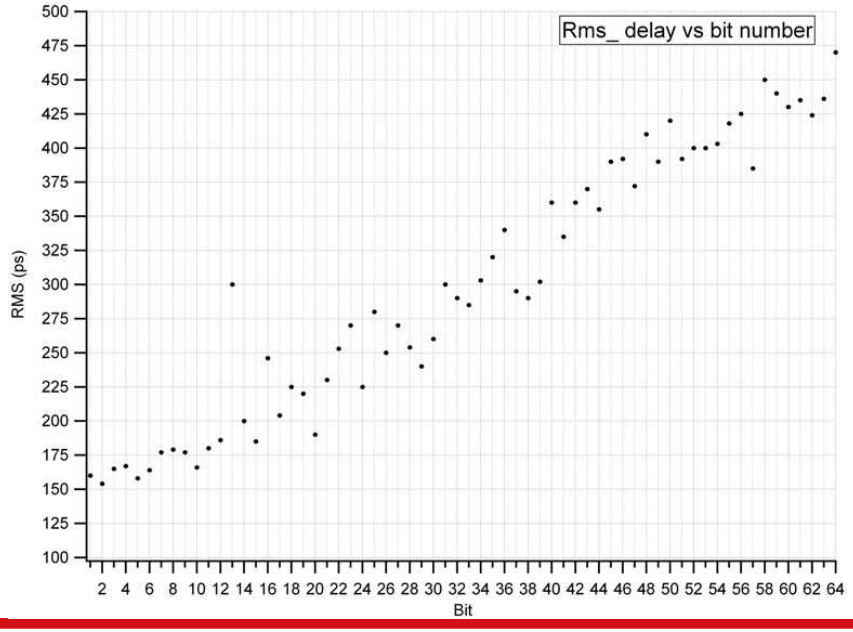
Linearity of 12bit Wilkinson ADC

Delay box measurement

- Delay box to hold peak
  - 6 bits,
  - Span : 30-200 ns
  - step : 3 ns
  - Linearity : 1%
  - Jitter 150-450 ps

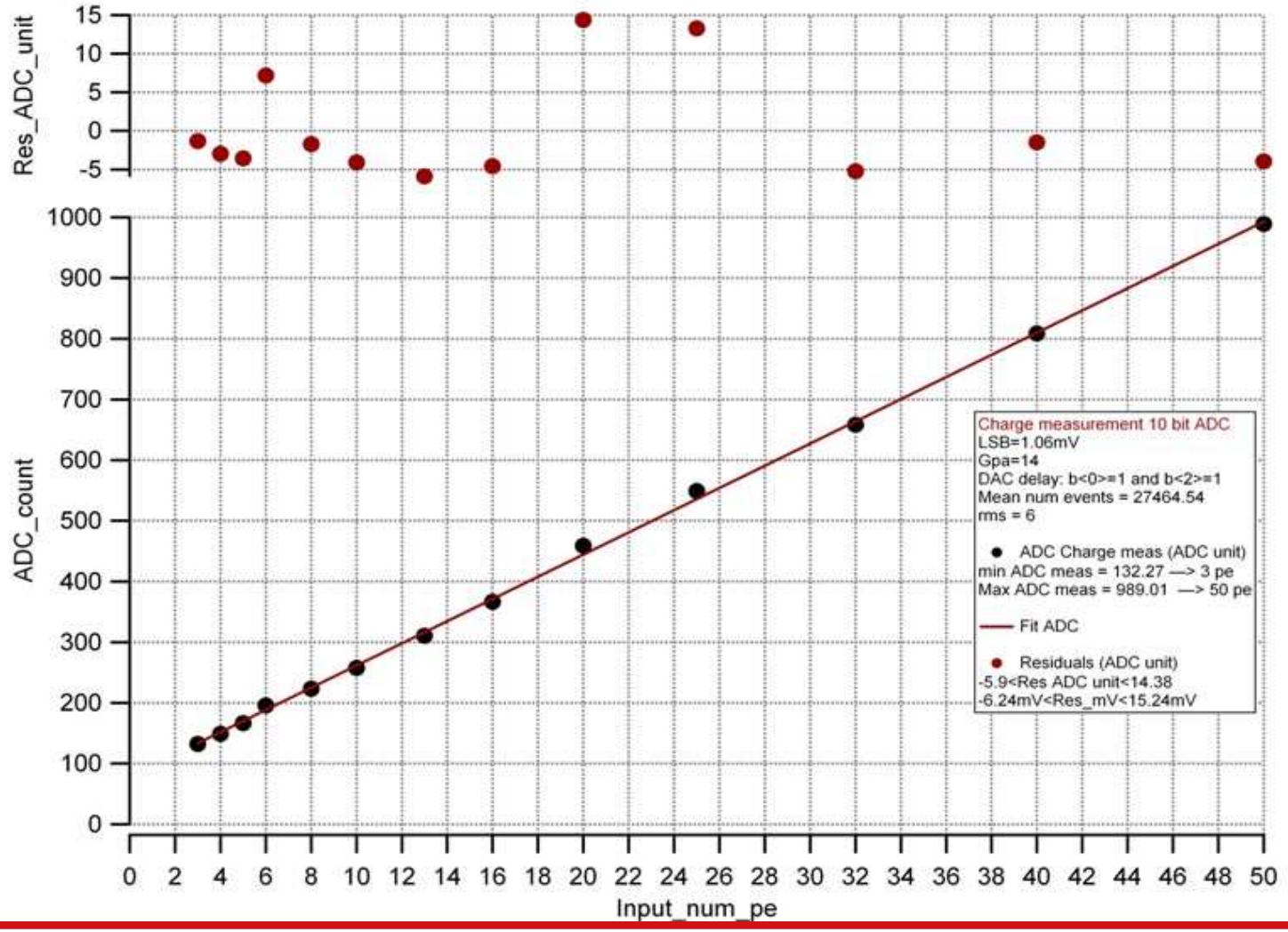






Overall behaviour in 10 bits

- Complete chain : autotrigger + T&H + internal ADC
- Linearity : 1%, noise 6 UADC



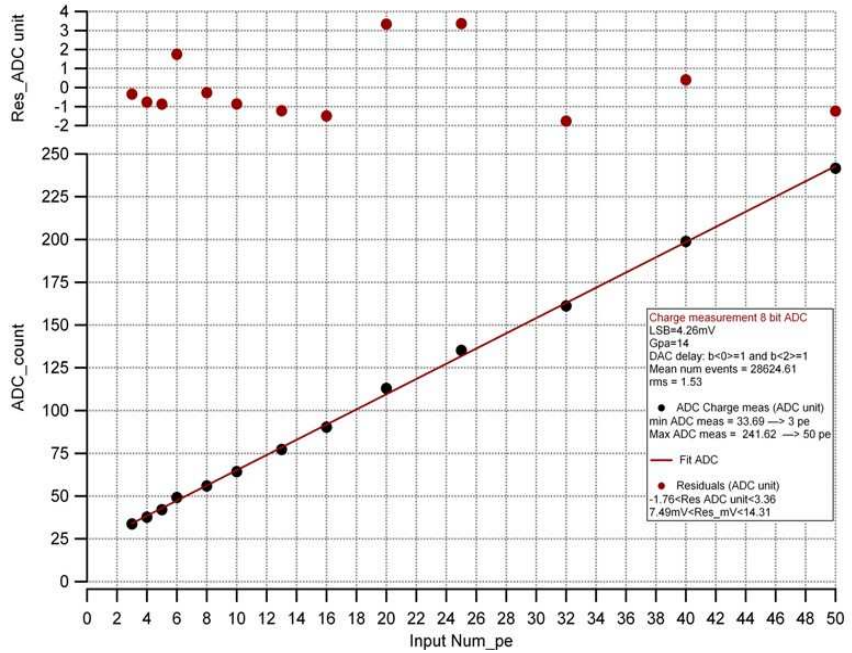
Overall behaviour

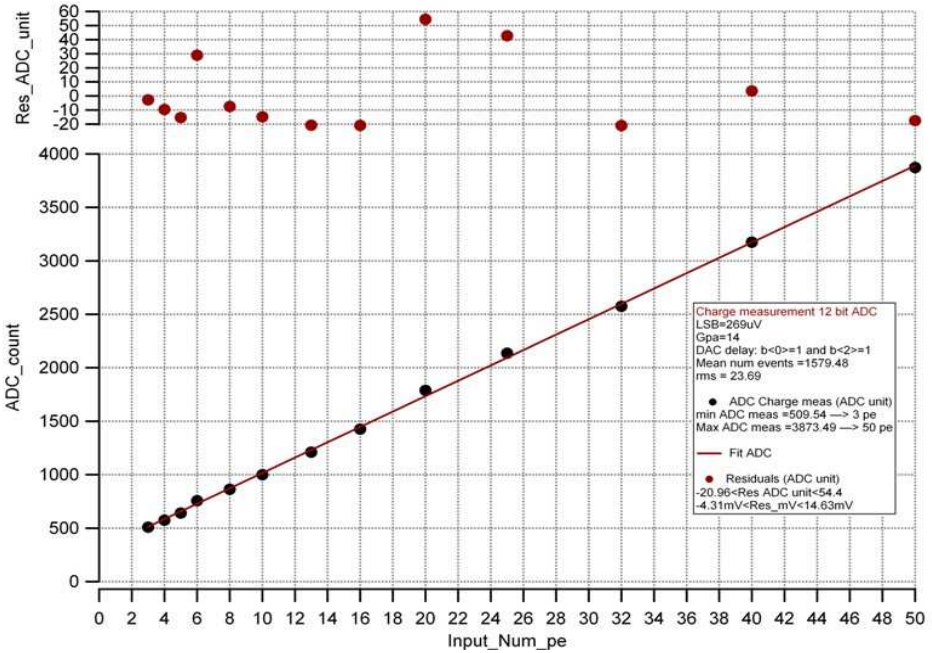
8 bit ADC

G_pa=14 (Cin=7pF , Cf=0.5pF)
Slow shaper=50ns
DAC_delay: bit<0>=1
bit<2>=1
LSB=4.26mV
Min ADC count=33 at 3 pe
Max ADC count=241 at 50pe
Residuals: from 2 to 3 ADC unit

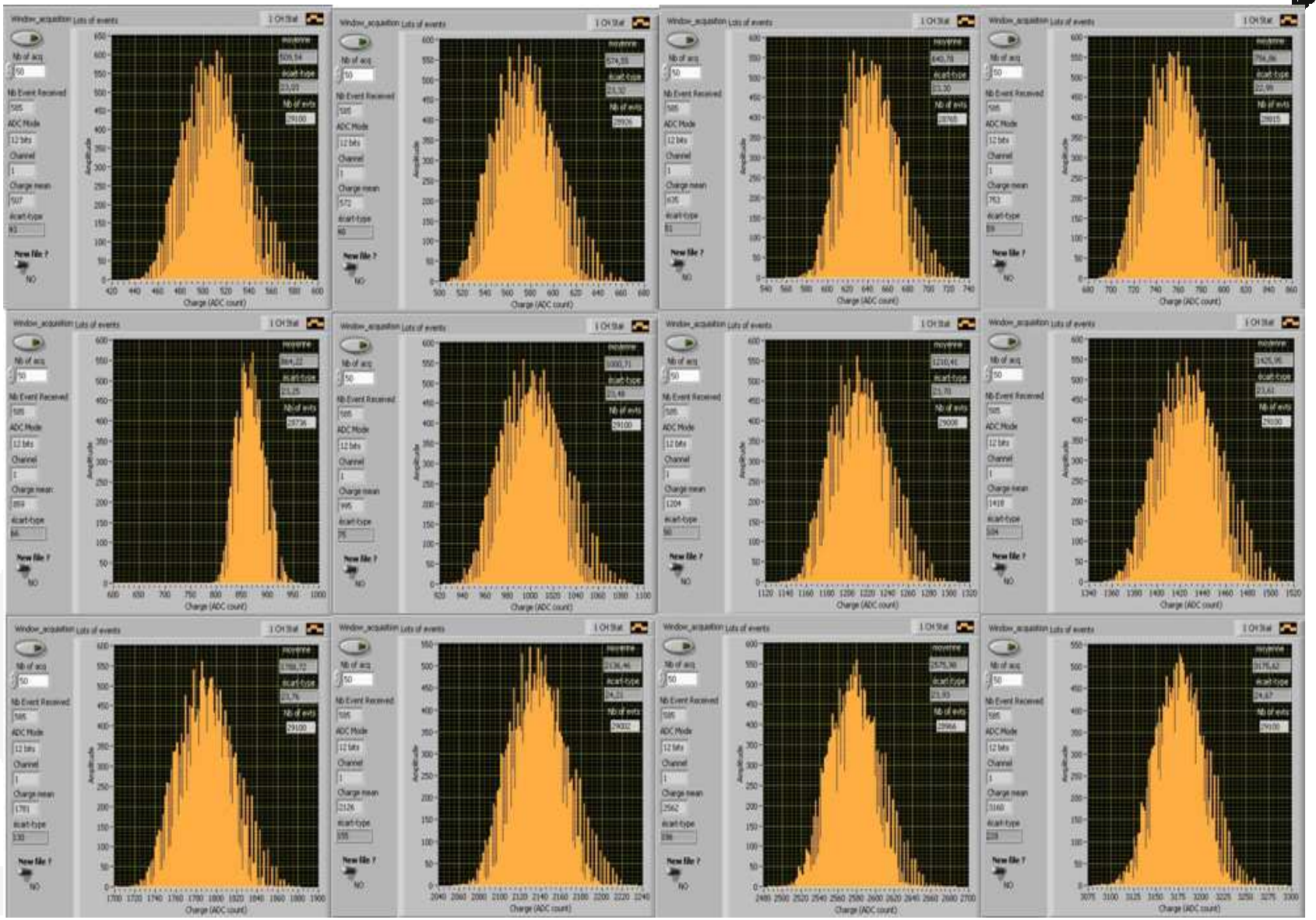
12 bit ADC

G_pa=14 (Cin=7pF , Cf=0.5pF)
Slow shaper=50ns
DAC_delay: bit<0>=1
bit<2>=1
LSB=269uV
Min ADC count=509 at 3 pe
Max ADC count=3873 at 50pe
Residuals: from 21 to 54 ADC unit





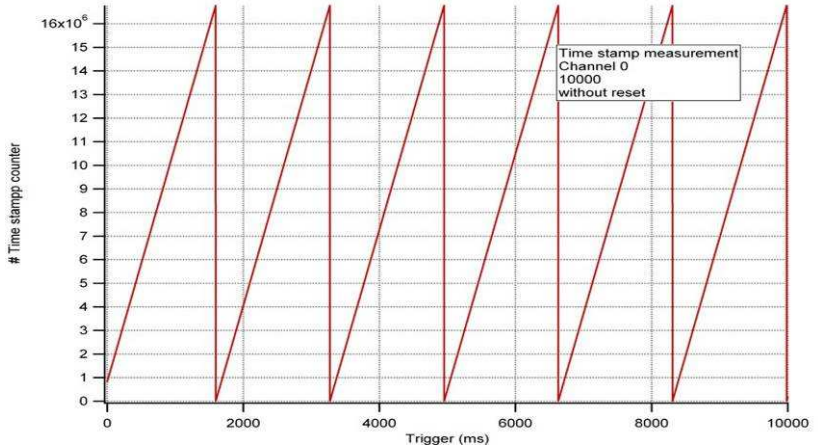
Overall behaviour



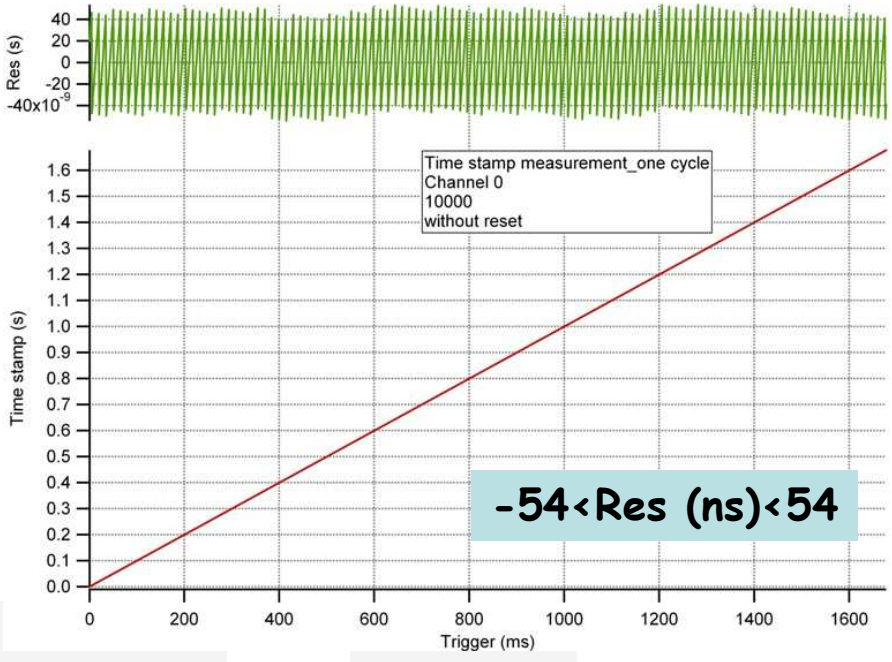
Time stamp measurement [E. Wanlin IPNO]

10000 events
Input signal=-20mv;
Rising edge 5ns;
Falling edge 5ns;
FWHM 8ns.
DAC=256
Cin=7pF

Time stamp_10000 events; without reset



Time stamp_10000 events; without reset; One cycle.

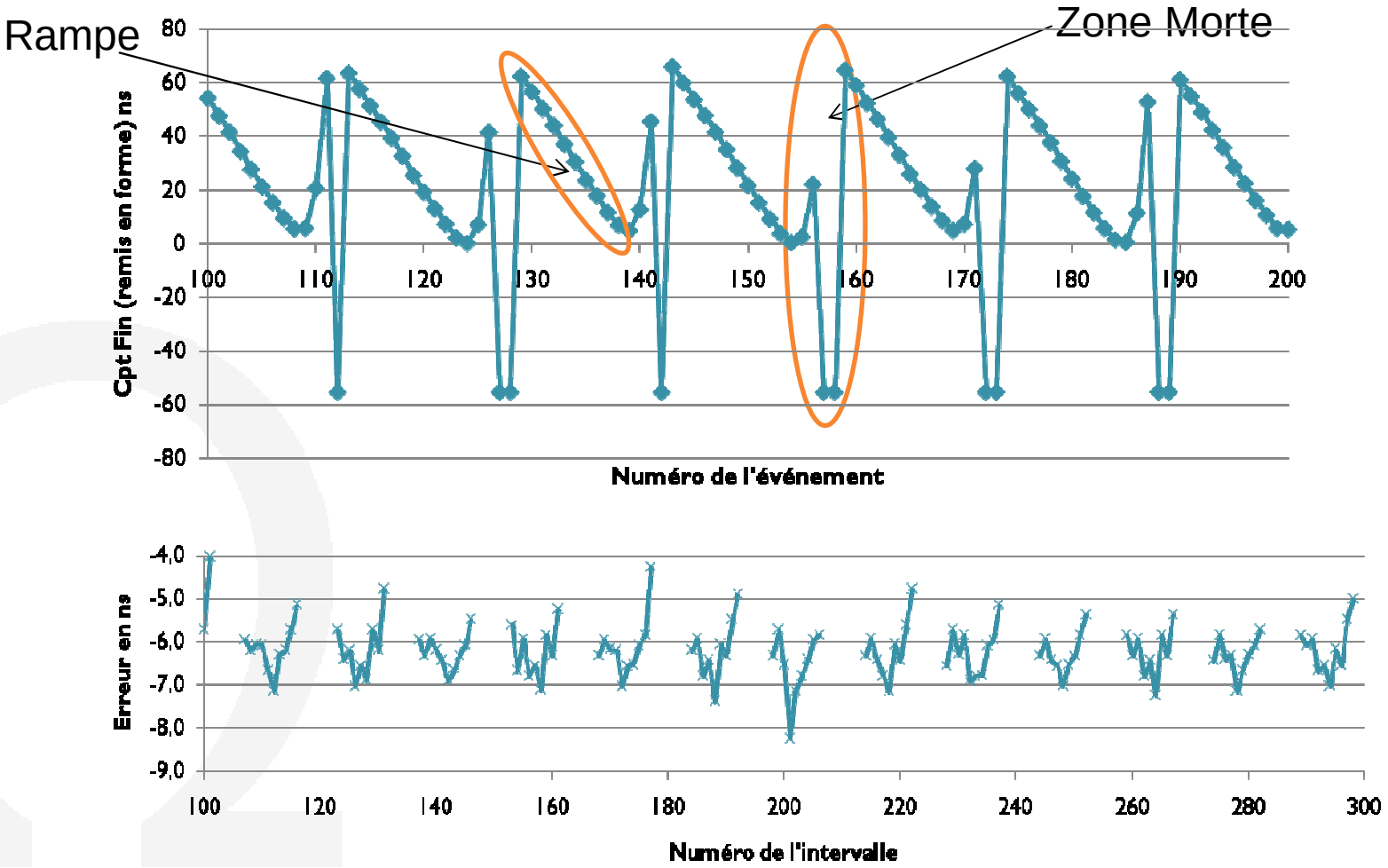


-54<Res (ns)<54

Fine TDC measurement

[S. Drouet IPNO]

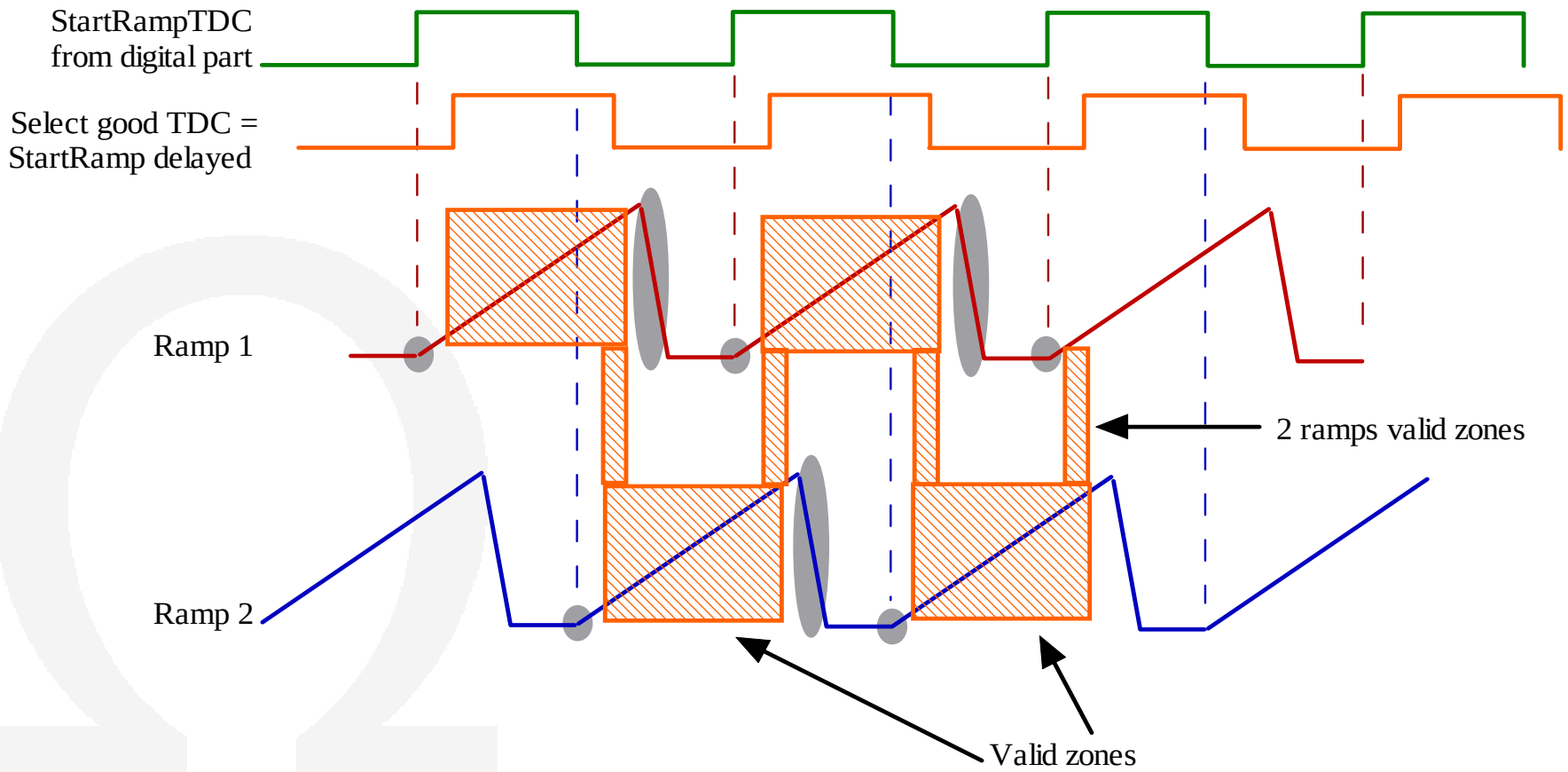
- Fine time digital data output
- Rms of clean part : rms = 0.62 ns



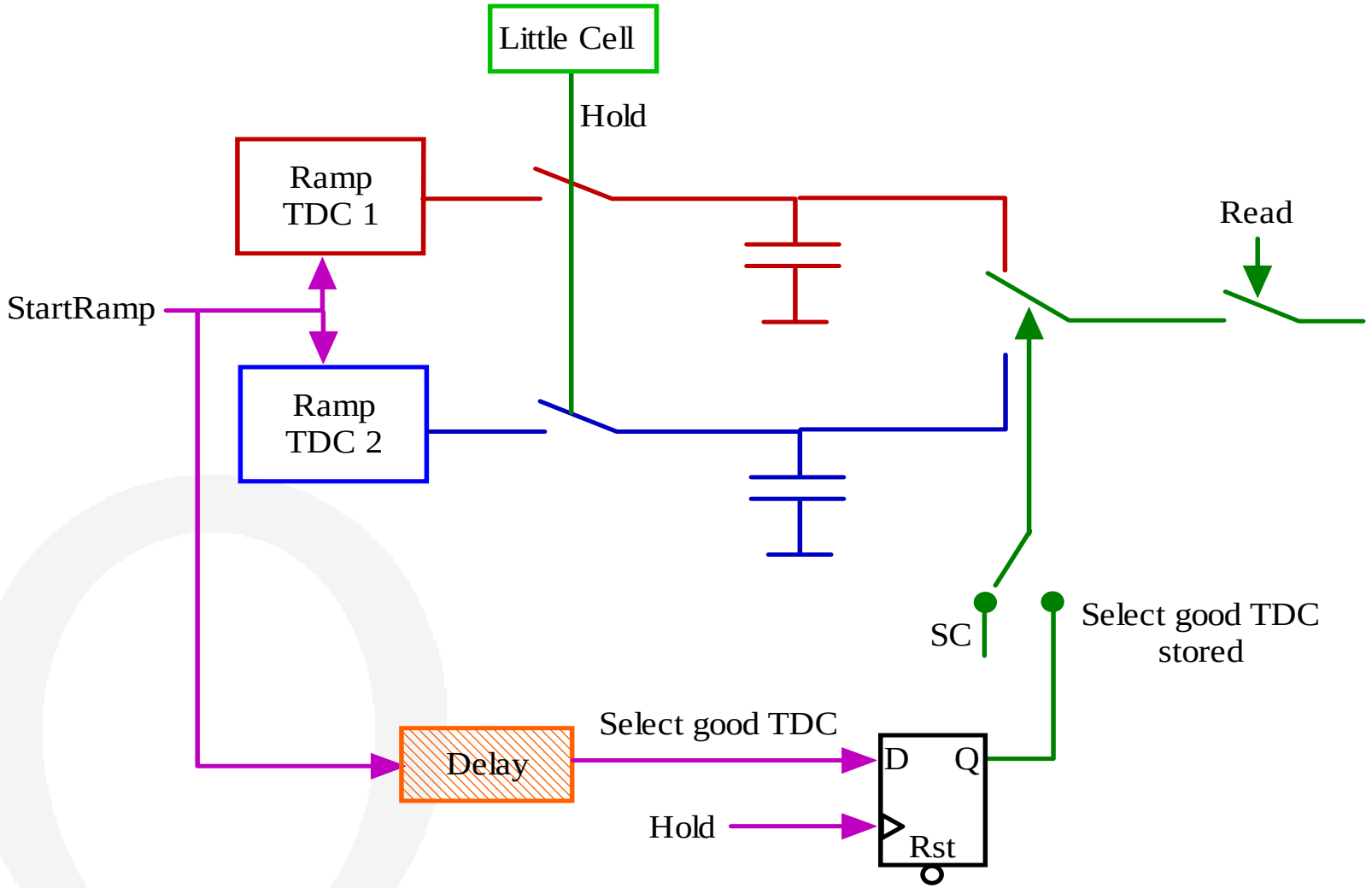
Sébastien DROUET – drouet@lpsc.in2p3.fr

Fine time: two ramps scheme

- 2 separate ramps to avoid glithces
- Need to have a signal to inform which TDC is active and linear. This signal will be sample during “Hold” of TDC (asynchronously) => need overlap to solve metastability.

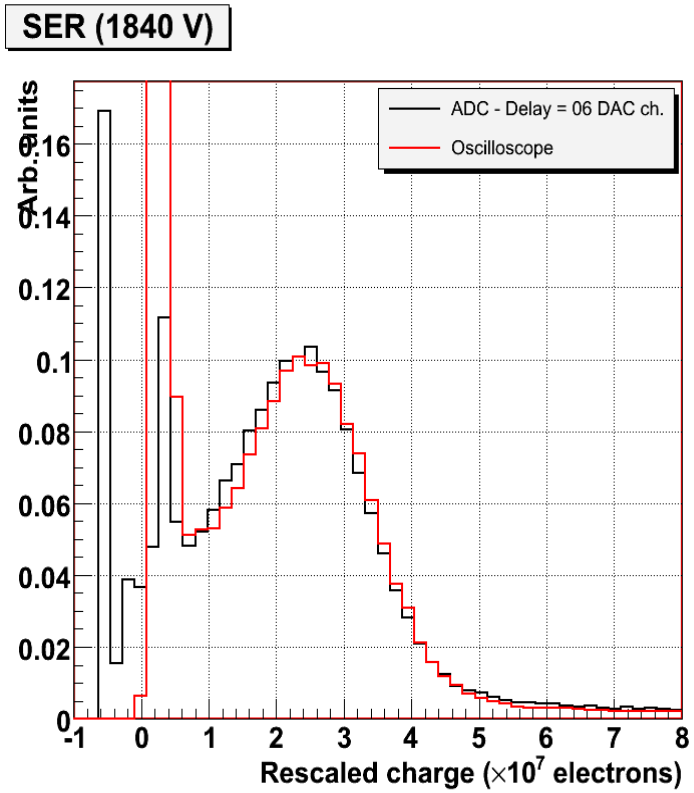


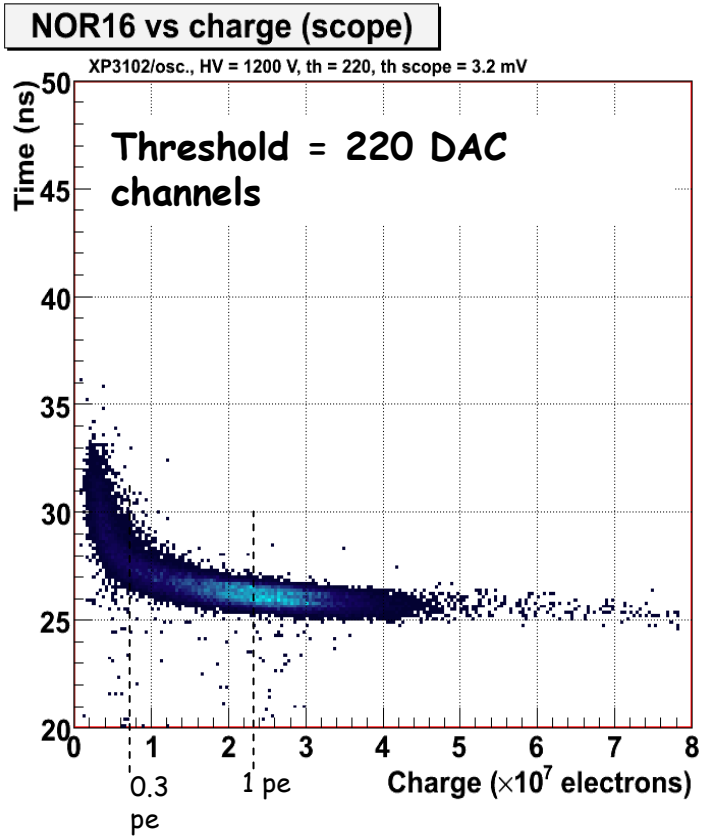
Fine time: Result…



Measurement with PMT [B. Genolini IPNO]

- SPE spectrum with 10’’ PMT X
  - Complete chain : autotrigger + 10bit internal ADC
- Time measurment with 2’’ PMT (XP3102)
  - Trigger output jitter : 600 ps





Conclusion and next steps

- Good overall performance of PARISROC
  - Autotrigger and internal digitization
  - Good operation with PMT
  - Demonstrator being built in Orsay for tests with detector
  - Complex chip => long measurements
- A second version will be done in sept 09
  - Possible PM gain increase
  - reduce dead time for Water Cerenkov needs : 8-9 bits ADC
  - Increase dynamic range with 2 gains 8-9-10 bits
  - Double fine TAC and reduce clock noise
- Chip being evaluated by several experiments : Megaton, DUSEL, LHASSO…