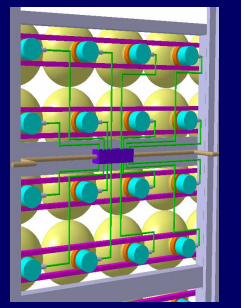
Status Report

ANR-06-BLAN-0186 (LAL, IPNO, LAPP and Photonis)

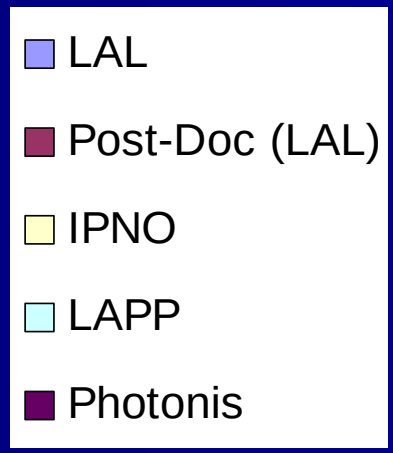
J.E Campagne project leader

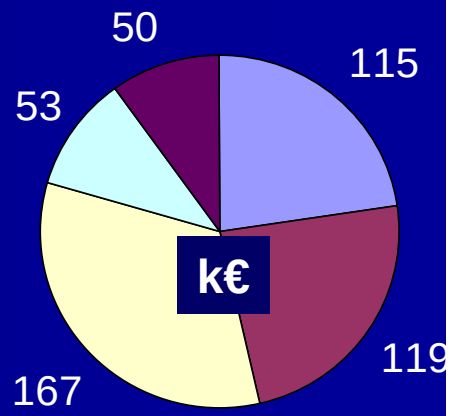
PMm^2 ANR (2007-2009)



- LAL: front end electronics + water tight box
- IPNO: photodetector tests + mechanics + integrated electronic board
- LAPP: Data network (electronics + cables + protocol)
- ~~Photonis~~: PMTs provider

Funded 500k€/3yrs (1 post-doc included) designed to involve 5FTE Engineers
And in fact ~20p participate to our "monthly" meeting.





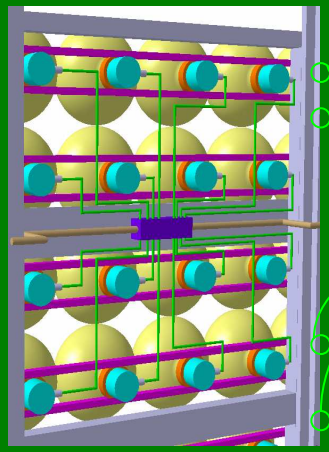
Recently ULB Bruxells (K. Hanson) has joined for DAQ

Concept: digitize everything!

(supported by low energy physics)

10bars water pressure

IPNO & Photonis



16

2m x 2m
12'' PMs

LAL & IPNO

Triggerless Front-End from preamp. to Q & T digitization

FPGA

Common HV

Integration Board

LAPP

100ml cable power + data

ULB

TCP/IP

µControler

FPGA

Power + Decoding Board

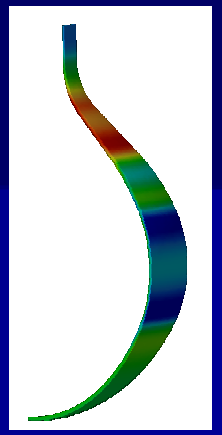
LAPP

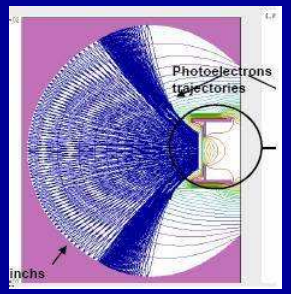
Size: manageable 12'' PMs: no manual operation for large production, better ratio cost/QExCE

Photodetector

IPNO shape and glass thickness computation to subtend 10 bars

Photonis Electrostatic and realisation of 9 pieces (Sept. 08)





First measurements:

- Photocathode:
  - uniformity quite good
  - Skcb=10.5µA/lmF (with corning blue filter)
  - Skb=77µA/lm (with white source)
  - ~24% at peak => reasonable for first attempt

  (nb: 8" XP1886 new process bialkali super² gives 36% at peak)
- Gain:
  - 10^5 @ 2kV => low value compared to expectation 10^6 (8 stages)
  - Redesign of the first dynode

Potting tested

PHOTONIS had halt the PM activity March 09

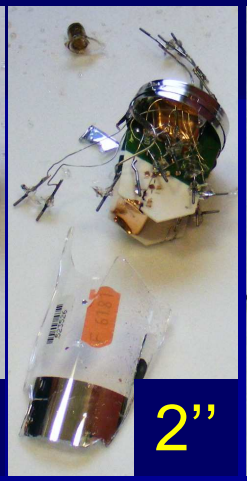
IPNO

High pressure tests

BNL tank (150b)

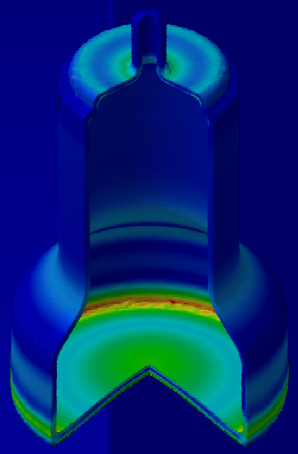
Mid-Feb 09

3,2 atm



6,5 atm

16,3 atm



Preliminary comparison simulation/measurements indicates

Beaking limit of glass : 40 - 50 MPa

In agreement with glass properties given by Manufacturer. This is a good news to design a 12'' shape and choose glass thickness to subtend 10 atm. (first test with 12'' end march 09')

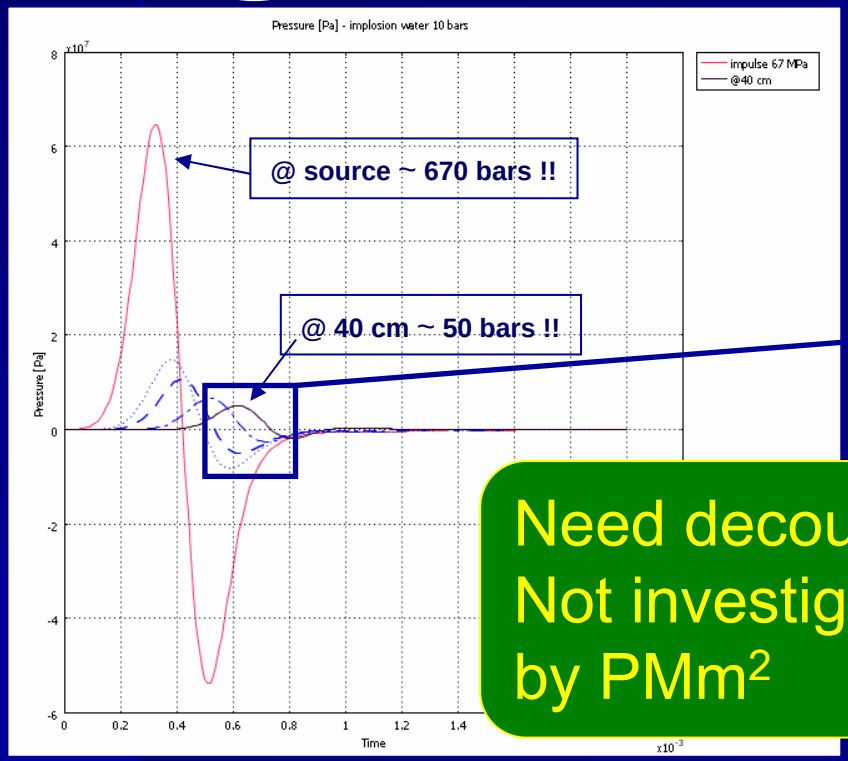
8'' XP18060 for Daya Bay (reinforced) does not break at 10 atm

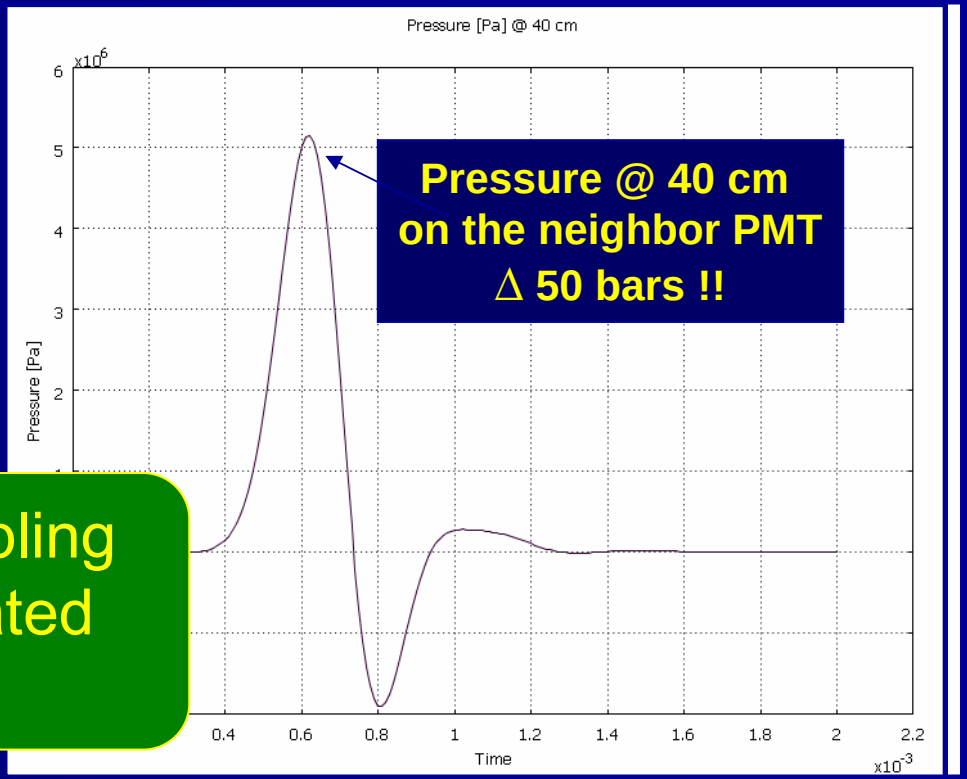
IPNO

Implosion simulation

12”:31cm

CONSOL software
+
Semi-analytical approach
Preliminary validated with exp. data





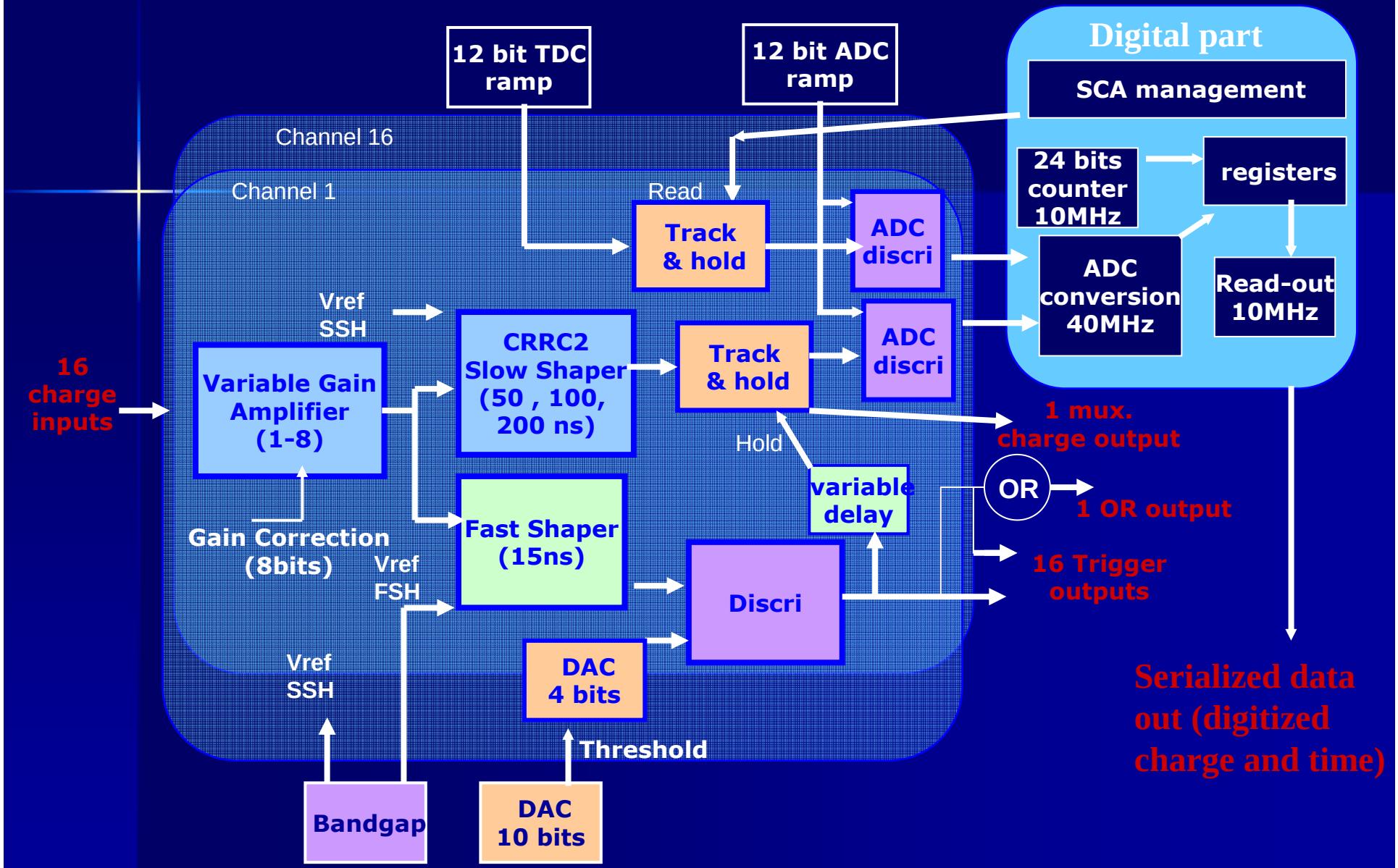
Need decoupling
Not investigated
by PMm²

PARISROC

- **Target features:**
  - **16 independent channels**
  - **Variable gain to allow single HV for all PMs**
  - **1/3pe 100% efficiency**
  - **Triggerless**
  - **1ns time resolution**
  - **Scalability**
  - **Low cost**

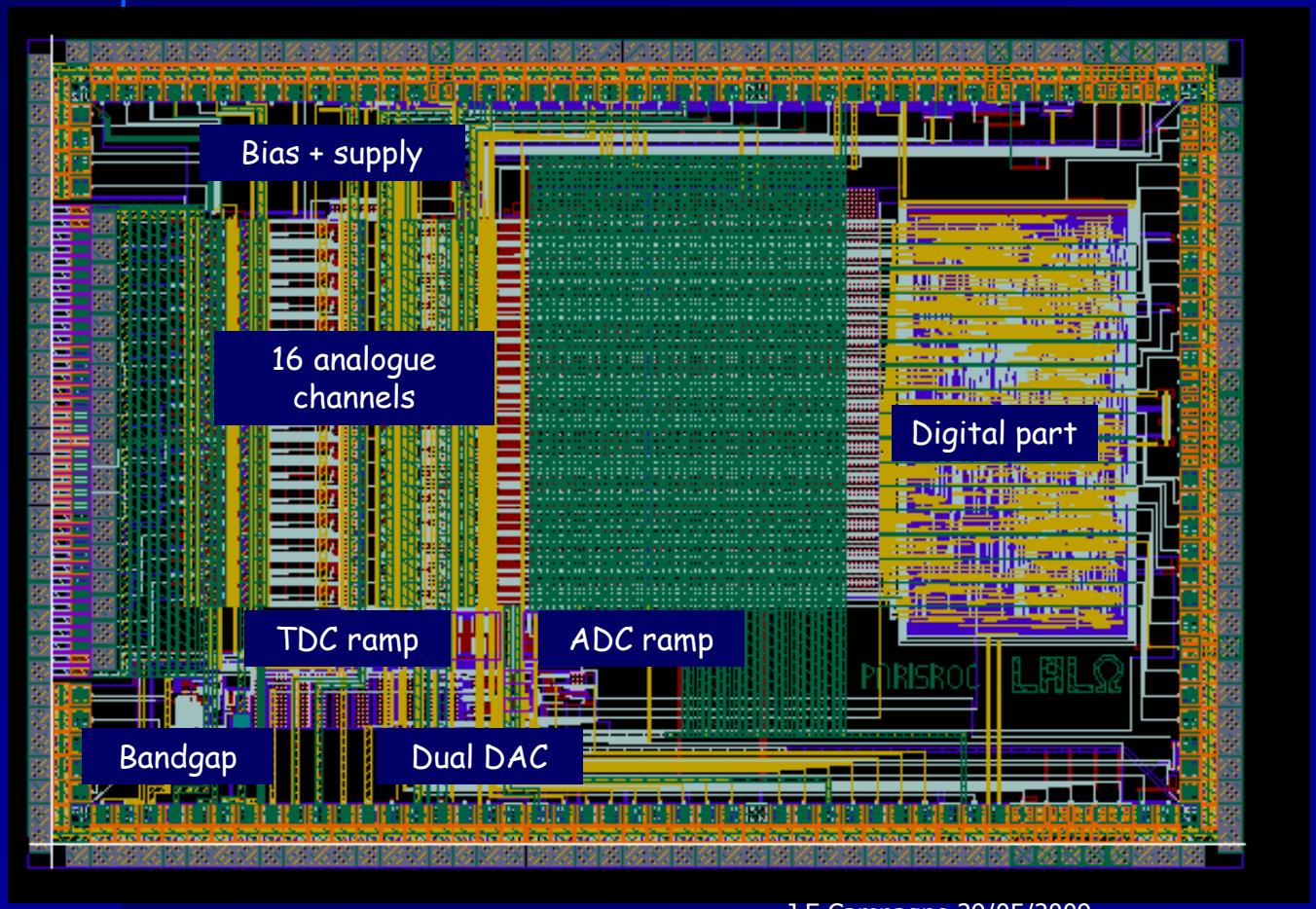
PArISROC v1 architecture

LAL



LAL

PARISROC v1



Submitted July 08

Technology :

AMS SiGe 0.35µm

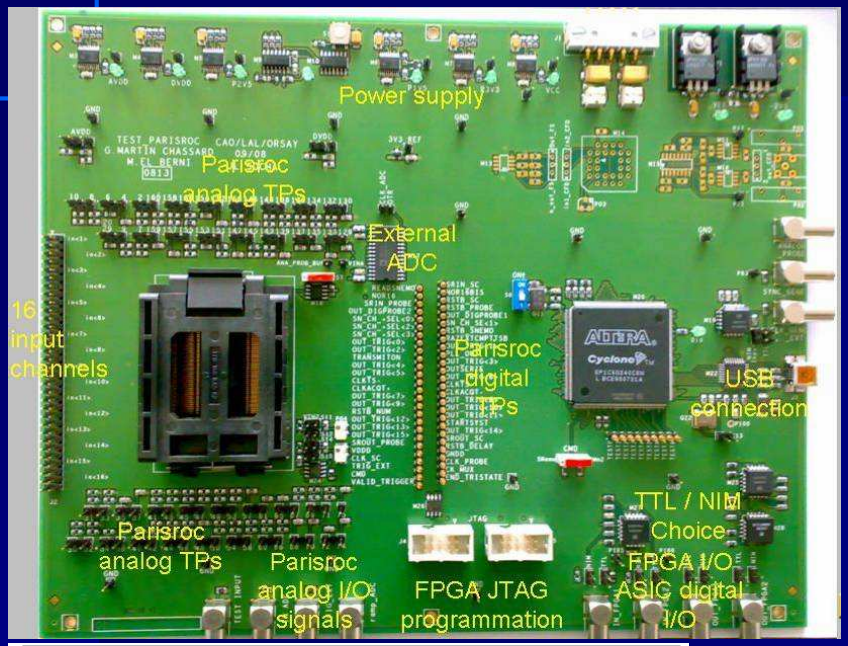
Size :

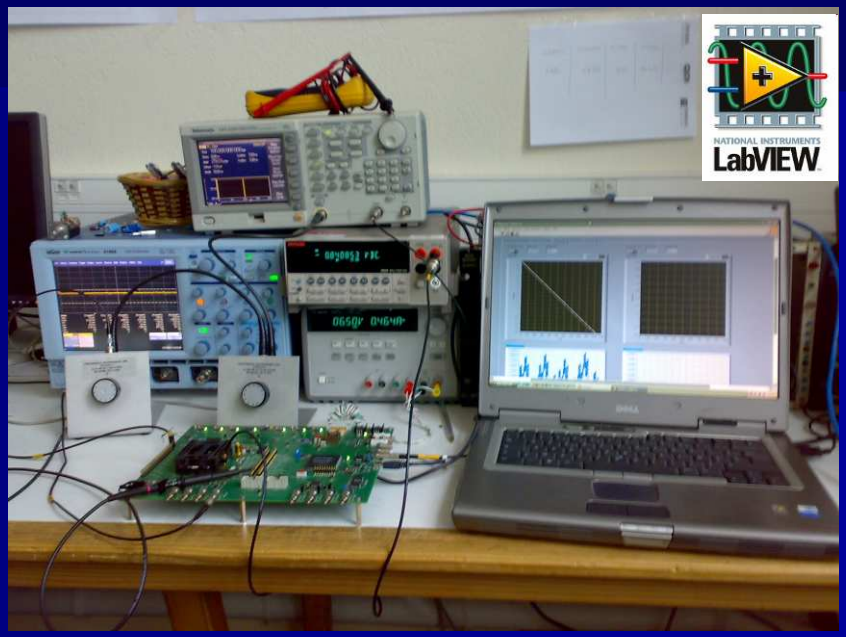
5mm X 3.4mm

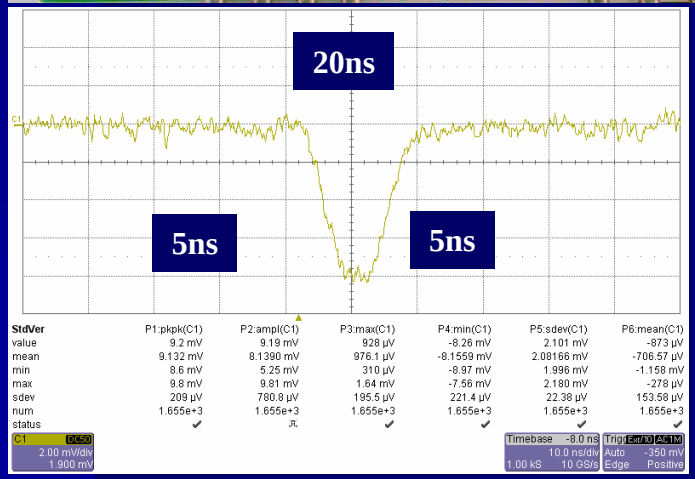
Package :

CQFP160

Measurements







Start Dec 08'

- input signal : *Ii= 0 to 5mA*
- 0 to 300 pe -> 0 to 50 pC
- PM's Gain =10^6 (1pe=160 fC)

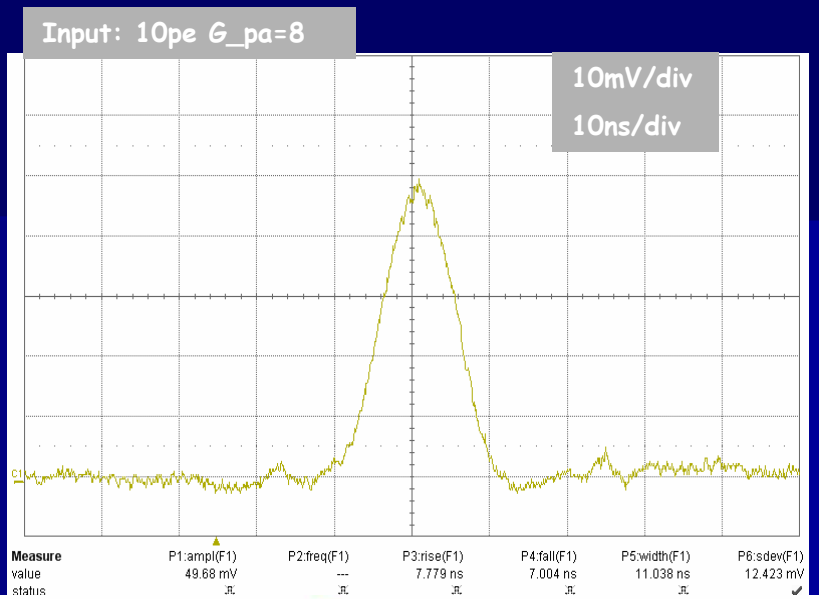
default value to present the results

Preamplifier measurements

LAL

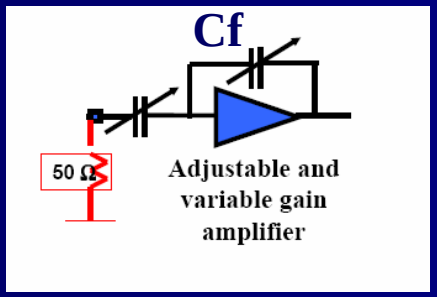
Preamp	meas	sim
Vout(1pe)	5 mV	5.2 mV
Rms noise	1 mV	316 µV
Noise in pe	0.2	0.06
SNR	5	16

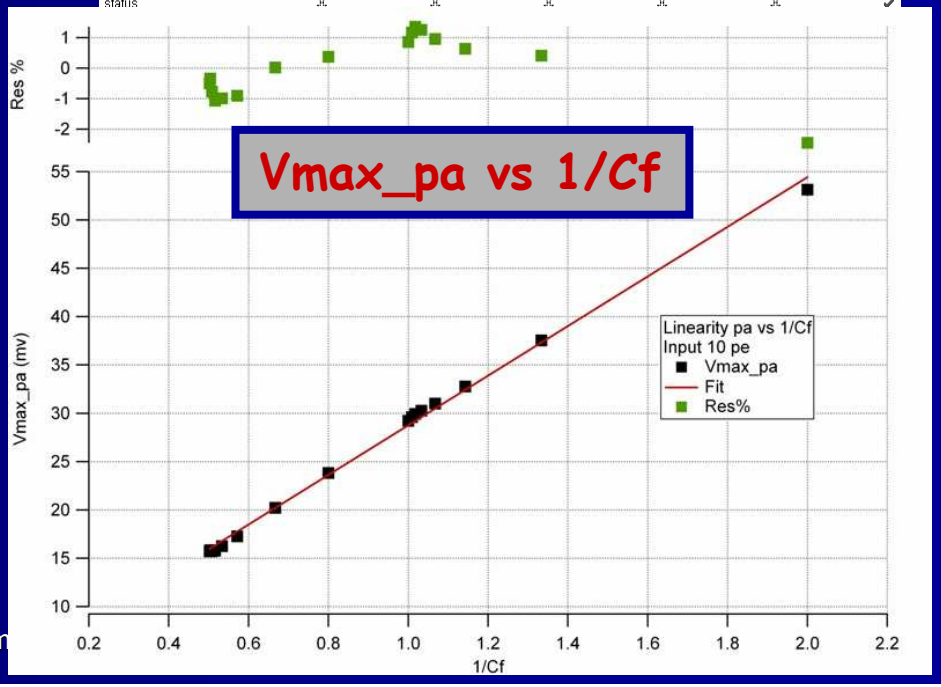
Some clock noise and low frequency noise under investigation



Gain adjustment linearity :

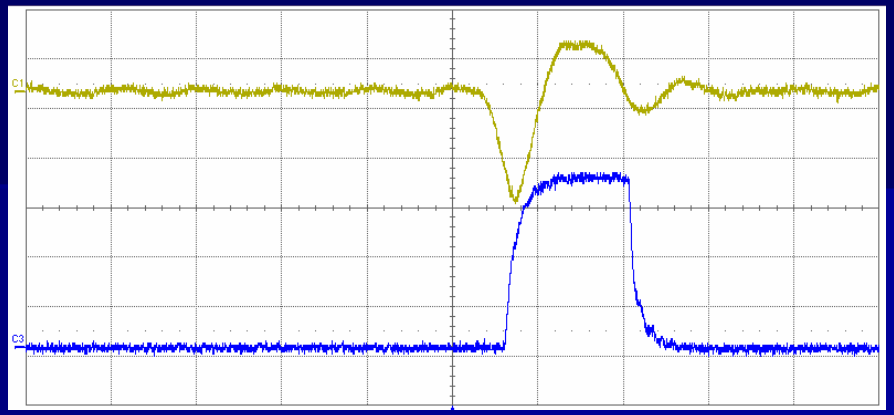
- Vout/vin = Cin/Cf
- 8 bits range
- 2% non linearity

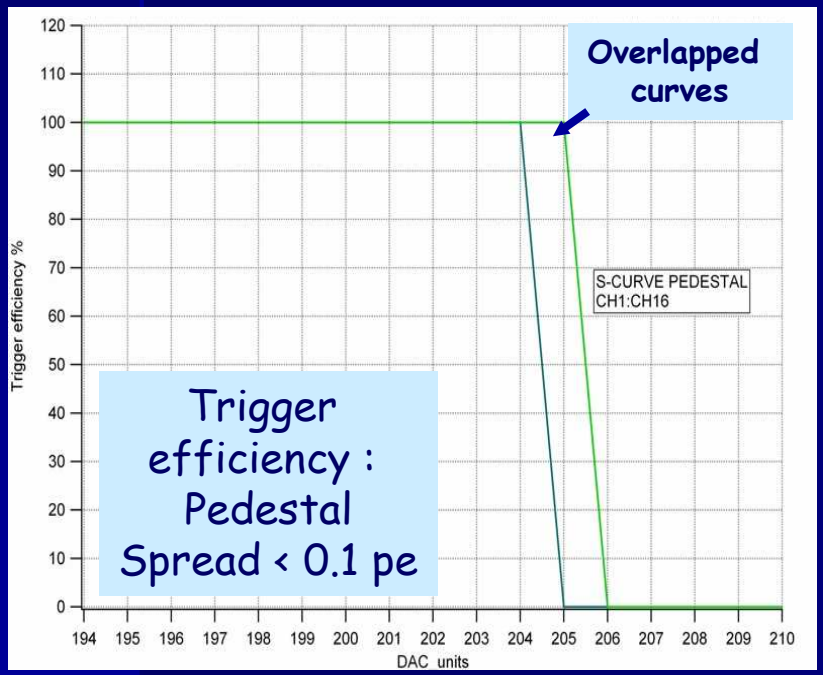


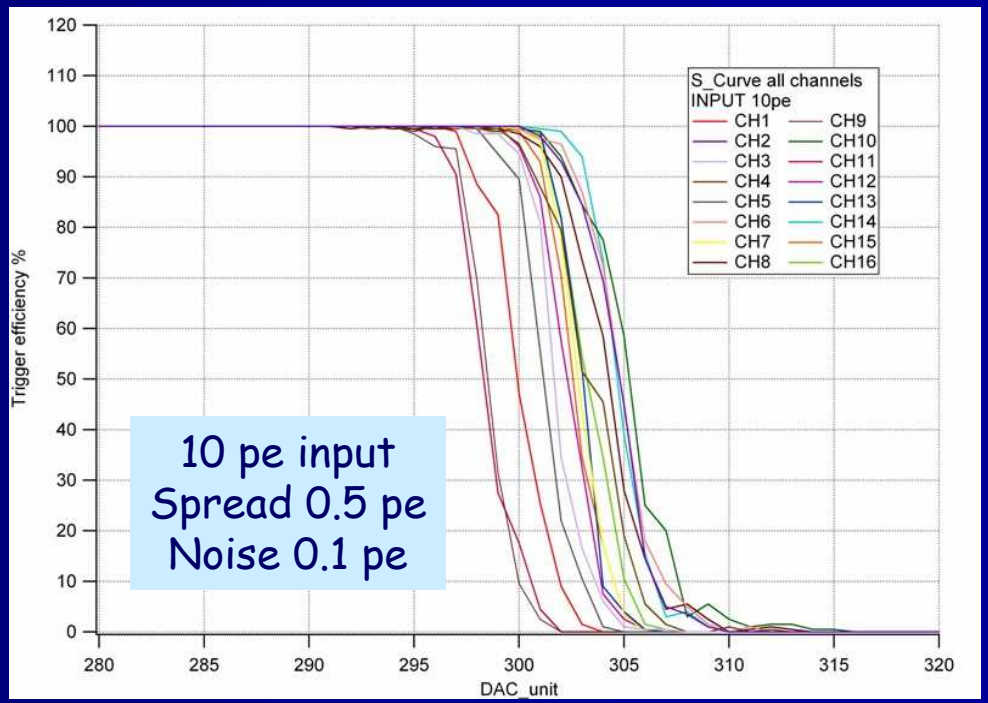


Fast shaper & discriminator LAL

Fast shaper	meas	sim
Vout (1pe)	30 mV	37 mV
Rms noise	2.5 mV	2 mV
SNR	12	16
Rise time	7 ns	5 ns





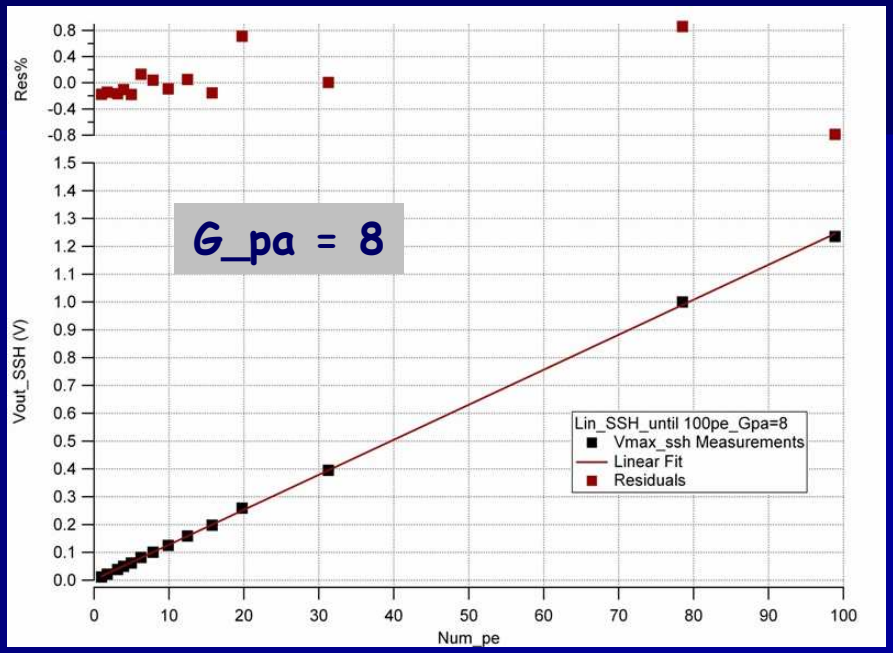


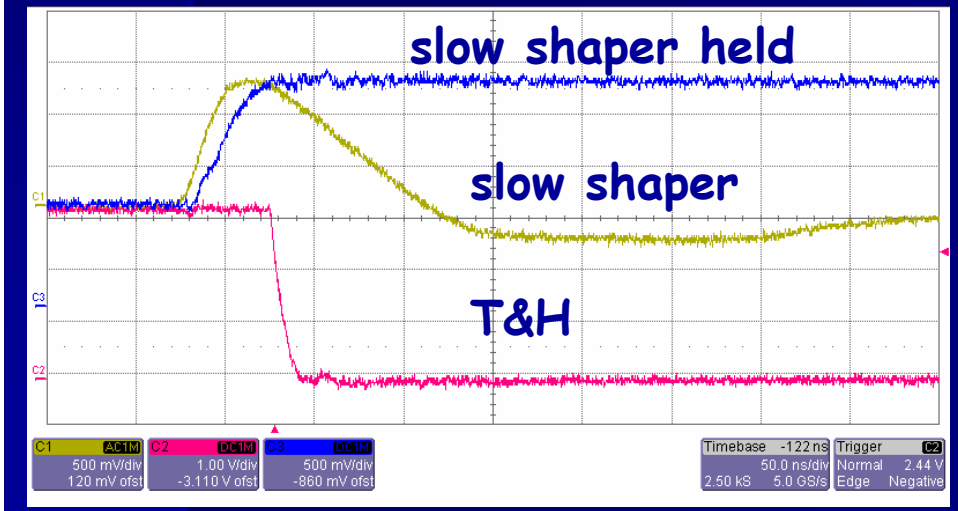
Slow shaper

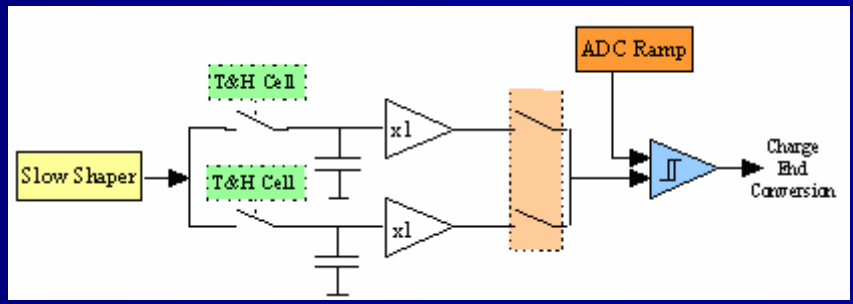
LAL

Slow shaper	meas	sim
Vout (1pe)	12 mV	18 mV
Rms noise	3.5 mV	1 mV
SNR	3.5	18
Rise time	28 ns	27 ns

Low frequency to be understood and removed (power supply noise ?)







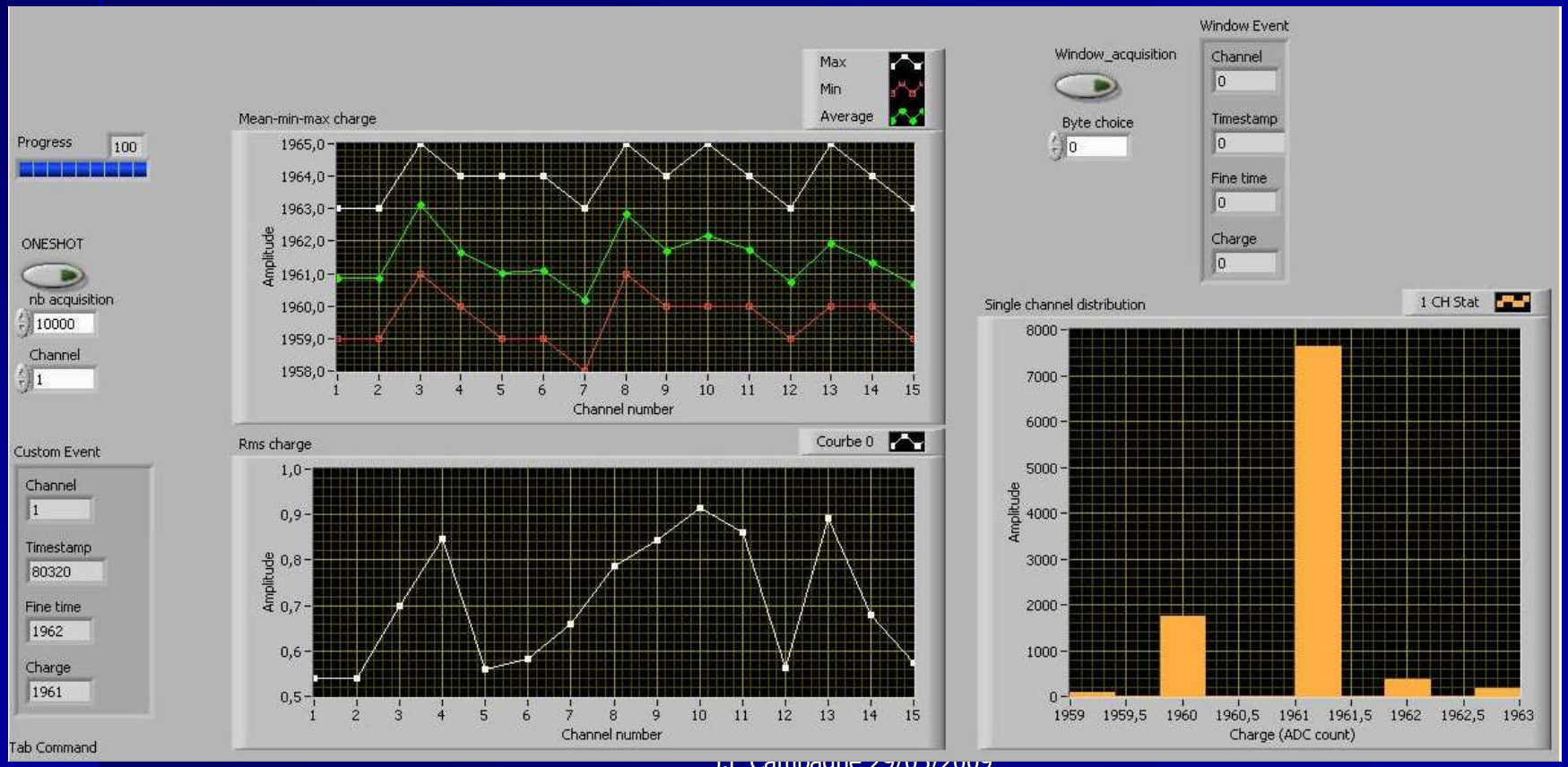
Internal 12bit Wilkinson ADC

LAL

ADC_UNITS =1961
ΔADC_units = 4

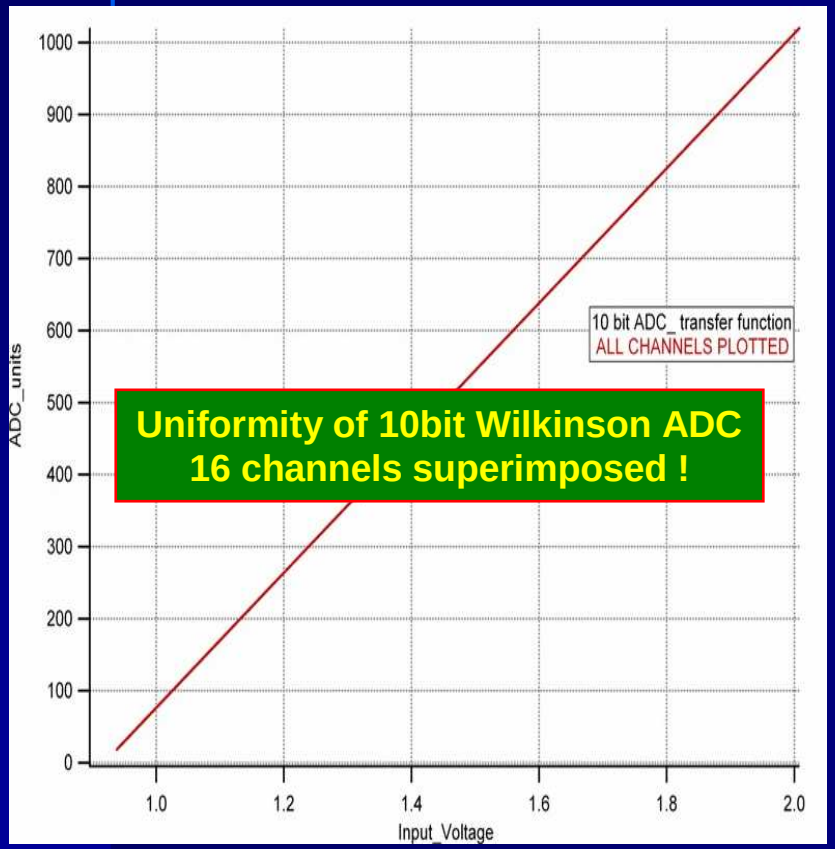
0,2% accuracy !

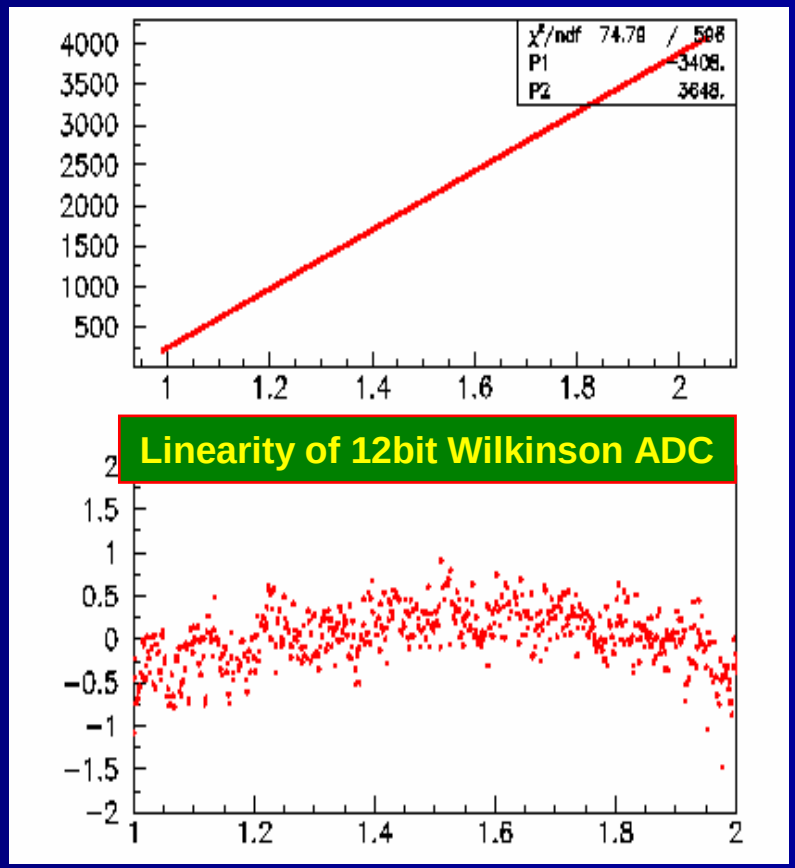
DAC=500=1.4523V
Number of acquisitions: 10000



Internal Wilkinson ADC

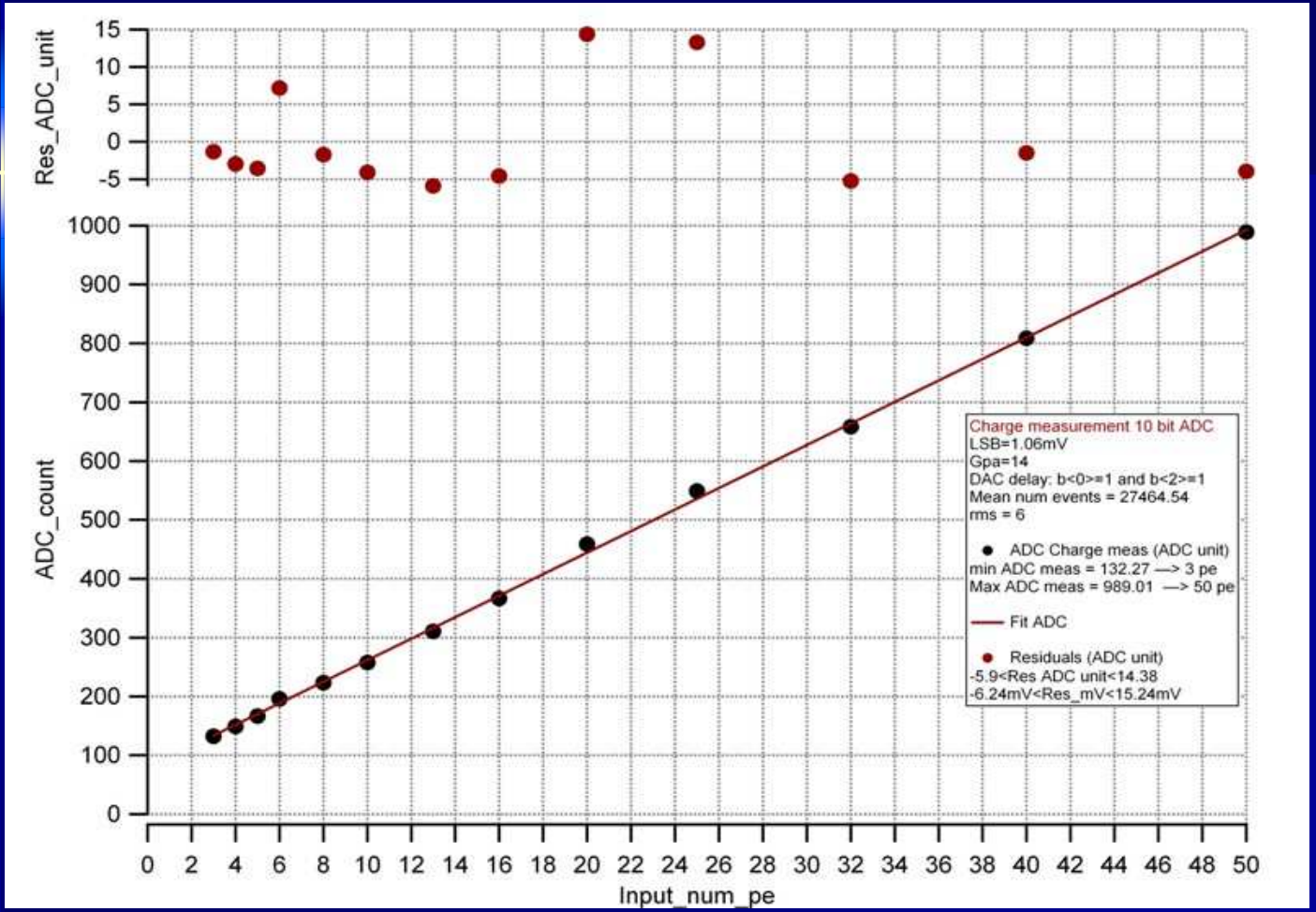
- Wilkinson ADC well suited to multichannel conversion
- Very good uniformity and linearity





Overall behaviour

LAL



- Complete chain : autotrigger + T&H + internal ADC

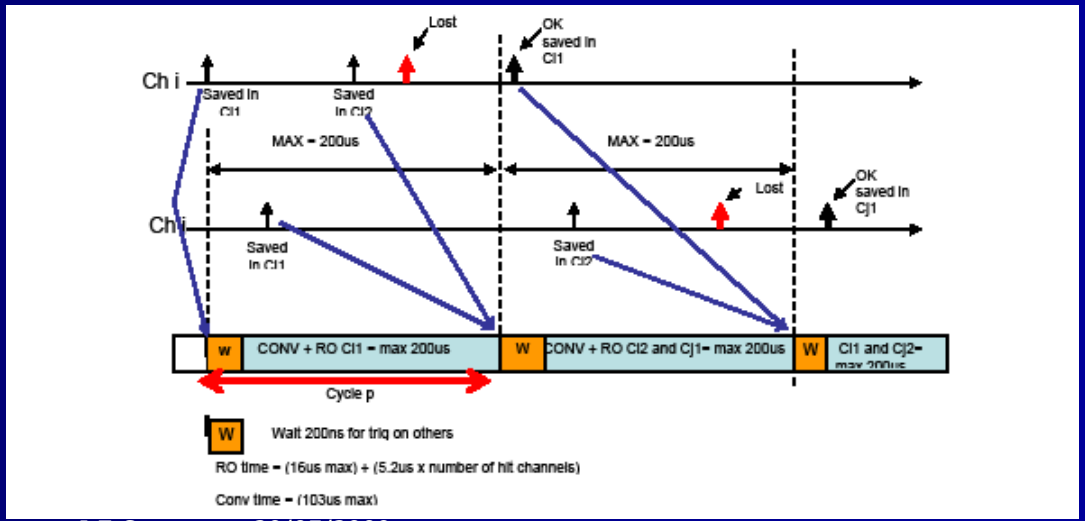
LAL

PARISROC v2

simulation

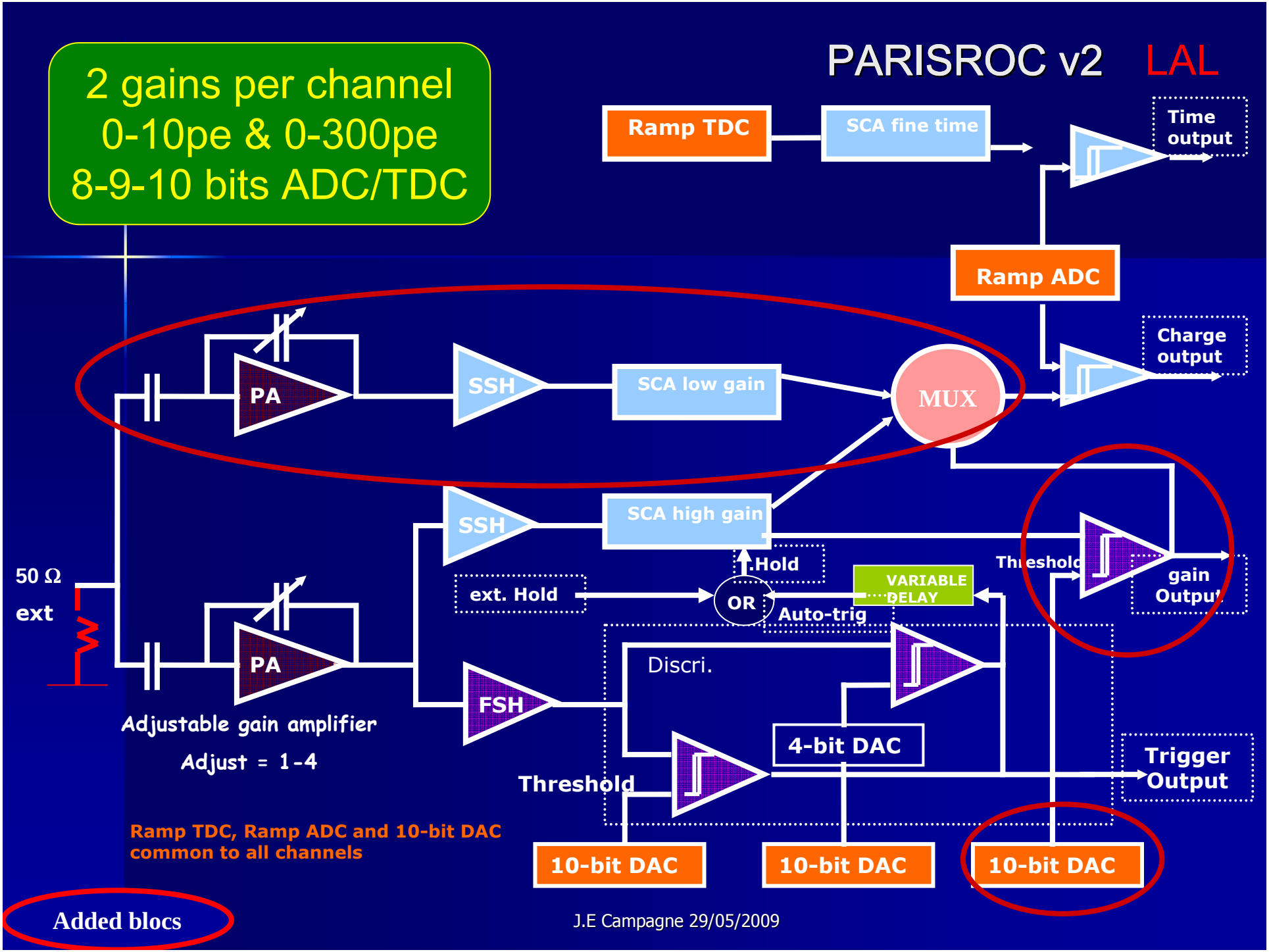
PM noise	# buffers per channel	ADC bits number	Readout frequency	loss (%)	
5 kHz	2	12	10 MHz	16 ± 12	V1
0.1 kHz	2	12	10 MHz	0.008 ± 0.6	
5 kHz	2	8*	40 MHz	0.24 ± 3.1	V2
5 kHz	4	9*	40 MHz	0.007 ± 0.7	

After discrimination p.e can be lost by the digital part of PARISROC depending on the dark current rate of the PMs and readout parameters.



PARISROC v2 LAL

2 gains per channel
0-10pe & 0-300pe
8-9-10 bits ADC/TDC

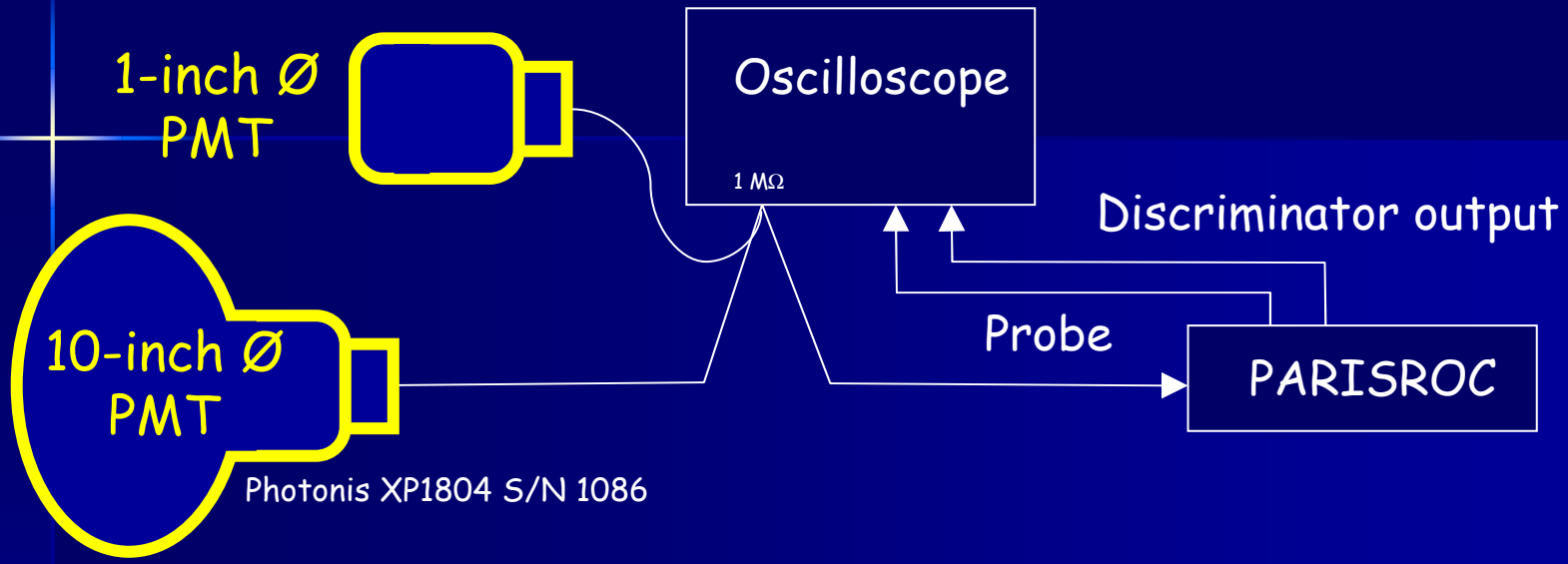


Digital improvments

- Management of 2 gains for charge (16 inputs to add)
  - Multiplex SCA depth 1 and SCA depth 2 gain (analog part)
  - Store Gain in 1-bit register
- Conversion 8-9-10 bits by selecting ramp slope
  - Internal counter 10-bit (Parisroc1: 12-bit)
  - Max conversion time : 25 us @ 10 bits (Parisroc1: 100us)
- Readout @ 40 MHz
  - Max readout time 25 us (Parisroc1: 100us @ 10 MHz)
- Readout format (50 bits / hit channel unchanged) :
  - (MSB) 4 bits channel #
  - 24 bits timestamp
  - 1 bit timestamp counter
  - 1 bit gain
  - 10 bits charge
  - (1 bit "TDC ramp 1 or 2 converted" if needed)
  - 10 bits time (LSB)

Chip submission Q4 2009
Design will end July 09

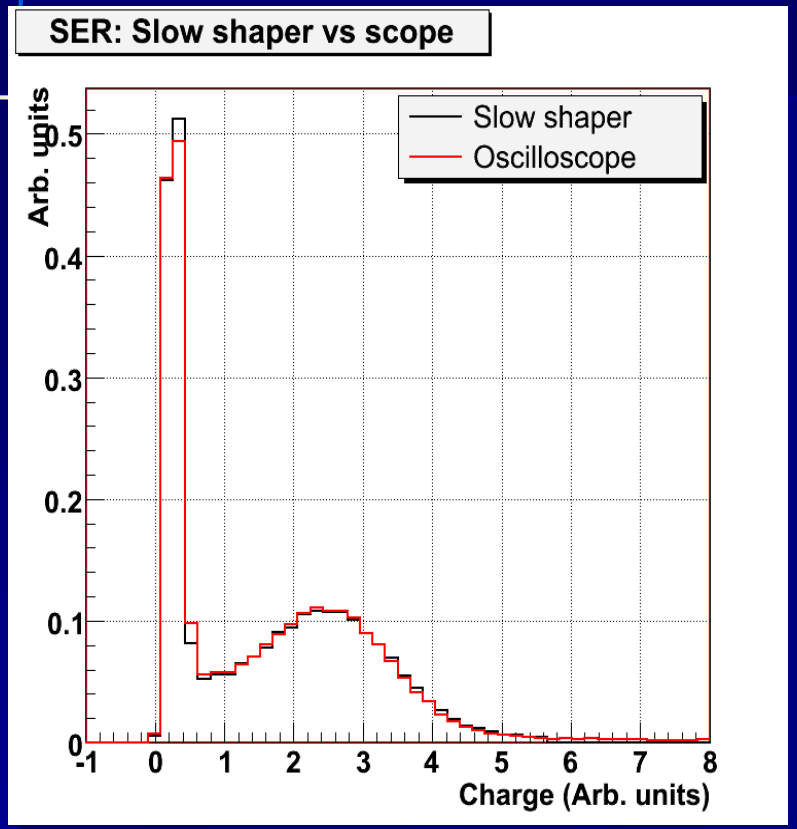
PARISROC v1 (1st tests) IPNO+LAL

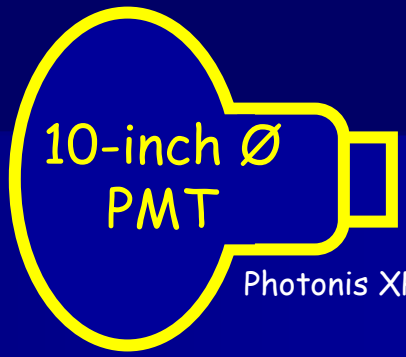


- PARISROC test board (S/N #3)
- Analog signal read on high impedance on the oscilloscope, the adaptation being achieved by the PARISROC input
- Probe signal: can be the fast or the slow shaper. Software controlled
- Discriminator output: chip output, measured with an oscilloscope probe
- 10-inch Ø PMT for « standard » measurements, 1-inch Ø PMT for pressure / time measurement

Slow shaper test

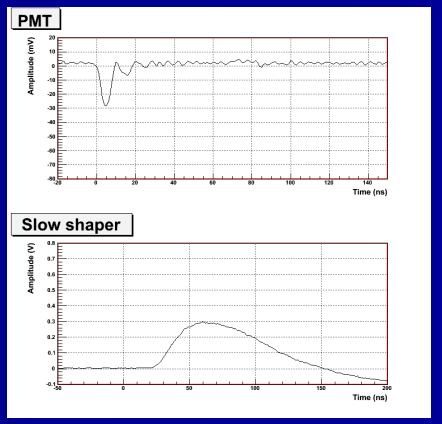
IPNO+LAL





gain = 2.4×10^7

Noise : around 1 kHz at room temperature

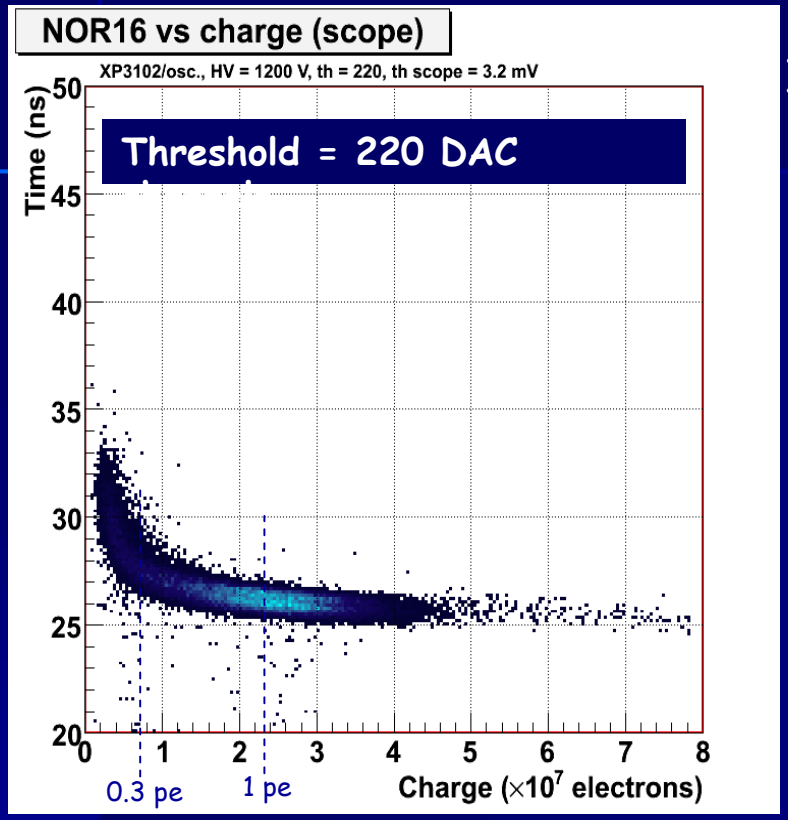


Nearly the same SER* shape obtained with the oscilloscope and the slow shaper signal fit.

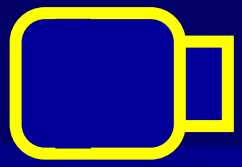
*:Single Electron Response

Discri. test

IPNO+LAL

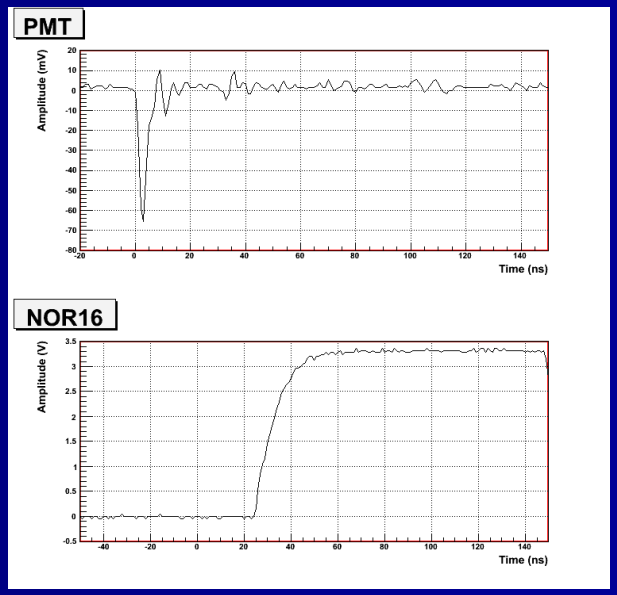


1-inch Ø PMT



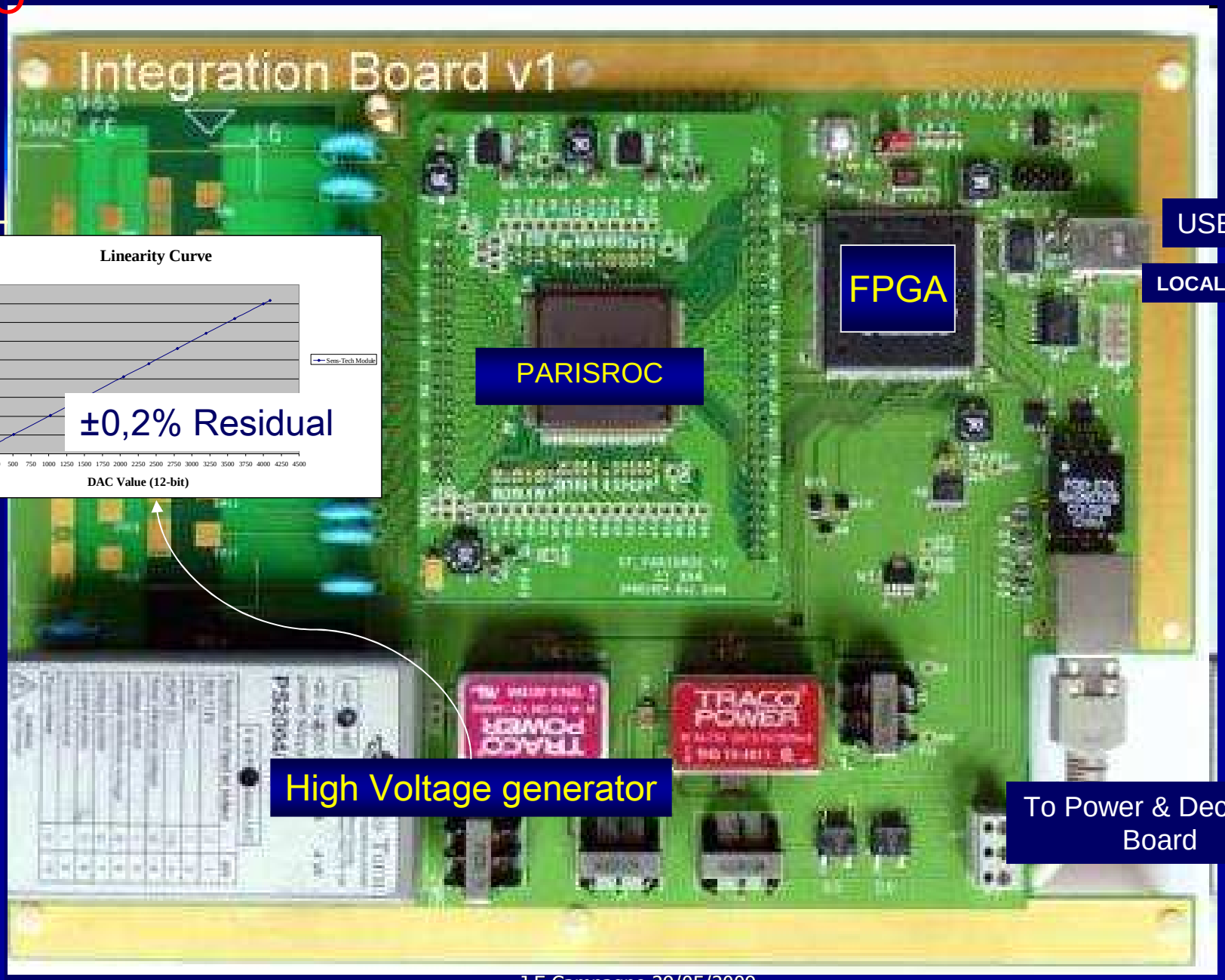
Photonis XP3102 (10 stages) special design

2.4×10^7 at 1200 V Small PMT ⇒ much faster than the 10-inch Ø PMT + lower noise (≈ 100 cps) = better for time resolution measurement



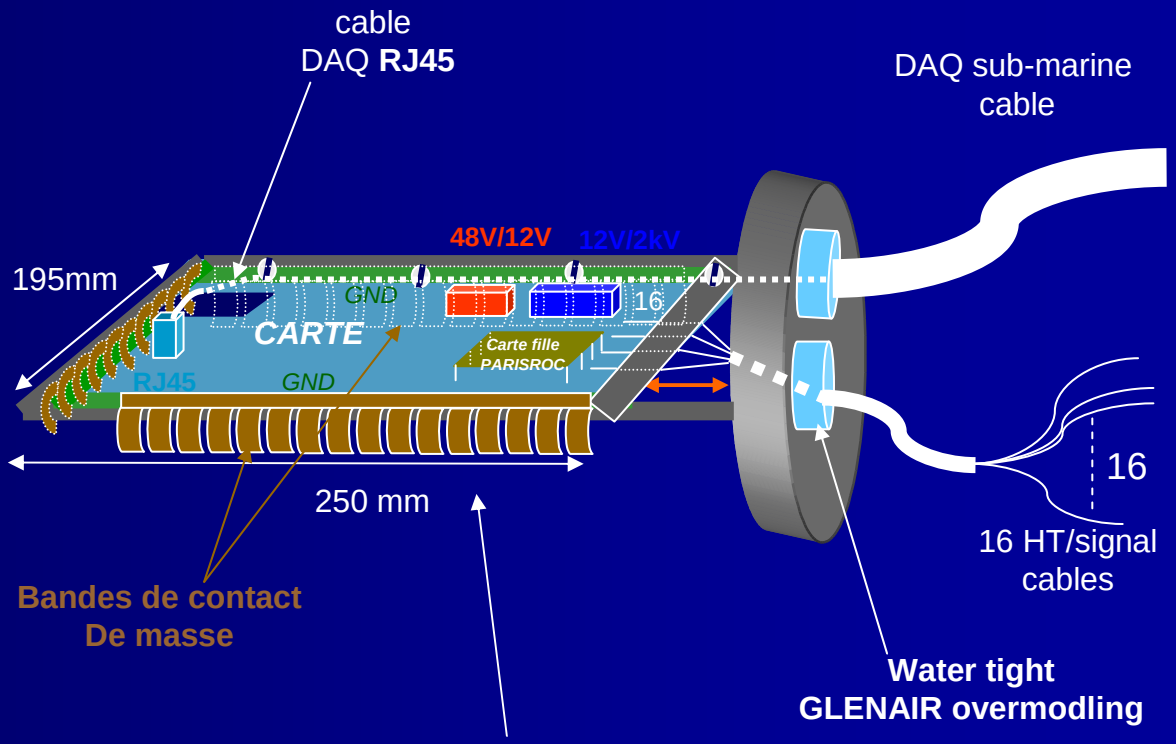
- PMT signal and discri. Signal leading-edge fitted
- Resolution = 600 ps RMS (> 0.3 pe) with a low threshold on PARISROC discriminator (220 DAC channels).

IPNO


Integration Board v1
Linearity Curve
High Voltage (Volt)
DAC Value (12-bit)
Sens-Tech Module
±0,2% Residual
FPGA
PARISROC
USB
LOCAL TEST
High Voltage generator
To Power & Decoding Board

Implementation in the water tight box (10bars)

Very crude « mecano » design

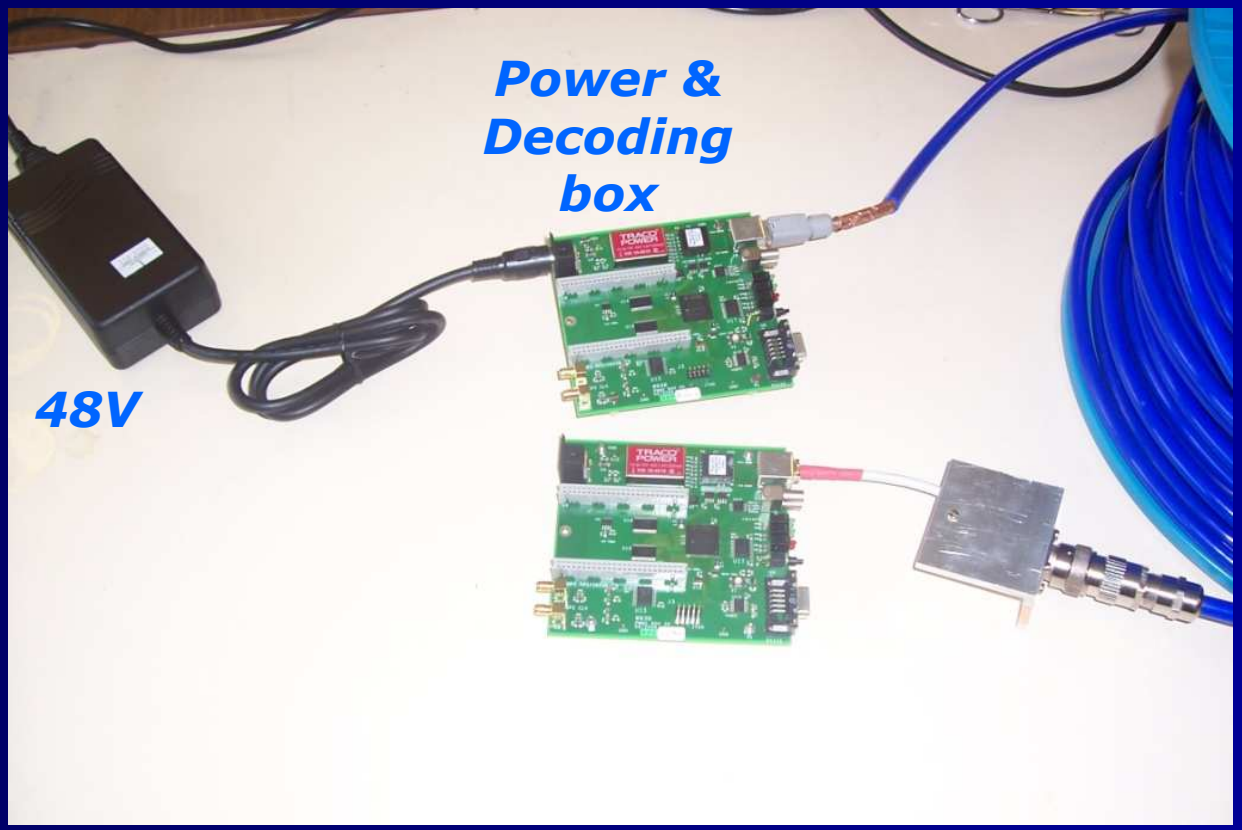


Integration board implementation

LAL

Cables and Data Transmission

LAPP



100ml

LAPP

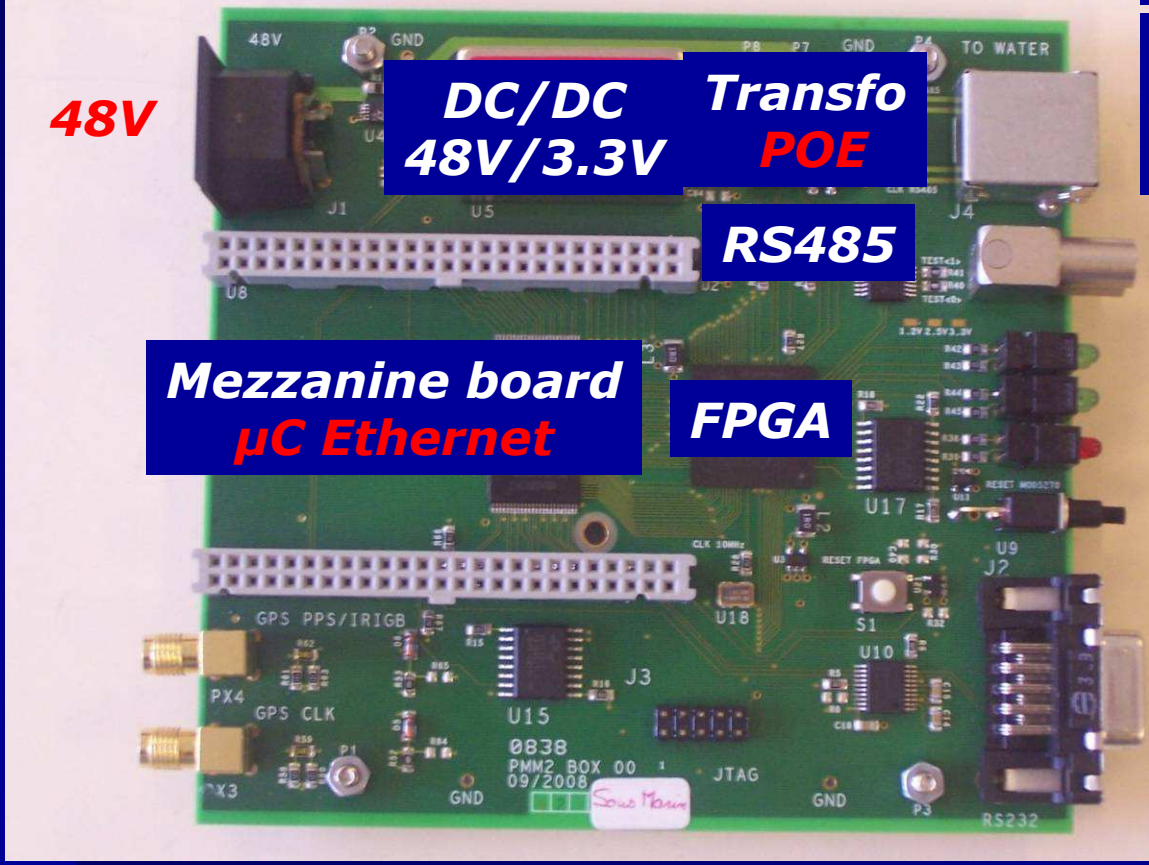
Power & Decoding board

5Mbits/s
5kHz/PM dark current

Cable to water tight box

2 twisted pairs
Clock
Data bi-direct.

POE: Power (30W/48V) over Ethernet

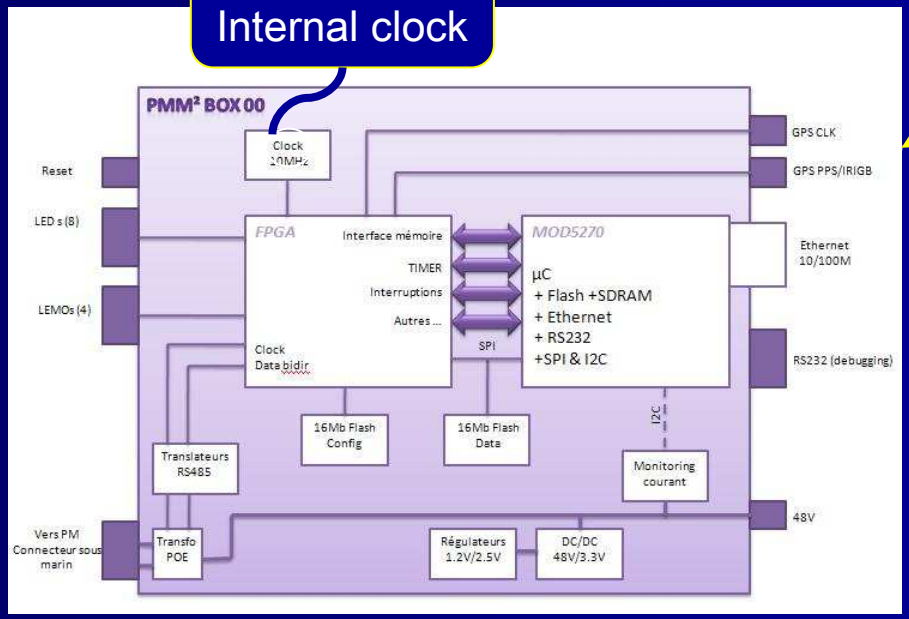


LAPP

Power & Decoding board

10MHz
Internal clock

GPS 10MHz



FPGA
synchronisation and dialogue with submarine electronics (RS485)

MOD570
Connexion with external networks (TCP/IP)

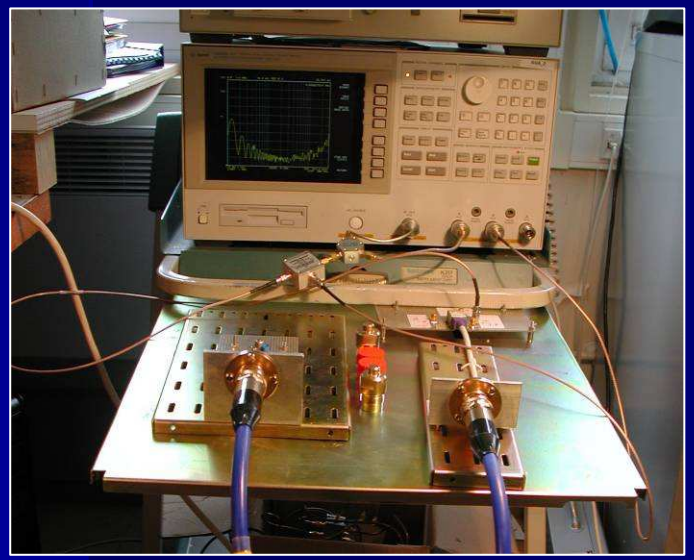
External power supply 48V/50W

The dialog between this board and the Integration Board is home made (simple serial protocol with 32bits words) transmitted coded in Manchester (Phase Encoding) on RS485 diff. pair.

Data integrity test @ 8Mbits/s during 2h: no failure

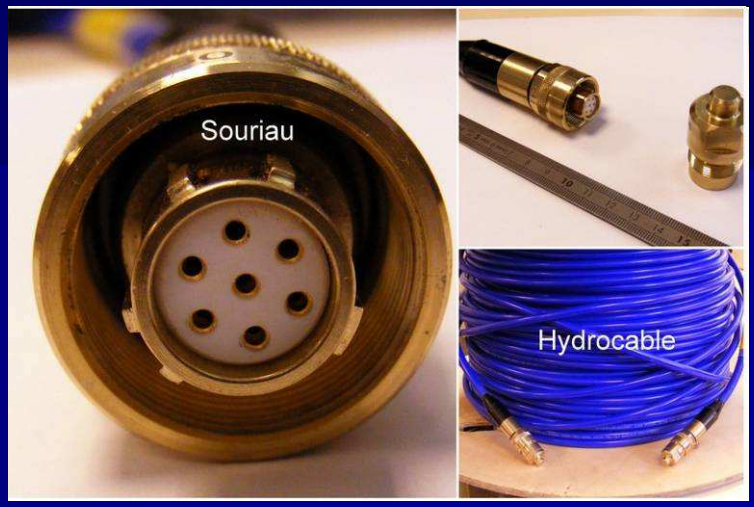
Cables

- Bi-directional Cat. 5 type of data network cables
- At least 2 twisted pairs (may be revisited)
- 100 ml
- The only connector we accept to ease the mounting and maintenance.



LAPP

Tests with connectors (mai 09)



Hydrocable with Souriau connectors

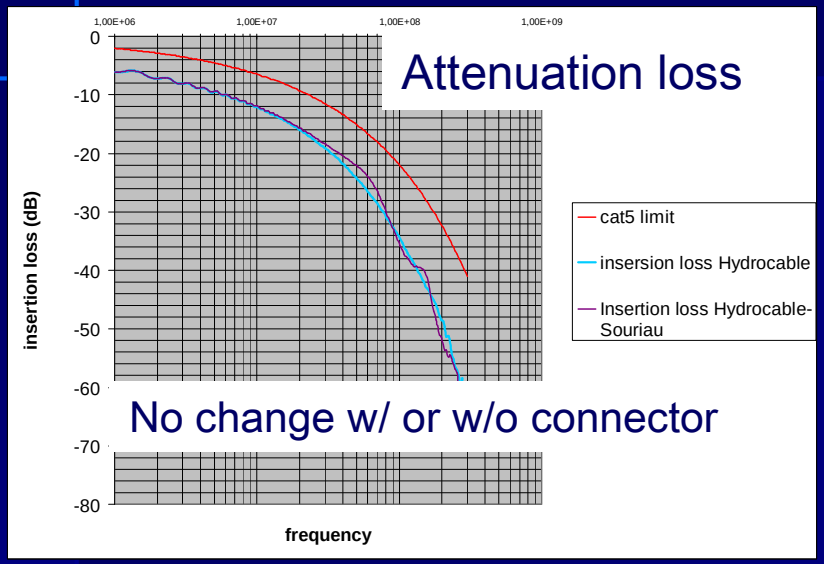
Prelim. price large prod. ~650€
(cable + connectors)

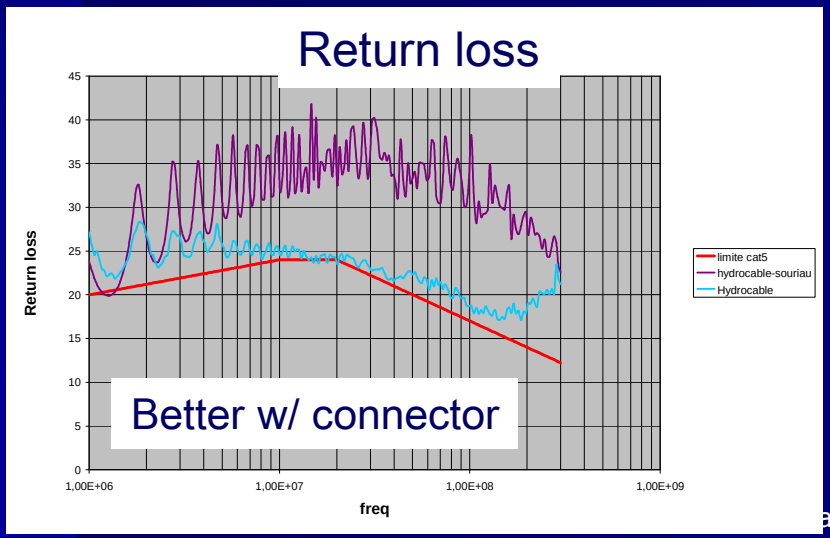
EUROCEANIQUE with GISMA connectors

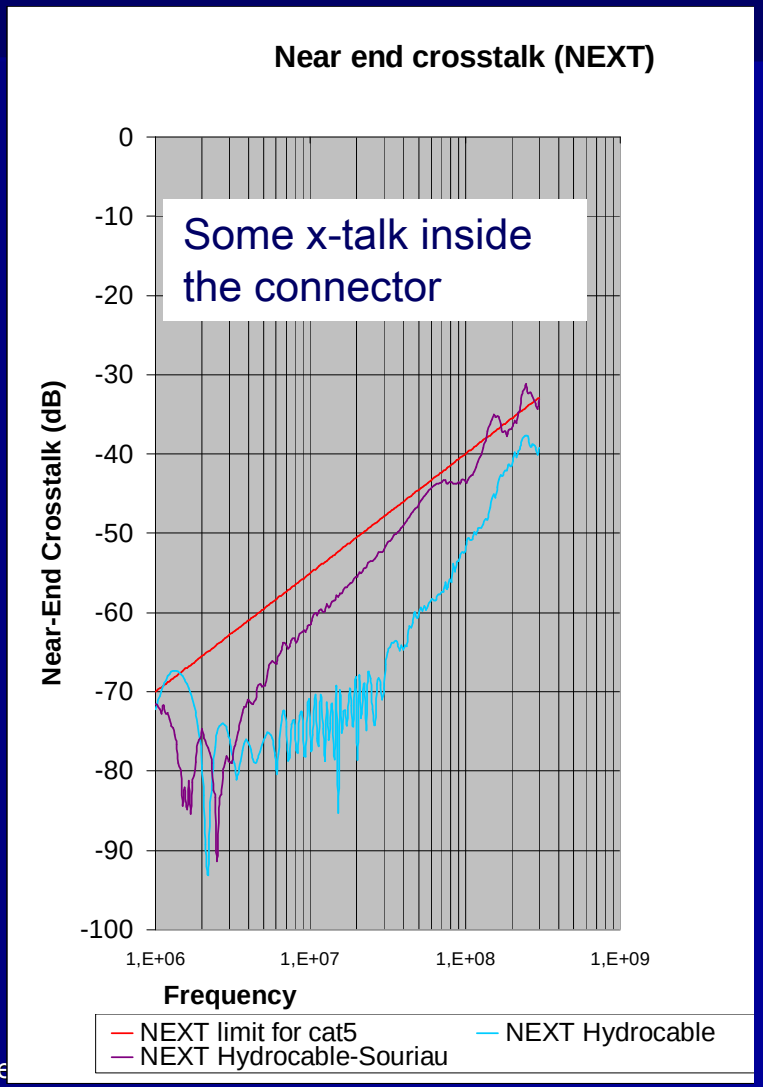
HYDROCABLE with GLENAIR connectors

LAPP

Cable tests with connectors

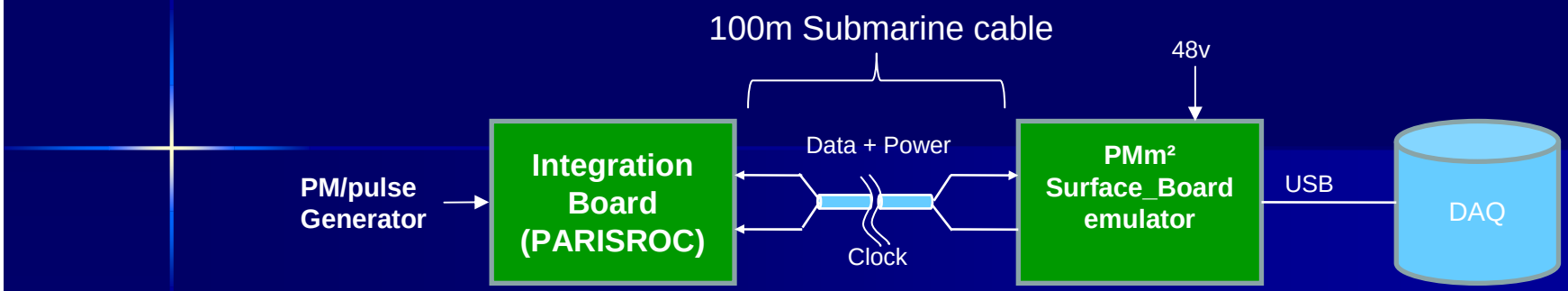






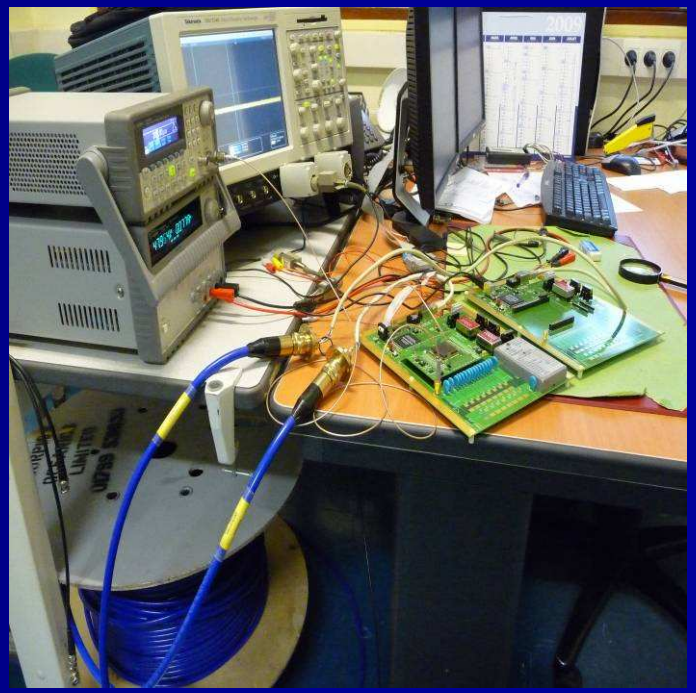
PMm² DAQ tests

IPNO+LAPP+LAL



Injection up to 16 channels (test input)
Pulse period 200µs

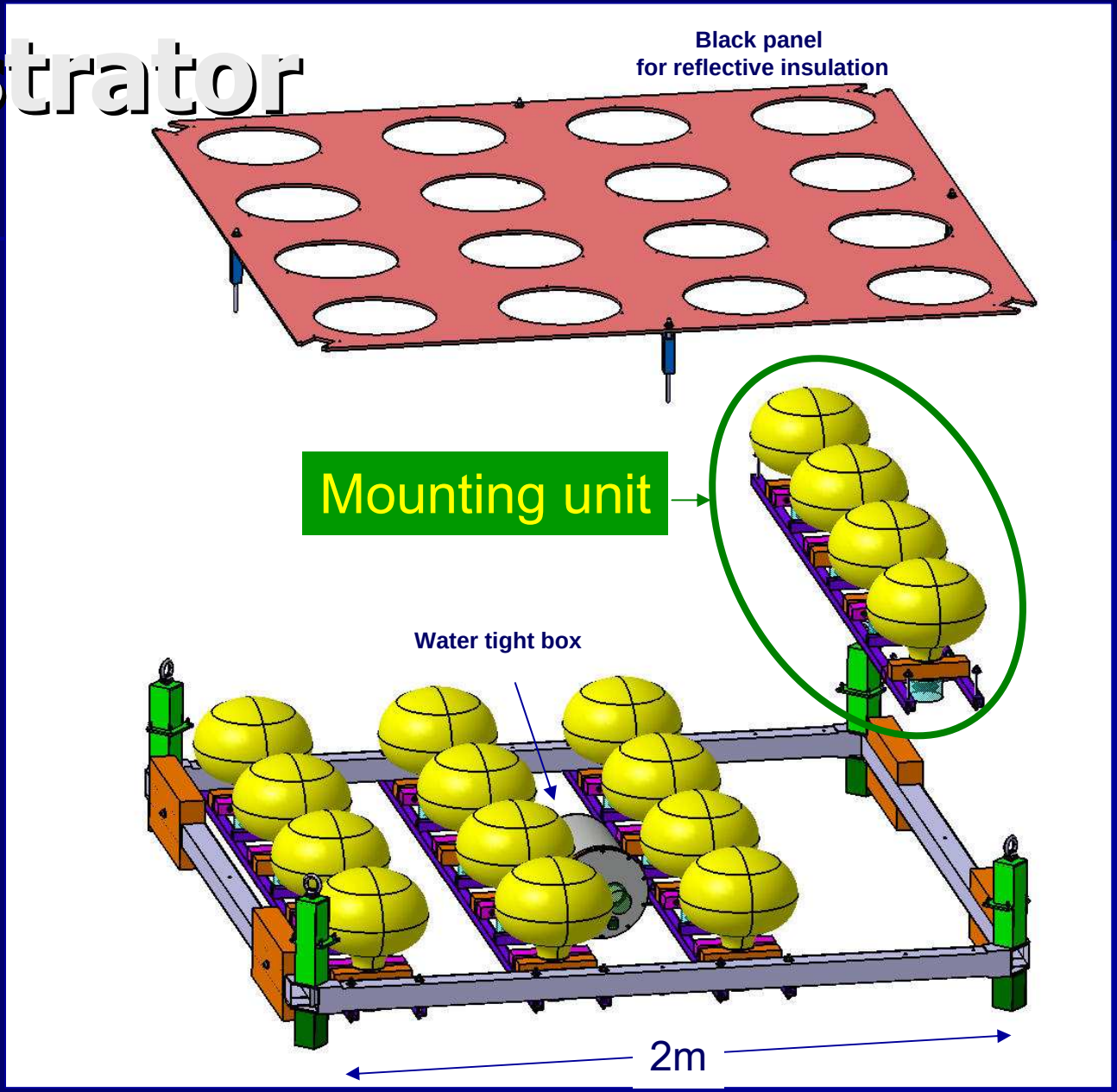
Transmission tests during 12hours Ok



More tests to be done end of June 09 with the complete DAQ system.

(Intermediate TCP/IP tests with ULB/PC-LAPP/PMm2 Surface board, ~mid June 09)

Demonstrator



Compatible with MEMPHYNO water vessel (join LAL-IPNO-APC and ULB)

Coming next…

- Large Photodetectors:
  - We are in contact with Hamamatsu & ETL to purchase 8″ PMTs for the demonstrator ⇒ End 09′
  - To transfer to the how-know to use these new PMTs will take some times
  - Finalize the glass & PMT shape breakdown studies
- PARISROC
  - Next version submission scheduled Sept 09′
- Electronics Demonstrator @ 10bars (BNL vessel)
  - 16 x 1″ Photonis PMTs
  - All the present versions of the PARISROC, submarine & surface boards, TCP/IP DAQ
- Final Demonstrator
  - Design will be finished July 09′
  - Start building Sept 09′
  - Will wait for Large PMTs delivery
  - Tests with all the electronics + DAQ will start early 2010.
- We have asked for 6 months continuation of the R&D due to Photonis halt ⇒ mid 2010.

Backup