Super Nemo Absolute Time Stamper

A high resolution and large dynamic range time stamper chip

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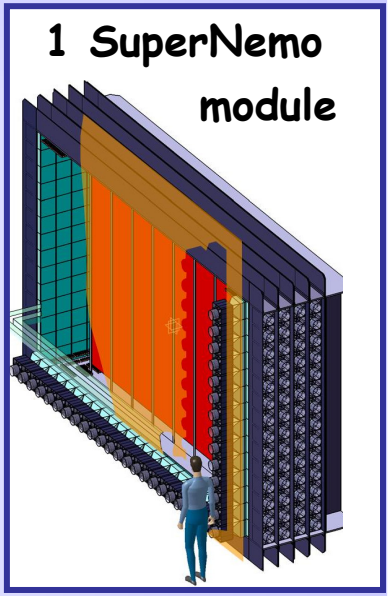
Context

Aim : investigation of neutrinoless double-beta decay

To answers to questions on the nature of the neutrino.



The SuperNemo detector :

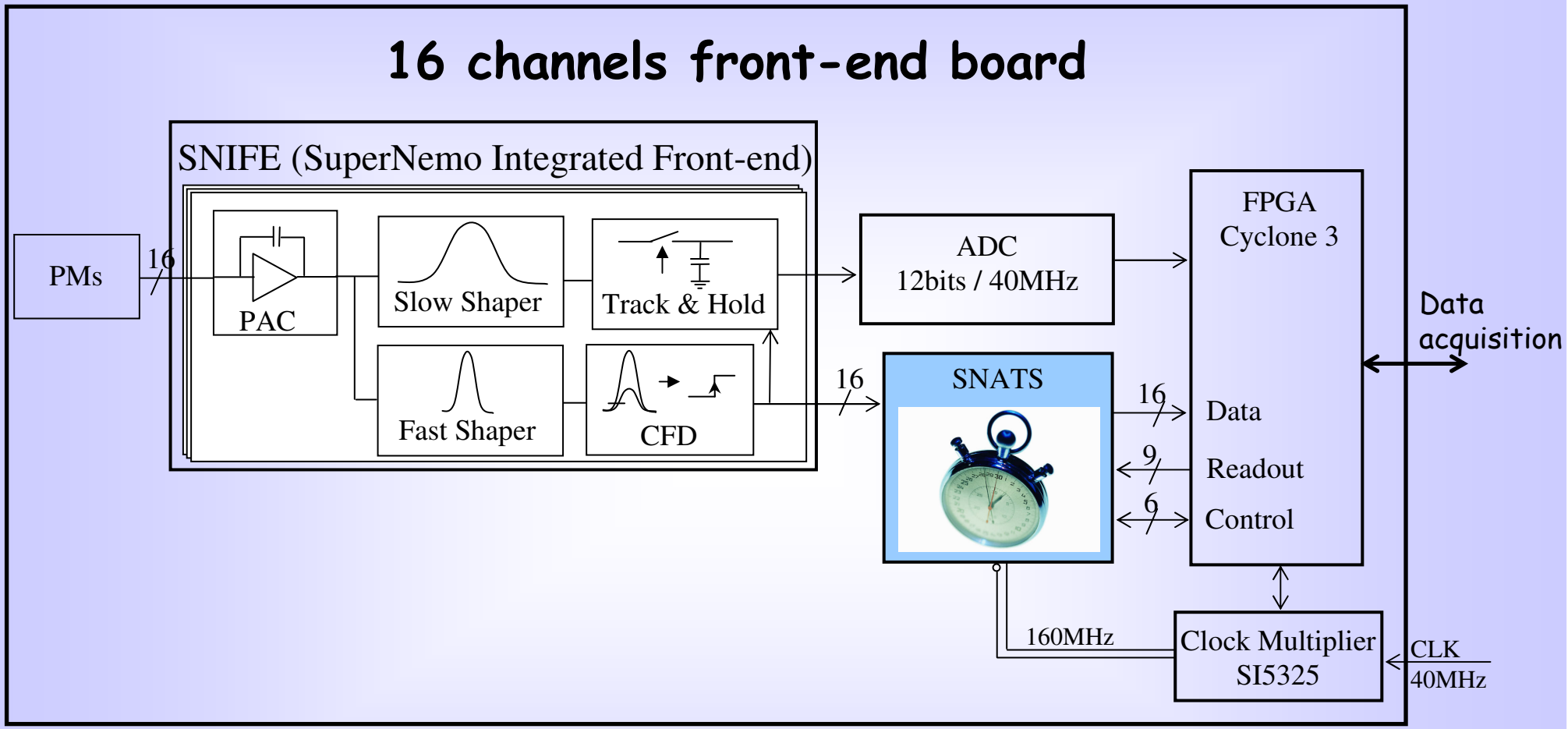
20 modules composed of tracker to identify the particle path and a calorimeter to measure the particle energy

Requirements for the Calorimeter Front-End Electronics

To work without a hardware trigger and with absolute time measurements providing a time resolution about 100 ps RMS

SNATS: Super Nemo Absolute Time Stamper

a high performance TDC chip with
a high resolution of 70ps RMS and large dynamic range of 53 bits



20000 photomultipliers ⇨ 1250 SNATS chips

AMS CMOS 0.35µm Technology (C35B4)

Clok frequency : 160MHz

32 cells DLL

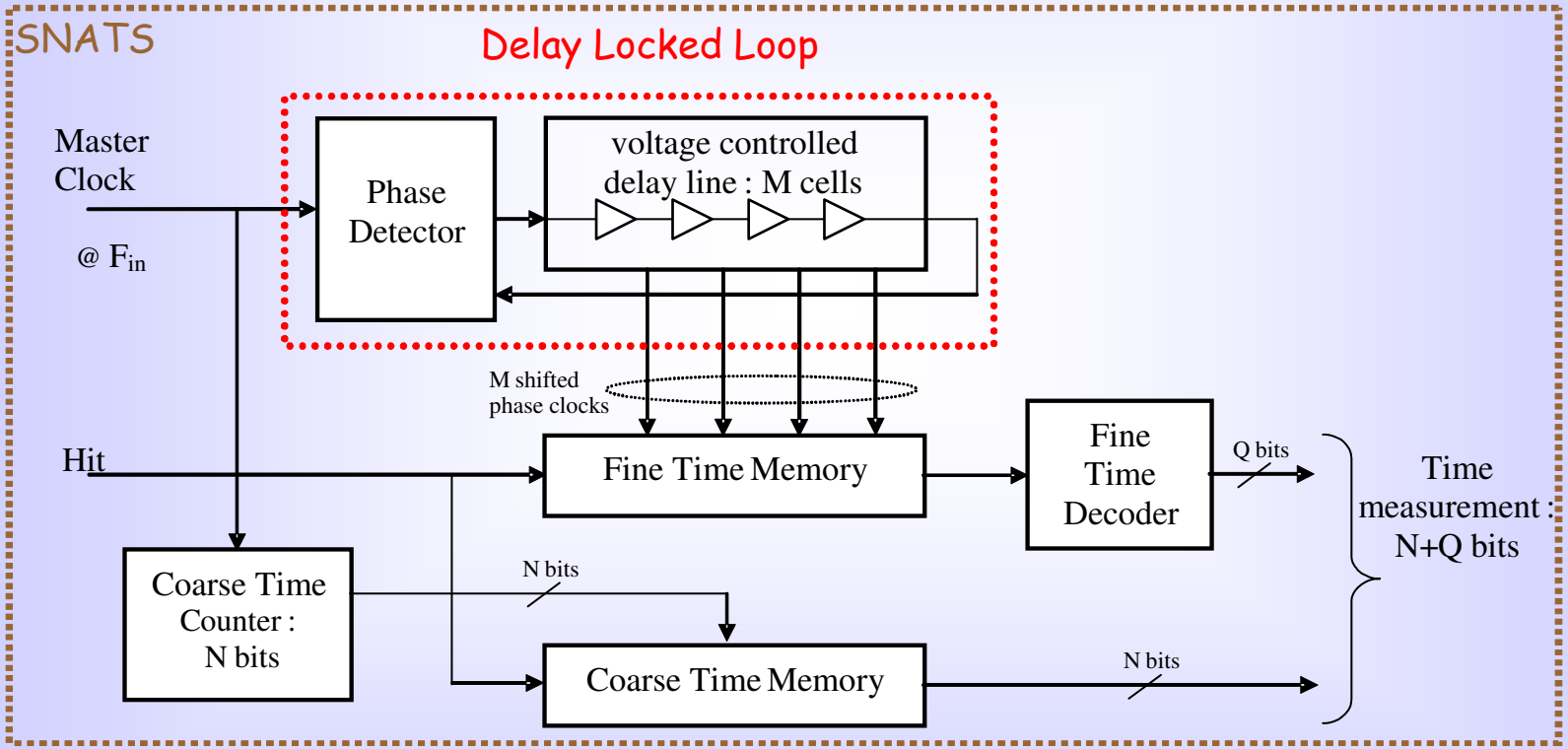
} delay cell ≈ 195ps

DNL <10%

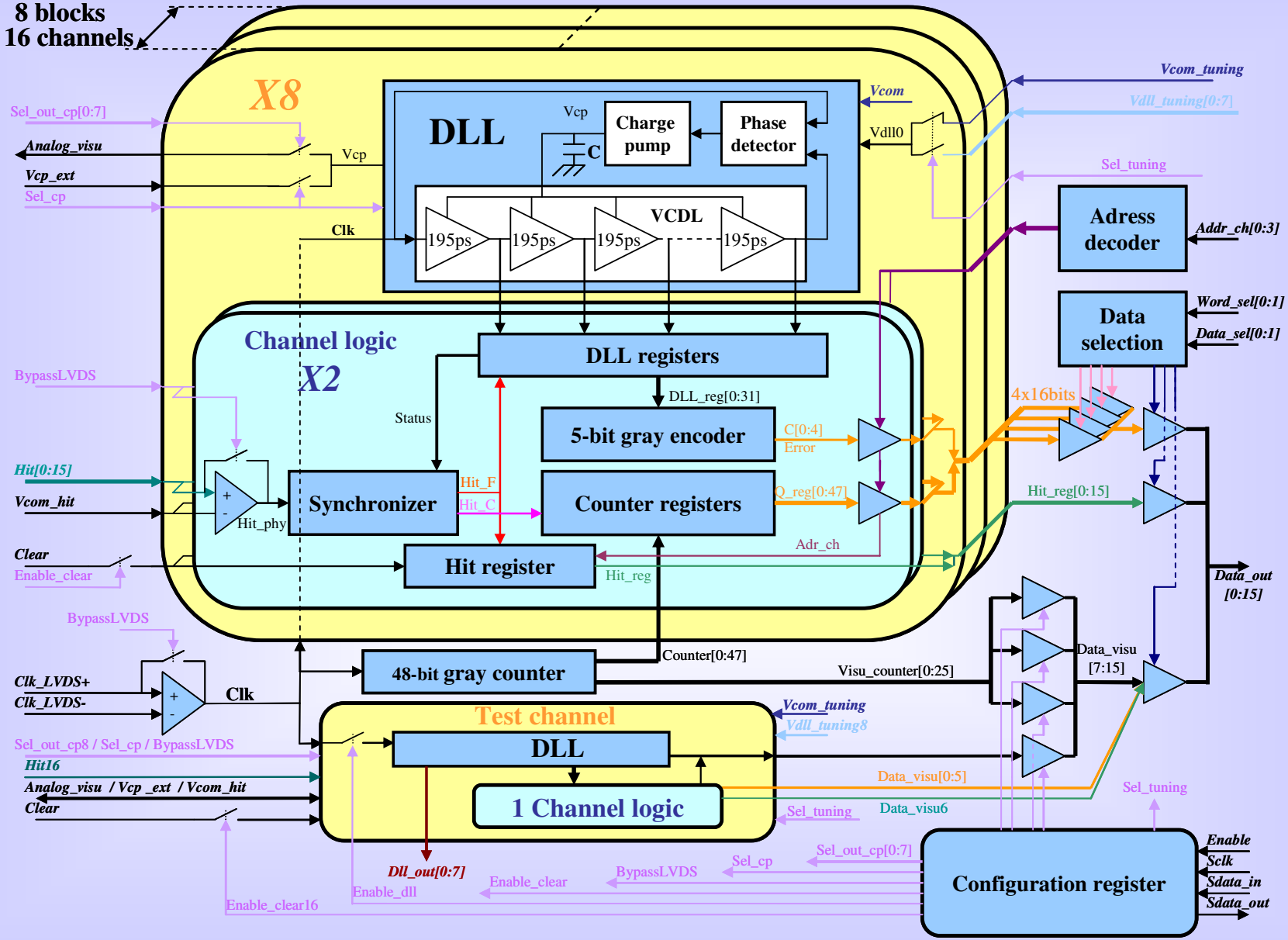
Range : 53 bits
- 48-bit gray counter (≈ 20 days)
- 5-bit gray encoder for status of DLL
- 16-bit parallel data output (4 words of 16 bits)

16 channels/chip

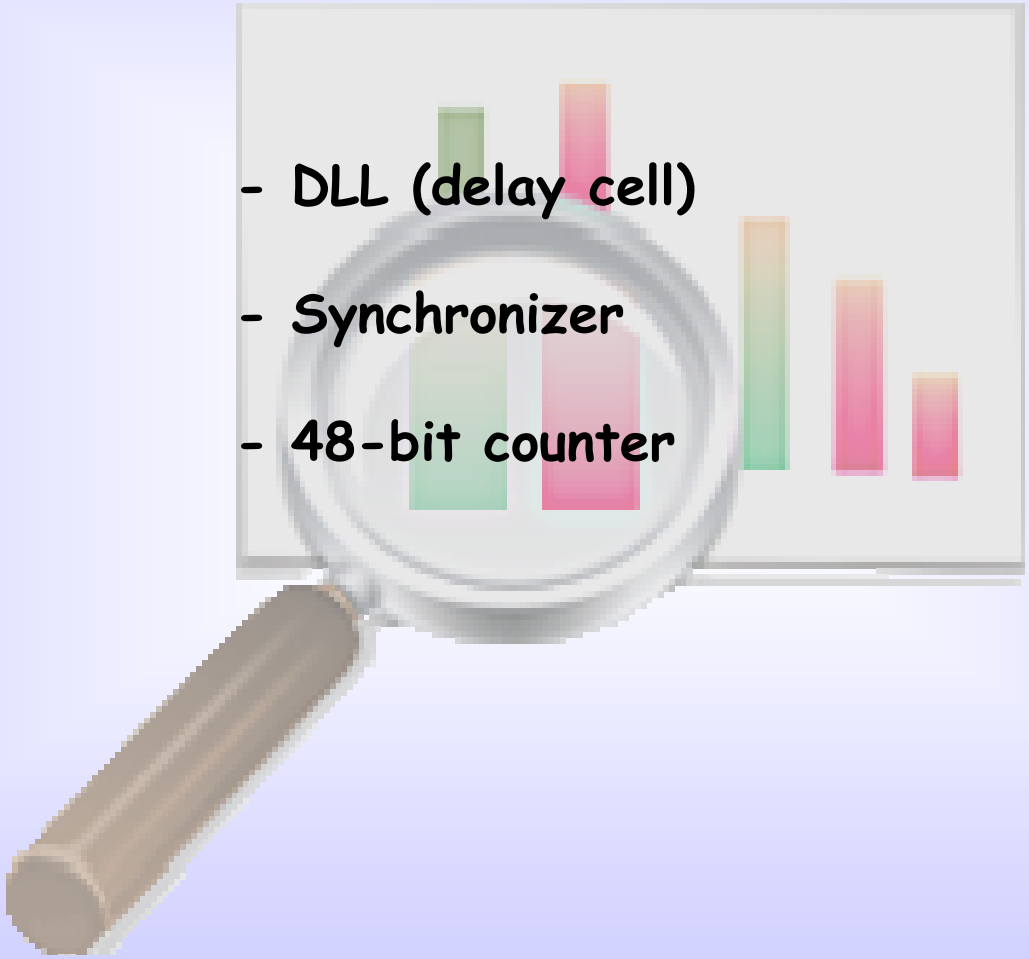
One fine time measurement (High resolution) ⇨ DLL
One coarse time measurement (range) ⇨ N-bit counter



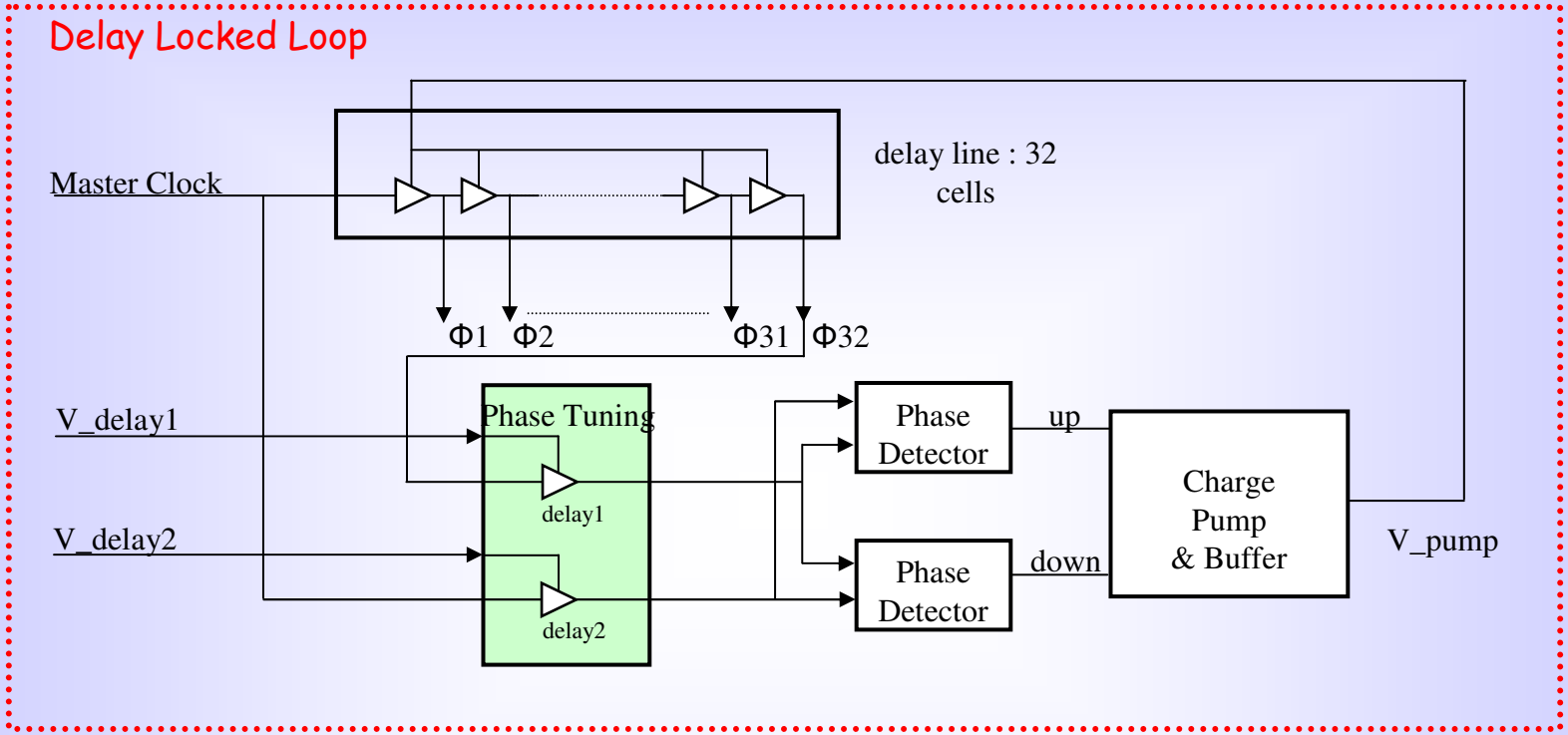
SNATS : architecture



SNATS : Detail of principal blocks



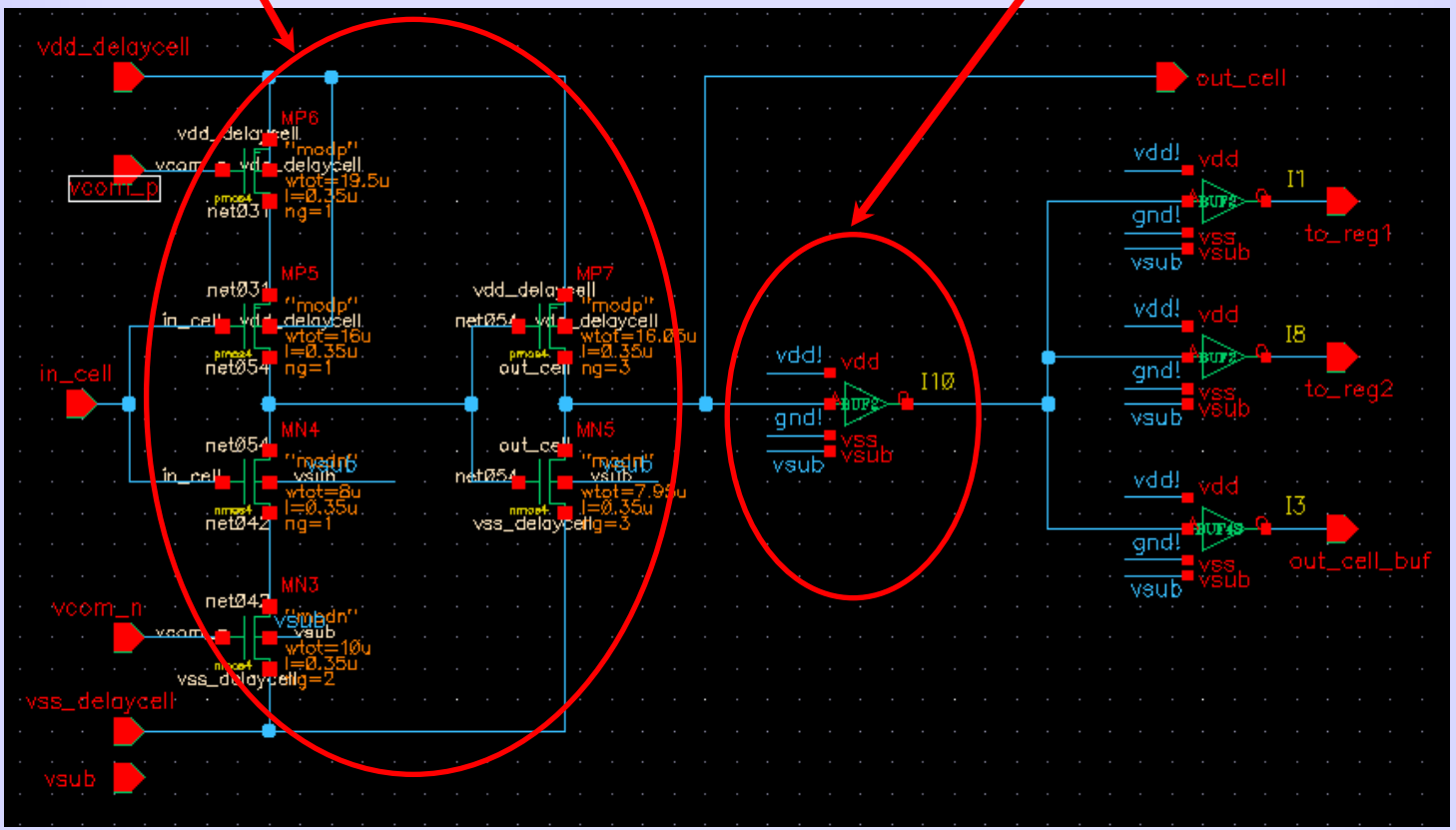
- DLL (delay cell)
- Synchronizer
- 48-bit counter



↳ **Phase error < 20ps**

A starved inverter followed by a standard inverter : gain ≈ 30ps

1 buffer : gain ≈ 30ps



↳ **nominal delay ≈ 195ps with a 30ps margin**

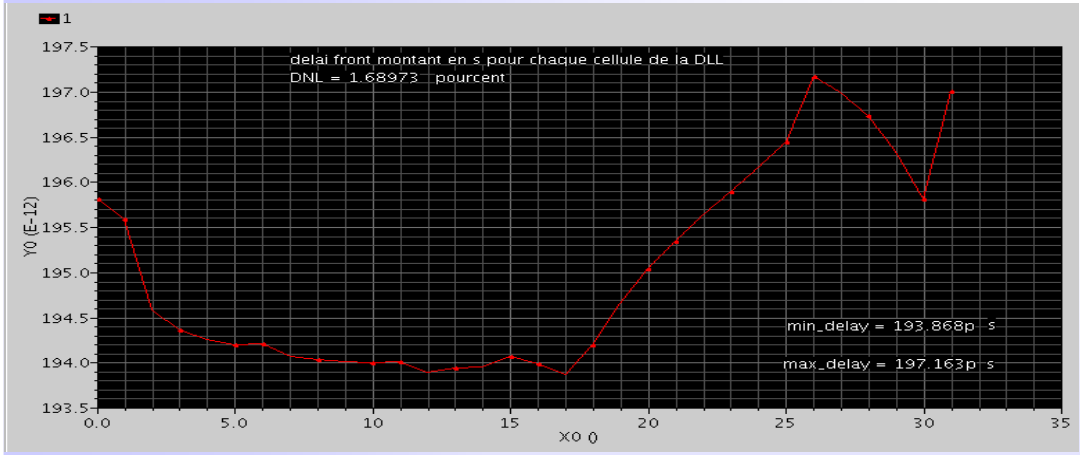
SNATS : post layout simulations (typical parameters)

Slope of delay cell ≈ 0.15ps/mV

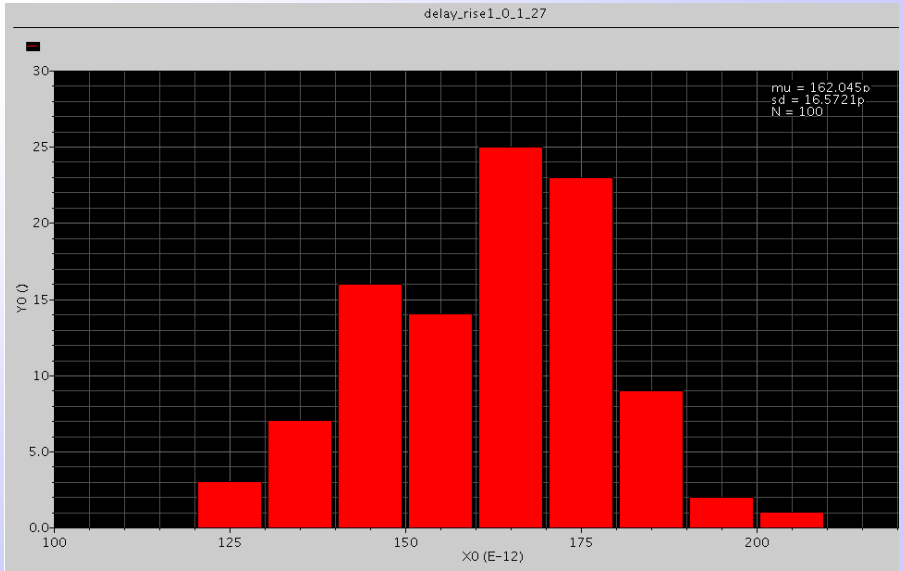
Minimum delay ≈ 150ps at 27°C

≈ 166ps at 60°C

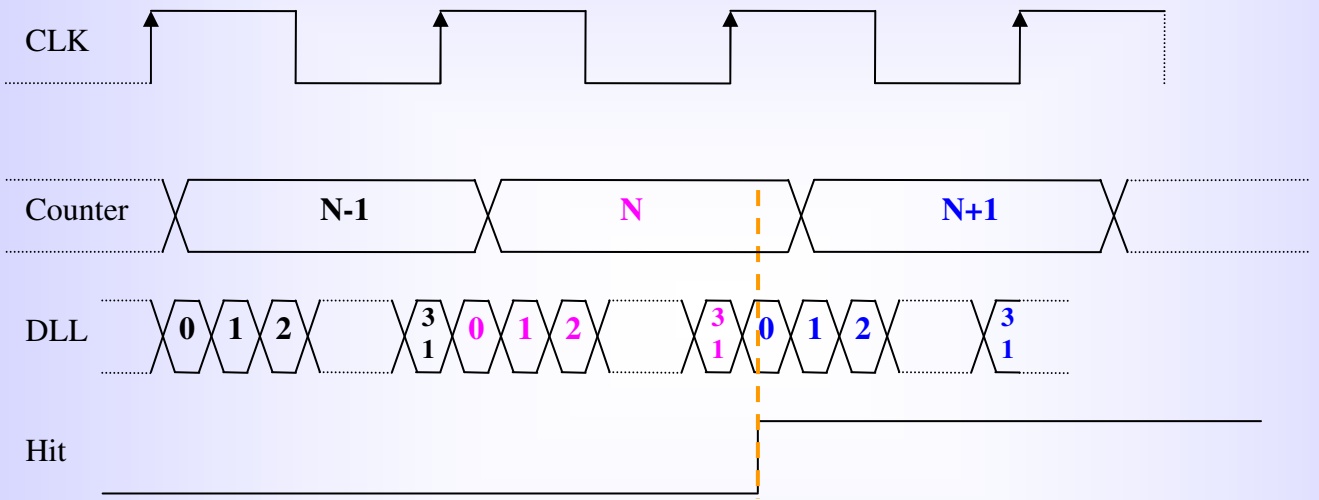
DNL of DLL <2% at 27°C



Montecarlo « Process & Mismatch »



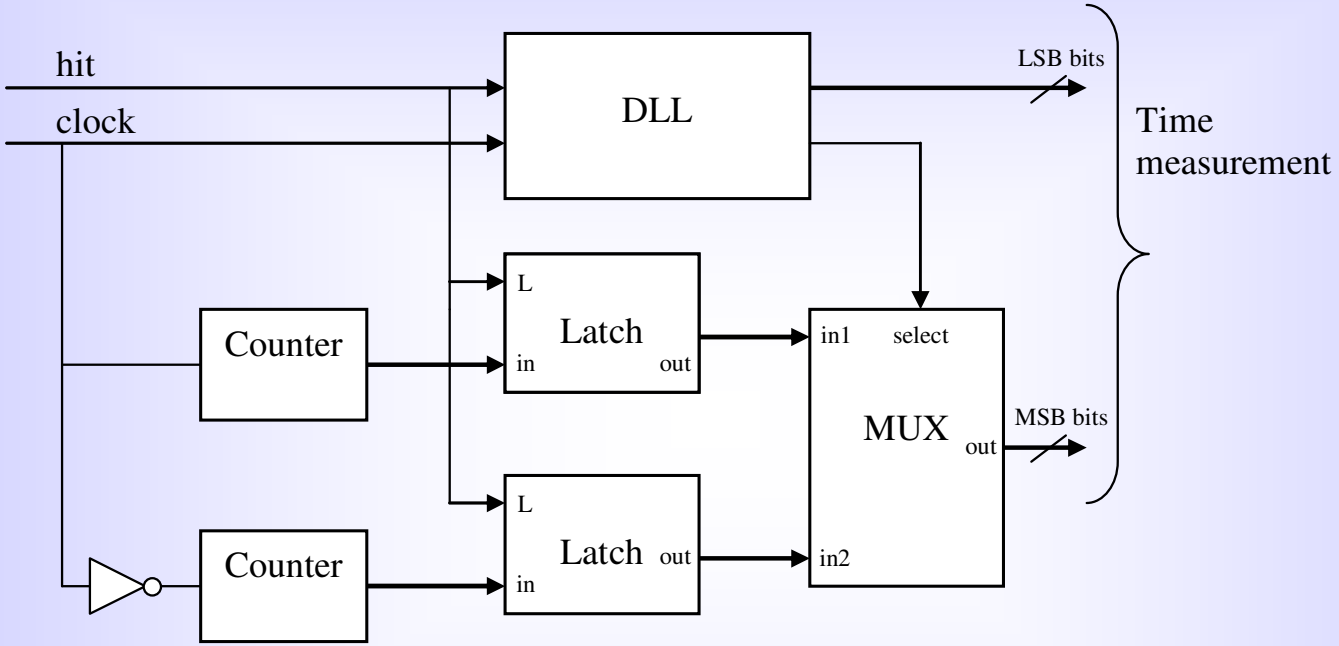
Pb : DLL and counter are synchronous but not in phase!



Code DLL memorized : 0
Code counter memorized : N instead of N+1

} **Error of one clock period**

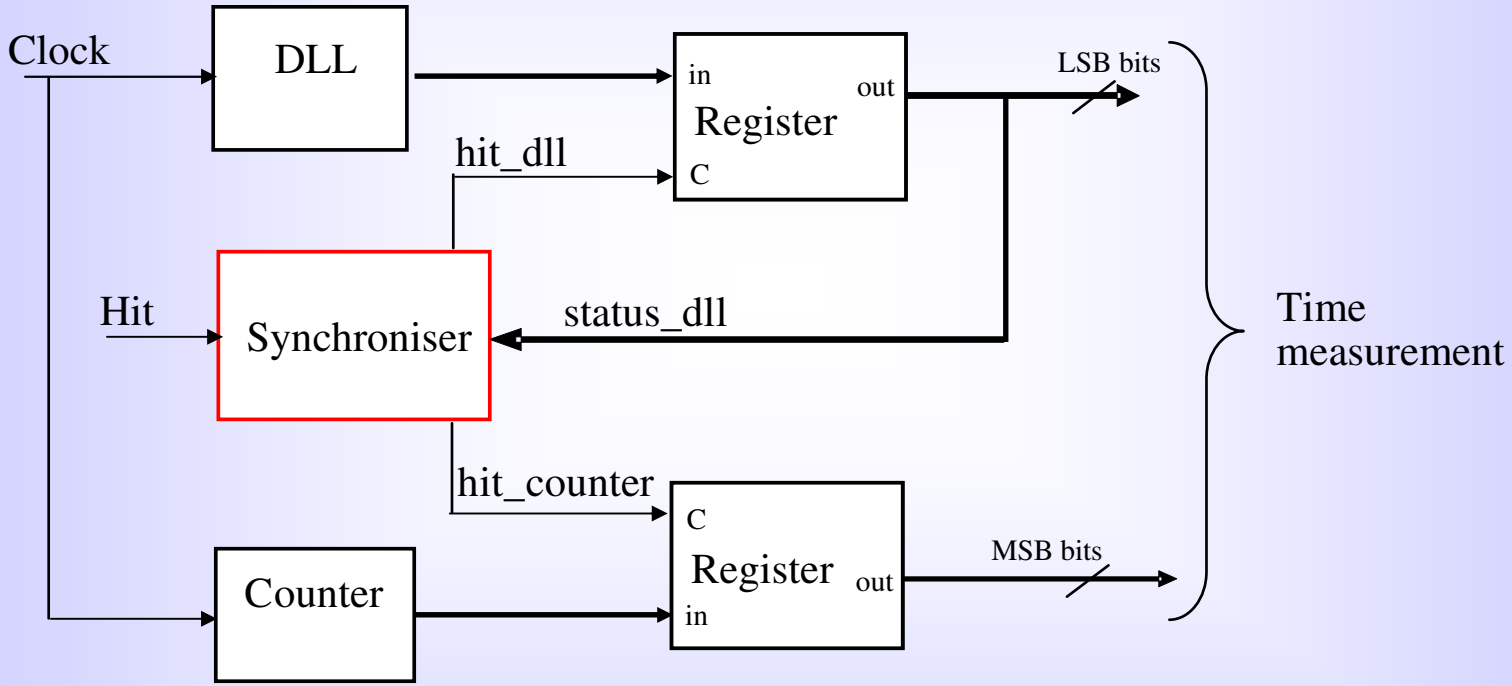
Usually, dual counter structure is used:



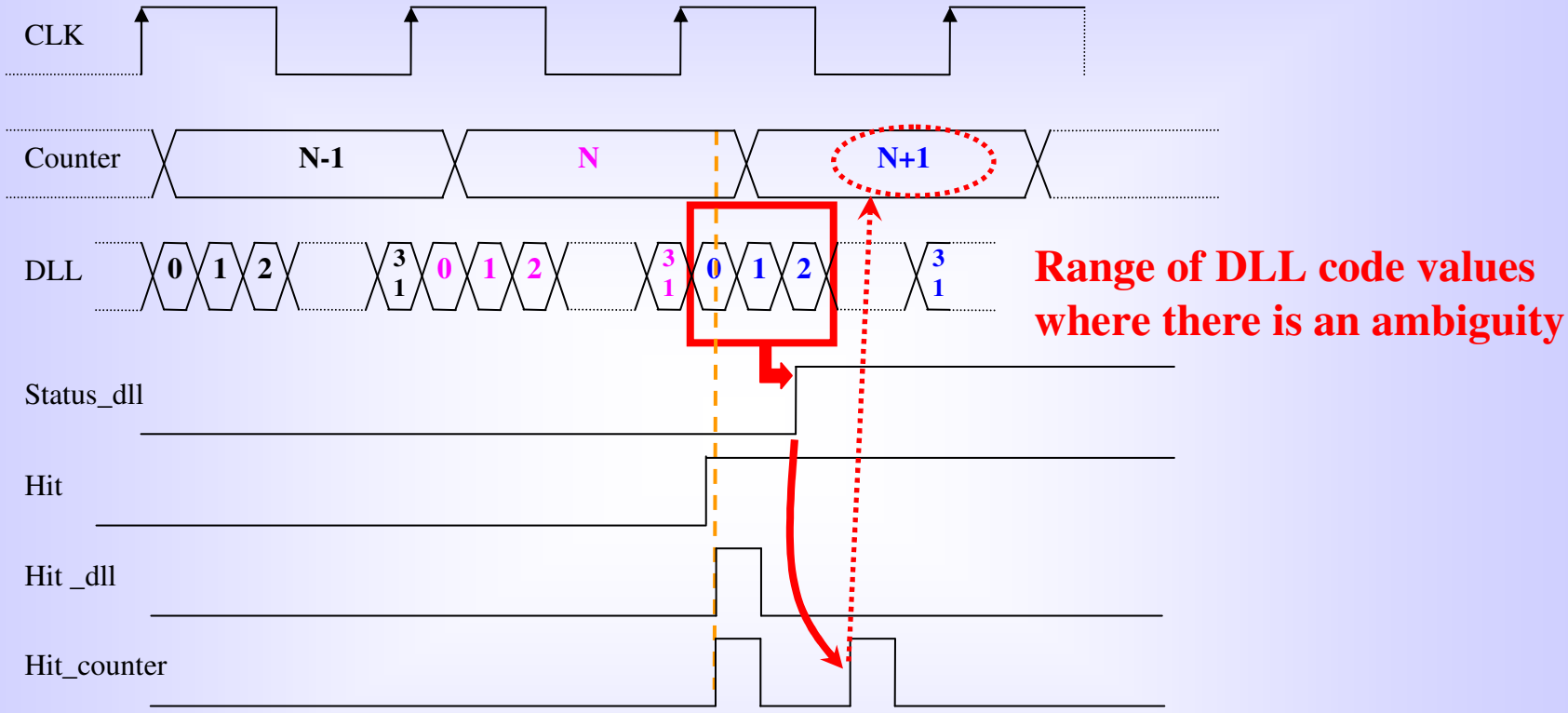
Disadvantages:

- ↗ silicon area (2 counters + multiplexer)
- ↗ power consumption

Principle: production of a 'DLL last cells' flag to delay the counter latch



Event with correction:



Range of DLL code values where there is an ambiguity

DLL code memorized : 0
Counter code memorized in function of DLL code : N+1

} **Code is correct**

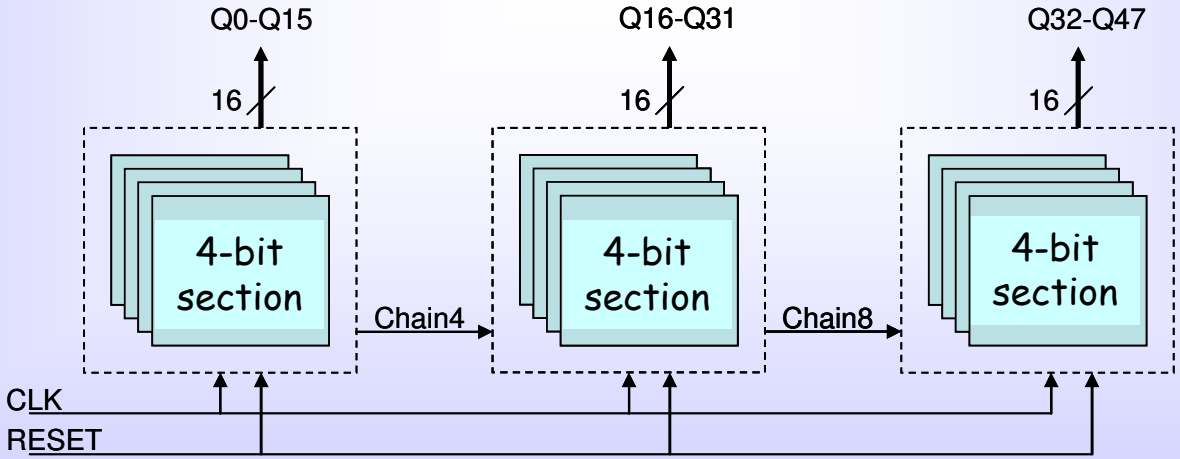
Requirements :

- Operating frequency : 160MHz
- Range : 48 bits (20 days)
- Low consumption
- No transient state

} Code Gray

Optimization between complexity / performance:

↳ counter in 3 blocks of 16 bits each consisting of 4 sections of 4 bits

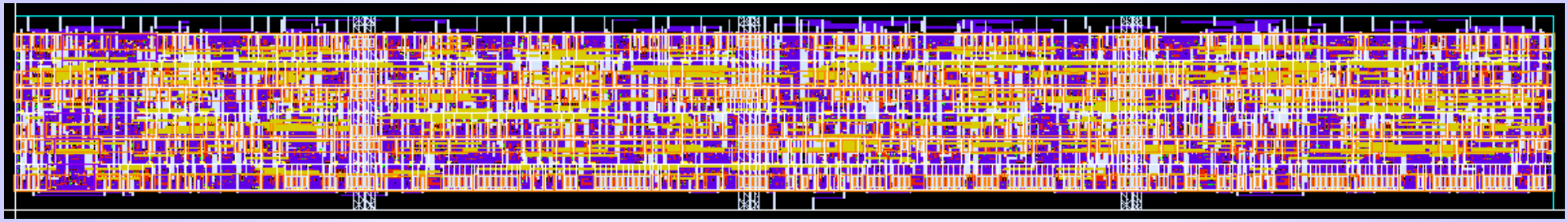


Maximum operating frequency : 200MHz (post layout simulation)

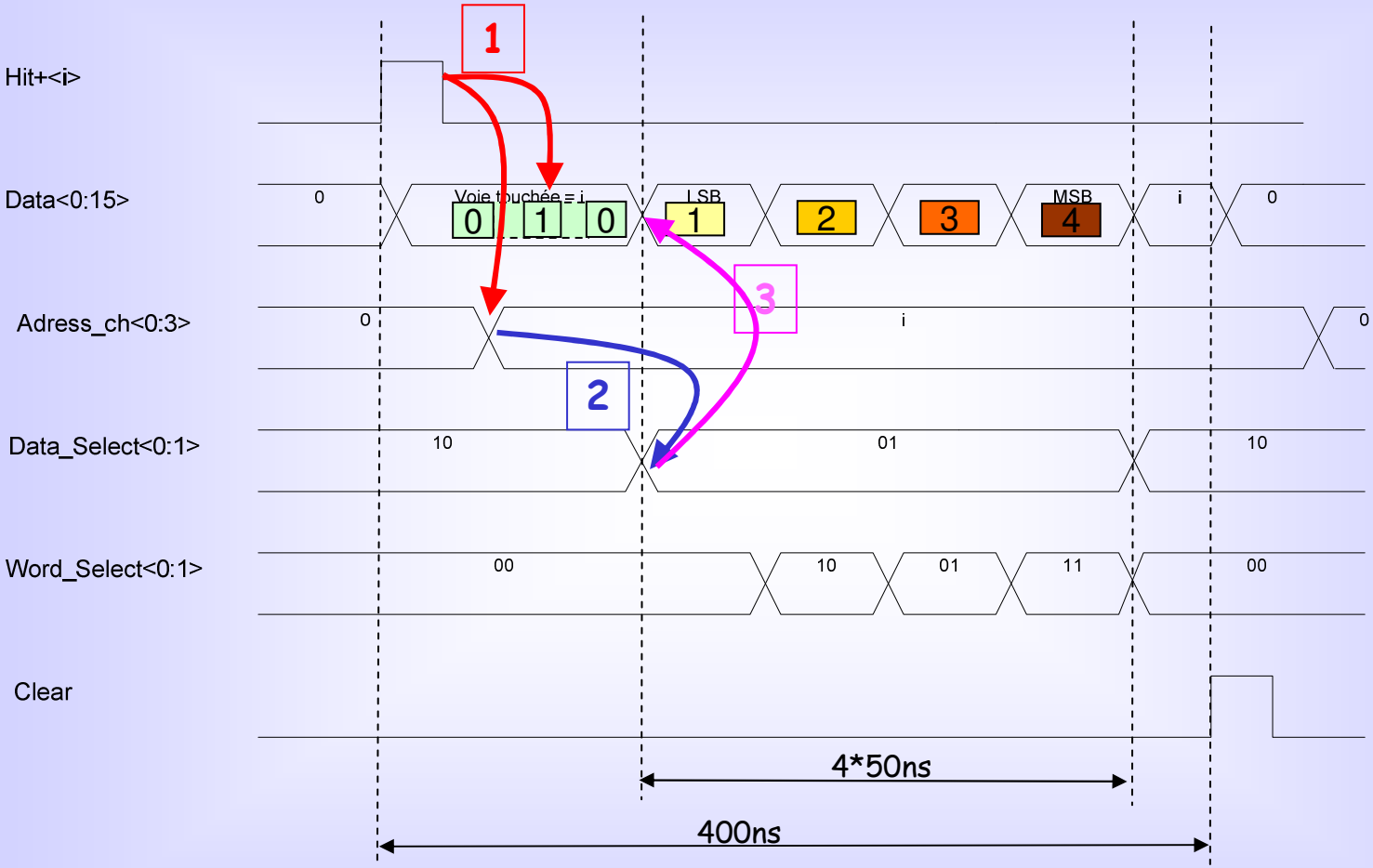
Settling time output < 1.5ns

Size :780µm X 100µm

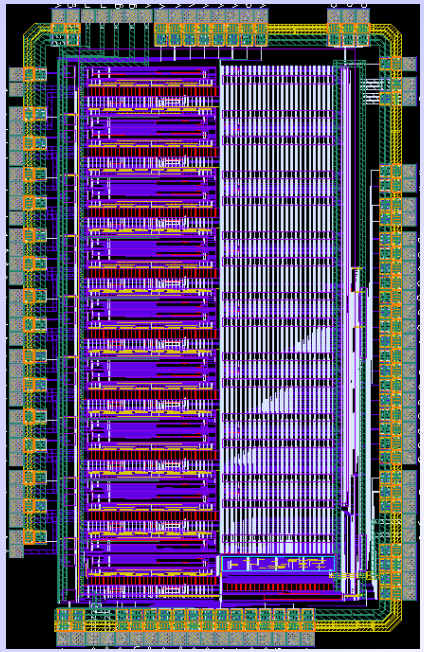
Layout made by Soc Encounter with the help of the IPHC-Strasbourg (Strasbourg / Abdelkader Himmi)



SNATS : readout sequence



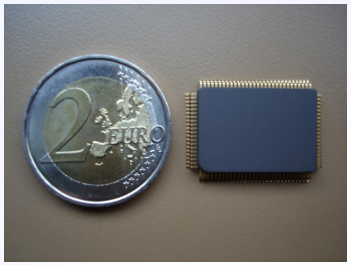
SNATS layout and package

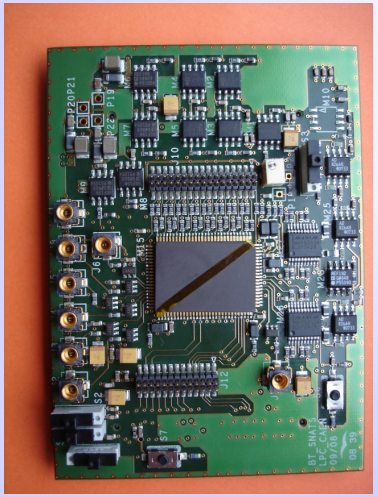


Size : 4467µm X 2853µm

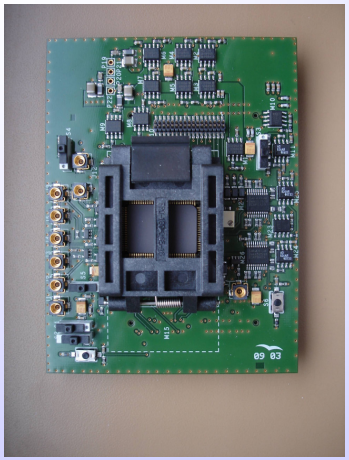
Chip area : ≈ 12.7mm²

Package : CQFP100





test-board for fine tests



test-board for yield tests

Consumption:

- 3.3V supply
- 10mA/DLL + 35mA for the rest
- For 8 DLLs: 115 mA ⇨ P= 380 mW

Clock signal:

- LVDS or single input
- Frequency : 160MHz
- Low jitter : qq ps RMS

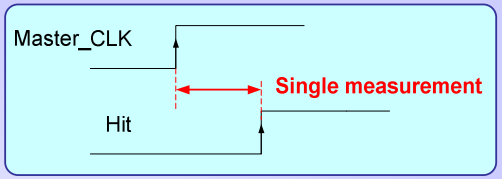
Hit signal :

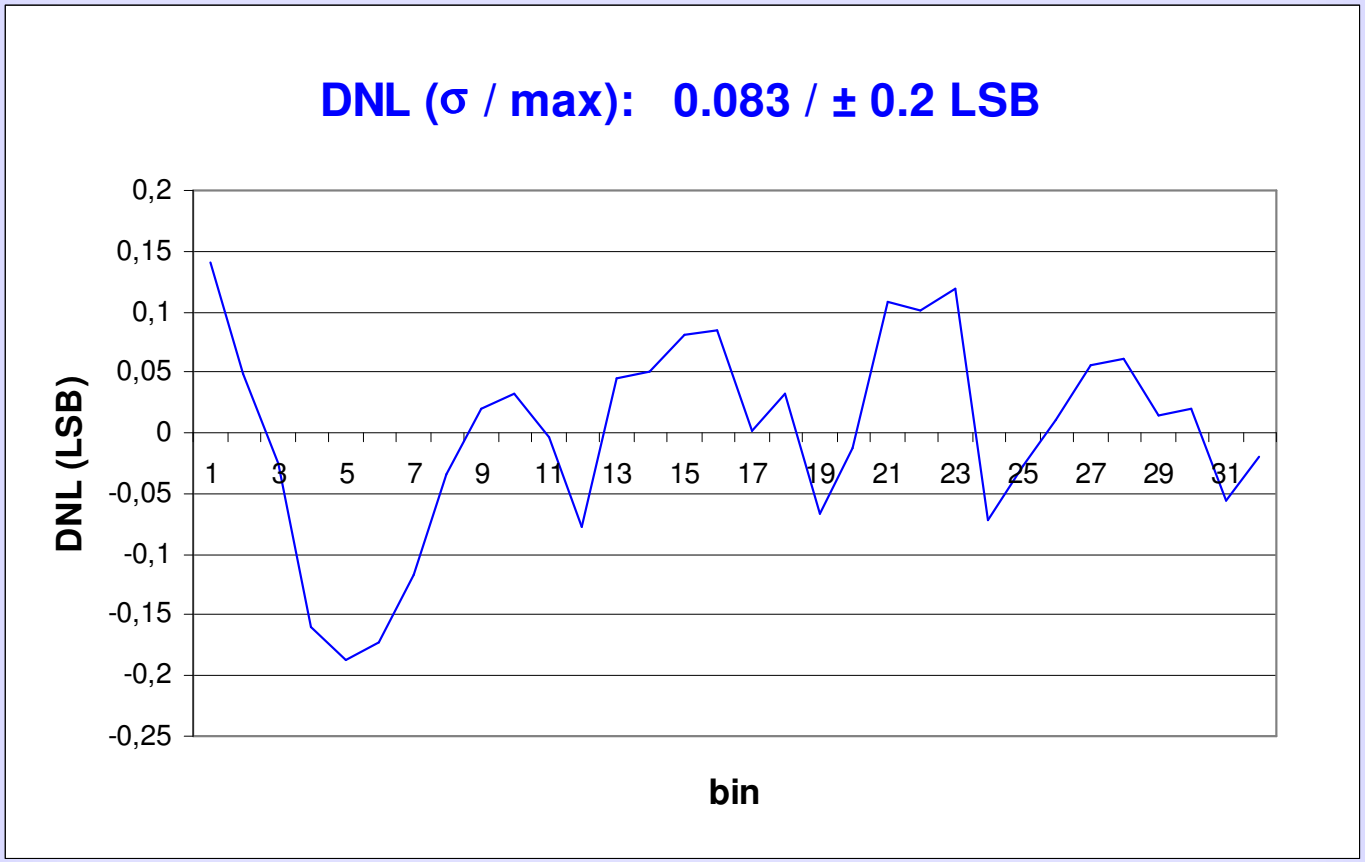
- Input level between 1V and 3.3V
- Trigger on rising edge

Readout and control signals:

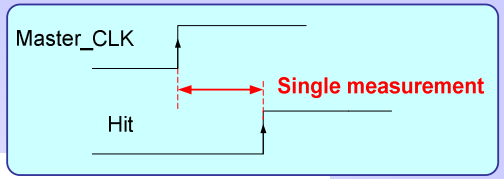
- 3.3V CMOS Standard

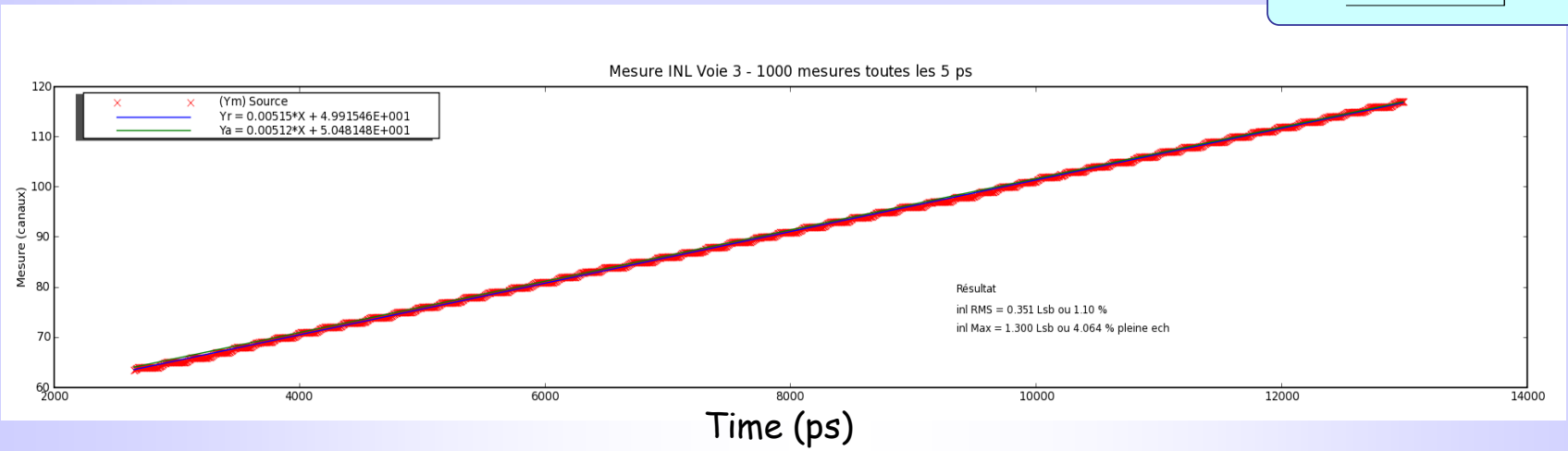
Differential Non Linearity (DNL):



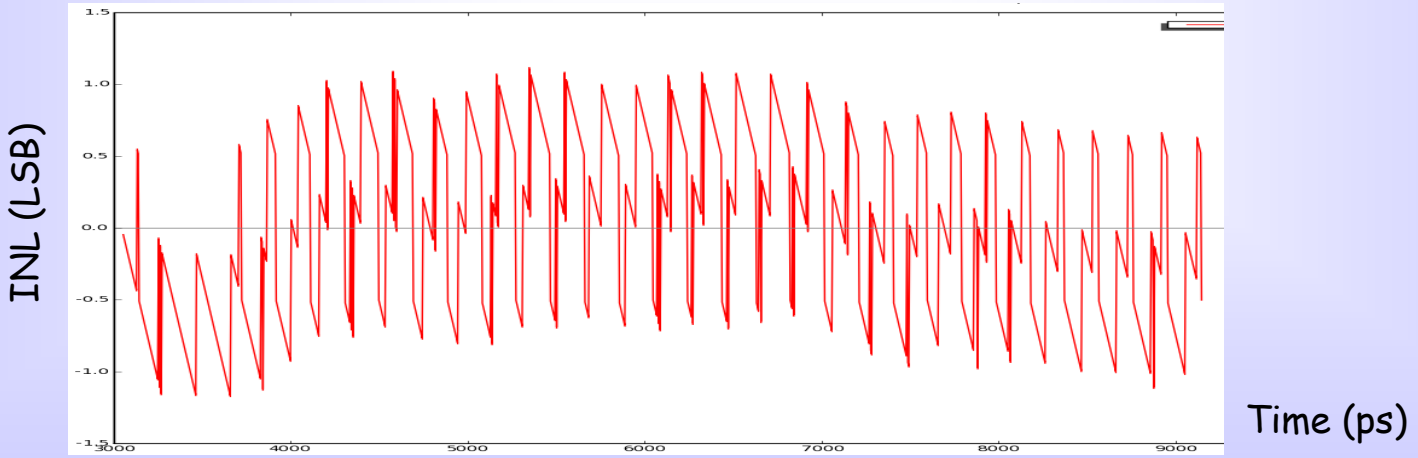


Transfert function:

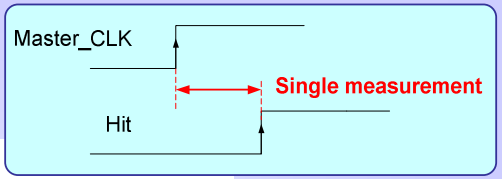


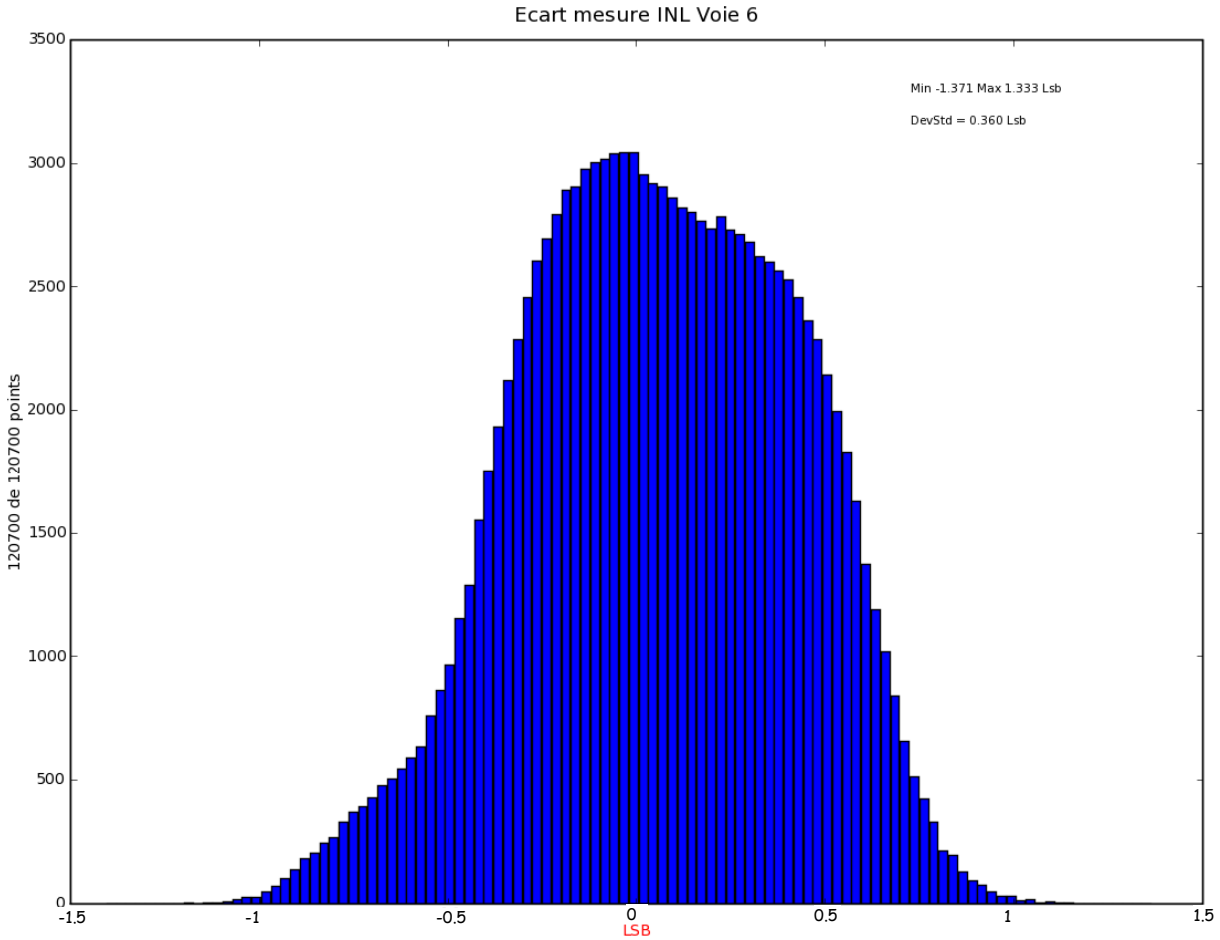


Integral Non Linearity (σ/ max): 0.083 / ± 0.2 LSB

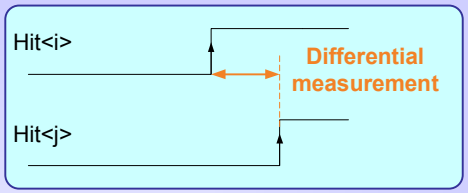


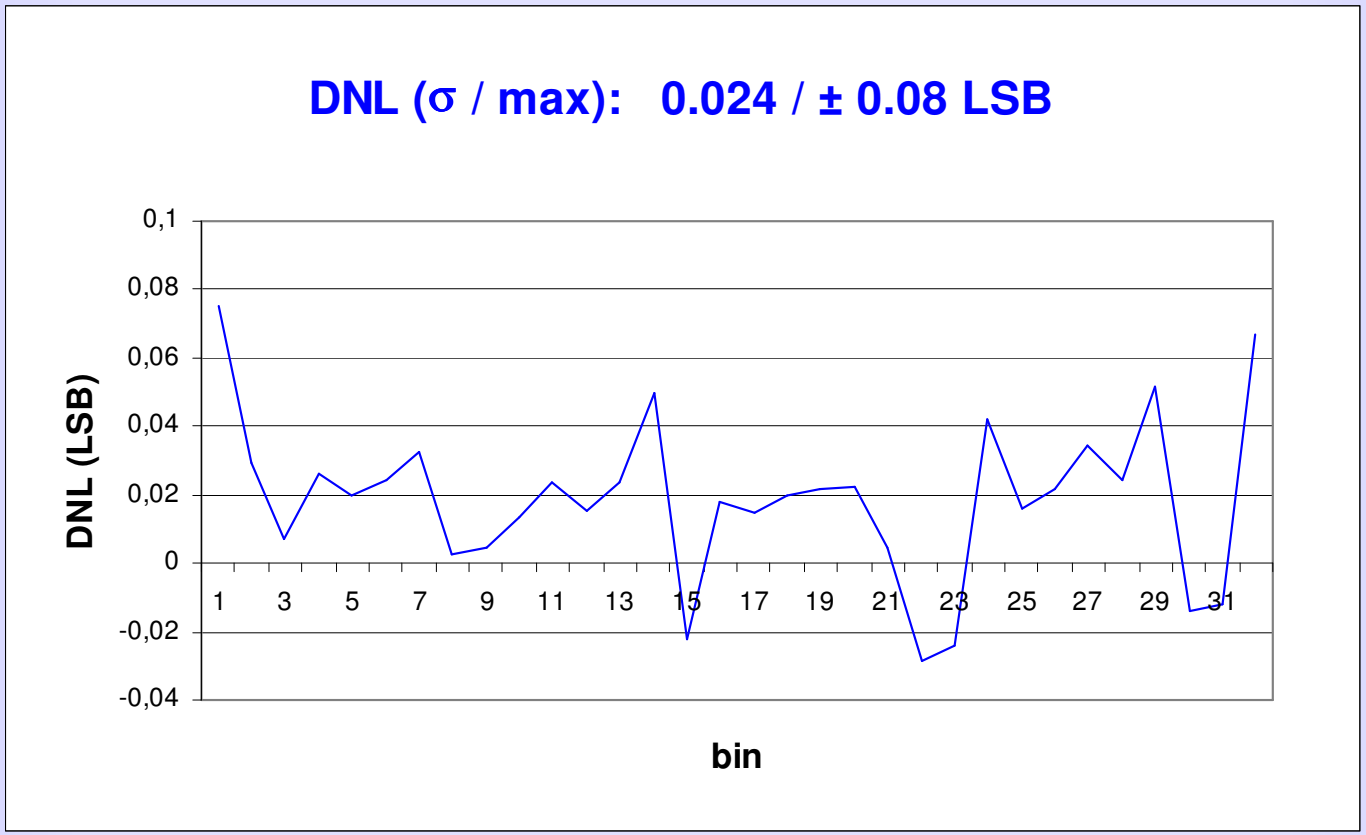
Resolution : σ = 71 ps





Differential Non Linearity (DNL):





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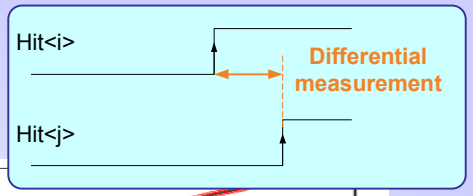
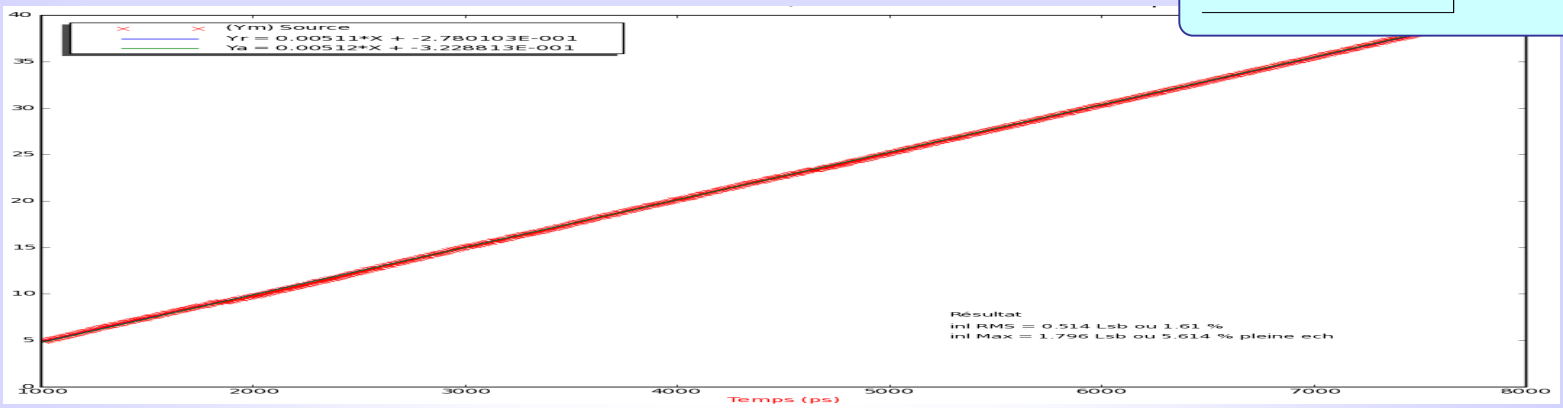
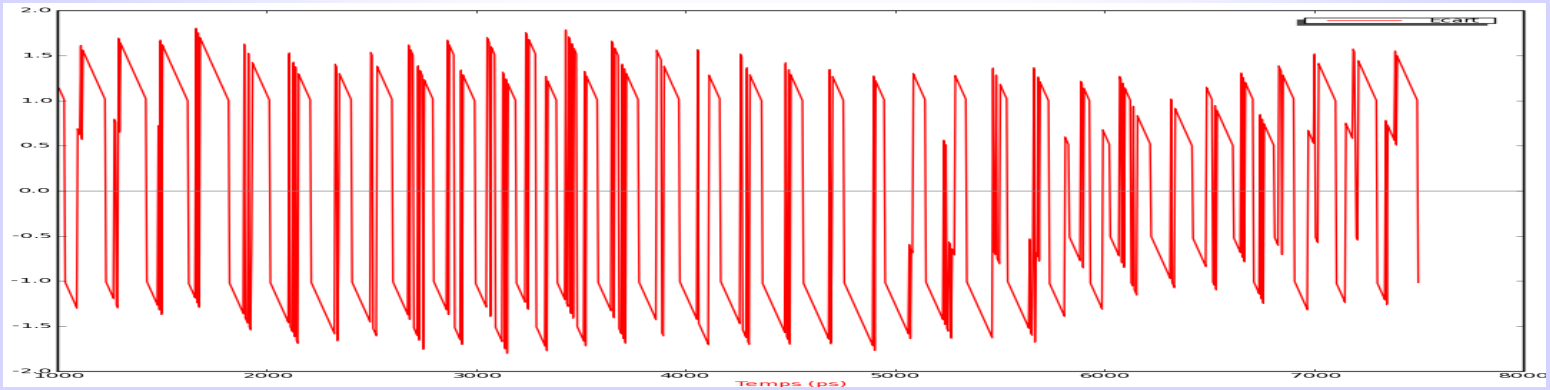




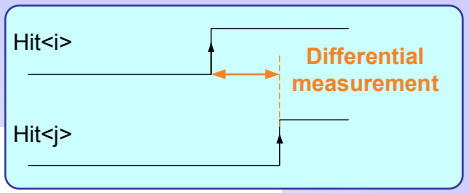
Time interval (ps)

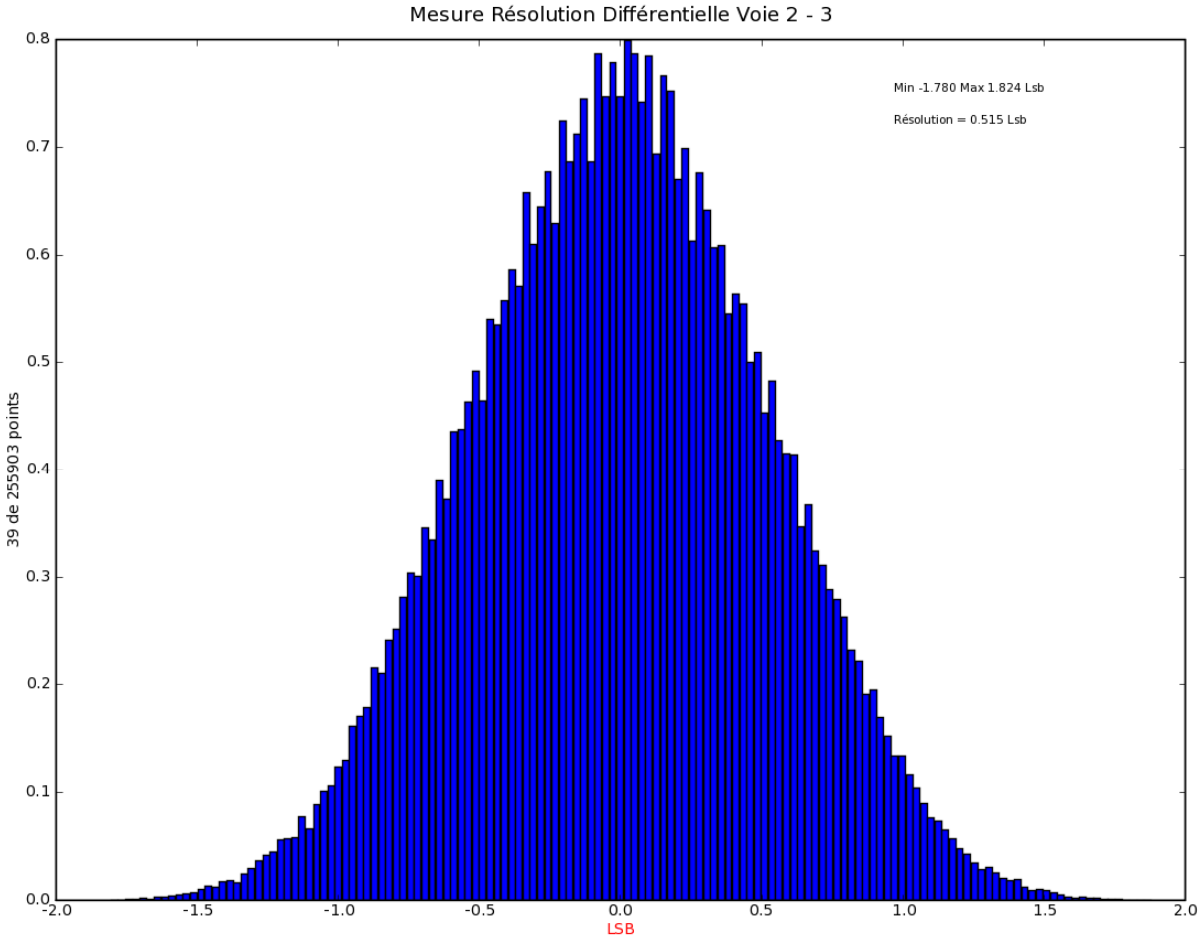
Integral Non Linearity (σ/ max): 0.514 / ± 1.8 LSB



Time interval (ps)

Resolution : σ = 101 ps





Timing characteristics:

Bin size (LSB)	195.3ps	
Clock frequency	160 MHz	⇨ **Dynamic range** ~20 days
	Single channel mode	**Differential channel mode**
Resolution	70ps RMS	101ps RMS
DNL (σ / max)	0.083 / ± 0.2 LSB	0.024 / ± 0.08 LSB
INL (σ / max)	0.36 / ± 1.3 LSB	0.514 / ± 1.8 LSB
Crosstalk	< ±1 bin	

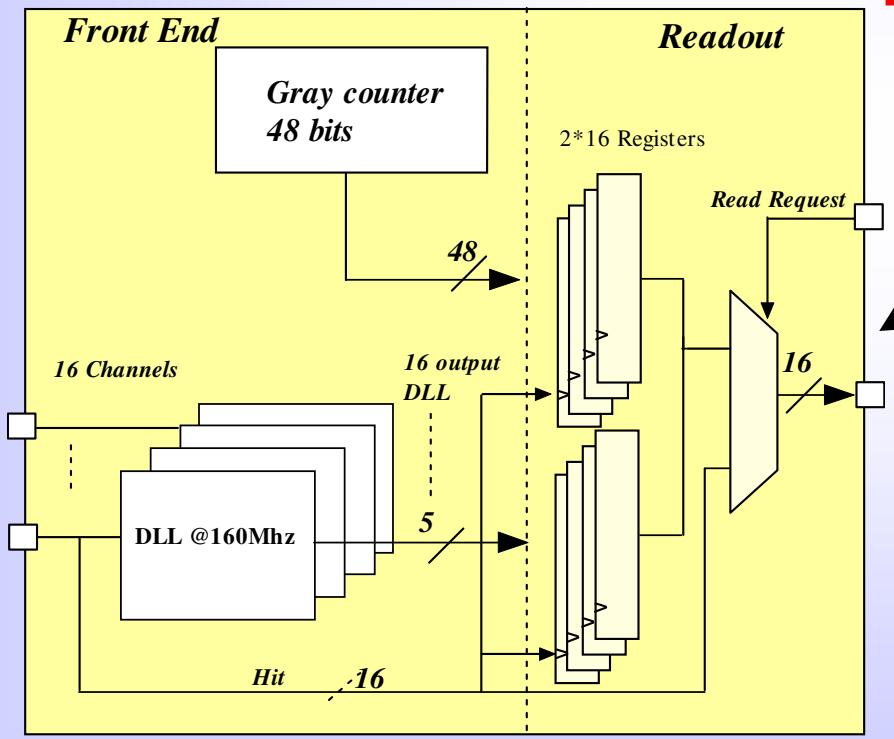
SNATS chip is functional and meets the requirements for the SuperNEMO calorimeter

DNL for single mode is high and must be improved
↳next submission in 2010

Stakes: High counter rate detectors

- INL, DNL, resolution … : same requirements.
- Increase the Input data rate up to the Mhz per chip per channel.
  - SNATS: 2.5MHZ per channel but ~150 kHz per chip

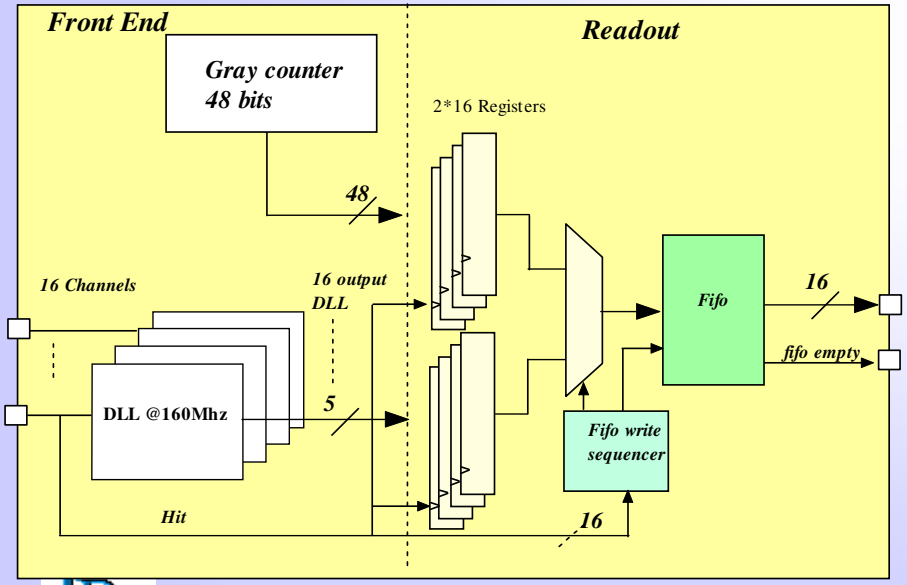
Need to reduce dead time due to transfert protocol between Asic et Pga = 50 ns per 16 bit word



2 options (over many others …)

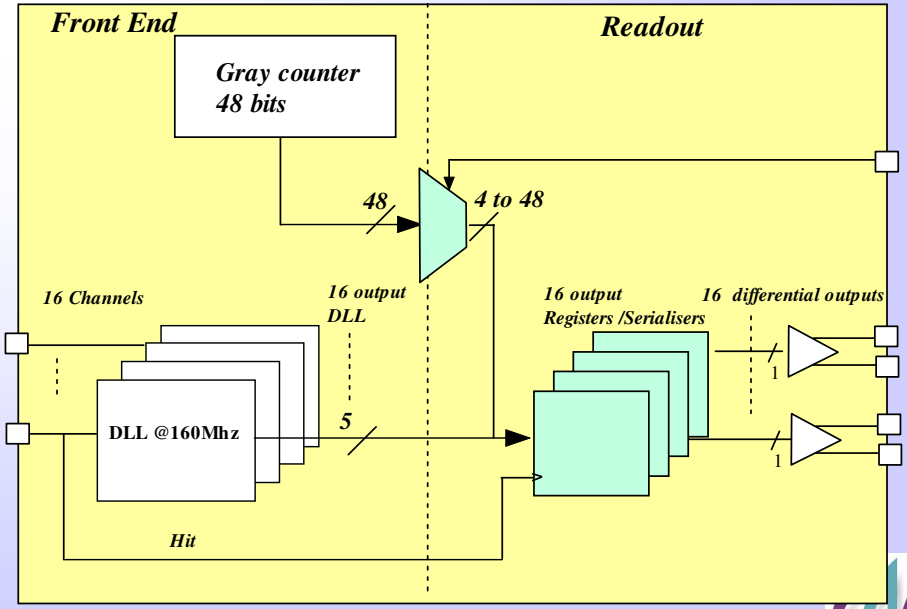
- Keep almost the same design by just adding a fifo at the output.
  - ↳ increase the input channel rate in burst mode but keep the average readout rate as the previous version.
  - ↳ The fifo size is costly.

- Max performance :
  - ➢ Mhz/channel in burst mode but limited by the size of the fifo.



- Keep the gray counter inside the Asic with an output variable bus width set by user to reduce the amount of data to be transferred. The gray counter is duplicated inside the associated PGA.
  - ↳The serial output is synchronous to the clock to ensure the matching between the 2 counters.
  - ↳ 16 differential output channels @ 80 Mhz (160MHz?).

- Max performance
  - ➢5 DLL bits + 4 gray bits + start bit = 10b @ 80 Mhz = 8Mhz input rate !
  - ➢ Link to performance of the readout acquisition



The end