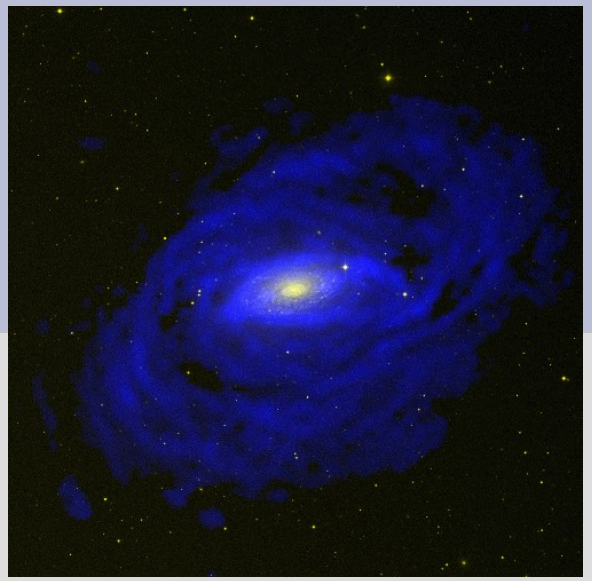
BAO project in radio



BAO Aquisition system status

Electronic chain schematic view

8 dipôles → LNA → Mixer → ADC → FFT en temps (Re, Im, f)

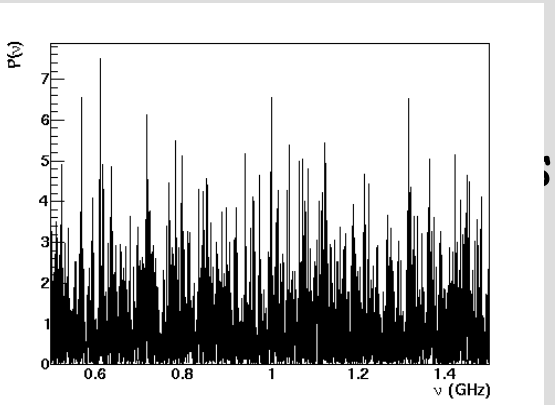
X 1024

Cylindre 1

Cylindre 2

Transposition Regroupement par colonne de fréquence

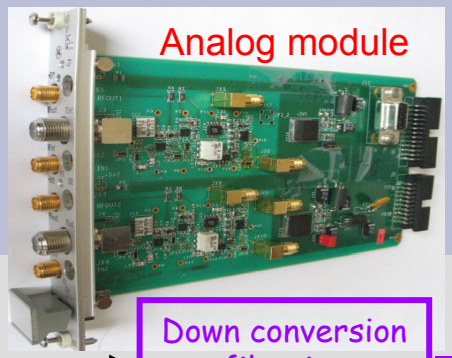
FFT en y Corrélation le long du cylindre

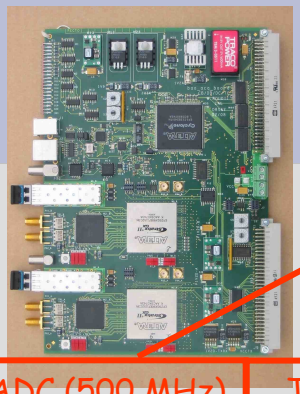


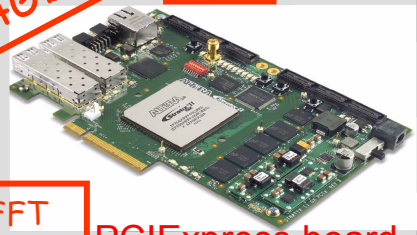
F sinα/λ

Corrélation classique en x entre cylindres

Electronics chain







X 4

Down conversion filtering

2nd

2x4Gbit/s

PC

Antenna board 4 dipoles

128 dipoles

X 4

Antenna board 4 dipoles

X 4

Down conversion filtering

2nd

ADC (500 MHz) 4 channels

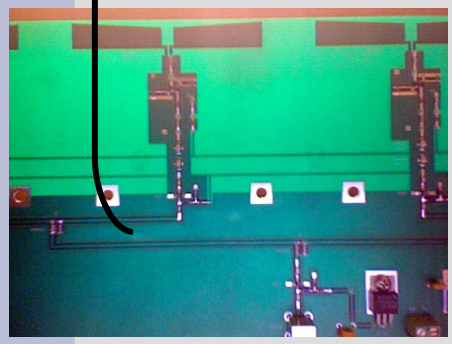
Time FFT FPGA

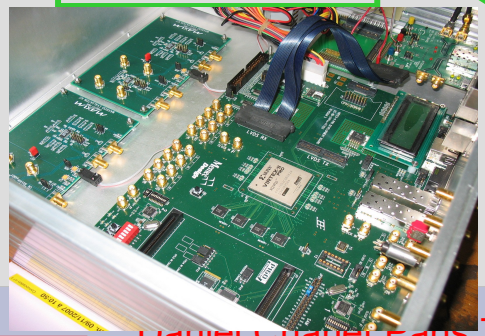
2x4 Gbit/s

Spatial FFT (FPGA)

X 8

Clock distribution





ADC (500MHz) 4 channels

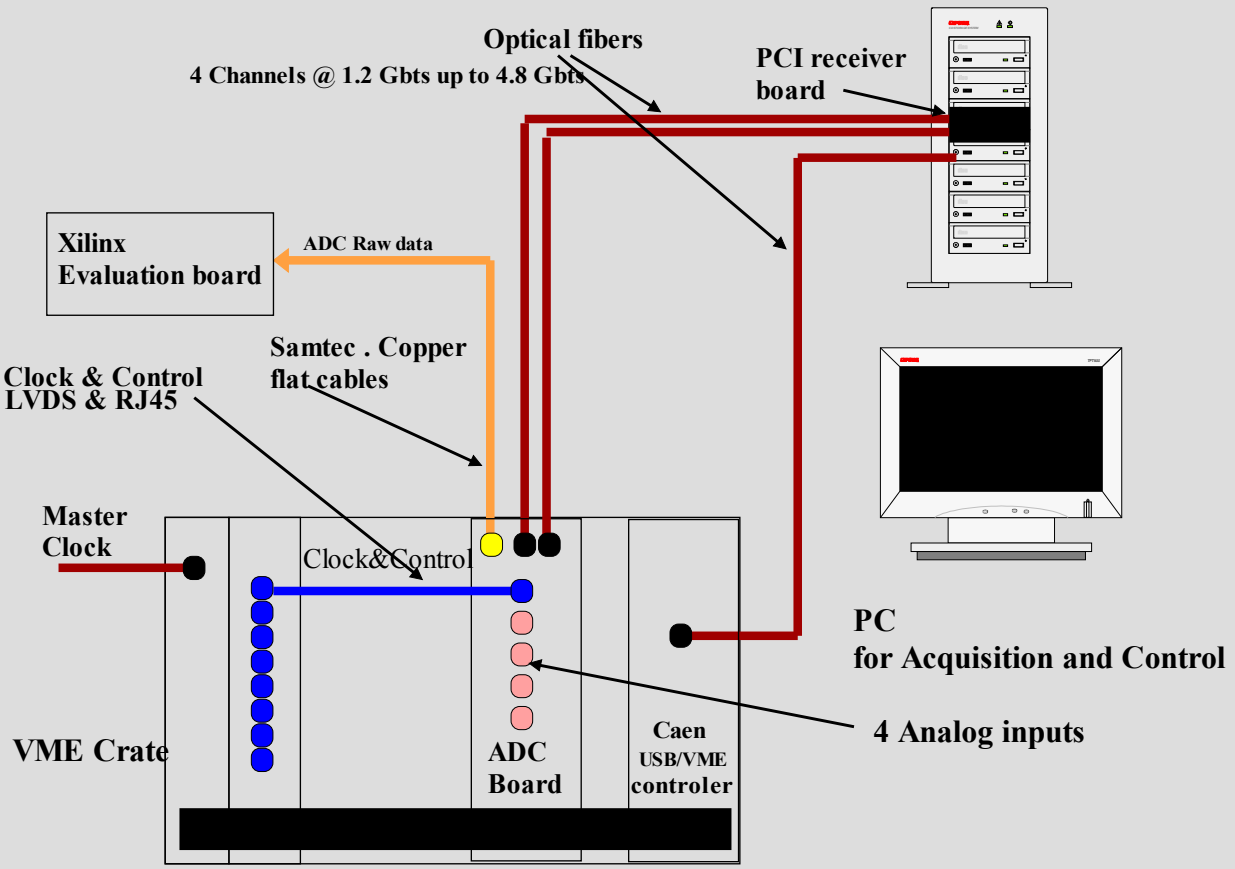
Time FFT FPGA

2x4.Gbit/s

2x4 Gbit/s

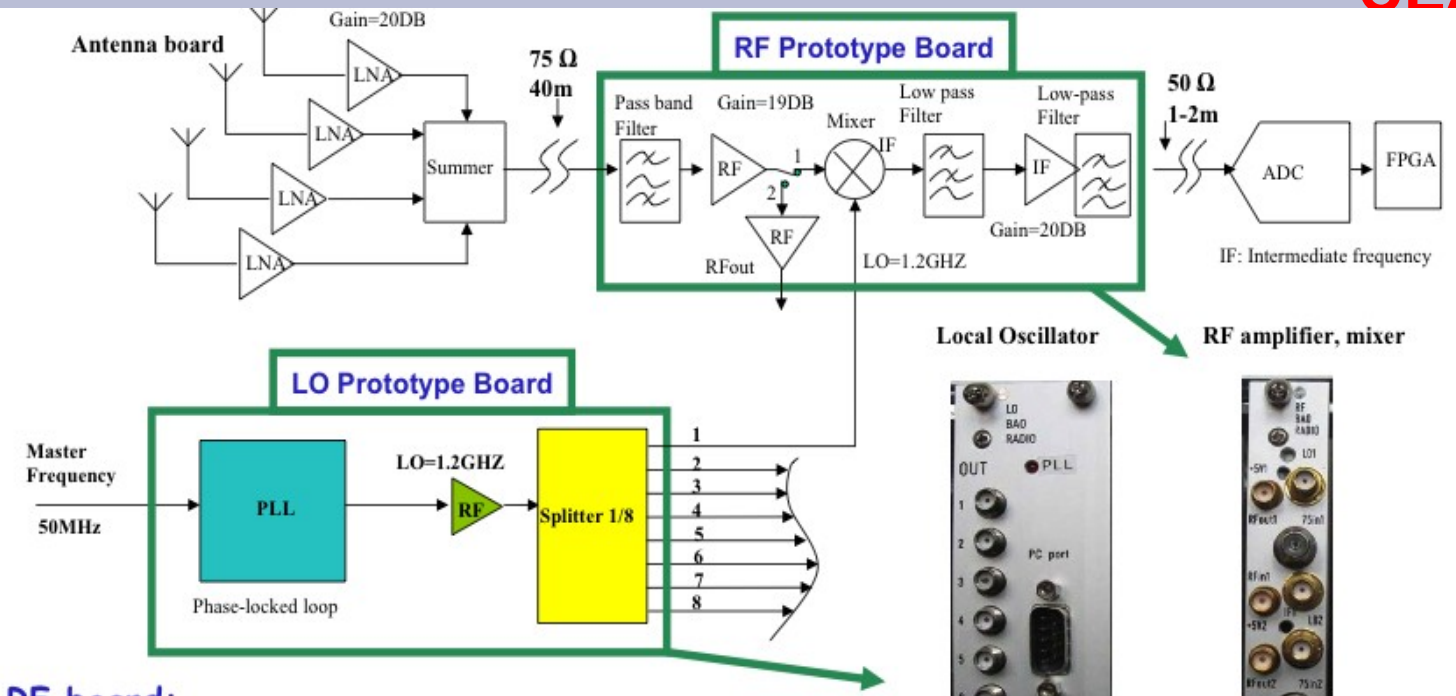
PC

Interconnection Design



Analog chain for RF prototype board

CEA irfu

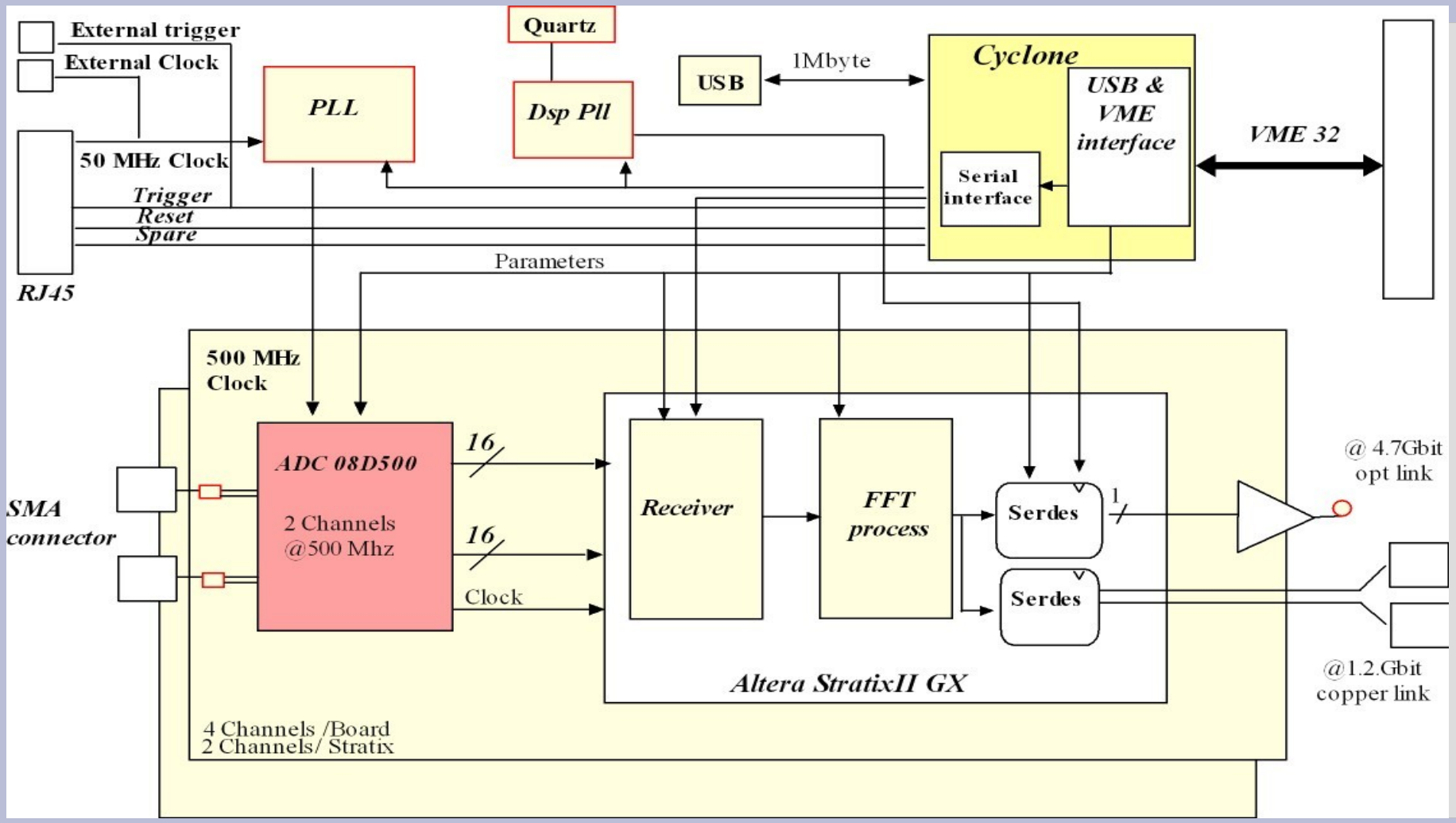


RF board:

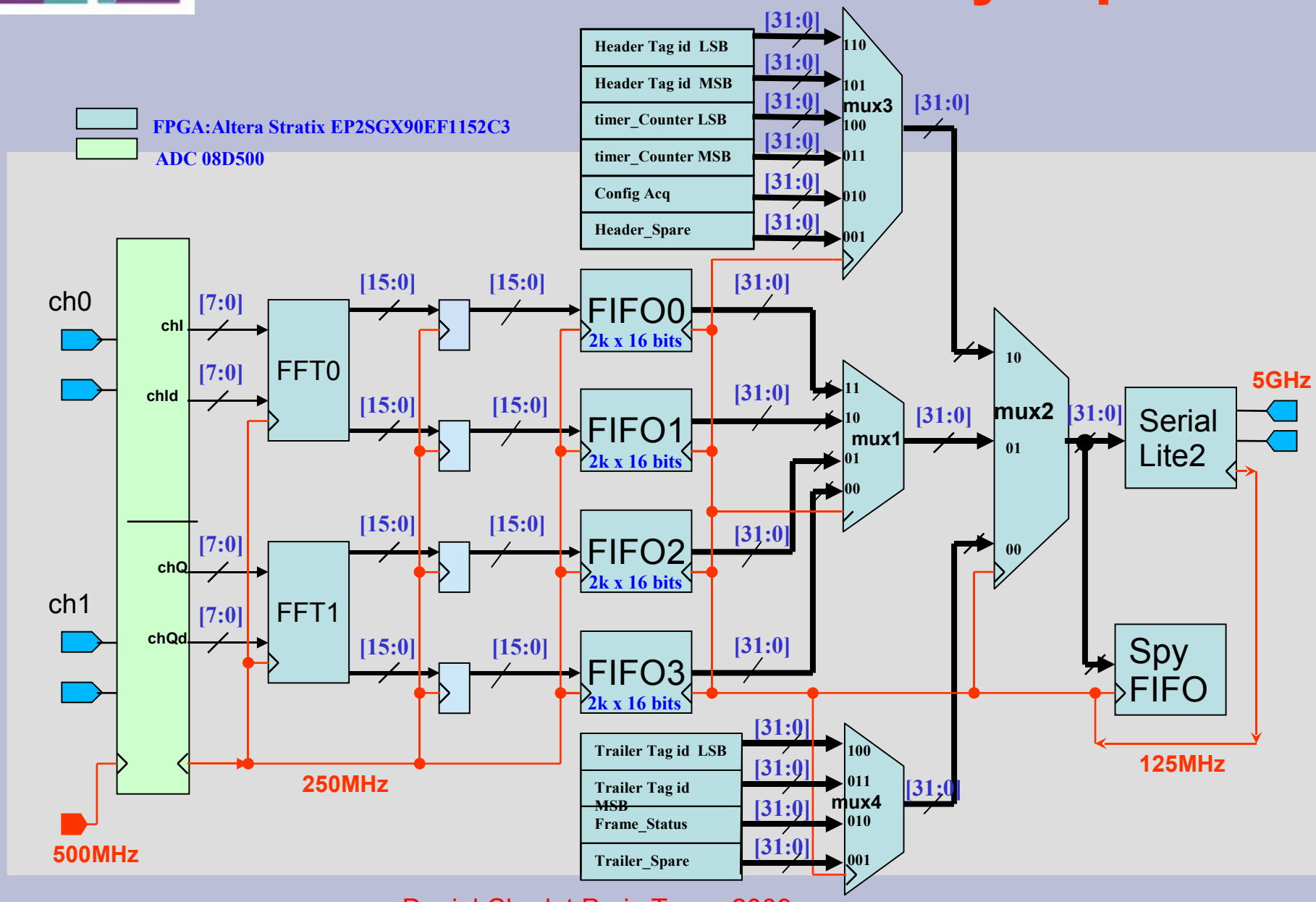
- 75Ω/50Ω inputs
- 2 channels per board
- Possibility of by-passing mixer to test the under-sampling approach.
- Possibility to "tune" the pass band filter

Front panel plug-in (3U EuroCard)

LAL ADC board Synoptic

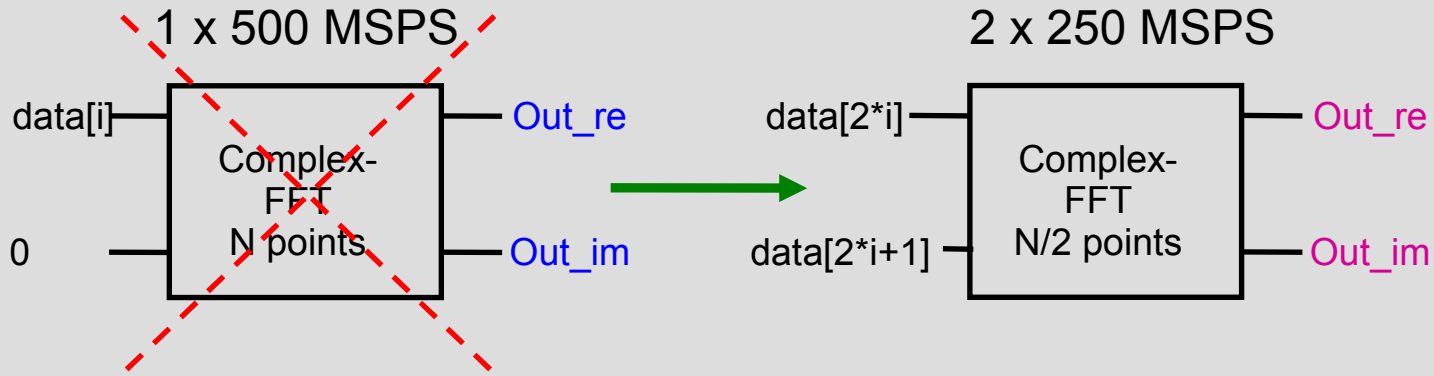


ADC board FPGA Synoptic



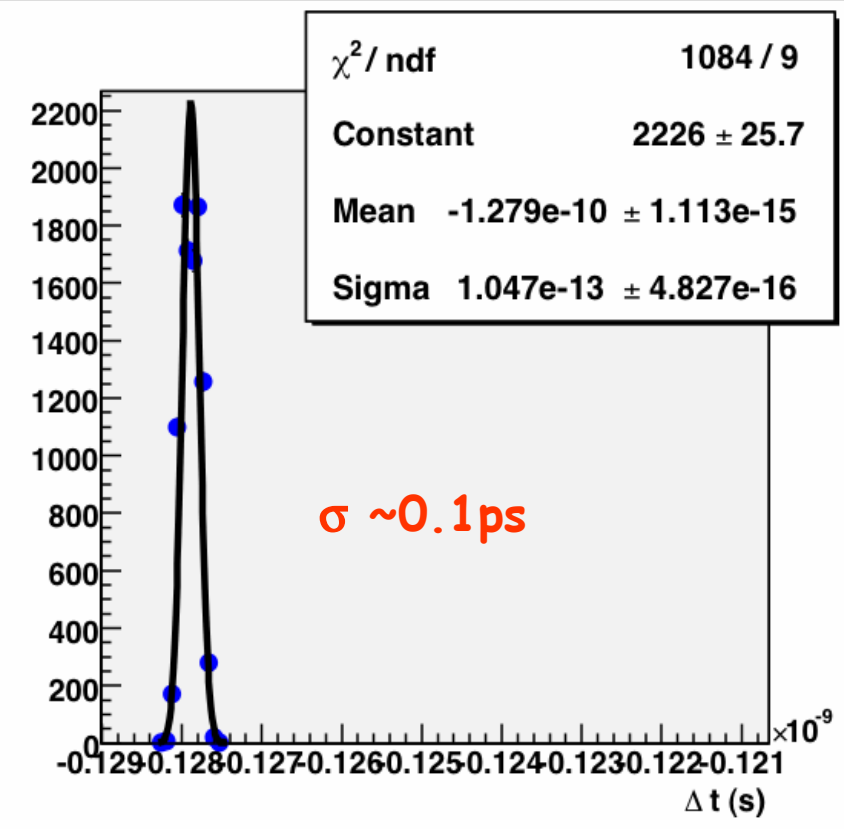
Post ADC processing: Temporal FFT

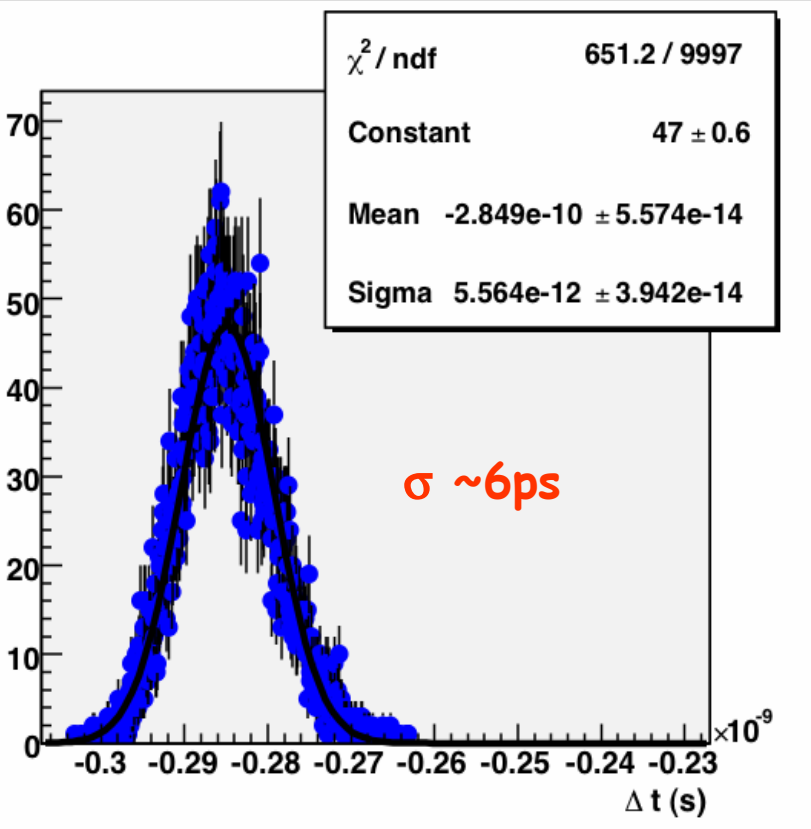
FPGA Implementation of real-FFT using a IP Core:
to save hardware resources, we use a N/2 points complex-FFT to compute a N-points real-FFT



the real signal s[i=0:N-1] is transformed into a complex signal : c[i] = s[2*i]+j*s[2*i+1]

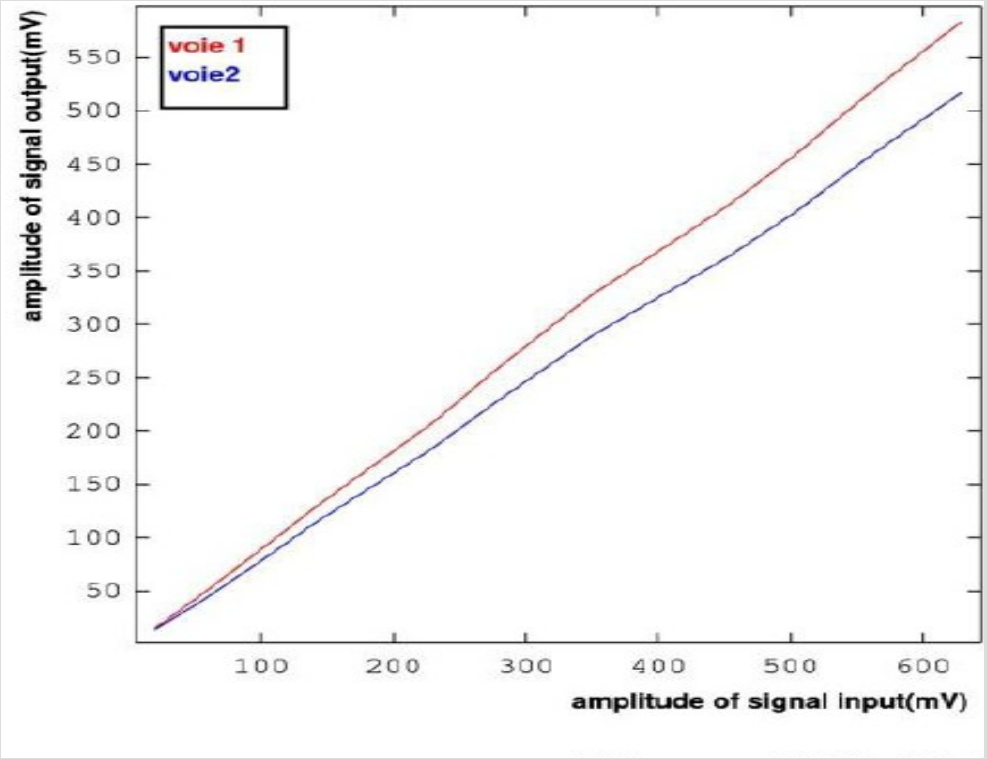
Analog characteristic: 1
Time resolution



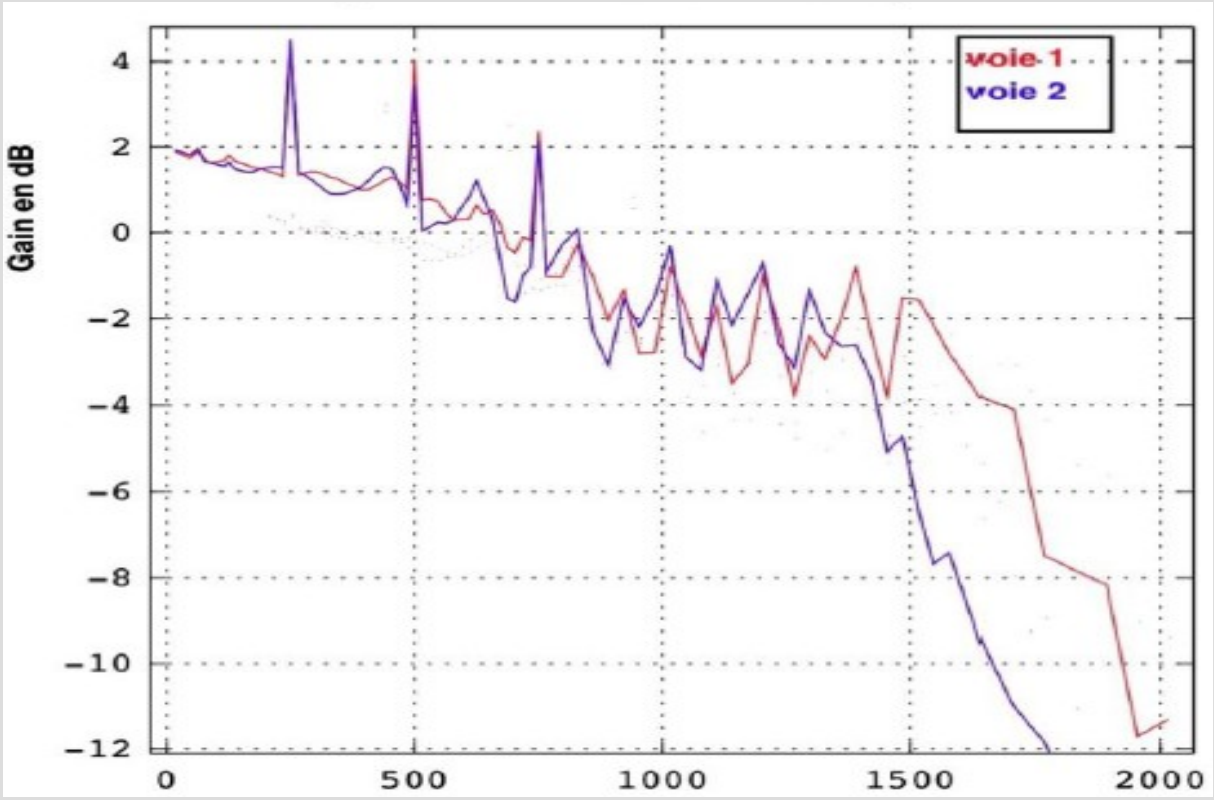


Analog characteristic :2 Linearity

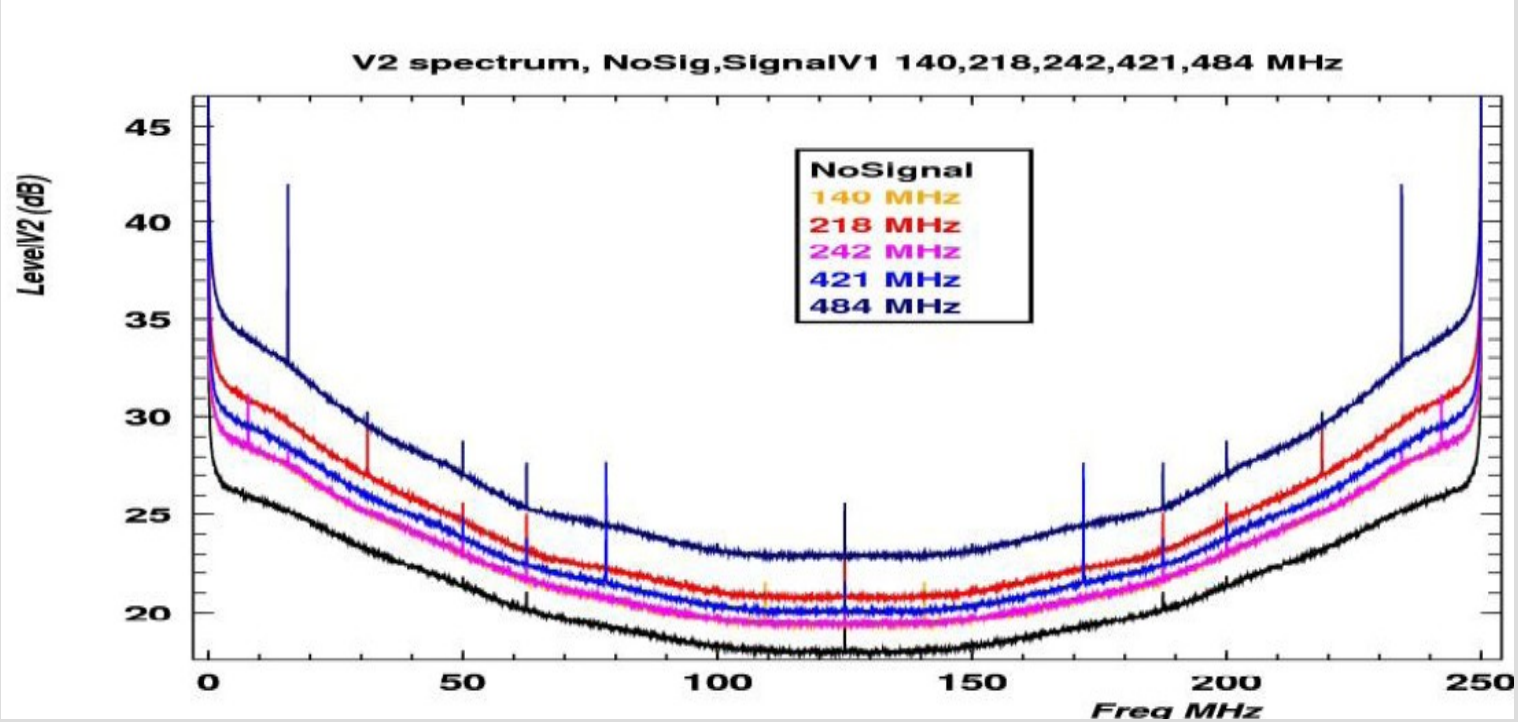
Linearity at 1.4GHz



Analog characteristic : 3
Bode diagram



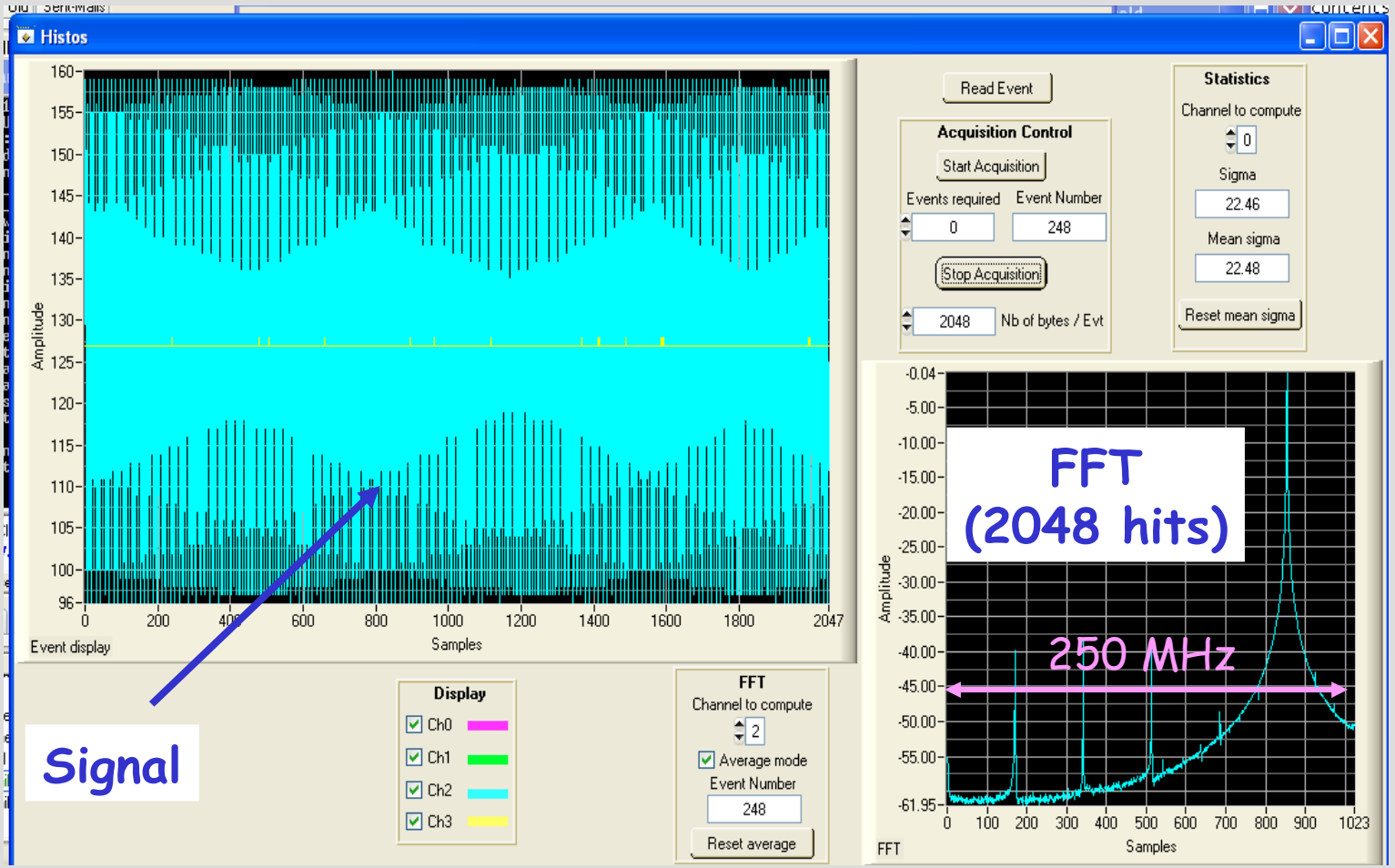
Analog characteristic: 4
Noise signal & diaphony



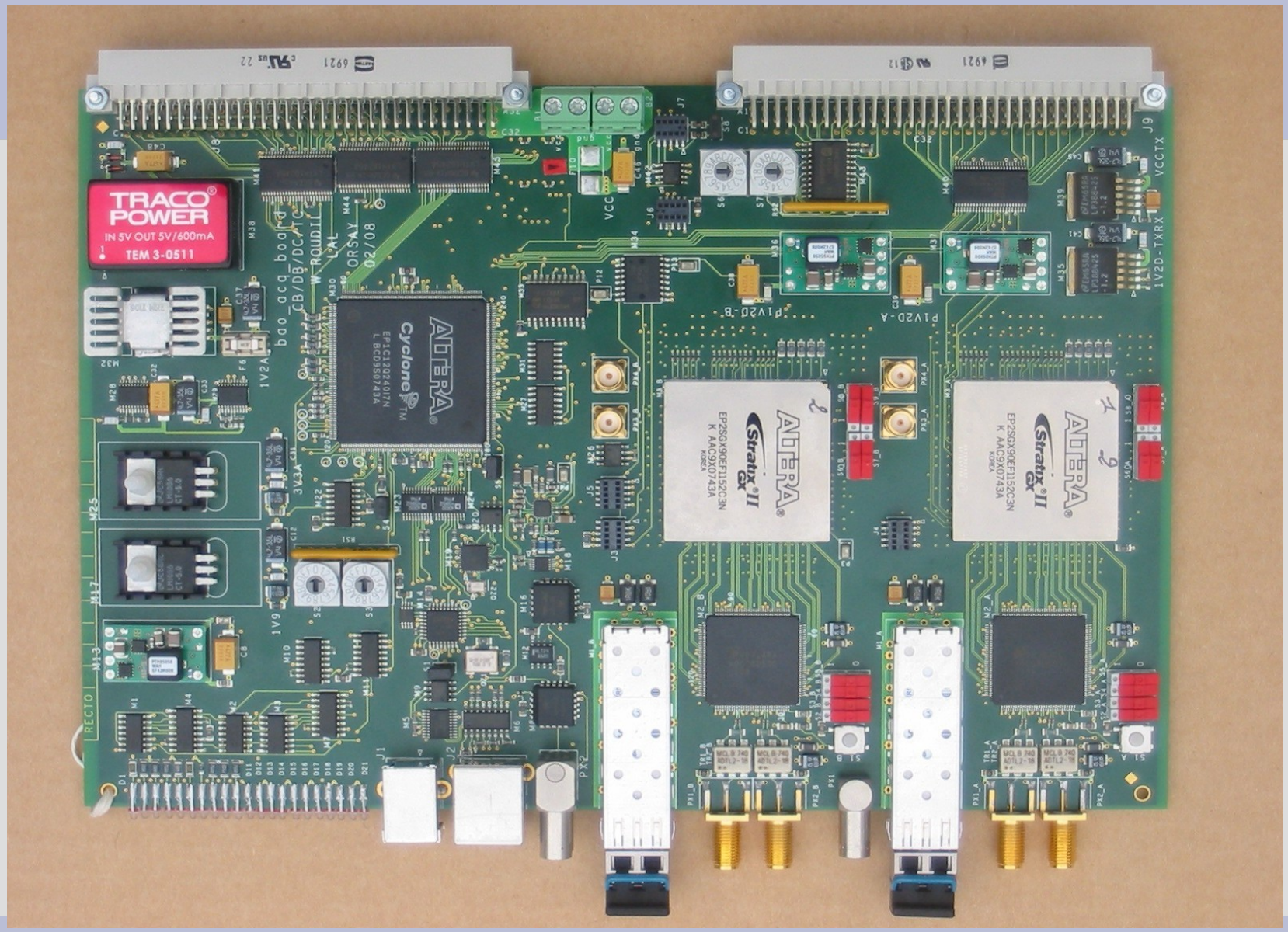
ADC board: Under-sampling

- Tests for different frequencies
- Under-sampling up to 750 MHz

f_{in}= 300MHz
Amp= 500mV
Gain= -10dBm
Fiber: 5Gbit/s



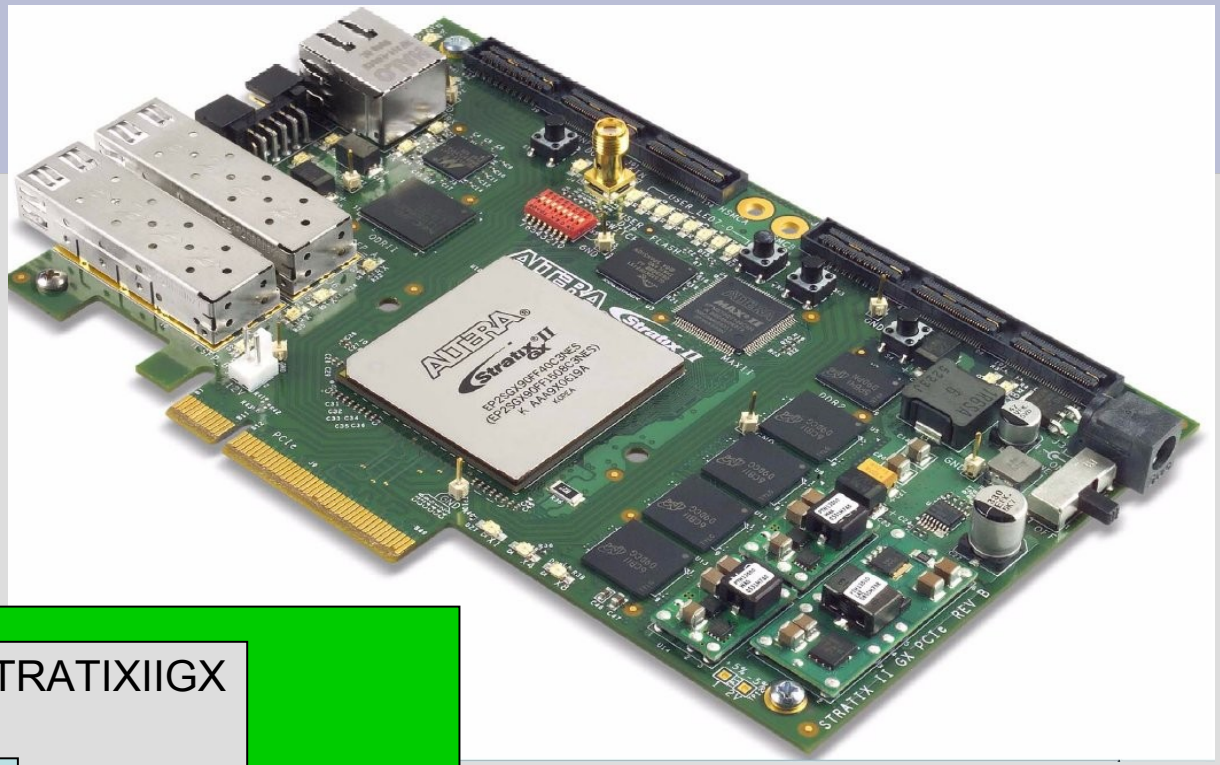
LAL ADC board

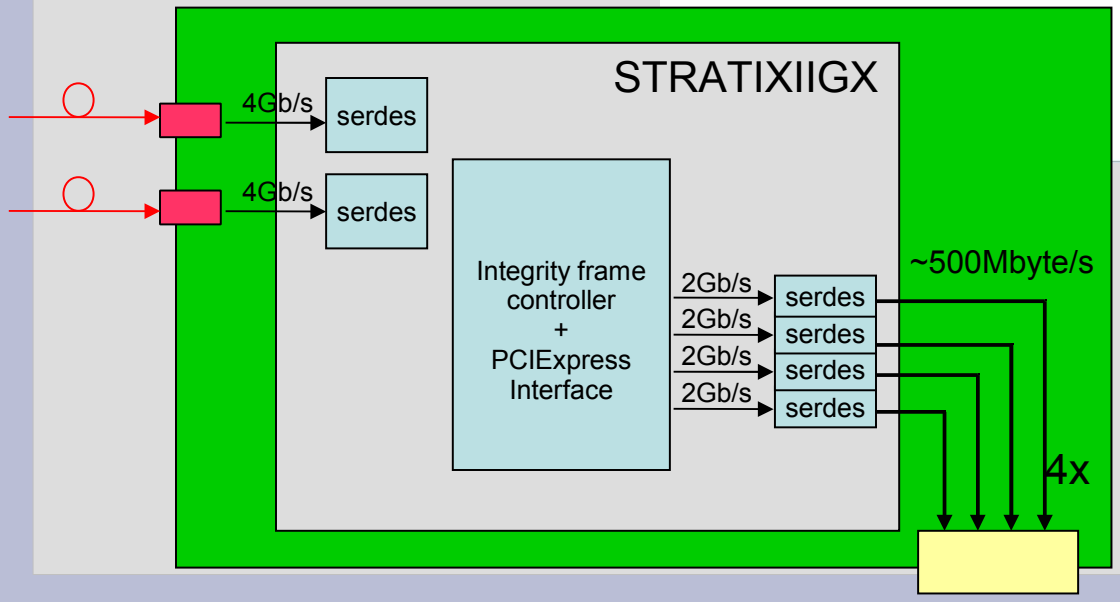


ADC board status

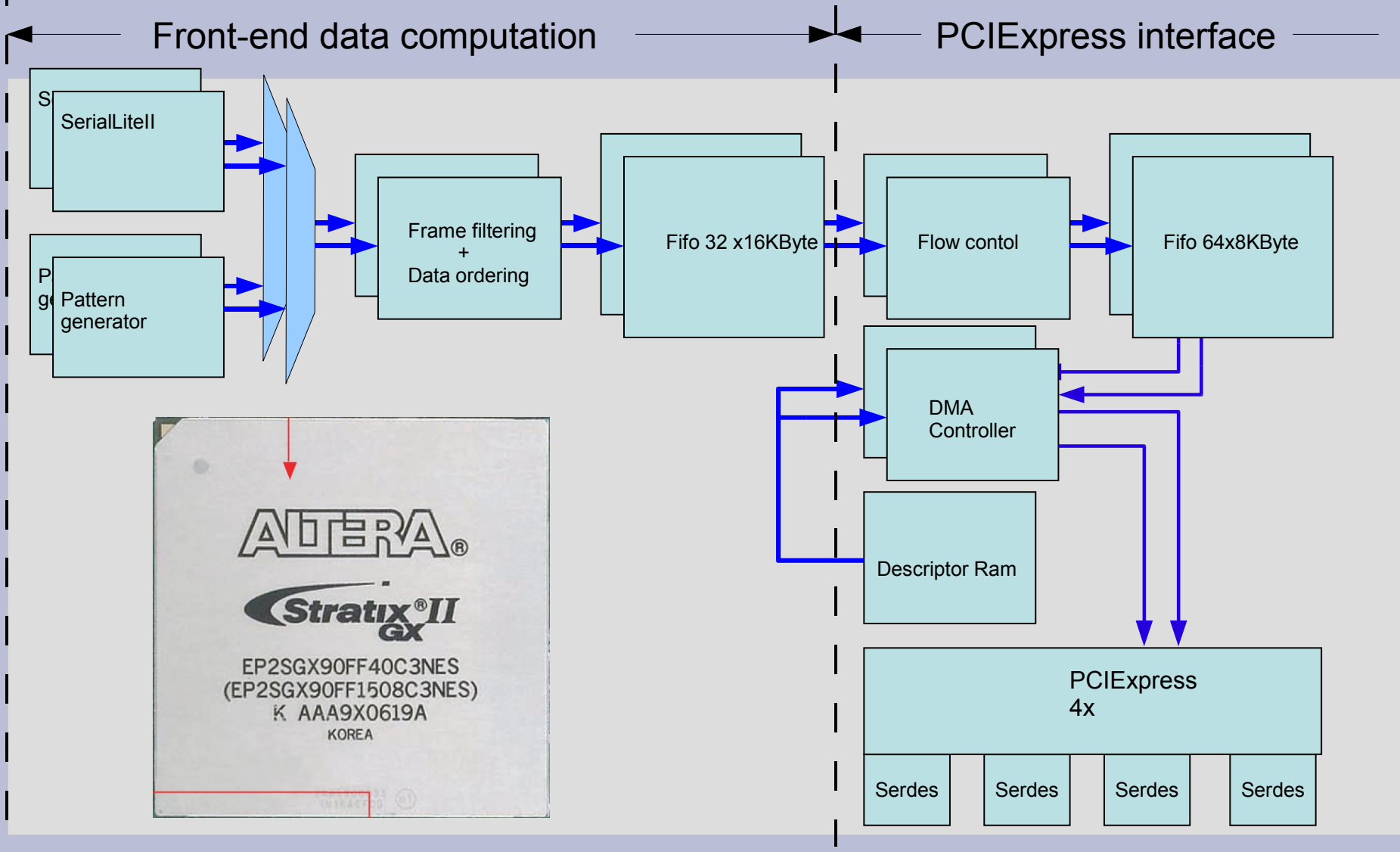
- ADC board 1.1 :
  - 2 in orsay 1 Saclay.
  - Tested :
    - PPL
    - Hardware VME, firmware not complete.
- ADC board 1.2 :
  - 2 in orsay.
    - Bode diagram of the 2 channels.
    - Paramaters transfert by DISCLK.
  - Components for 7 boards.
- VME rack OK.
-

PCIExpress evaluation board



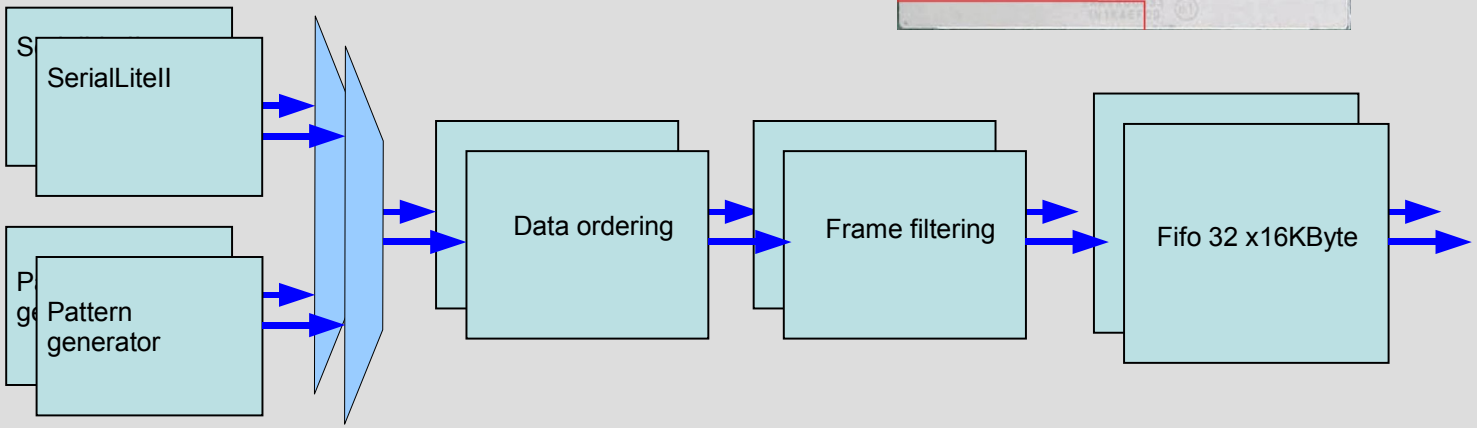


Synoptic FPGA PCIExpress Evaluation board

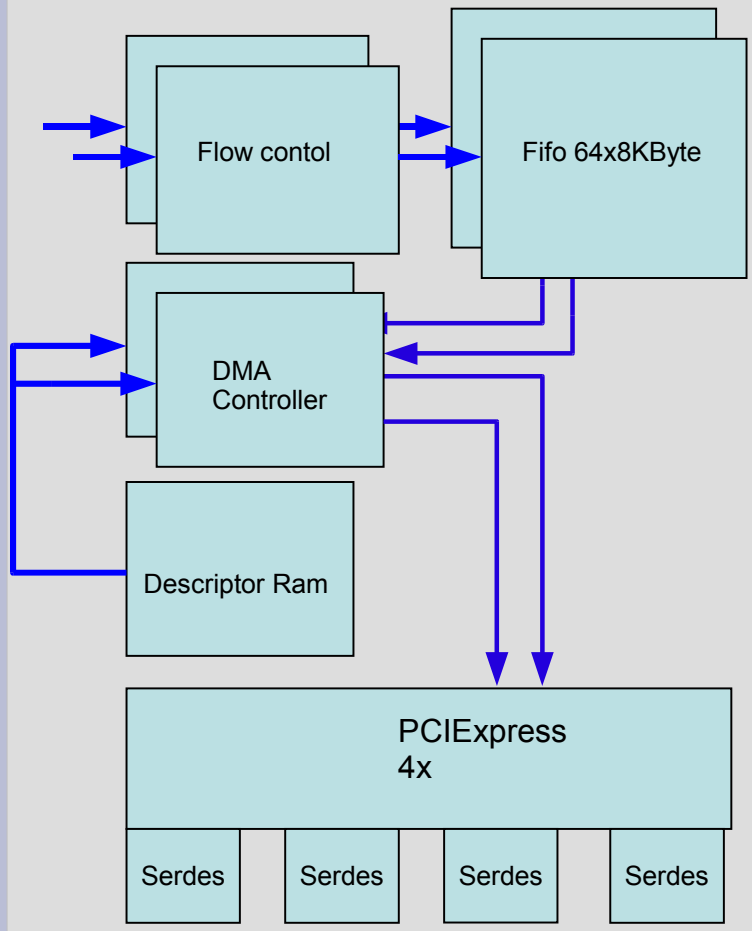


FPGA synoptic: Front-end data computation

- Link interface: SerialLiteII.
- Pattern generator.
- Data ordering.
- Frame filtering.
- Buffering: FIF0 64KByt

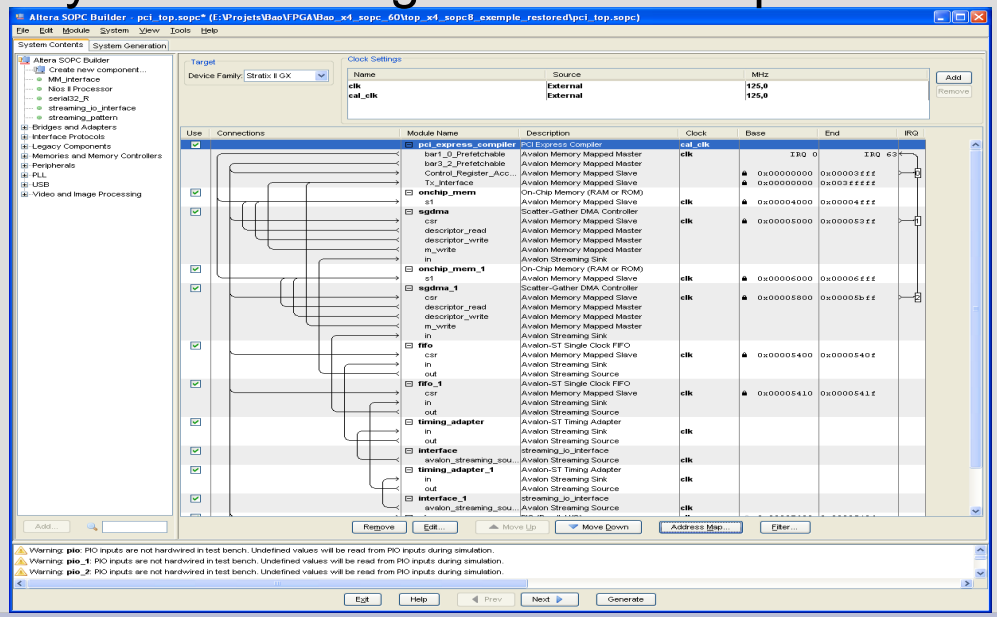


FPGA synoptic: PCIExpress interface



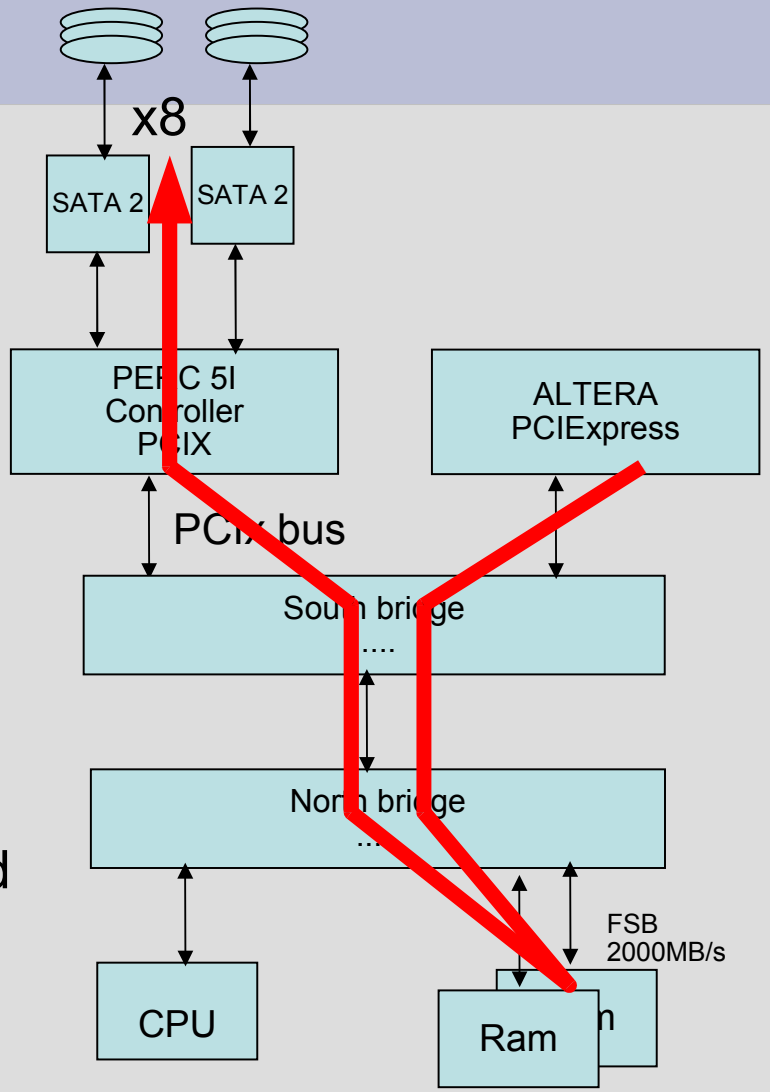
- FIFO buffering
- Scatter-gather DMA
- PCIExpress:
  - End point
  - 4X

System On Programmable Chip module



Aquisition test

- Poweredge 2900
  - 2 hardware configuration:
    - 1 double core cpu, 2GB ram, 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
    - 1 quadruple core cpu, 4GB ram 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
  - Software configuration
    - Multi thread acquisition:
      - Data reading in DMA mode PCIExpress board and
      - Reading the shared memory and writing on disk



In conclusion

- Powerful & versatile multi-channel acquisition system
  - Distributed over several hundred meters
  - Sample rate 500MHz with a input bandwidth of 1,5Gz
  - 500MB/s Streaming data
  - Time resolution between channels better than 10ps
  - Noise level ~ 35db
  - 300MB/s data processing & hard disk writing one 1 PC
- Ongoing
  - Multiprocessor synchronisation
  - Real time operating system
  - Interrupt mode on PCIExpress