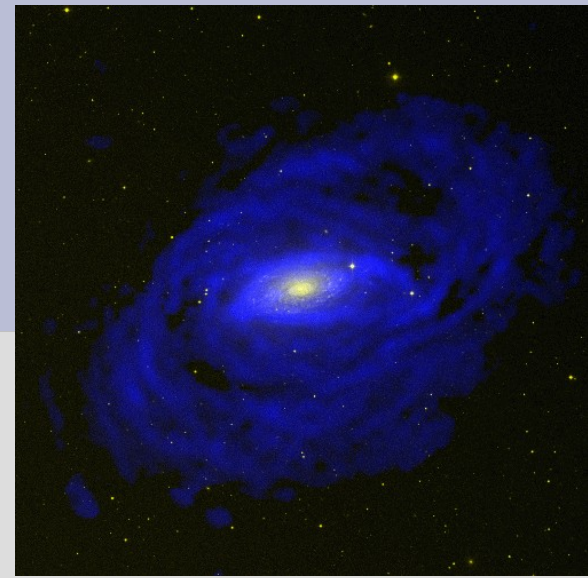




BAO project in radio

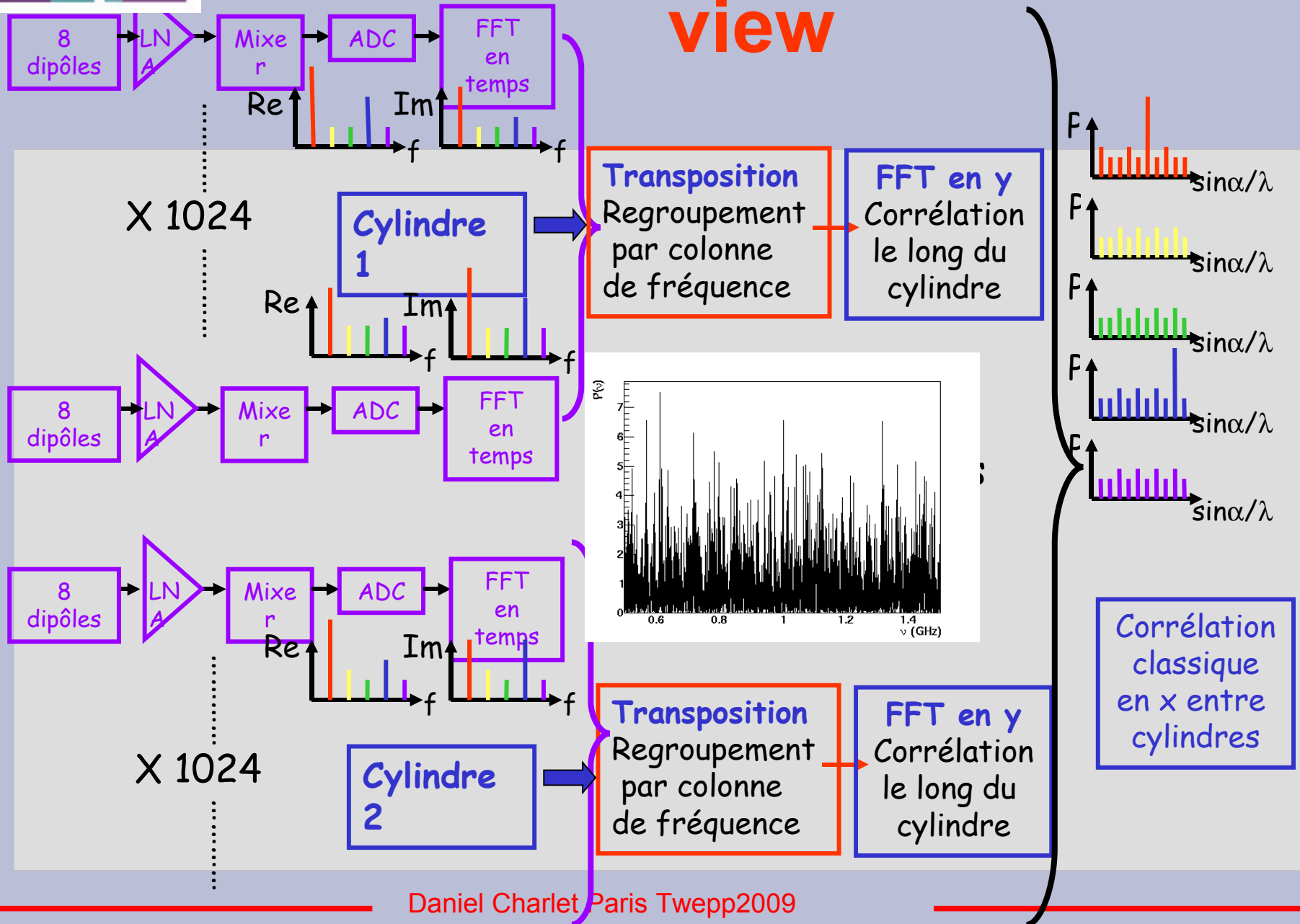


BAO Aquisition system status



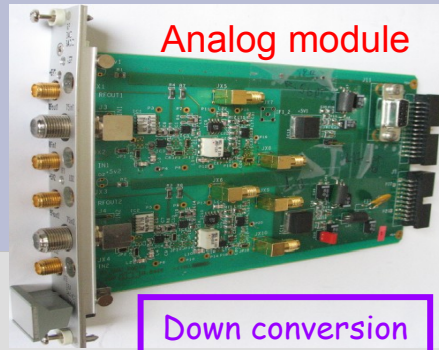
Electronic chain schematic

view



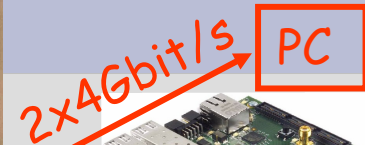
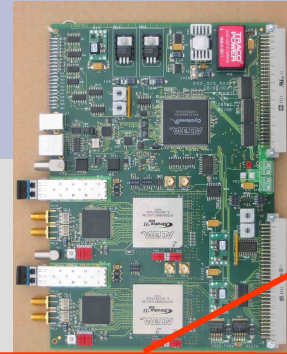


Electronics chain



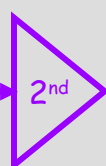
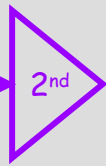
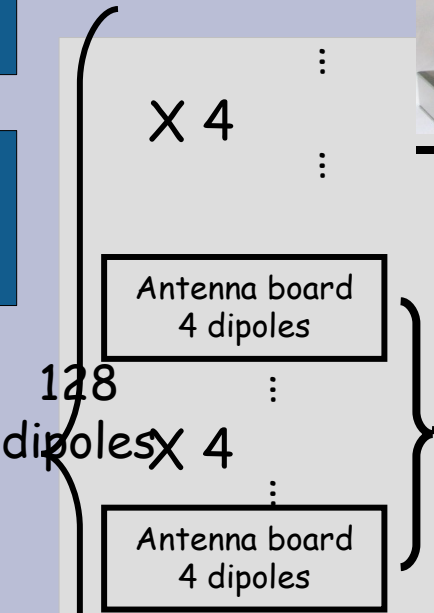
Analog module

ADC board



PC

PCIExpress board



PC

2x4Gbit/s

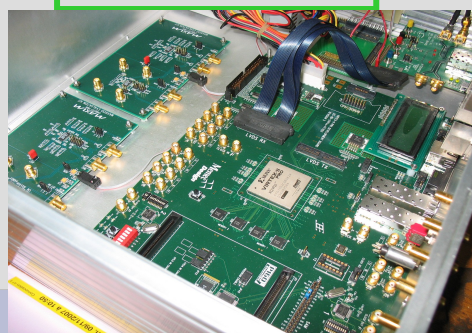
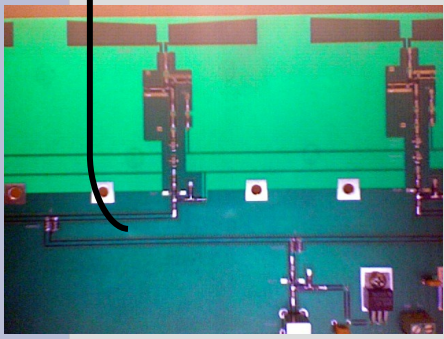
2x4 Gbit/s

2x4.Gbit/s

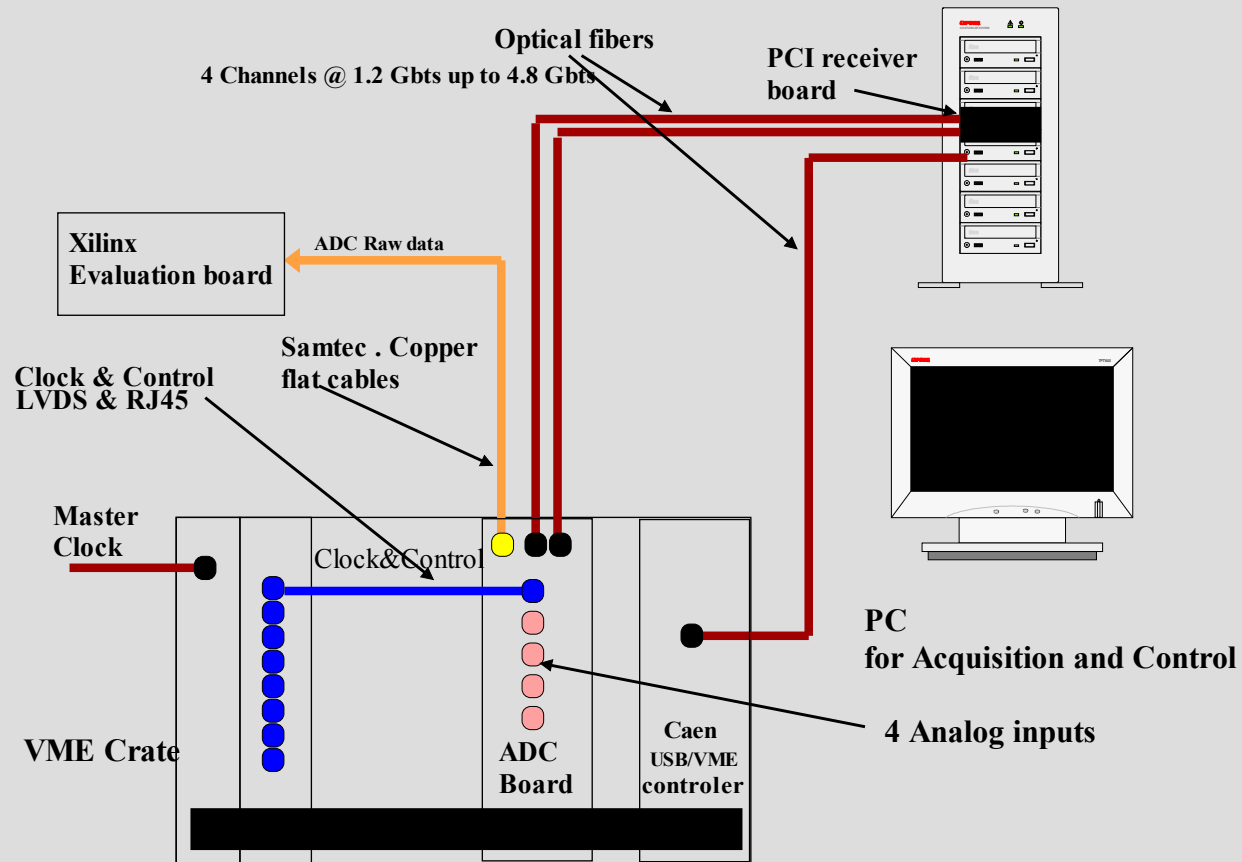
X 8

2x4 Gbit/s

X 4



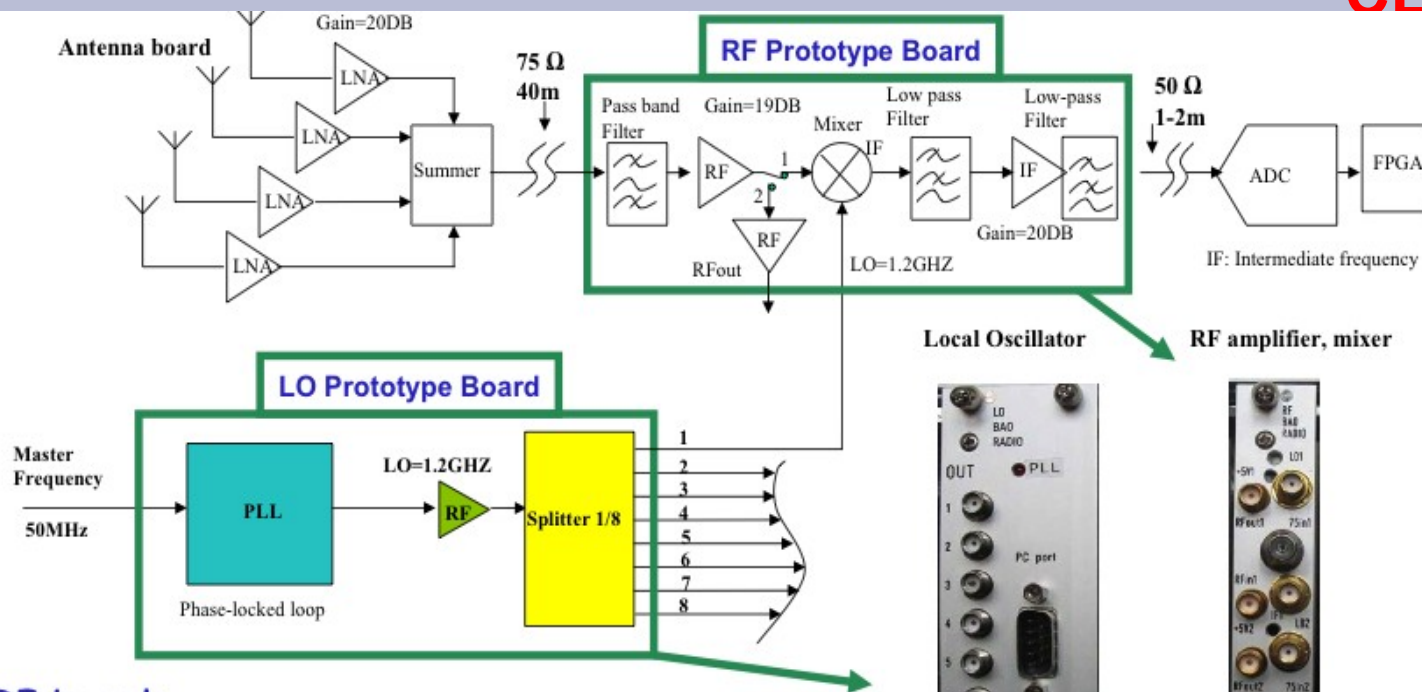
Interconnection Design





Analog chain for RF prototype board

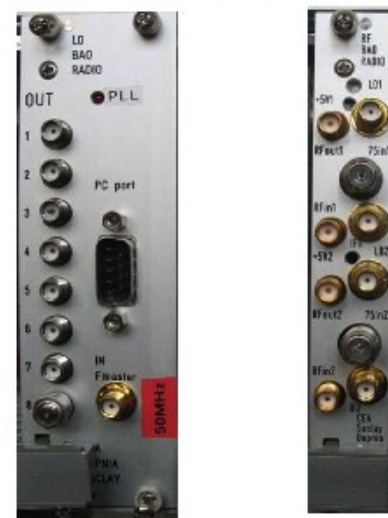
CEA irfu



RF board:

- 75Ω/50Ω inputs
- 2 channels per board
- Possibility of by-passing mixer to test the under-sampling approach.
- Possibility to "tune" the pass band filter

BAO Radio HSHS project



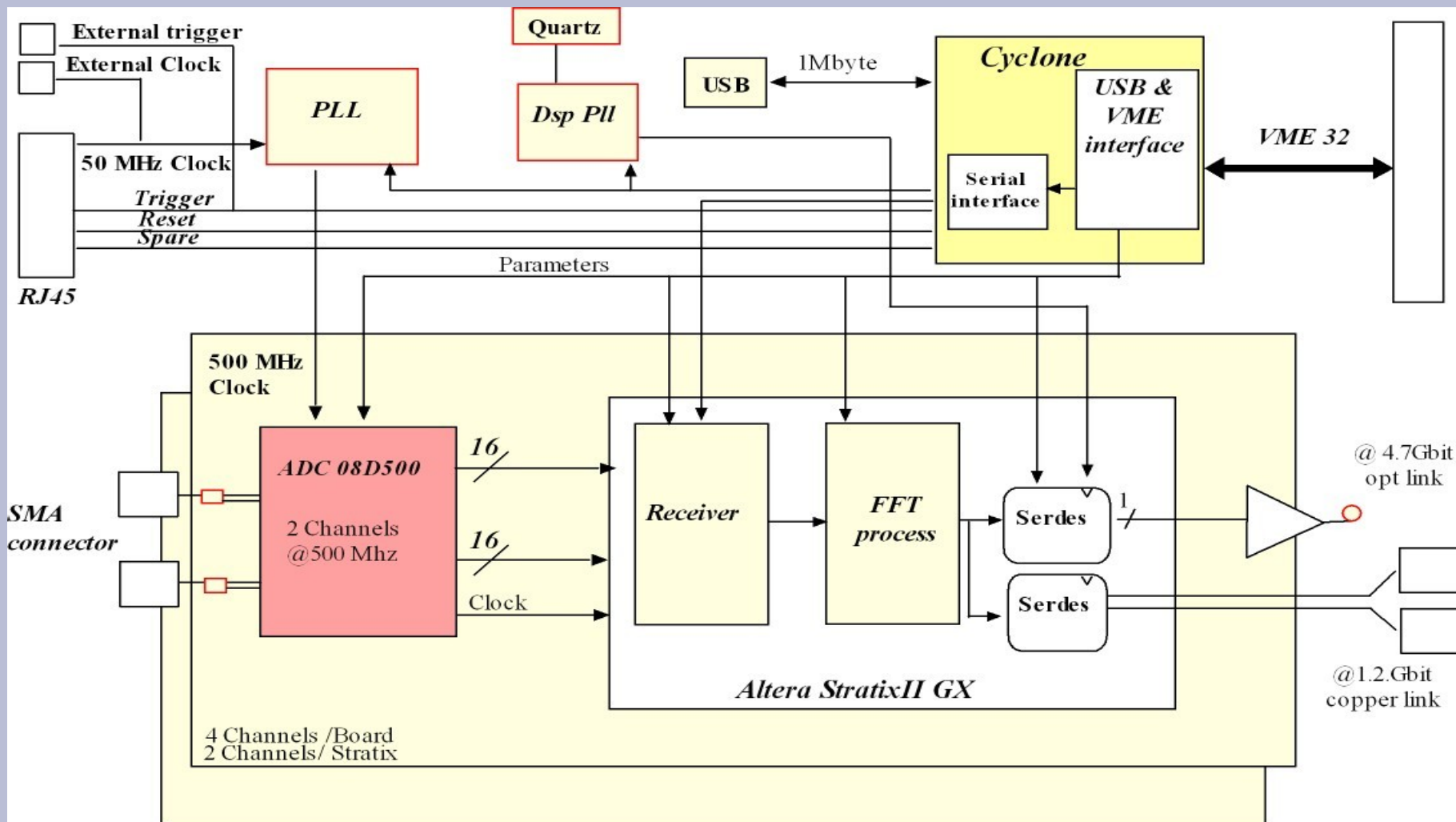
Front panel plug-in (3U EuroCard)

January 10, 2008

4

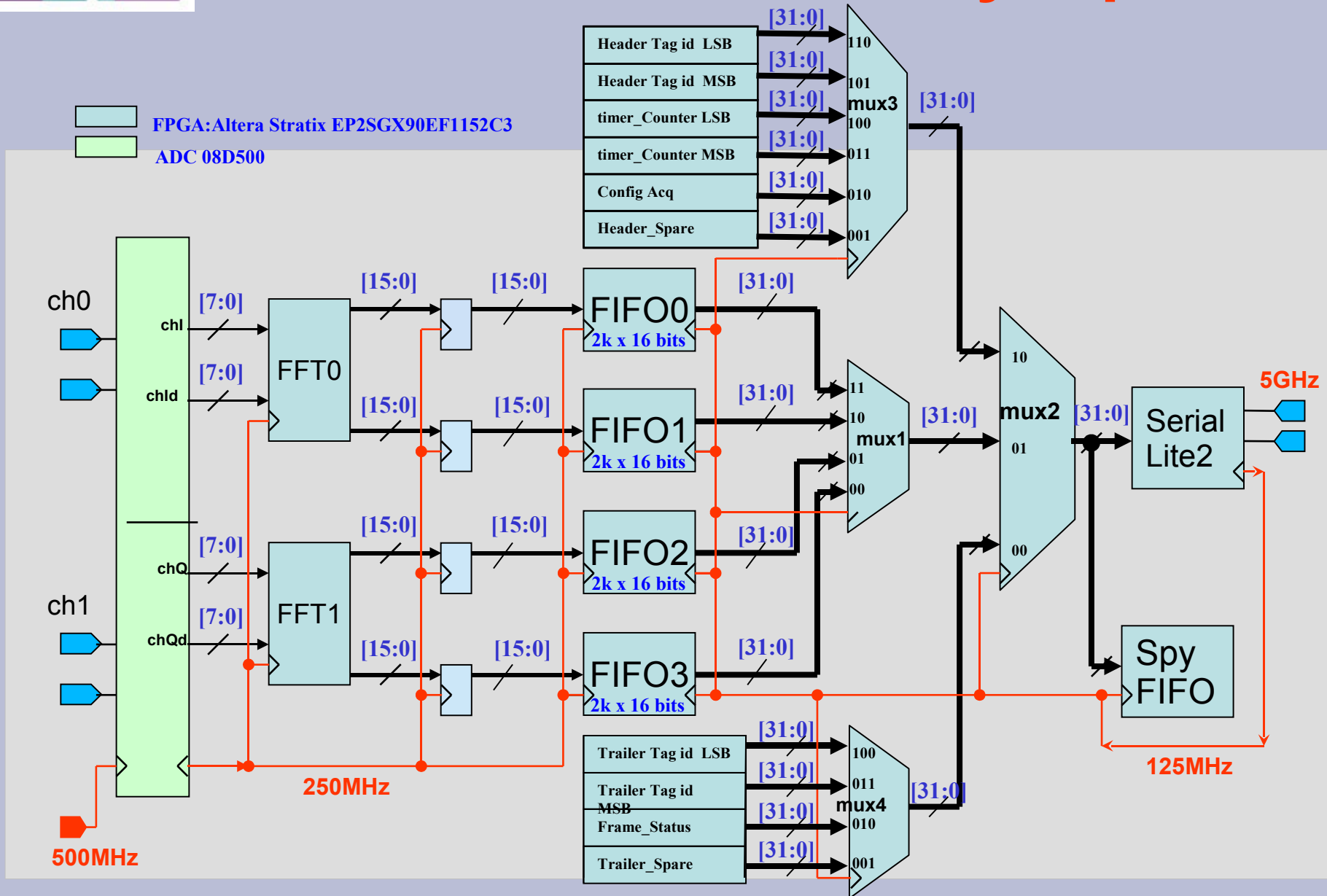


LAL ADC board Synoptic





ADC board FPGA Synoptic

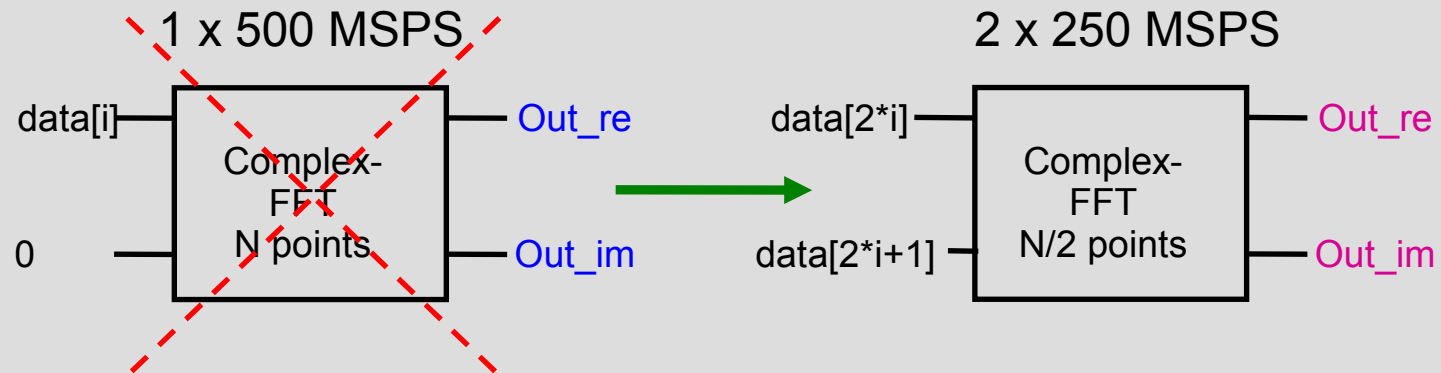




Post ADC processing: Temporal FFT

FPGA Implementation of real-FFT using a IP Core:

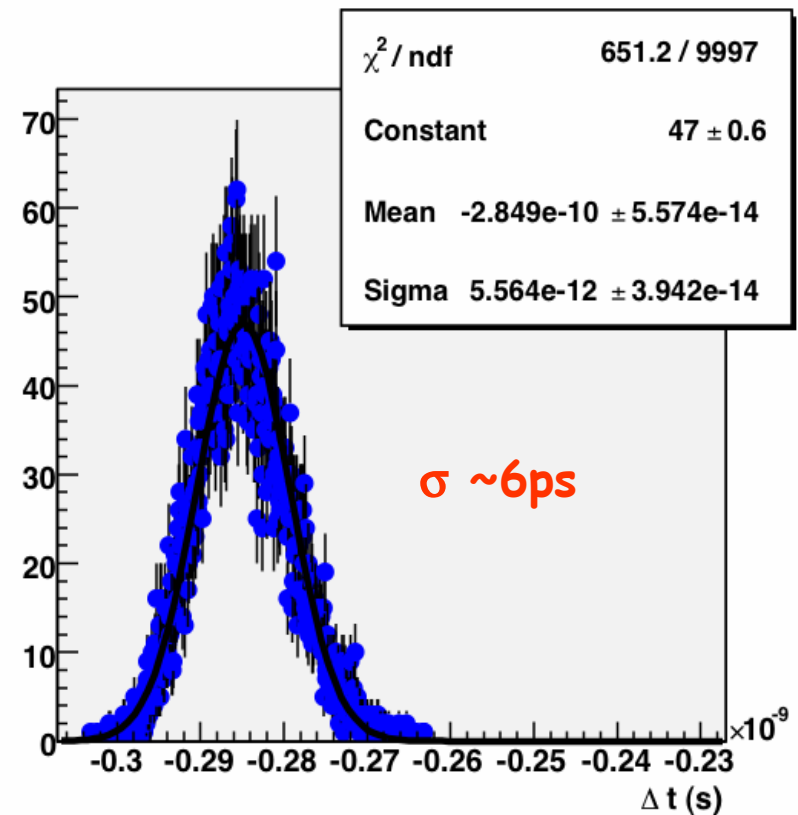
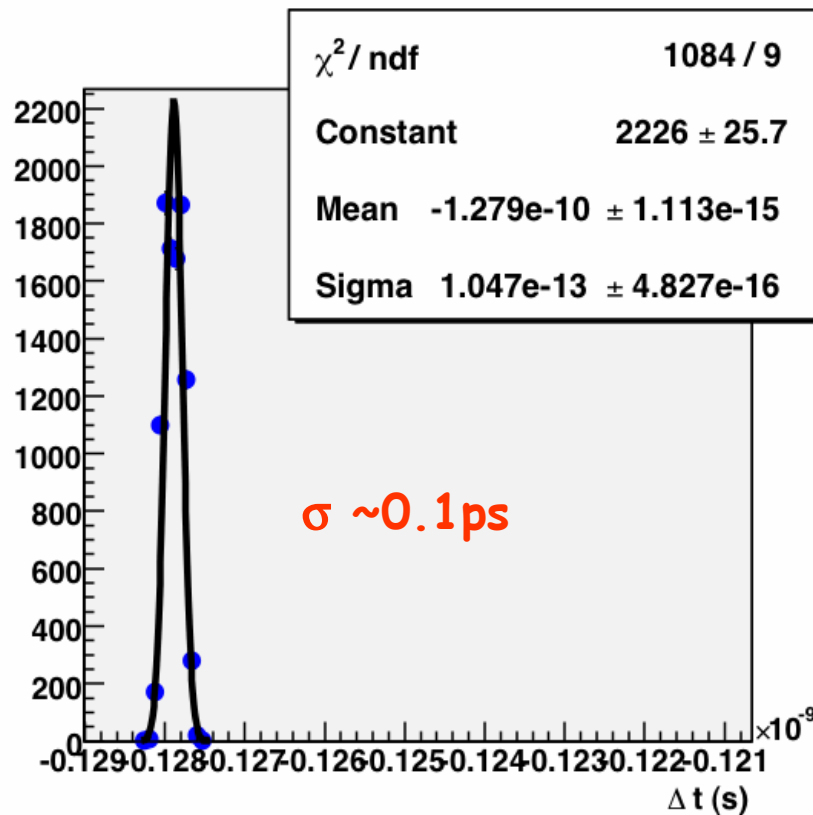
to save hardware resources, we use a $N/2$ points complex-FFT to compute a N -points real-FFT



the **real** signal $s[j=0:N-1]$ is transformed into a **complex** signal : $c[i] = s[2*i] + j*s[2*i+1]$

Analog characteristic: 1

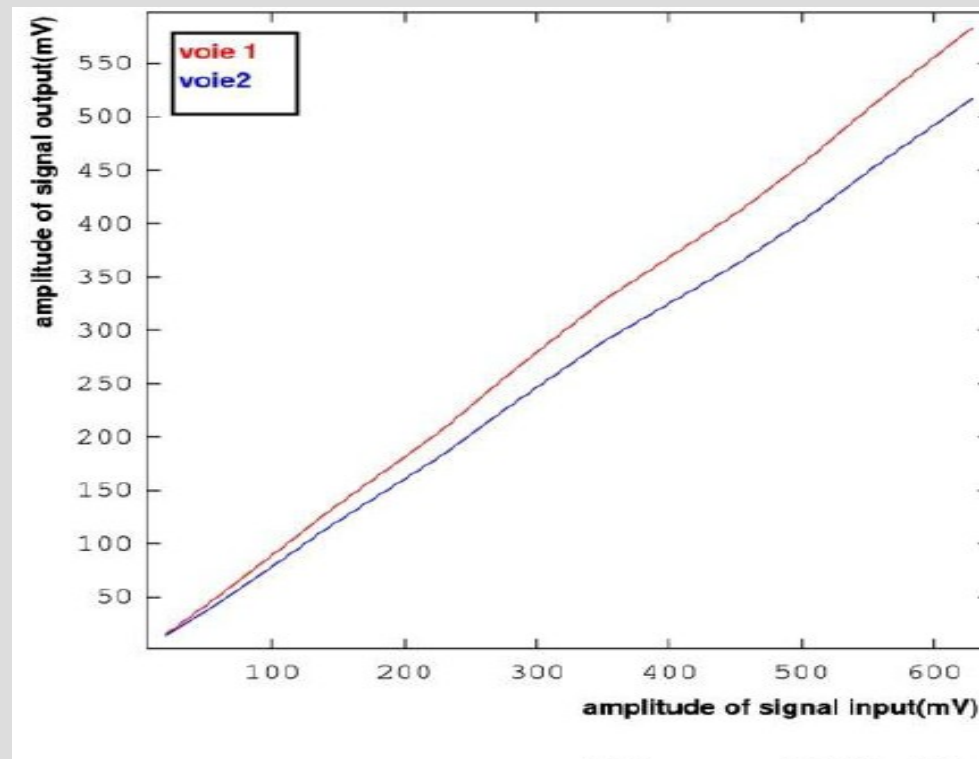
Time resolution



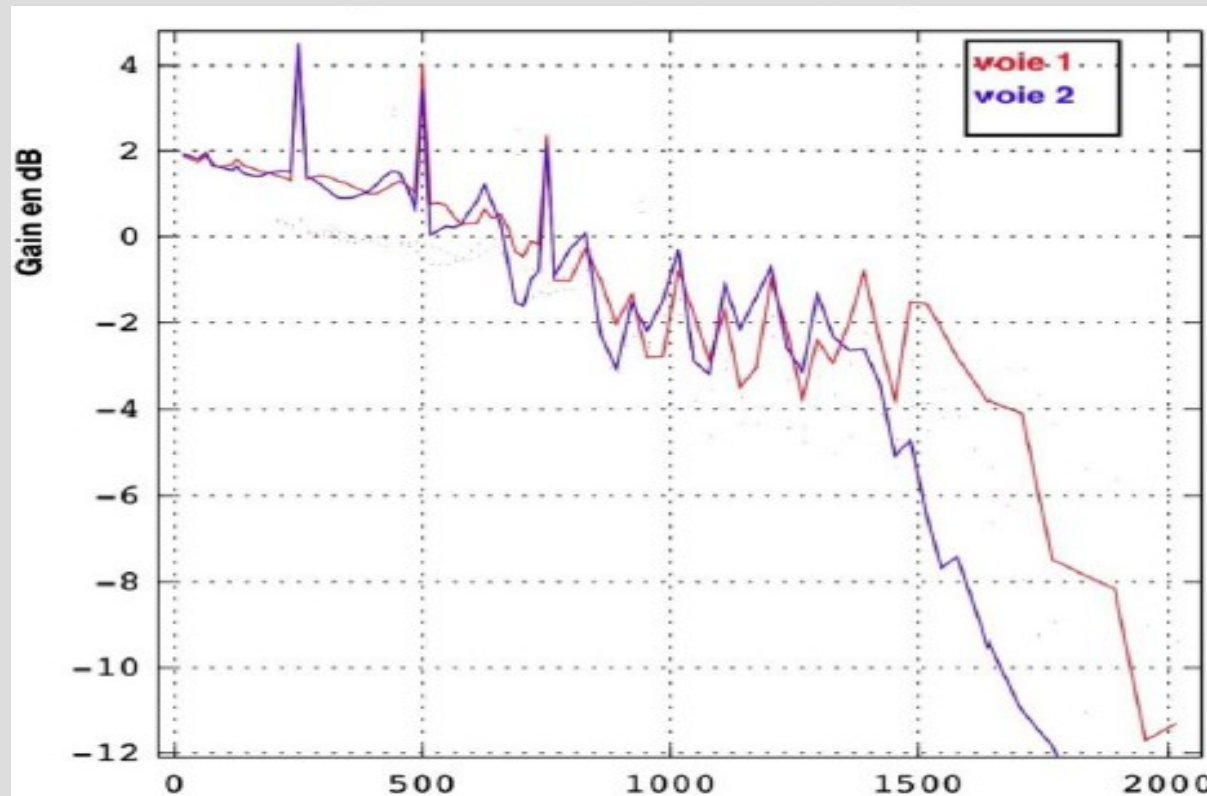
Analog characteristic :2

Linearity

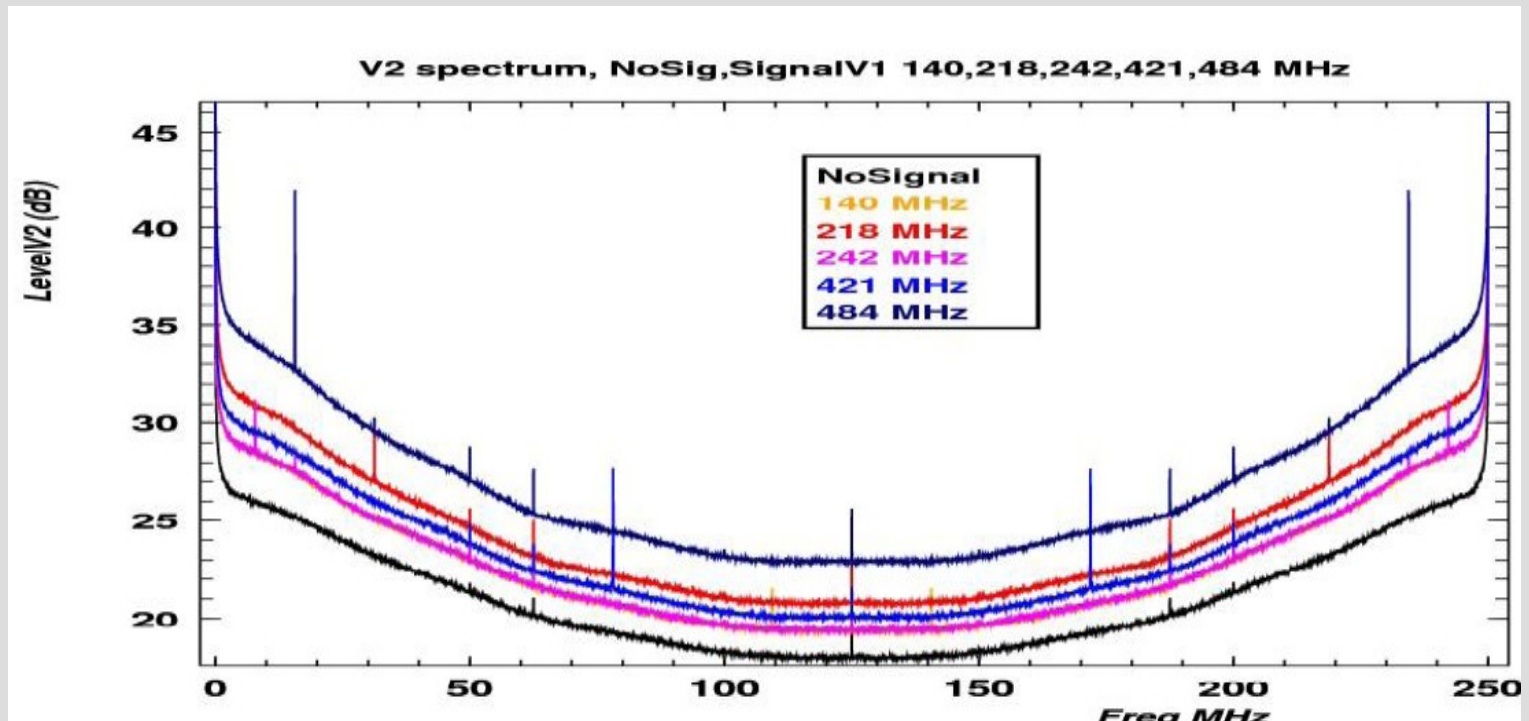
Linearity at 1.4GHz



Analog characteristic : 3 Bode diagram



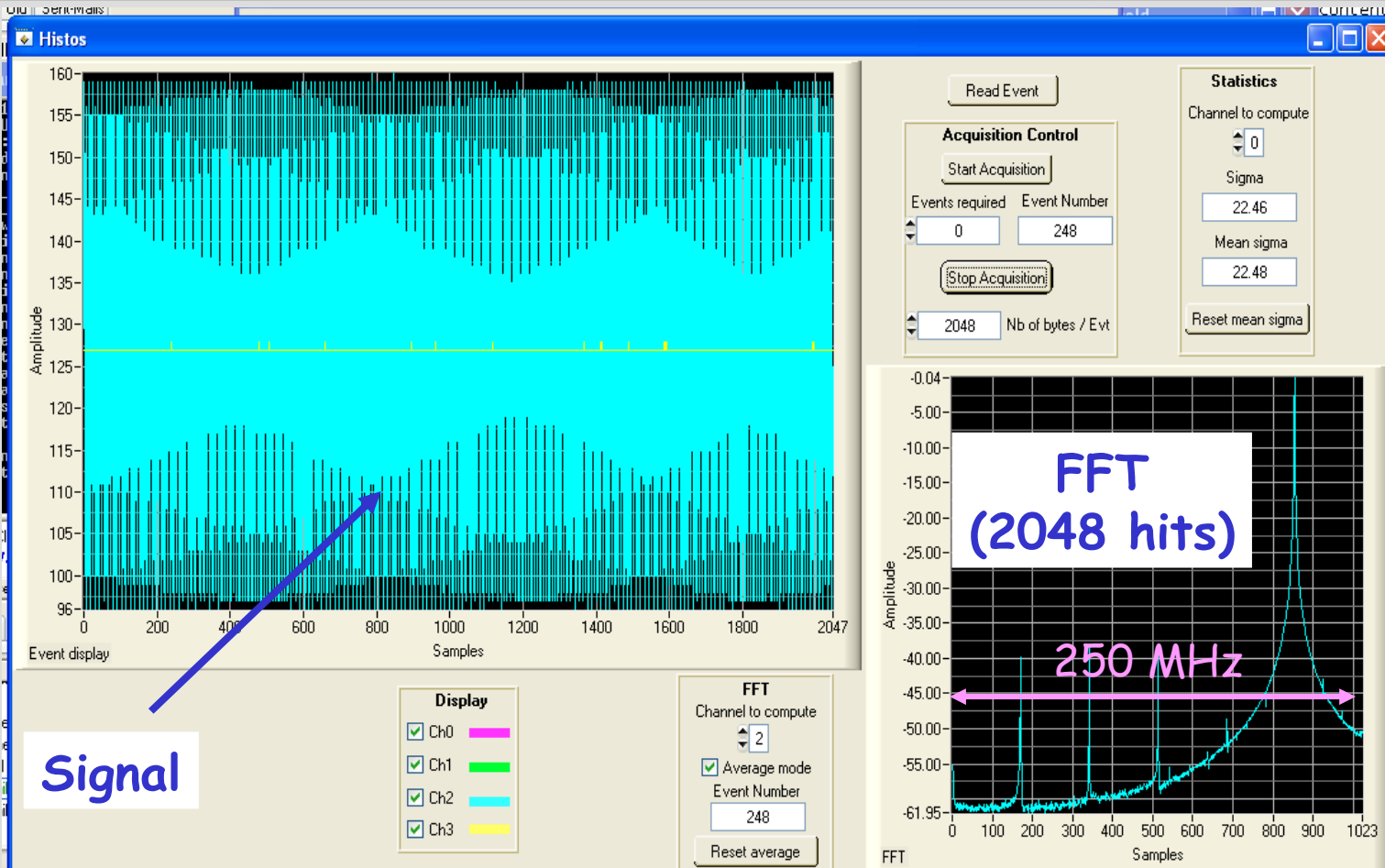
Analog characteristic: 4 Noise signal & diaphony



ADC board: Under-sampling

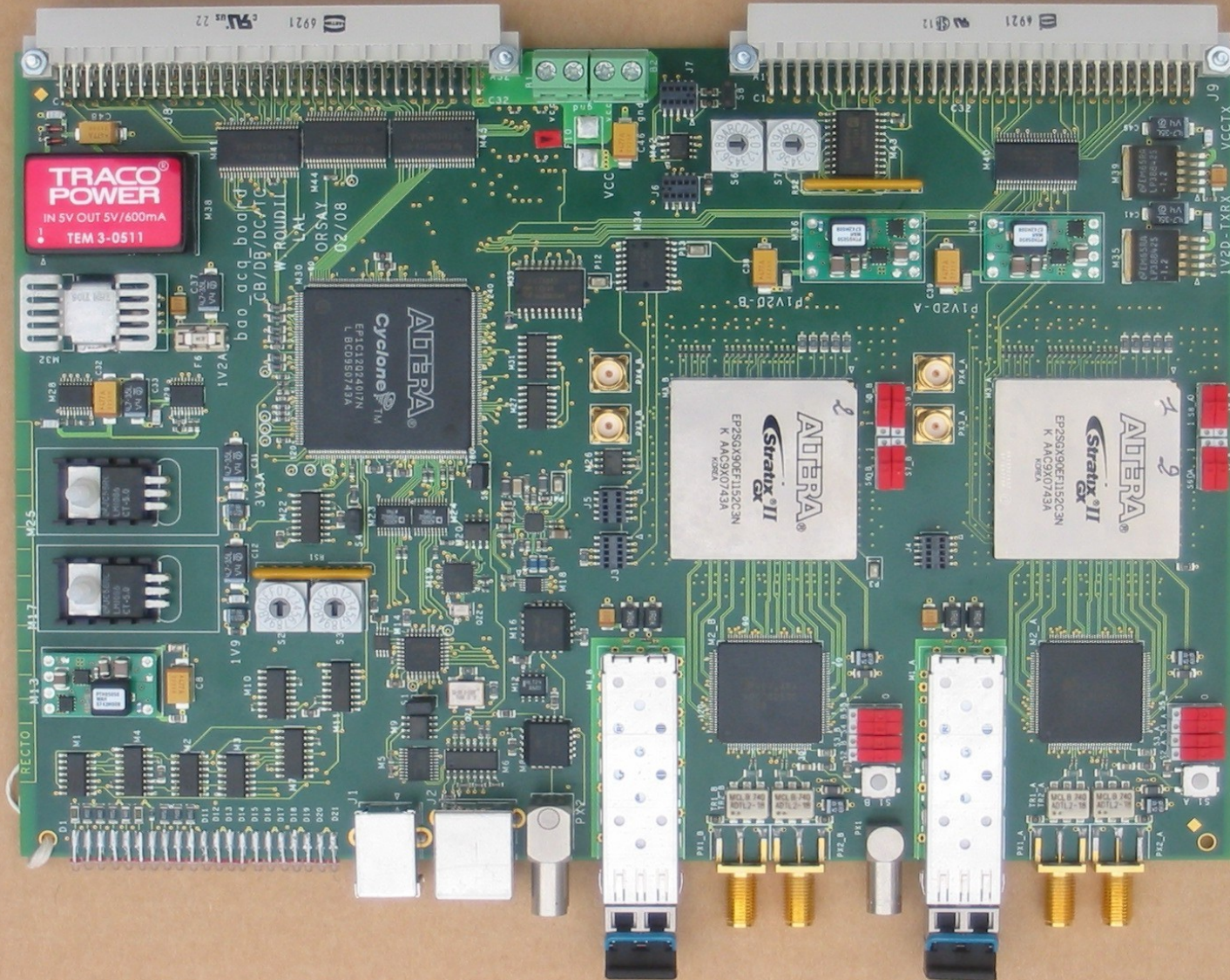
- Tests for different frequencies
- Under-sampling up to 750 MHz

$f_{in} = 300\text{MHz}$
Amp = 500mV
Gain = -10dBm
Fiber: 5Gbit/s





LAL ADC board

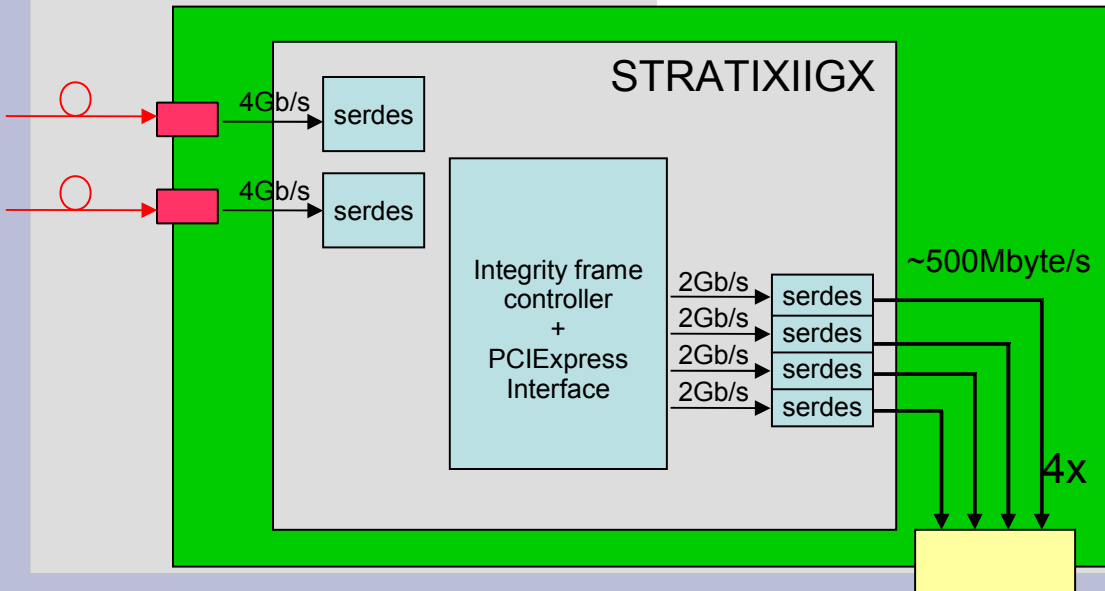
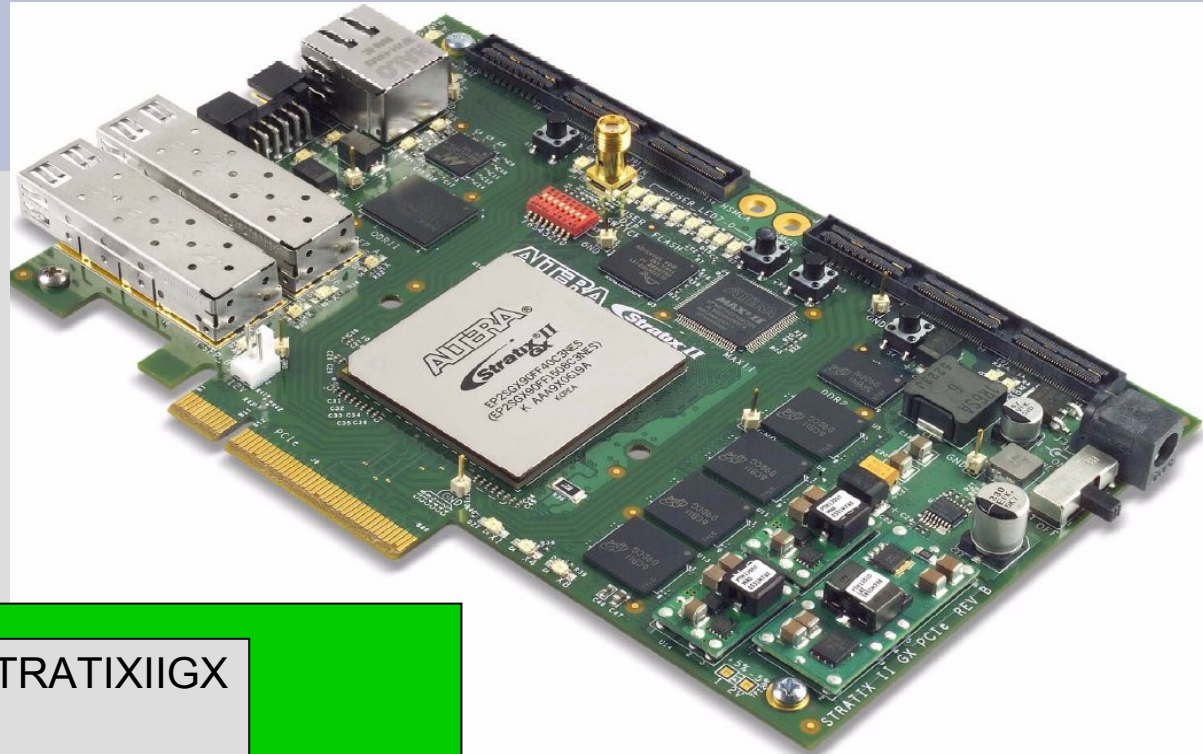


ADC board status

- ADC board 1.1 :
 - 2 in orsay 1 Saclay.
 - Tested :
 - PPL
 - Hardware VME, firmware not complete.
- ADC board 1.2 :
 - 2 in orsay.
 - Bode diagram of the 2 channels.
 - Paramaters transfert by DISCLK.
 - Components for 7 boards.
- VME rack OK.
-

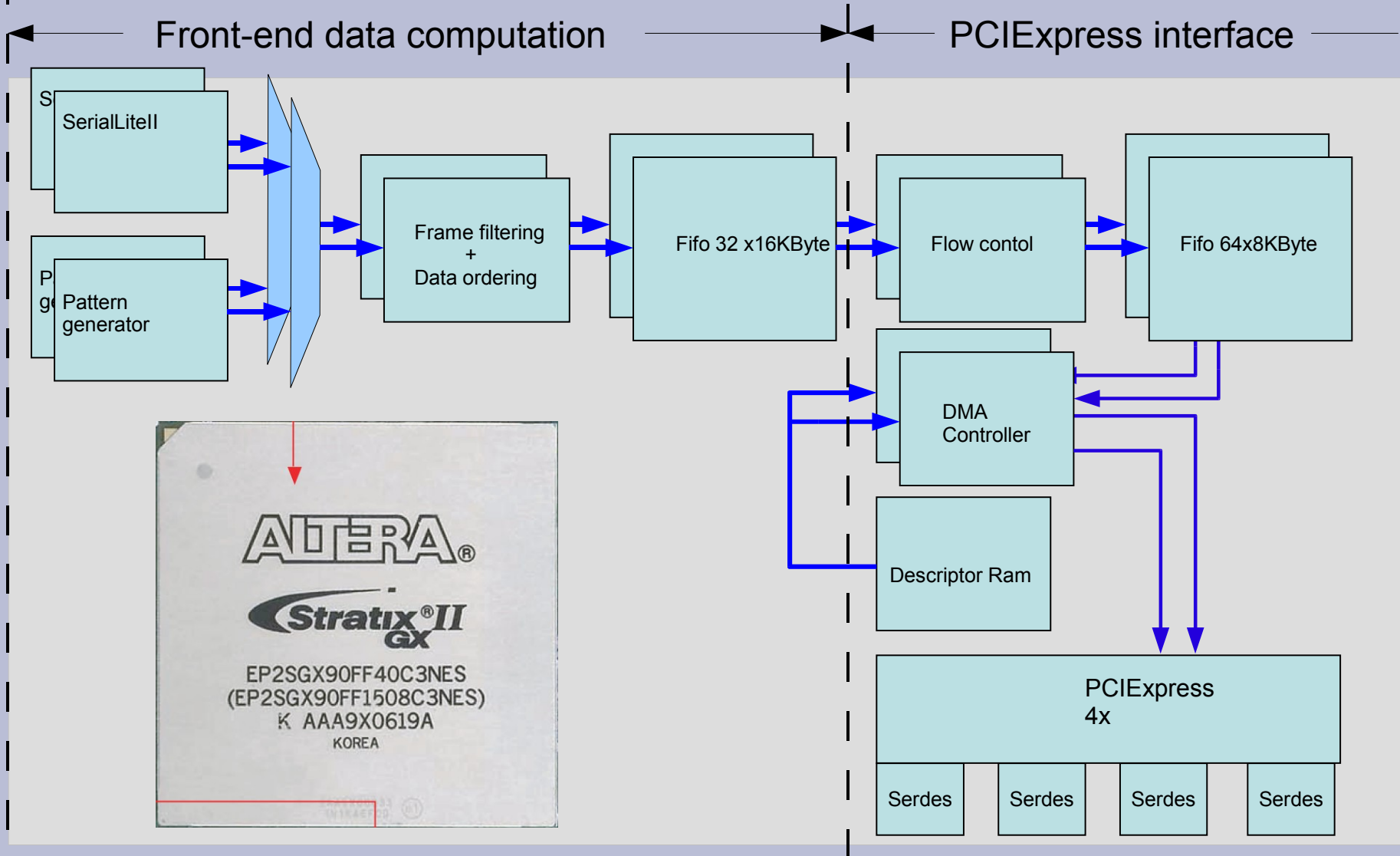


PCIExpress evaluation board





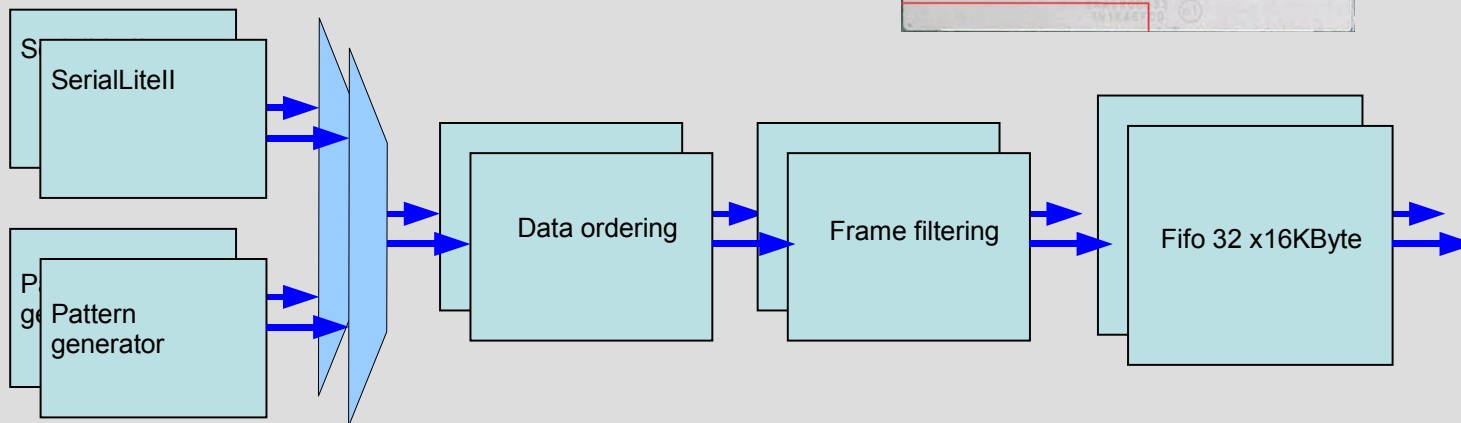
Synoptic FPGA PCIeExpress Evaluation board





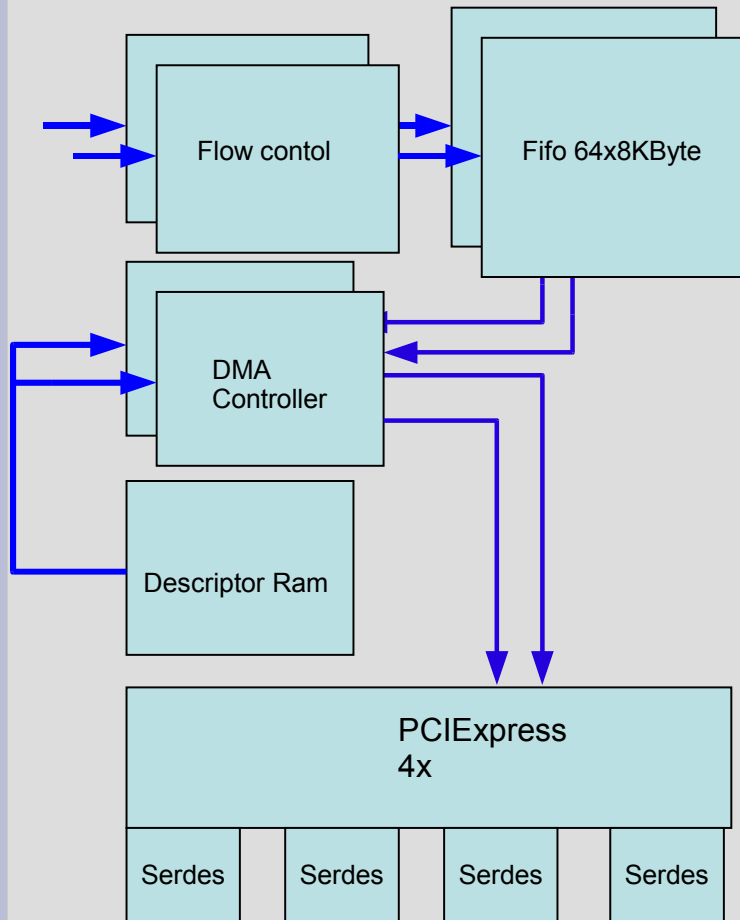
FPGA synoptic: Front-end data computation

- Link interface: SerialLiteII.
- Pattern generator.
- Data ordering.
- Frame filtering.
- Buffering: FIFO 64KByt





FPGA synoptic: PCIExpress interface



- FIFO buffering
- Scatter-gather DMA
- PCIExpress:
 - End point
 - 4X

System On Programmable Chip module

The screenshot shows the Altera SOPC Builder interface. The 'Clock Settings' table is as follows:

| Name | Source | MHz |
|---------|----------|-------|
| clk | External | 125.0 |
| cal_clk | External | 125.0 |

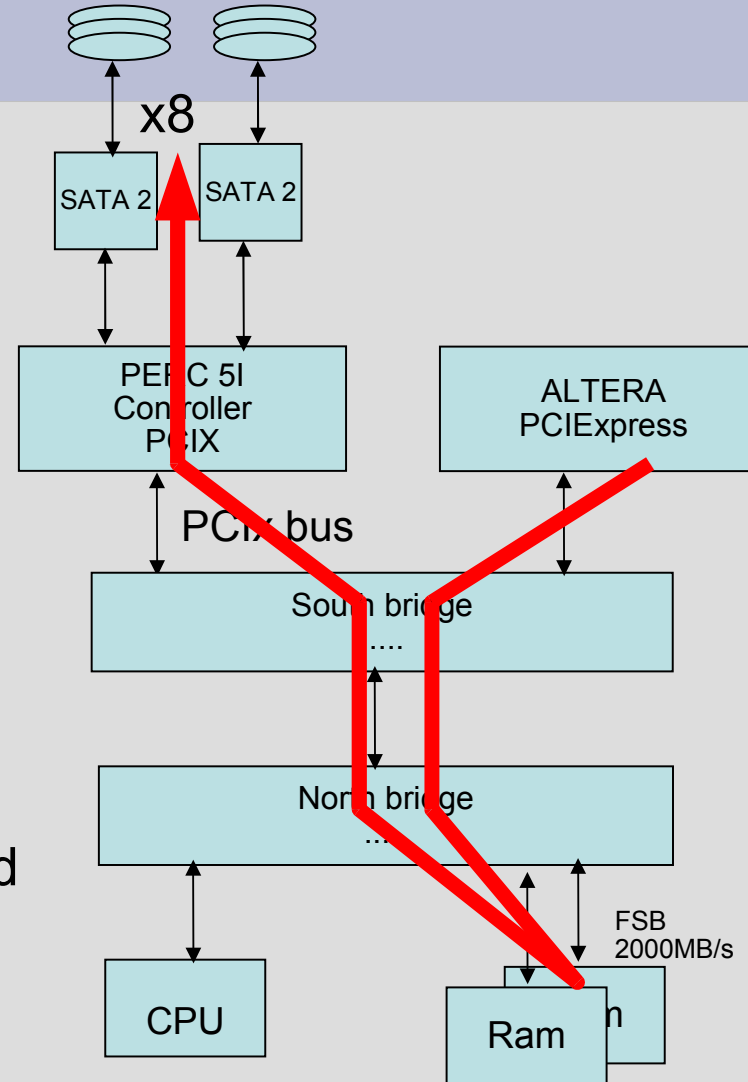
The 'Connections' table shows the following modules and their connections:

| Module Name | Description | Clock | Base | End | IRD |
|-----------------------|-------------------------------|---------|------------|------------|-----|
| pci_express_computer | PCI Express Computer | cal_clk | | | |
| bar1_0_Prefetchable | Avion Memory Mapped Master | clk | 0x00000000 | 0x00003FFF | |
| bar2_0_Prefetchable | Avion Memory Mapped Master | clk | 0x00000000 | 0x00003FFF | |
| Control_Register_Acc | Avion Memory Mapped Slave | clk | 0x00000000 | 0x00003FFF | |
| ti_interface | On-Chip Memory (RAM or ROM) | clk | 0x00004000 | 0x00004FFF | |
| s1 | Avion Memory Mapped Slave | clk | 0x00005000 | 0x00005FFF | |
| sgdma | Scatter-Gather DMA Controller | clk | 0x00006000 | 0x00006FFF | |
| csr | Avion Memory Mapped Master | clk | 0x00006000 | 0x00006FFF | |
| descriptor_read | Avion Memory Mapped Master | clk | 0x00005800 | 0x00005BFF | |
| descriptor_write | Avion Memory Mapped Master | clk | 0x00005800 | 0x00005BFF | |
| m_write | Avion Memory Mapped Master | clk | 0x00005800 | 0x00005BFF | |
| in | Avion Streaming Sink | clk | 0x00005400 | 0x000054FF | |
| out | Avion Streaming Sink | clk | 0x00005400 | 0x000054FF | |
| ififo_1 | Avion-ST Single Clock FIFO | clk | 0x00005410 | 0x0000541F | |
| ififo_2 | Avion-ST Single Clock FIFO | clk | 0x00005410 | 0x0000541F | |
| in | Avion Streaming Sink | clk | 0x00005410 | 0x0000541F | |
| out | Avion Streaming Sink | clk | 0x00005410 | 0x0000541F | |
| timing_adapter | Avion-ST Timing Adapter | clk | | | |
| in | Avion Streaming Sink | clk | | | |
| out | Avion Streaming Sink | clk | | | |
| interface | Avion Streaming Source | clk | | | |
| avion_streaming_sou_1 | Avion Streaming Source | clk | | | |
| avion_streaming_sou_2 | Avion Streaming Source | clk | | | |
| avion_streaming_sou_3 | Avion Streaming Source | clk | | | |
| avion_streaming_sou_4 | Avion Streaming Source | clk | | | |



Aquisition test

- Poweredge 2900
 - 2 hardware configuration:
 - 1 double core cpu, 2GB ram, 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
 - 1 quadruple core cpu, 4GB ram 1 raid controller with 8 sata2 disc of 160GB (Western Digital)
 - Software configuration
 - Multi thread acquisition:
 - Data reading in DMA mode PCIExpress board and
 - Reading the shared memory and writing on disk





In conclusion

- Powerful & versatile multi-channel acquisition system
 - Distributed over several hundred meters
 - Sample rate 500MHz with a input bandwidth of 1,5Gz
 - 500MB/s Streaming data
 - Time resolution between channels better than 10ps
 - Noise level ~ 35db
 - 300MB/s data processing & hard disk writing one 1 PC
- Ongoing
 - Multiprocessor synchronisation
 - Real time operating system
 - Interrupt mode on PCIExpress