2D Pixel detector design for TWOCRYST

SARA CESARE

3° WORKSHOP ON ELECTROMAGNETIC DIPOLE MOMENTS OF UNSTABLE PARTICLES – 11/12/2023

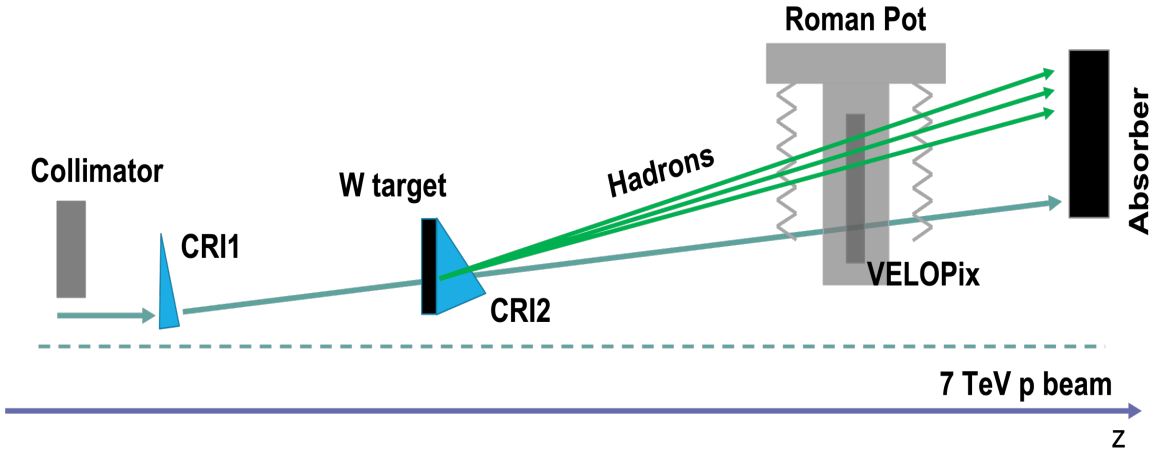
Proof-of-principle test

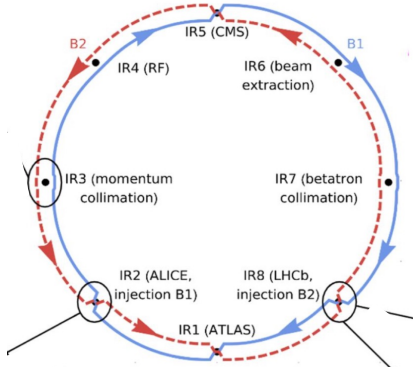
Goals of the test

1. Measure channeling efficiency of long crystals at TeV energies
2. Background studies

Experimental set-up

- Short crystal for beam-halo deflection
- W target
- Long crystal for Λ_c^+ channeling
- One tracking station in a Roman Pot
- Absorber





credits to S. Redaelli

Detector specifications

Detector requirements

- Minimum 1 layer for background studies and channelling efficiency, more layers could be used for detailed tracking studies

- Distance target-first layer is optimised for the reconstruction of the invariant mass of $\boldsymbol{\Lambda_c}$

- Distance between main circulating beam and centre of the target is < 1 cm

↓

tracking detector is inside the beam pipe

↓

Solution: roman pot

Technology	Silicon pixel sensors
N layers	≥ 1
Distance target-first layer	70 ± 5 cm
Transverse distance from the LHC beam	0.5-1 cm
Active area	$\geq 2 \times 1\ cm^2$
Granularity	$< 100\ \mu m$
Radiation hardness	$\sim 10^{12}\ 1\ MeV\ n\ eq/cm^2$
Operational temperature	$<\ 20°\ C$

Detector specifications

Detector requirements

- Detect both channelled and unchanneled particles

↓

Active area $\geq 2\times1\ \mathrm{cm}^2$

- Resolve between background tracks at first layer

↓

Detector granularity < 100 µm

↓

Silicon pixel sensors

- Expected fluences of $\sim 10^{12}$ 1 MeV n eq/cm^2

↓

detector can operate at room temperature

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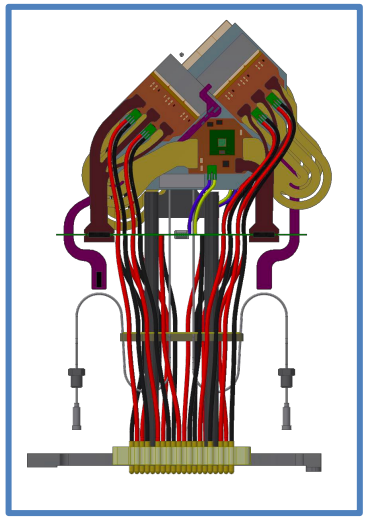
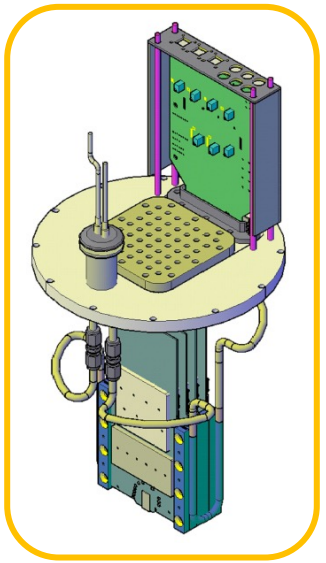
2D Pixel detector proposal

Modular tracking detector based on:

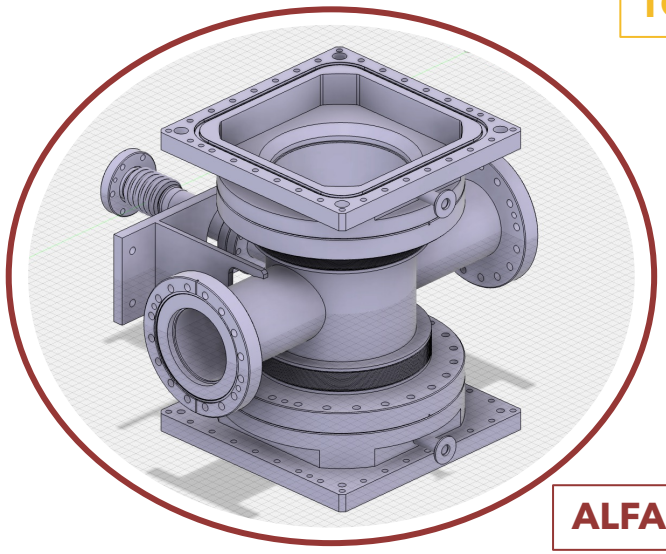
- LHCb Vertex Locator (VELO) silicon pixel sensors and ASIC and readout chain
- TOTEM experiment mechanical support and cooling
- ALFA experiment roman pot



VELO module



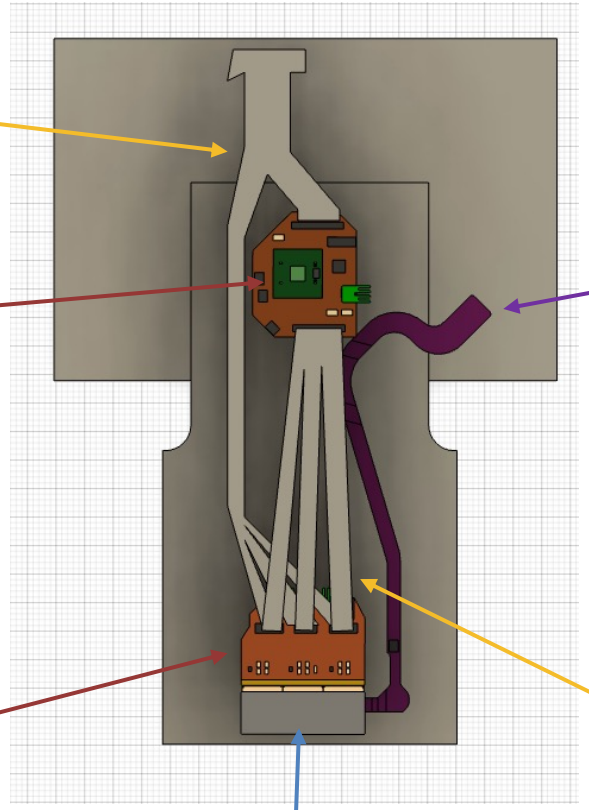
TOTEM support



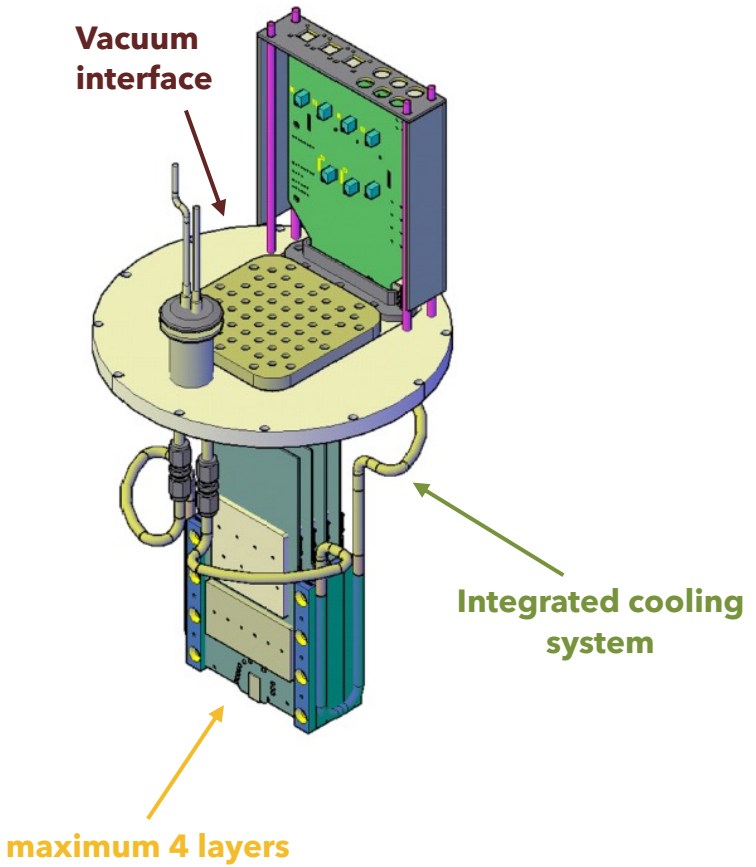
ALFA roman pot

Tracking module

Tracking module

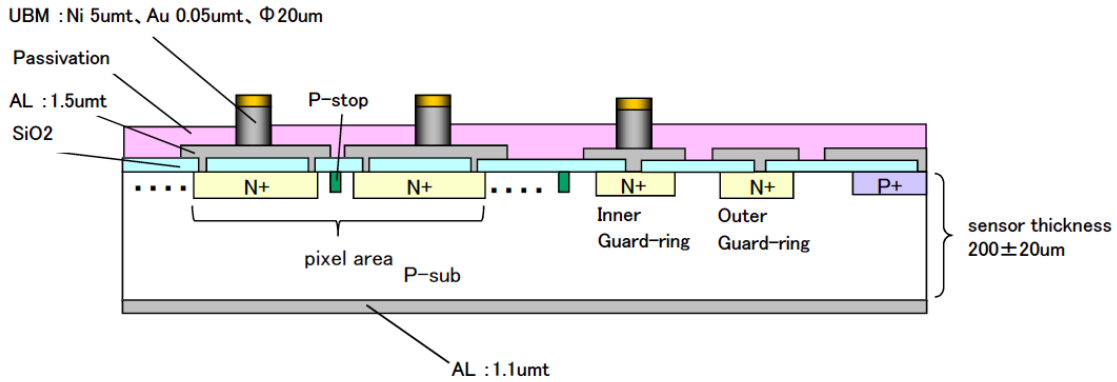


TOTEM mechanical suport



HAMAMATSU silicon sensors

- High resistivity p-type float-on silicon wafers
- Thickness – 200 μm
- Active area – 42.57 x 14.08 mm^2
- In the regions between ASICs the pixels are elongated by a factor 2.5 to allow a gap between the ASICs
- The pixels are metallised with Ni/Au UBM pads



Bulk material thickness	200 μm n-on-p silicon
Most probable unirradiated signal charge	16 000 e^-
Minimum end-of-life signal charge	6 000 e^-
Maximum operational voltage	1000 V
Required charge collection efficiency	> 99%

Sensors wafers have been purchased from HAMAMATSU and have already been delivered at CERN

https://edms.cern.ch/ui/#!master/navigator/document?P:1340134179:100310887:subDocs

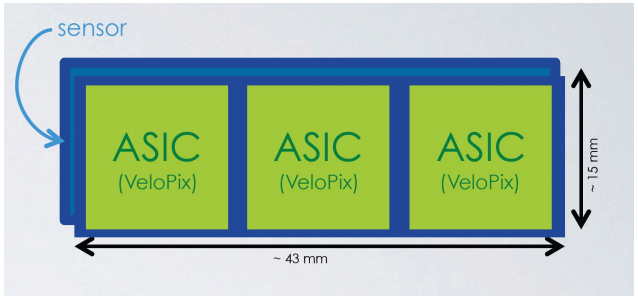
VeloPix ASICs

- Commercial 130 nm CMOS
- 256 x 256 pixel with 55 µm pitch
- Chip size 14.14 x 16.60 mm^2
- Radiation hardness up to 8×10^{15} 1 MeV n eq/cm^2
- Super-pixel readout logic
  - Minimum decay time - 300 ns
  - 2 event deep buffer
  - Maximum data transfer rate 13.3 M packet/s

VeloPix have been borrowed from the VELO group and have been shipped together with the sensors to ADVAFAB company for the bump bonding

Estimated delivery date – February 2024

3 ASICs = 1 tile



Technology	TSMC 130 nm CMOS
Radiation hardness	> 4 MGy, SEU tolerant
Pixel size (analogue part)	55 µm × 55 µm (55 µm × 14.5 µm)
Peak rate per ASIC (per pixel)	9×10^8 hits/s (5×10^4 hits/s)
Maximum of charge distribution	16 000 e^-
Minimum threshold	500 e^-
Timing resolution (range)	25 ns (9 bits)
Super-pixel data size	30 bits
Maximum data rate per ASIC	20.48 Gbit/s
Power consumption per ASIC	~ 1.2 W (spec. 3 W)

https://cds.cern.ch/record/2692574/files/MCWG_LHC_TID_Run2_report_ostein_kbilko_08102019.pdf
https://dx.doi.org/10.1088/1748-0221/9/01/C01007

FE and GBTx hybrids

Front End hybrid

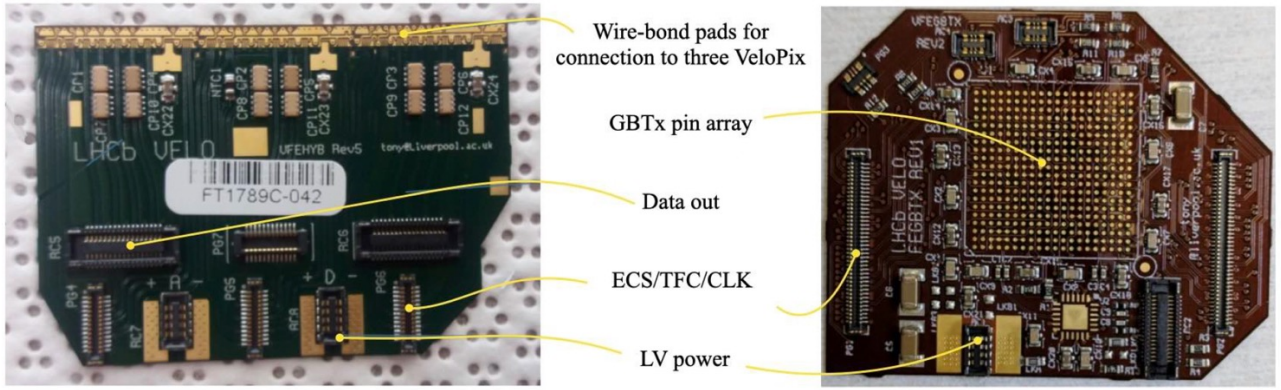
- Route the signals from the VeloPix ASIC
- Minimised material contribution – 4 copper layers
- Optimised for high speed signals

GBTx hybrid

- Provides control and timing information to the VeloPix FE
- Provides monitoring information back to the control room
- Each GBTx can operate two tiles

For the moment there will be 1 GBTx and 1 tile for each module

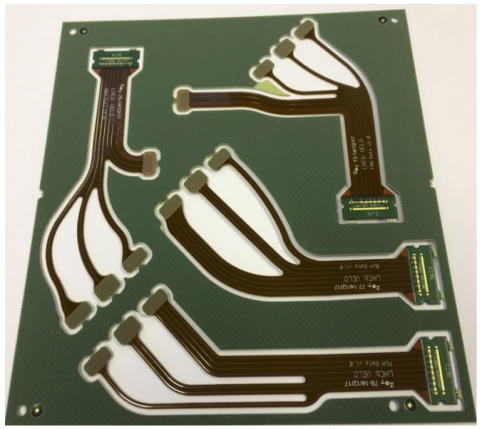
First units of GBTx and FE hybrids will be provided by the VELO group

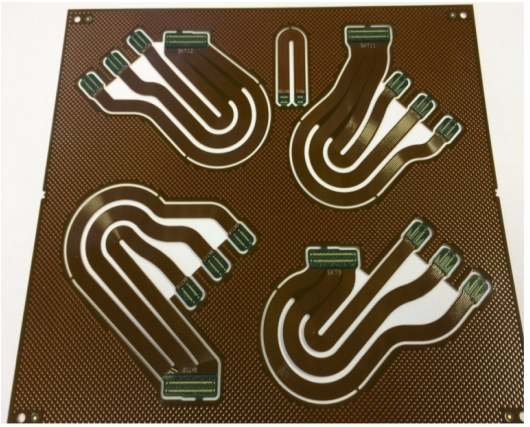


Flex cables

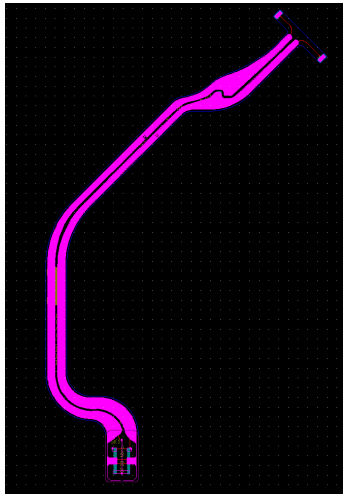
VELO SIGNALS

- ECS In, Out, Clock
- TFC Out, Clock
- Master Clock
- Reset





Interconnecting tapes



HV tapes

DATA cables

- Connect the velopix data output streams, uplink, down link, reset lines to the long data cables
- These are flexible, double sided, 100um track and gap, with controlled impedance, 100" differential traces.

New straight design of the flex cables in progress with the collaboration of the LumiTracker group of LHCb

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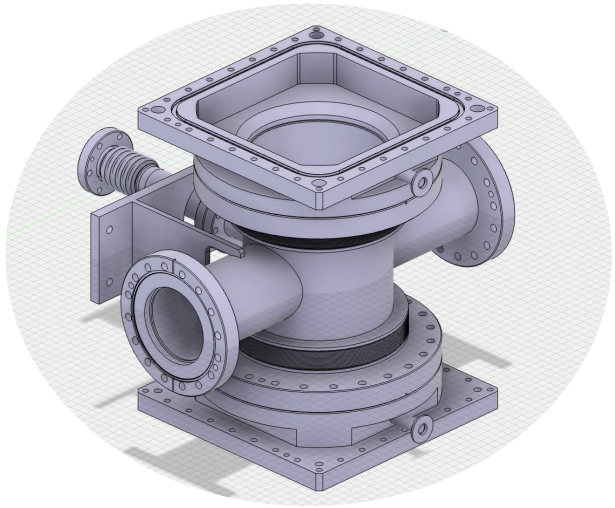
Roman pot box and cooling system



ALFA roman pot

- Two ALFA roman pot have already been extracted from the LHC tunnel
- Control system for vertical movement
- Possibility to use both ALFA and TOTEM inner box

- Diameter of the outer cylinder of the pot ~ 15 cm

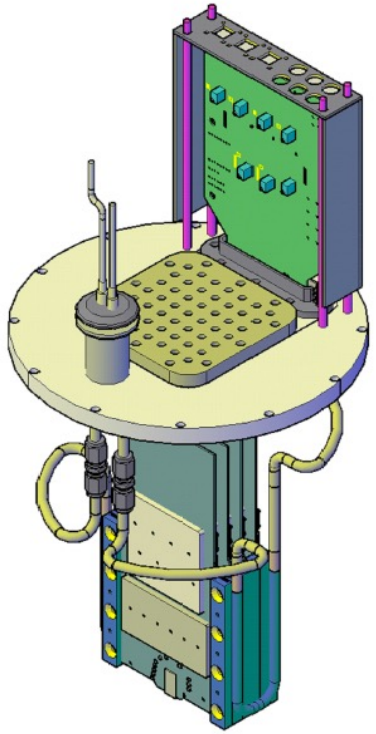
Cooling system

- Each VeloPix generate up to 3W
- Each ASIC additional 5 W

- Maximum 4 module/rp ~ 30 W

- Proof of principle operational temperature ~ 20 ° C

- Water cooling system + thermally conductive support board



Future experiment – need to go to negative temperature: new solution is needed!

Off detector electronics

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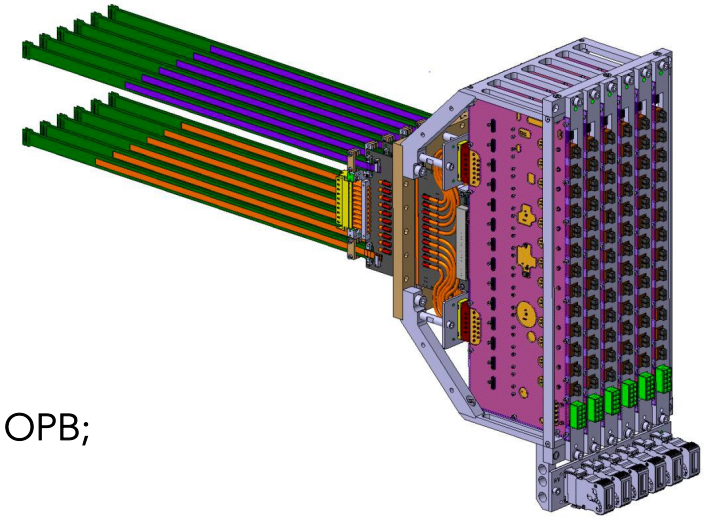
Vacuum feed-through

- Allow to pass from the secondary vacuum inside the roman pot to the outside area
- Need for a custom-made solution

Opto and Power Board



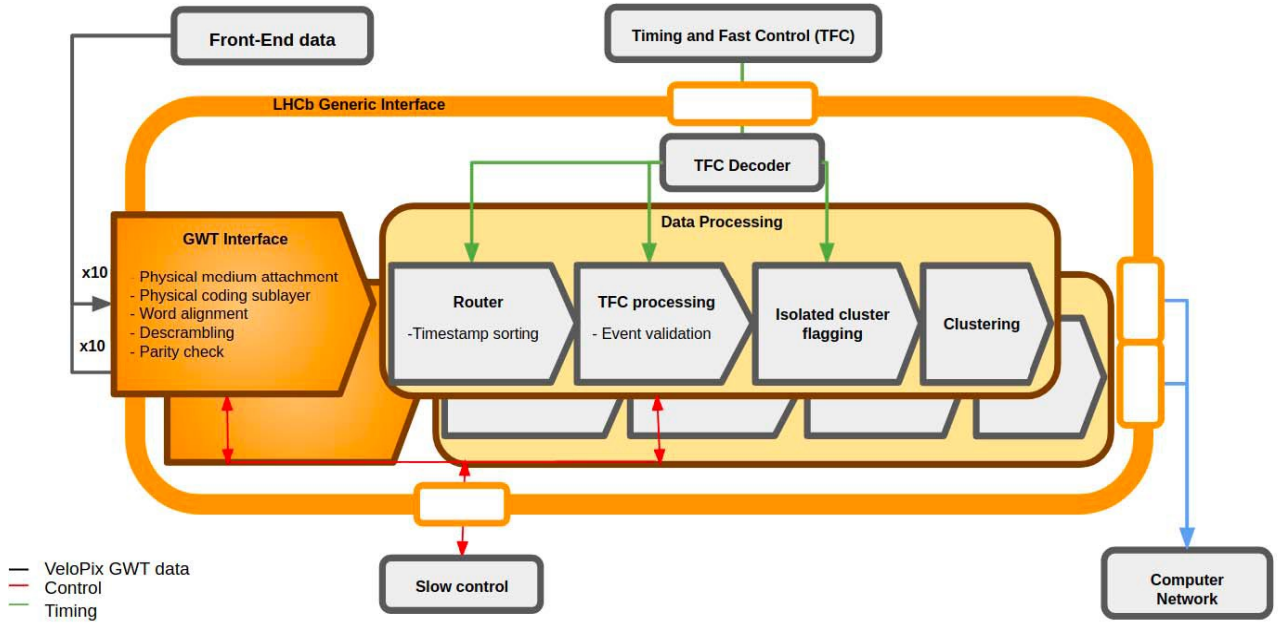
- Located immediately outside the roman pot .
- They provide the following functionality:
  - Electrical to optical conversion for the data sent from the detector module;
  - Electrical to optical conversion of the timing, trigger and fast control signals;
  - Electrical to optical conversion of the control signals for the components of the OPB;
  - DC/DC conversion of the supply voltages for the hybrids and OPB itself;
  - Monitoring of the supplied voltages on the OPB and detector module;
  - Routing of the temperature monitoring signals (NTCs) from the detector module and the OPB.
- Each OPB can serve 2 GBTx hybrids – with the current design idea 2 OPBs are needed for each roman pot

New production will be launched soon together with VELO group and LumiTracker group

VELO firmware

- VELO has a specific control interface firmware to act as a bridge between PCIe and FE
- PCIe 40 card configured as cntrol interface
- 1 GBTx for commanding the OPB and monitoring temperature and analog signals
- 1 GBTx for up to 2 VeloPix tiles

The readout board firmware architecture



FERNÁNDEZ PRIETO et al.: PHASE I UPGRADE OF THE READOUT SYSTEM OF THE VERTEX DETECTOR AT THE LHCb EXPERIMENT

The experts from INFN Pisa are already in contact with the VELO group to learn how to operate the firmware + PCIe40 and minidaq are being purchased

Long cables and services

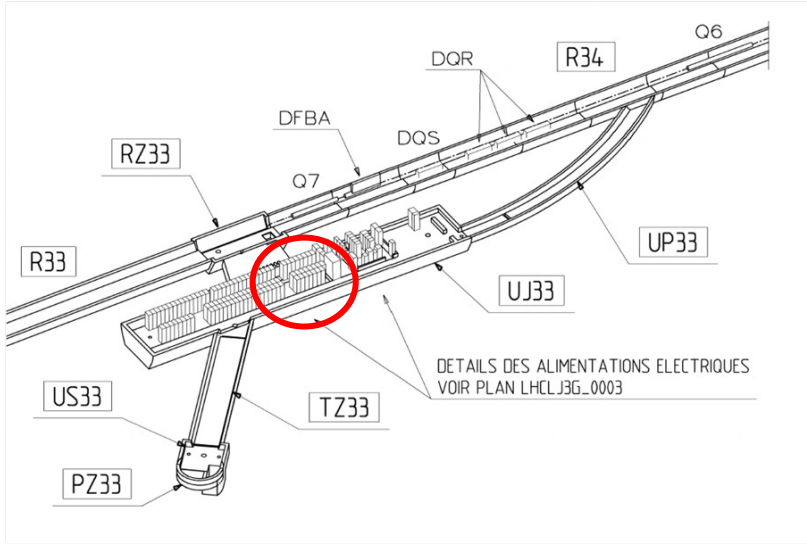
See presentation from José at the meeting of 31/10/2023 https://agenda.infn.it/event/38196/

Long cables

- Power distribution has three segments before reaching the Roman Pot/OPB.
- This three segments are separated by patch panels that use terminal blocks to connect/disconnect each line.
  - First segment is fully enclosed in the racks where the power supplies are installed and (initially) only affect LV power lines.
  - Second segment is the longest one ~250m running through the tunnel
  - The final segment is a final segment between OPB and electronics and includes vacuum region.

Two groups from CERN are available to share with us their space in the rack in room UJ33.

The Valencia group is already in contact with CAEN to study the best solution for the power supply system.

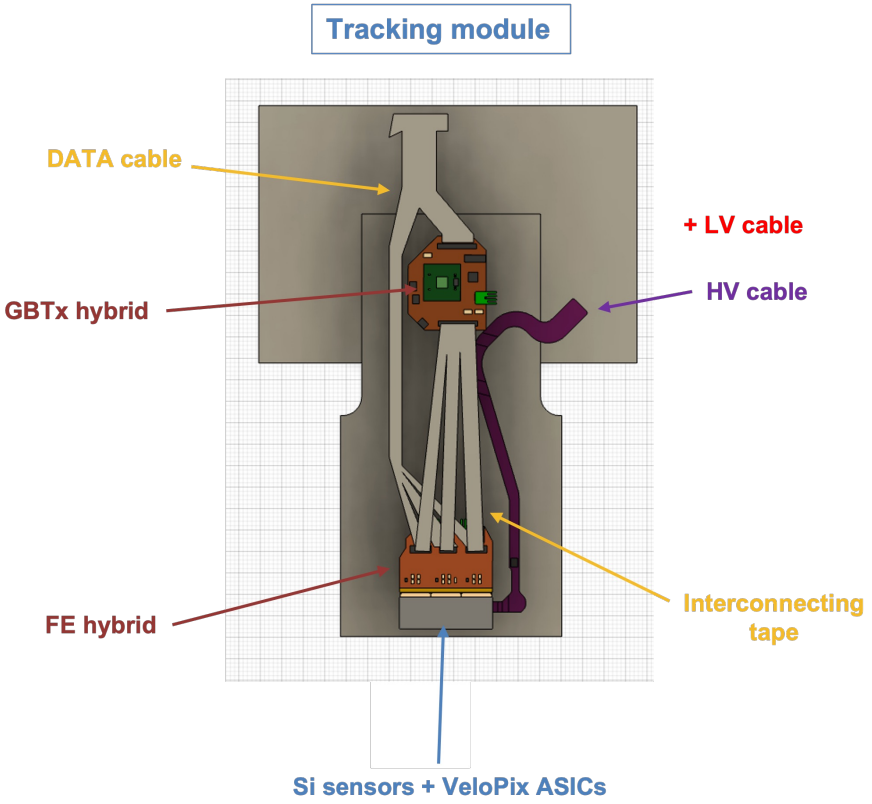


Summary

2D pixel detector design

- A tracking detector is being designed for the proof-of-principle test at the IR3
- Selected technology: Silicon pixel detector placed inside a roman pot
- Sensors and ASICs from the VELO detector of LHCb
- Roman pot from the ALFA experiment and mechanical support and cooling from the TOTEM experiment

- Installation foreseen during the YETS 2024/2025
- Good progresses:
  - Sensors and ASICs sent to ADVAFAB for the bump bonding
  - New flex cable design in progress
  - Contact with VELO group for other components and firmware
  - Contact with CAEN for the power supply system

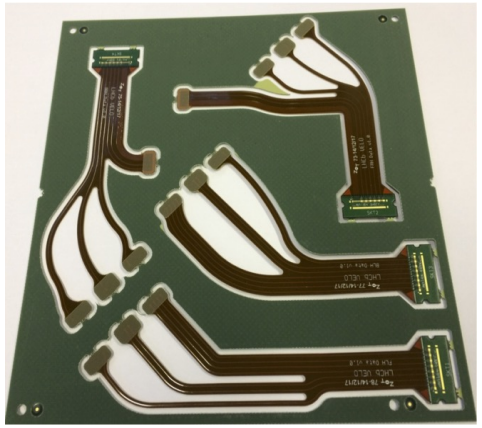


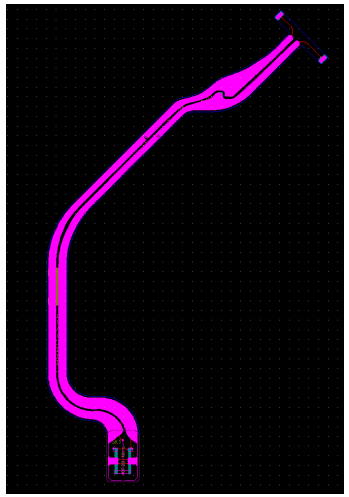
Backups

Flex cables

DATA cables

- Connect the velopix data output streams, uplink, down link, reset lines to the long data cables
- These are flexible, double sided, 100um track and gap, with controlled impedance, 100" differential traces.





Interconnecting tapes

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